NX3L2467

Dual low-ohmic double-pole double-throw analog switch

Rev. 3 — 29 December 2010 Product data sheet

1. General description

The NX3L2467 is a dual low-ohmic double-pole double-throw analog switch suitable for use as an analog or digital multiplexer/demultiplexer. It consists of four switches, each with two independent input/outputs (nY0 and nY1) and a common input/output (nZ). The two digital inputs (1S and 2S) are used to select the switch position. 1S is used in selecting the independent inputs/outputs switched to 1Z and 2Z, and 2S is used in selecting the independent inputs/outputs switched to 3Z and 4Z. Schmitt trigger action at the digital inputs makes the circuit tolerant to slower input rise and fall times. Low threshold digital inputs allows this device to be driven by 1.8 V logic levels in 3.3 V applications without significant increase in supply current I_{CC}. This makes it possible for the NX3L467 to switch 4.3 V signals with a 1.8 V digital controller, eliminating the need for logic level translation. The NX3L2467 allows signals with amplitude up to V_{CC} to be transmitted from nZ to nY0 or nY1; or from nY0 or nY1 to nZ. Its low ON resistance (0.5 Ω) and flatness (0.13 Ω) ensures minimal attenuation and distortion of transmitted signals.

2. Features and benefits

- Wide supply voltage range from 1.4 V to 4.3 V
- Very low ON resistance (peak):
  - 1.7 Ω (typical) at V_{CC} = 1.4 V
  - 1.0 Ω (typical) at V_{CC} = 1.65 V
  - 0.6 Ω (typical) at V_{CC} = 2.3 V
  - 0.5 Ω (typical) at V_{CC} = 2.7 V
  - 0.5 Ω (typical) at V_{CC} = 4.3 V
- Break-before-make switching
- High noise immunity
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
  - IEC61000-4-2 contact discharge exceeds 6000 V for switch ports
- CMOS low-power consumption
- Latch-up performance exceeds 100 mA per JESD 78B Class II Level A
- 1.8 V control logic at V_{CC} = 3.6 V
- Control input accepts voltages above supply voltage
- Very low supply current, even when input is below V_{CC}
- High current handling capability (350 mA continuous current under 3.3 V supply)
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Cell phone
- PDA
- Portable media player

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX3L2467PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
NX3L2467HR	−40 °C to +125 °C	HXQFN16U	plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; UTLP based; body 3 × 3 × 0.5 mm	SOT1039-1
NX3L2467GU	−40 °C to +125 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 × 2.60 × 0.50 mm	SOT1161-1

5. Marking

Table 2. Marking codes

Type number	Marking code
NX3L2467PW	X3L2467
NX3L2467HR	D67
NX3L2467GU	D67

6. Functional diagram

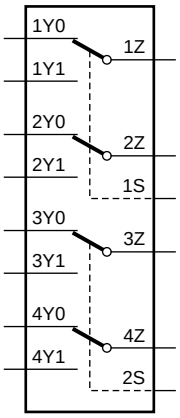


Fig 1. Logic symbol

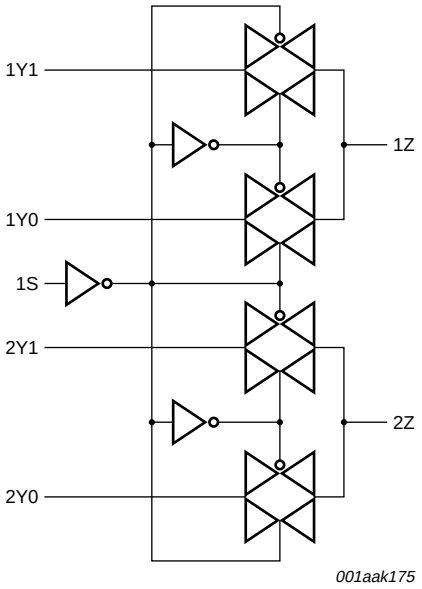


Fig 2. Logic diagram

7. Pinning information

7.1 Pinning

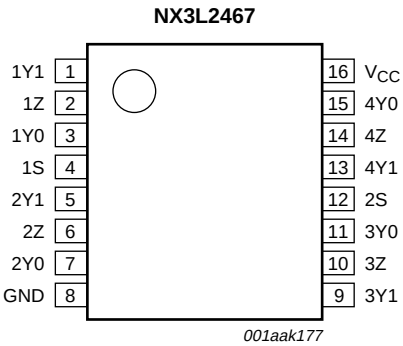
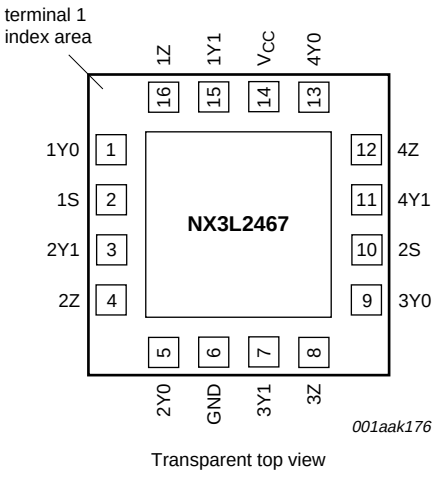


Fig 3. Pin configuration SOT403-1 (TSSOP16)



Transparent top view

Fig 4. Pin configuration SOT1039-1 (HXQFN16U)

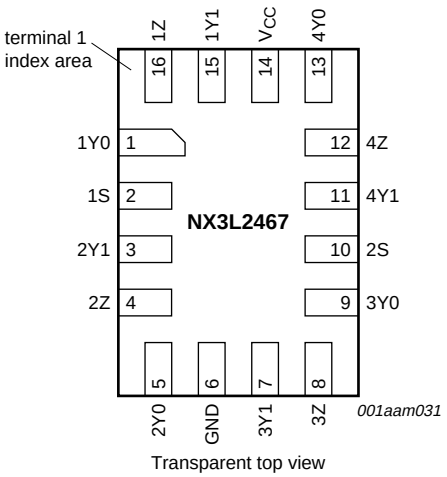


Fig 5. Pin configuration SOT1161-1 (XQFN16)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1039-1 and SOT1161-1	SOT403-1	
1Y0, 2Y0, 3Y0, 4Y0	1, 5, 9, 13	3, 7, 11, 15	independent input or output
1S, 2S	2, 10	4, 12	select input
1Y1, 2Y1, 3Y1, 4Y1	15, 3, 7, 11	1, 5, 9, 13	independent input or output
1Z, 2Z, 3Z, 4Z	16, 4, 8, 12	2, 6, 10, 14	common output or input
GND	6	8	ground (0 V)
V_{CC}	14	16	supply voltage

8. Functional description

Table 4. Function table[1]

Input nS	Channel on
L	nY0
H	nY1

[1] H = HIGH voltage level; L = LOW voltage level.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+4.6	V
V_I	input voltage	select input nS	[1]	−0.5	+4.6	V
V_{SW}	switch voltage		[2]	−0.5	V_{CC} + 0.5	V

Table 5. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{IK}	input clamping current	$V_I < -0.5$ V		−50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±50	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; source or sink current		-	±350	mA
		$V_{SW} > -0.5$ V or $V_{SW} < V_{CC} + 0.5$ V; pulsed at 1 ms duration, < 10 % duty cycle; peak current		-	±500	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +125 °C				
		TSSOP16	[3]	-	500	mW
		HXQFN16U	[4]	-	250	mW
		XQFN16	[5]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed but may not exceed 4.6 V.

[3] For TSSOP16 package: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K above.

[4] For HXQFN16U package: above 135 °C the value of P_{tot} derates linearly with 16.9 mW/K.

[5] For XQFN16 package: above 133 °C the value of P_{tot} derates linearly with 14.5 mW/K.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			1.4	4.3	V
V_I	input voltage	select input nS		0	4.3	V
V_{SW}	switch voltage		[1]	0	V_{CC}	V
T_{amb}	ambient temperature			−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.4 V to 4.3 V	[2]	-	200	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nYn. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

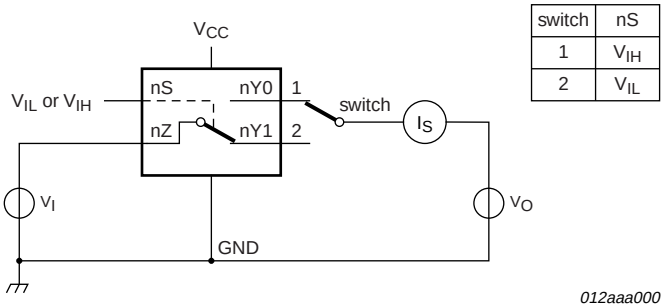
11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +125 °C			Unit
			Min	Typ	Max	Min	Max (85 °C)	Max (125 °C)	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.4 V to 1.6 V	0.9	-	-	0.9	-	-	V
		V_{CC} = 1.65 V to 1.95 V	0.9	-	-	0.9	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.1	-	-	1.1	-	-	V
		V_{CC} = 2.7 V to 3.6 V	1.3	-	-	1.3	-	-	V
		V_{CC} = 3.6 V to 4.3 V	1.4	-	-	1.4	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.4 V to 1.6 V	-	-	0.3	-	0.3	0.3	V
		V_{CC} = 1.65 V to 1.95 V	-	-	0.4	-	0.4	0.3	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.4	-	0.4	0.4	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	0.5	V
		V_{CC} = 3.6 V to 4.3 V	-	-	0.6	-	0.6	0.6	V
I_I	input leakage current	select input nS; V_I = GND to 4.3 V; V_{CC} = 1.4 V to 4.3 V	-	-	-	-	±0.5	±1	µA
$I_{S(OFF)}$	OFF-state leakage current	nY0 and nY1 port; see Figure 6							
		V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
$I_{S(ON)}$	ON-state leakage current	nZ port; V_{CC} = 1.4 V to 3.6 V; see Figure 7							
		V_{CC} = 1.4 V to 3.6 V	-	-	±5	-	±50	±500	nA
		V_{CC} = 3.6 V to 4.3 V	-	-	±10	-	±50	±500	nA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}							
		V_{CC} = 3.6 V	-	-	100	-	500	5000	nA
		V_{CC} = 4.3 V	-	-	150	-	800	6000	nA
ΔI_{CC}	additional supply current	V_{SW} = GND or V_{CC}							
		V_I = 2.6 V; V_{CC} = 4.3 V	-	2.0	4.0	-	7	7	µA
		V_I = 2.6 V; V_{CC} = 3.6 V	-	0.35	0.7	-	1	1	µA
		V_I = 1.8 V; V_{CC} = 4.3 V	-	7.0	10.0	-	15	15	µA
		V_I = 1.8 V; V_{CC} = 3.6 V	-	2.5	4.0	-	5	5	µA
		V_I = 1.8 V; V_{CC} = 2.5 V	-	50	200	-	300	500	nA
C_I	input capacitance		-	1.0	-	-	-	-	pF
$C_{S(OFF)}$	OFF-state capacitance		-	35	-	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance		-	130	-	-	-	-	pF

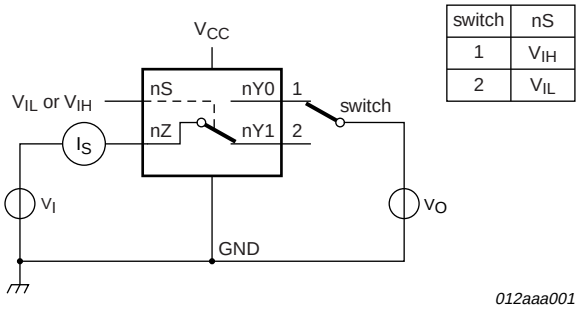
11.1 Test circuits



switch	nS
1	V_{IH}
2	V_{IL}

V_I = 0.3 V or V_{CC} − 0.3 V; V_O = V_{CC} − 0.3 V or 0.3 V.

Fig 6. Test circuit for measuring OFF-state leakage current



switch	nS
1	V_{IH}
2	V_{IL}

V_I = 0.3 V or V_{CC} − 0.3 V; V_O = V_{CC} − 0.3 V or 0.3 V.

Fig 7. Test circuit for measuring ON-state leakage current

11.2 ON resistance

Table 8. ON resistance[1]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 9 to Figure 15.

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ[2]	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	V_I = GND to V_{CC}; I_{SW} = 100 mA; see Figure 8						
		V_{CC} = 1.4 V	-	1.7	3.7	-	4.1	Ω
		V_{CC} = 1.65 V	-	1.0	1.6	-	1.7	Ω
		V_{CC} = 2.3 V	-	0.6	0.8	-	0.9	Ω
		V_{CC} = 2.7 V	-	0.5	0.75	-	0.9	Ω
		V_{CC} = 4.3 V	-	0.5	0.75	-	0.9	Ω

Table 8. ON resistance[1]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for graphs see Figure 9 to Figure 15.

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ[2]	Max	Min	Max	
ΔR_{ON}	ON resistance mismatch between channels	V_I = GND to V_{CC}; I_{SW} = 100 mA [3]						
		V_{CC} = 1.4 V; V_{SW} = 0.4 V	-	0.18	0.3	-	0.3	Ω
		V_{CC} = 1.65 V; V_{SW} = 0.5 V	-	0.18	0.2	-	0.3	Ω
		V_{CC} = 2.3 V; V_{SW} = 0.7 V	-	0.07	0.1	-	0.13	Ω
		V_{CC} = 2.7 V; V_{SW} = 0.8 V	-	0.07	0.1	-	0.13	Ω
		V_{CC} = 4.3 V; V_{SW} = 0.8 V	-	0.07	0.1	-	0.13	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to V_{CC}; I_{SW} = 100 mA [4]						
		V_{CC} = 1.4 V	-	1.0	3.3	-	3.6	Ω
		V_{CC} = 1.65 V	-	0.5	1.2	-	1.3	Ω
		V_{CC} = 2.3 V	-	0.15	0.3	-	0.35	Ω
		V_{CC} = 2.7 V	-	0.13	0.3	-	0.35	Ω
		V_{CC} = 4.3 V	-	0.2	0.4	-	0.45	Ω

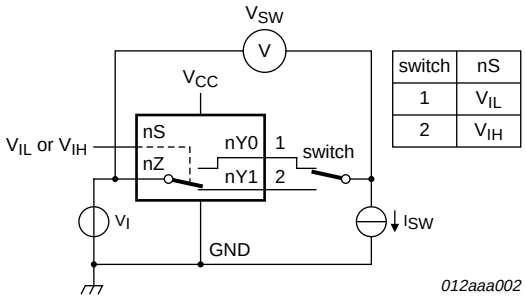
[1] For NX3L2467PW (TSSOP16 package), all ON resistance values are up to 0.05 Ω higher.

[2] Typical values are measured at T_{amb} = 25 °C.

[3] Measured at identical V_{CC}, temperature and input voltage.

[4] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

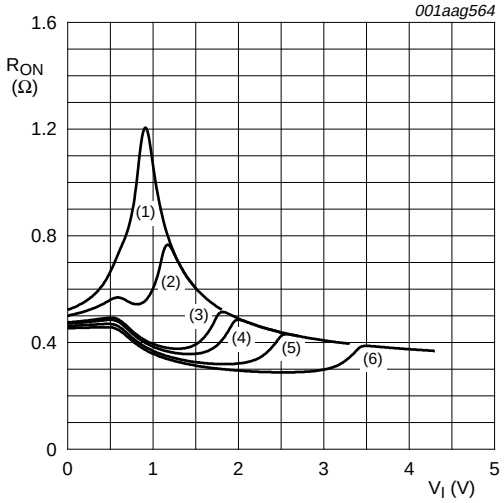
11.3 ON resistance test circuit and graphs



switch	nS
1	V_{IL}
2	V_{IH}

$R_{ON} = V_{SW} / I_{SW}$.

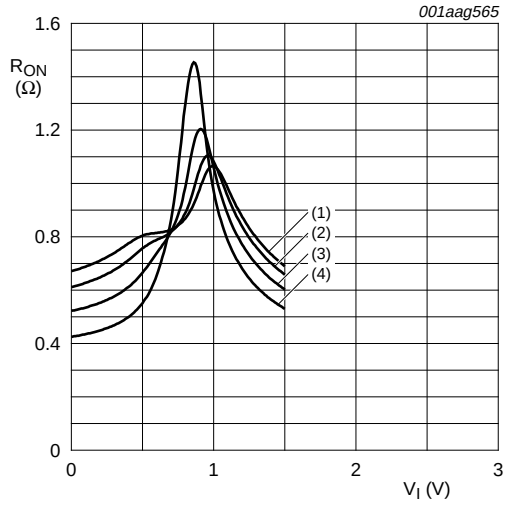
Fig 8. Test circuit for measuring ON resistance



(1) V_{CC} = 1.5 V.
(2) V_{CC} = 1.8 V.
(3) V_{CC} = 2.5 V.
(4) V_{CC} = 2.7 V.
(5) V_{CC} = 3.3 V.
(6) V_{CC} = 4.3 V.

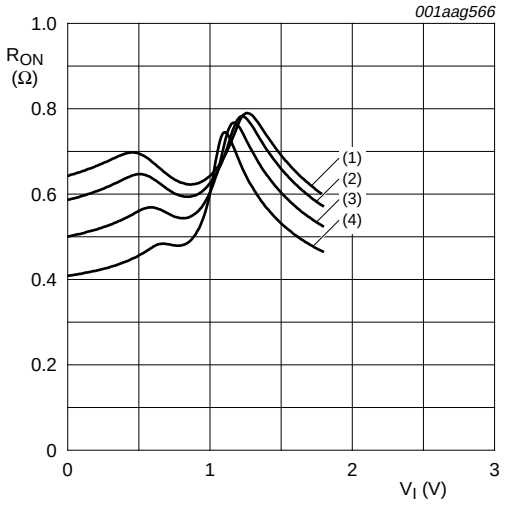
Measured at T_{amb} = 25 °C.

Fig 9. Typical ON resistance as a function of input voltage



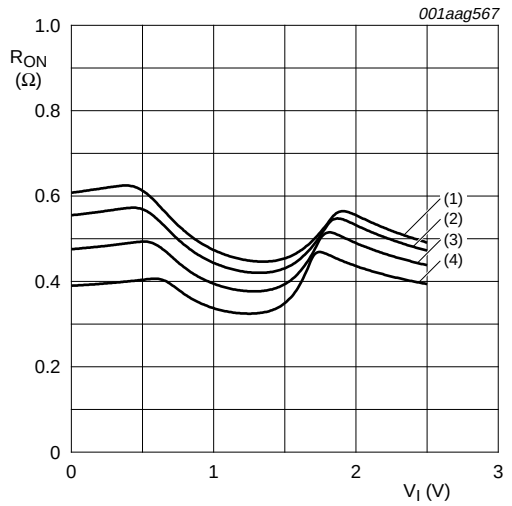
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 10. ON resistance as a function of input voltage; V_{CC} = 1.5 V



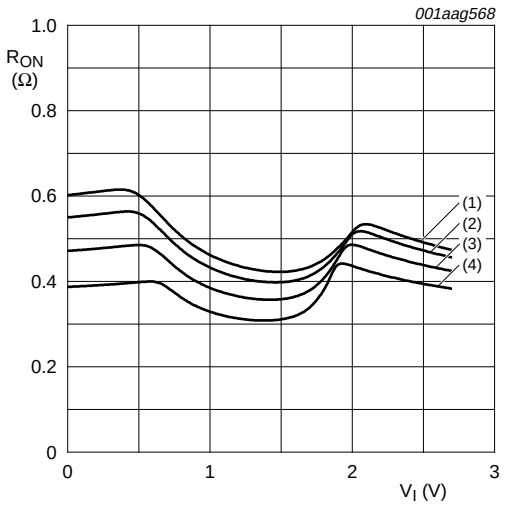
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 11. ON resistance as a function of input voltage; V_{CC} = 1.8 V



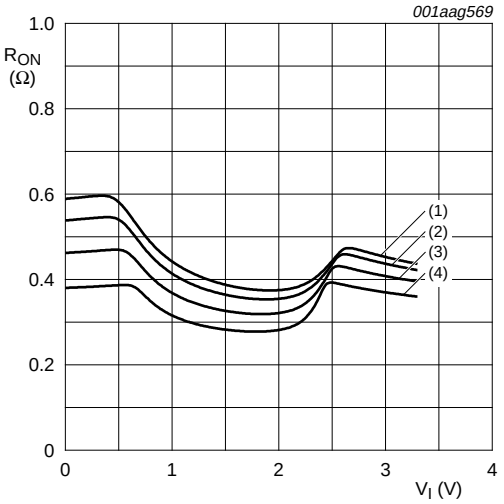
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 12. ON resistance as a function of input voltage; V_{CC} = 2.5 V



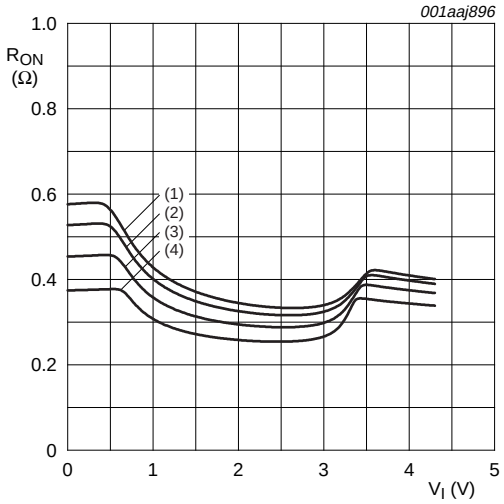
(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 13. ON resistance as a function of input voltage; V_{CC} = 2.7 V



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 14. ON resistance as a function of input voltage; V_{CC} = 3.3 V



(1) T_{amb} = 125 °C.
(2) T_{amb} = 85 °C.
(3) T_{amb} = 25 °C.
(4) T_{amb} = −40 °C.

Fig 15. ON resistance as a function of input voltage; V_{CC} = 4.3 V

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 18.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{en}	enable time	nS to nZ or nYn; see Figure 16							
		V_{CC} = 1.4 V to 1.6 V	-	41	90	-	120	120	ns
		V_{CC} = 1.65 V to 1.95 V	-	30	70	-	80	90	ns
		V_{CC} = 2.3 V to 2.7 V	-	20	45	-	50	55	ns
		V_{CC} = 2.7 V to 3.6 V	-	19	40	-	45	50	ns
		V_{CC} = 3.6 V to 4.3 V	-	19	40	-	45	50	ns
t_{dis}	disable time	nS to nZ or nYn; see Figure 16							
		V_{CC} = 1.4 V to 1.6 V	-	24	70	-	80	90	ns
		V_{CC} = 1.65 V to 1.95 V	-	15	55	-	60	65	ns
		V_{CC} = 2.3 V to 2.7 V	-	9	25	-	30	35	ns
		V_{CC} = 2.7 V to 3.6 V	-	8	20	-	25	30	ns
		V_{CC} = 3.6 V to 4.3 V	-	8	20	-	25	30	ns

Table 9. Dynamic characteristics *...continued*

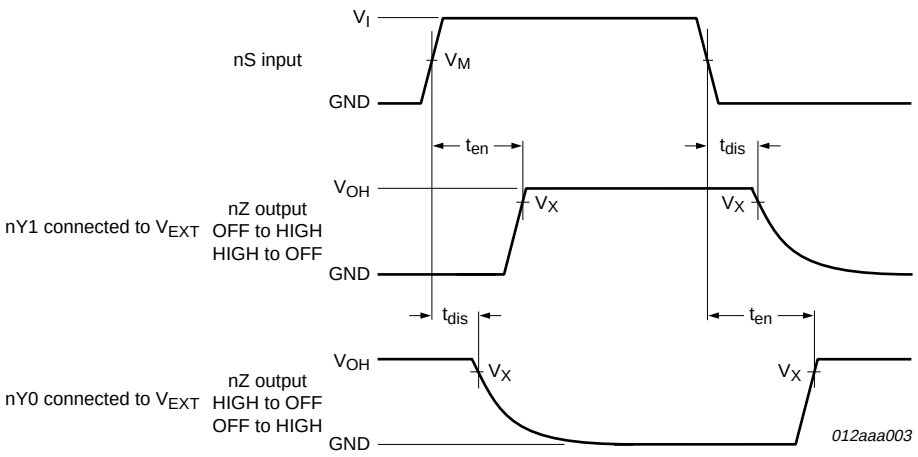
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 18.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{b-m}	break-before-make time	see Figure 17 [2]							
		V_{CC} = 1.4 V to 1.6 V	-	20	-	9	-	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	17	-	7	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	13	-	4	-	-	ns
		V_{CC} = 2.7 V to 3.6 V	-	11	-	3	-	-	ns
		V_{CC} = 3.6 V to 4.3 V	-	11	-	2	-	-	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V, 3.3 V and 4.3 V respectively.

[2] Break-before-make guaranteed by design.

12.1 Waveform and test circuits



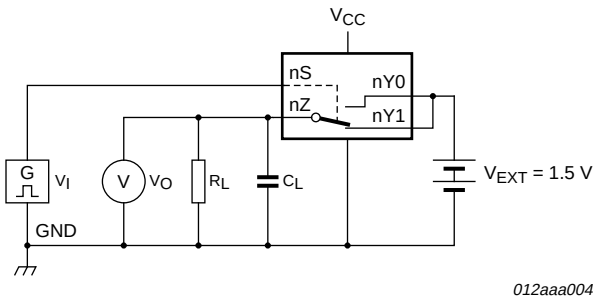
Measurement points are given in Table 10.

Logic level: V_{OH} is typical output voltage level that occurs with the output load.

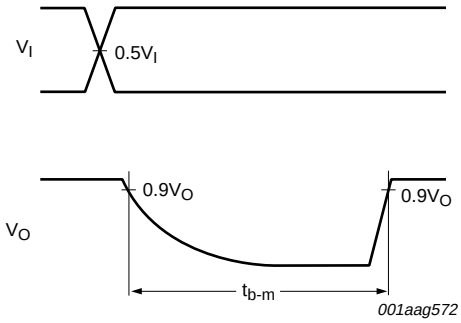
Fig 16. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
1.4 V to 4.3 V	$0.5V_{CC}$	$0.9V_{OH}$

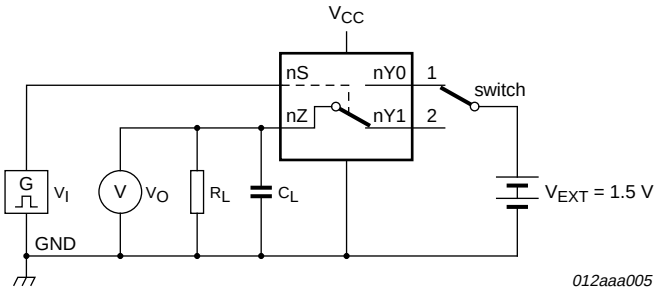


a. Test circuit



b. Input and output measurement points

Fig 17. Test circuit for measuring break-before-make timing



Test data is given in Table 11.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 18. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
1.4 V to 4.3 V	V_{CC}	≤ 2.5 ns	35 pF	50 Ω

12.2 Additional dynamic characteristics

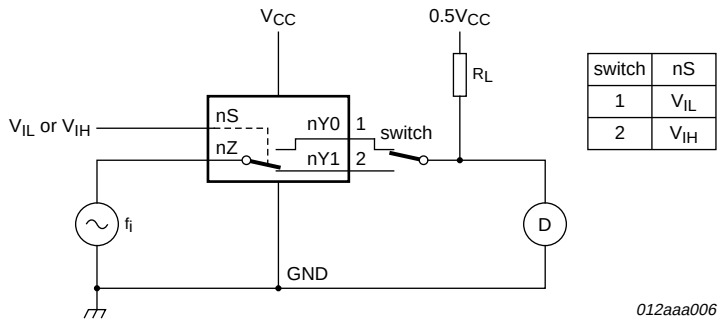
Table 12. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 20 Hz to 20 kHz; R_L = 32 Ω; see Figure 19	[1]				
		V_{CC} = 1.4 V; V_I = 1 V (p-p)		-	0.15	-	%
		V_{CC} = 1.65 V; V_I = 1.2 V (p-p)		-	0.10	-	%
		V_{CC} = 2.3 V; V_I = 1.5 V (p-p)		-	0.02	-	%
		V_{CC} = 2.7 V; V_I = 2 V (p-p)		-	0.02	-	%
		V_{CC} = 4.3 V; V_I = 2 V (p-p)		-	0.02	-	%
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; see Figure 20	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	60	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 100 kHz; R_L = 50 Ω; see Figure 21	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	−90	-	dB
V_{ct}	crosstalk voltage	between digital inputs and switch; f_i = 1 MHz; C_L = 50 pF; R_L = 50 Ω; see Figure 22					
		V_{CC} = 1.4 V to 3.6 V		-	0.2	-	V
		V_{CC} = 3.6 V to 4.3 V		-	0.3	-	V
Xtalk	crosstalk	between switches; f_i = 100 kHz; R_L = 50 Ω; see Figure 23	[1]				
		V_{CC} = 1.4 V to 4.3 V		-	−90	-	dB
Q_{inj}	charge injection	f_i = 1 MHz; C_L = 0.1 nF; R_L = 1 MΩ; V_{gen} = 0 V; R_{gen} = 0 Ω; see Figure 24					
		V_{CC} = 1.5 V		-	3	-	pC
		V_{CC} = 1.8 V		-	4	-	pC
		V_{CC} = 2.5 V		-	6	-	pC
		V_{CC} = 3.3 V		-	9	-	pC
		V_{CC} = 4.3 V		-	15	-	pC

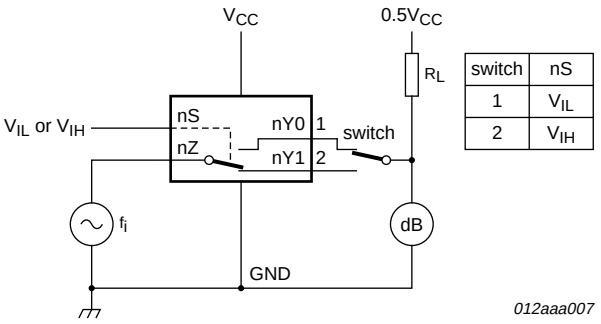
[1] f_i is biased at $0.5V_{CC}$.

12.3 Test circuits



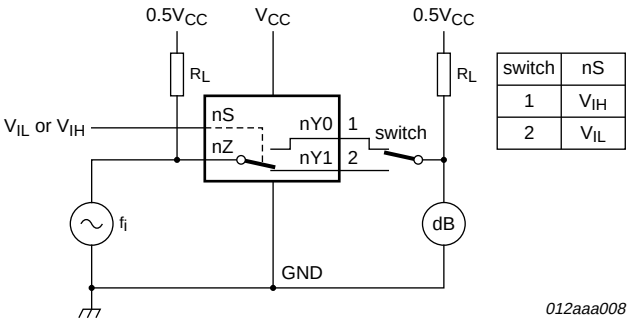
switch	nS
1	V_{IL}
2	V_{IH}

Fig 19. Test circuit for measuring total harmonic distortion



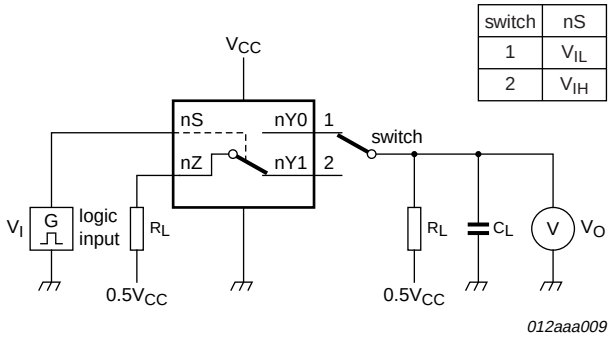
Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads −3 dB.

Fig 20. Test circuit for measuring the frequency response when channel is in ON-state

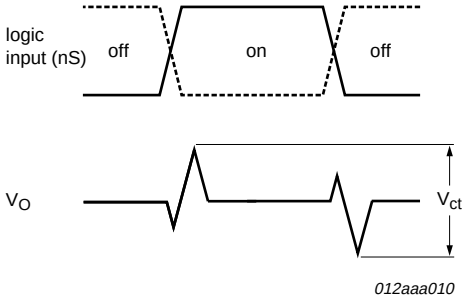


Adjust f_i voltage to obtain 0 dBm level at input.

Fig 21. Test circuit for measuring isolation (OFF-state)

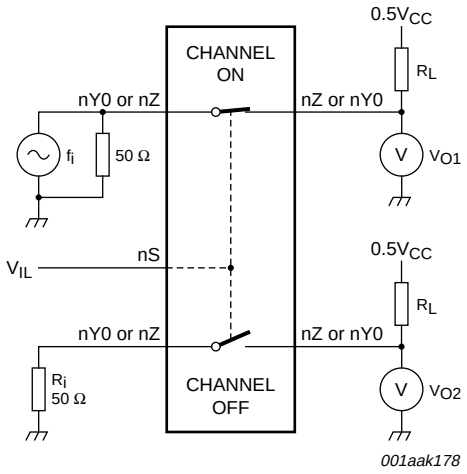


a. Test circuit



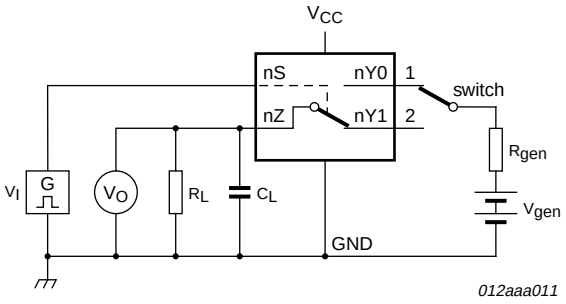
b. Input and output pulse definitions

Fig 22. Test circuit for measuring crosstalk voltage between digital inputs and switch

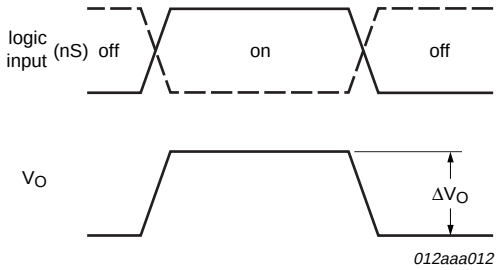


$20 \log_{10} (V_{O2} / V_{O1})$ or $20 \log_{10} (V_{O1} / V_{O2})$.

Fig 23. Test circuit for measuring crosstalk between switches



a. Test circuit



b. Input and output pulse definitions

Definition: $Q_{inj} = \Delta V_O \times C_L$.

ΔV_O = output voltage variation.

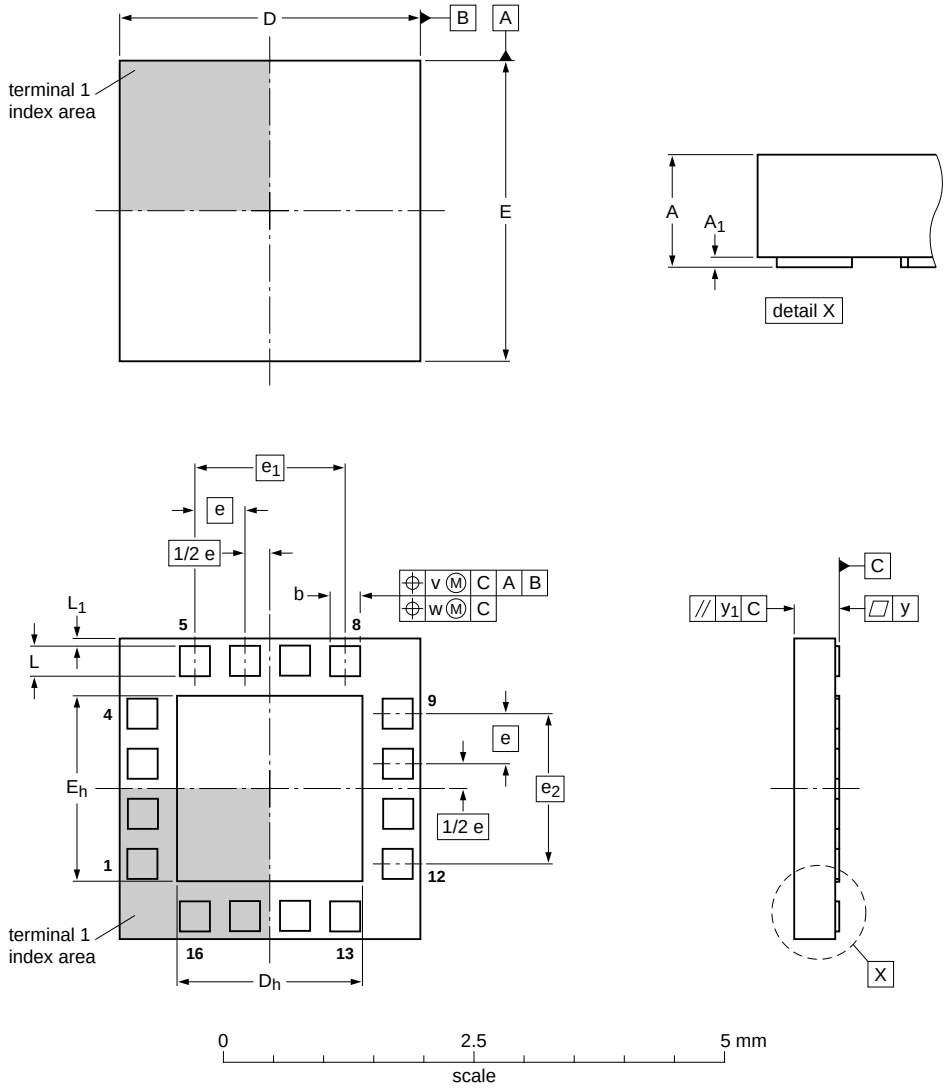
R_{gen} = generator resistance.

V_{gen} = generator voltage.

Fig 24. Test circuit for measuring charge injection

13. Package outline

HXQFN16U: plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; UTLP based; body 3 x 3 x 0.5 mm **SOT1039-1**



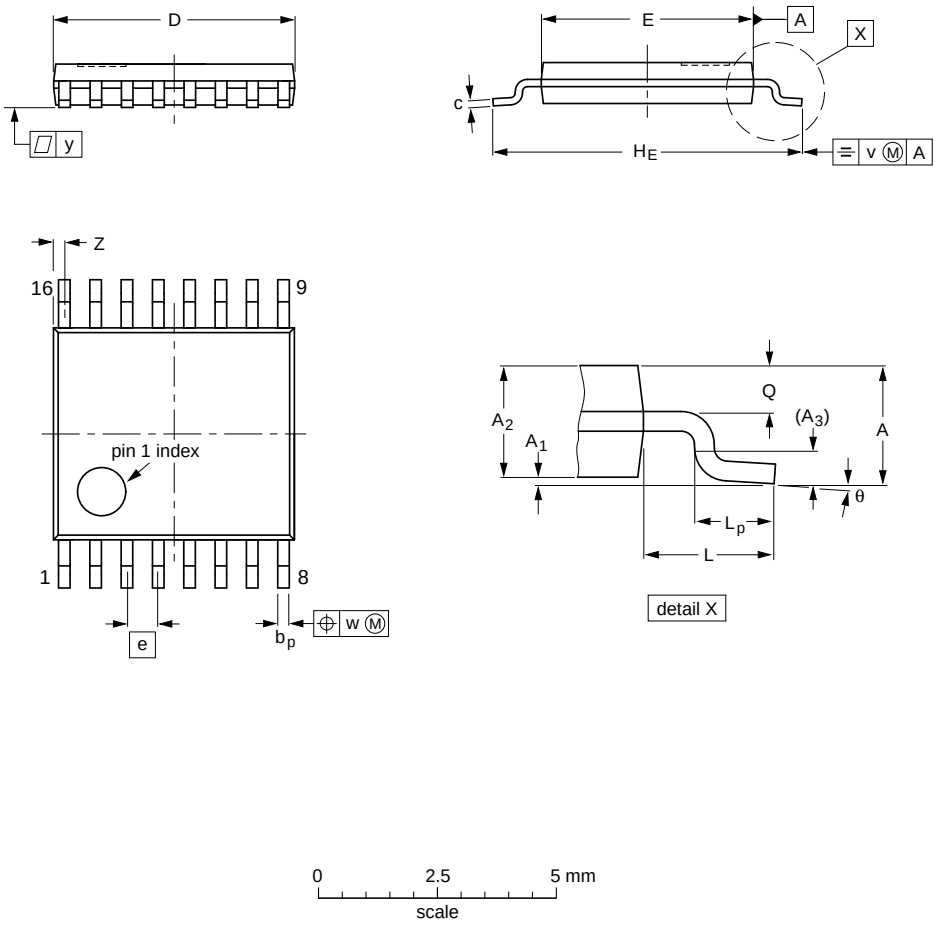
DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	D_h	E	E_h	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.35 0.25	3.1 2.9	1.95 1.75	3.1 2.9	1.95 1.75	0.5	1.5	1.5	0.35 0.25	0.1 0.0	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1039-1	- - -		- - -			~~07-11-14~~ 07-12-01

Fig 25. Package outline SOT1039-1 (HXQFN16U)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

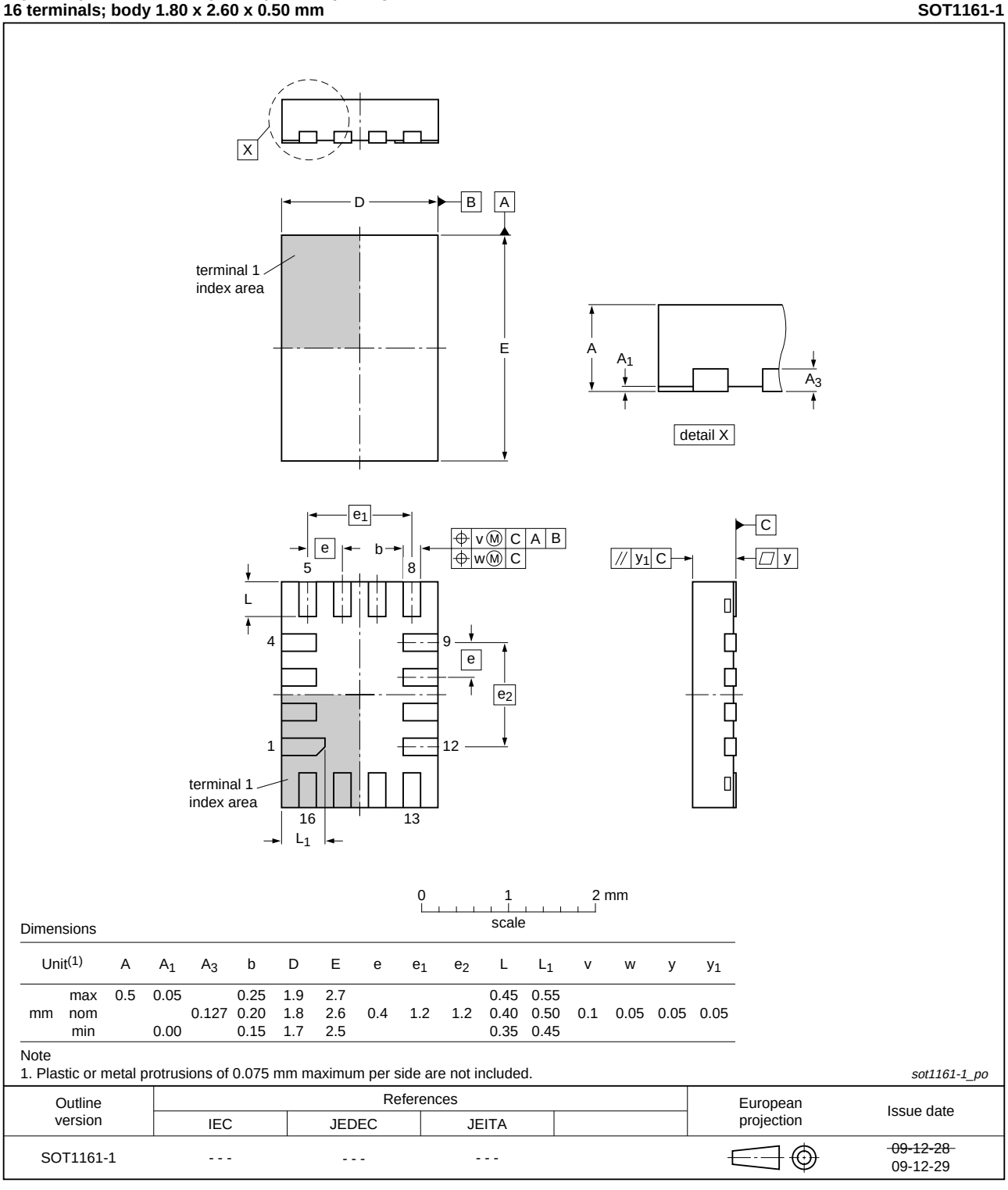
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 26. Package outline SOT403-1 (TSSOP16)

XQFN16: plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm **SOT1161-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	1.9	2.7				0.45	0.55				
mm	nom			0.127	0.20	1.8	2.6	0.4	1.2	1.2	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.7	2.5				0.35	0.45				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1161-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1161-1	- - -	- - -	- - -			~~09-12-28~~ 09-12-29

Fig 27. Package outline SOT1161-1 (XQFN16)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PDA	Personal Digital Assistant

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3L2467 v.3	20101229	Product data sheet	-	NX3L2467 v.2
Modifications:	• Section 2: IEC61000-4-2 added.			
NX3L2467 v.2	20100519	Product data sheet	-	NX3L2467 v.1
Modifications:	• Added type number NX3L2467GU (XQFN16 / SOT1161 package). • Figure 1 changed: pin numbers removed from logic symbol.			
NX3L2467 v.1	20090623	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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