NX3DV42

Dual high-speed USB 2.0 double-pole double-throw analog switch

Rev. 1 — 3 January 2012 Product data sheet

1. General description

The NX3DV42 is a double-pole double-throw analog switch suitable for use as an analog or digital multiplexer/demultiplexer. Its wide bandwidth and low bit-to-bit skew allows the NX3DV42 to pass high-speed differential signals with good signal integrity. Its high channel to channel crosstalk rejection results in minimal noise interference. The bandwidth is wide enough to pass high-speed USB 2.0 differential signals (480 Mb/s). It consist of two switches, each with two independent input/outputs (HSDn+ and HSDn−) and a common input/output (D+ or D−). One digital inputs (S) is used to select the switch position. When pin $\overline{OE}$ is HIGH, the switches are turned off. Schmitt trigger action at the select input (S) and enable input ($\overline{OE}$) makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 3.0 V to 4.3 V.

2. Features and benefits

- Supply voltage range from 3.0 V to 4.3 V
- 4 Ω typical ON resistance
- 7.3 pF typical ON capacitance
- 950 MHz typical bandwidth or data frequency
- Low crosstalk of −30 dB at 240 MHz
- Break-before-make switching
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4000 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
  - HBM exceeds 12000 V for power to GND protection
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Specified from −40 °C to +85 °C

3. Applications

- Cell phone, PDA, Digital camera and notebook
- LCD monitor, TV and set-top box

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX3DV42GM	–40 °C to +85 °C	XQFN10U	plastic extremely thin quad flat package; no leads; 10 terminals; UTLP based; body 2 × 1.55 × 0.5 mm	SOT1049-2
NX3DV42GU	–40 °C to +85 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm	SOT1160-1

5. Marking

Table 2. Marking

Type number	Marking code
NX3DV42GM	x4
NX3DV42GU	x4

6. Functional diagram

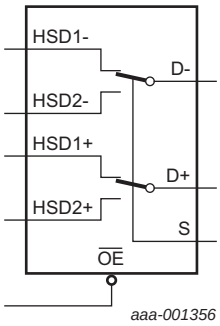


Fig 1. Logic symbol

7. Pinning information

7.1 Pinning

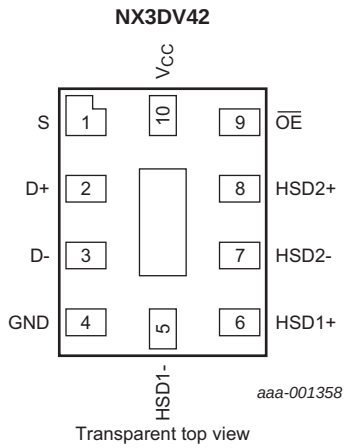


Fig 2. Pin configuration SOT1049-2 (XQFN10U)

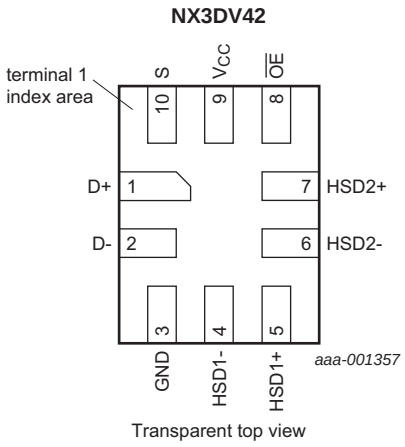


Fig 3. Pin configuration SOT1160-1 (XQFN10)

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT1049-2	SOT1160-1	
HSD1–, HSD2–	5, 7	4, 6	independent input or output
HSD1+, HSD2+	6, 8	5, 7	independent input or output
D+, D–	2, 3	1, 2	common output or input
GND	4	3	ground (0 V)
$\overline{OE}$	9	8	output enable input (active-LOW)
S	1	10	select input
V_{CC}	10	9	supply voltage

8. Functional description

Table 4. Function table[1]

Input		Channel on
S	$\overline{OE}$	
L	L	HSD1+ and HSD1–
H	L	HSD2+ and HSD2–
X	H	switch off

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+5.5	V
V_I	input voltage	pins S and $\overline{OE}$	[1]	–0.5	V_{CC}	V
V_{SW}	switch voltage			–0.5	+5.5	V
I_{IK}	input clamping current	V_I < –0.5 V		–50	-	mA
I_{SK}	switch clamping current	V_I < –0.5 V		-	±50	mA
I_{SW}	switch current			-	±100	mA
I_{CC}	supply current			-	+50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C		-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			3.0	4.3	V
V_I	input voltage	pins S and $\overline{OE}$		0	V_{CC}	V
V_{SW}	switch voltage		[1]	0	4.5	V
T_{amb}	ambient temperature			–40	+85	°C

[1] To avoid sinking GND current from terminals D+ and D– when switch current flows in terminals HSDn+ and HSDn–, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals D+ and D–, no GND current will flow from terminals HSDn+ and HSDn–. In this case, there is no limit for the voltage drop across the switch.

11. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 3.0 V to 3.6 V	1.3	-	-	V
		V_{CC} = 4.3 V	1.7	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 3.0 V to 3.6 V	-	-	0.5	V
		V_{CC} = 4.3 V	-	-	0.7	V
V_{IK}	input clamping voltage	V_{CC} = 3.0 V; I_I = –18 mA	-	-	–1.2	V
I_I	input leakage current	pins S and $\overline{OE}$; V_I = GND to 4.3 V; V_{CC} = 4.3 V	-	-	±1	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 4.3 V; see Figure 4	-	-	±2	µA

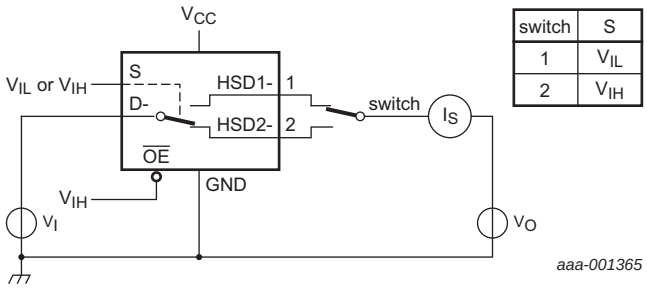
Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = –40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 4.3 V; V_{CC} = 0 V	-	-	±2	µA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{SW} = GND or V_{CC}; V_{CC} = 4.3 V	-	-	1	µA
ΔI_{CC}	additional supply current	V_I = 2.6 V; V_{SW} = GND or V_{CC}; V_{CC} = 4.3 V	-	-	10	µA
		V_I = 1.8 V; V_{SW} = GND or V_{CC}; V_{CC} = 4.3 V	-	-	15	µA
C_I	input capacitance	pins S and OE	-	1.0	-	pF
$C_{S(OFF)}$	OFF-state capacitance	pins HSDn+ and HSDn–; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	2.8	-	pF
$C_{S(ON)}$	ON-state capacitance	pins D+ and D–; V_{CC} = 3.3 V; V_I = 0 V to 3.3 V	-	7.3	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

11.1 Test circuits



switch	S
1	V_{IL}
2	V_{IH}

V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 4. Test circuit for measuring OFF-state leakage current

11.2 ON resistance

Table 8. ON resistance

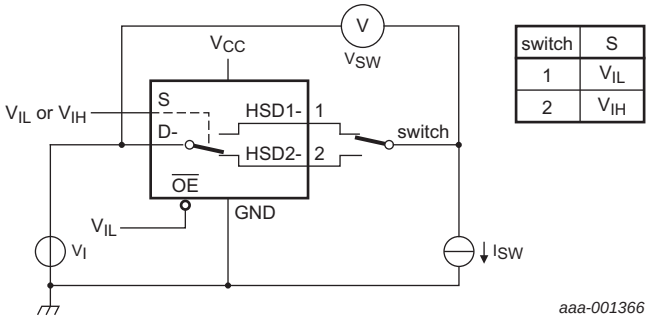
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
R_{ON}	ON resistance	V_I = 0.4 V; I_{SW} = 8 mA; see Figure 5					
		V_{CC} = 3.0 V		-	3.9	6.5	Ω
ΔR_{ON}	ON resistance mismatch between channels	V_I = 0.4 V; I_{SW} =8 mA	[2]				
		V_{CC} = 3.0 V		-	0.65	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Measured at identical V_{CC}, temperature and input voltage.

11.3 ON resistance test circuit and graphs



switch	S
1	V_{IL}
2	V_{IH}

$R_{ON} = V_{SW} / I_{SW}$.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 5. Test circuit for measuring ON resistance

12. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 9.

Symbol	Parameter	Conditions		T_{amb} = –40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
t_{pd}	propagation delay	HSDn+ to D+ or HSDn– to D– or D+ to HSDn+ or D– to HSDn–; see Figure 6	[2][3]				
		V_{CC} = 3.3 V		-	0.25	-	ns
t_{en}	enable time	S or $\overline{OE}$ to D+ or D–; see Figure 7	[4]				
		V_{CC} = 3.0 V to 3.6 V		-	11.2	30	ns
t_{dis}	disable time	S or $\overline{OE}$ to D+ or D–; see Figure 7	[5]				
		V_{CC} = 3.0 V to 3.6 V		-	3.9	25	ns
t_{b-m}	break-before-make time	see Figure 8	[3]				
		V_{CC} = 3.0 V to 3.6 V		2.0	5.9	-	ns
$t_{sk(p)}$	pulse skew time	see Figure 6					
		V_{CC} = 3.0 V to 3.6 V	[3]	-	20	-	ps
t_{jit}	jitter time	R_L = 50 Ω; C_L = 5 pF; t_r, t_f = 500 ps (10% to 90 %) at 480 Mbs (PRBS = $2^{15} - 1$)	[3]	-	200	-	ps

[1] Typical values are measured at T_{amb} = 25 °C, C_L = 5 pF and V_{CC} = 3.3 V.

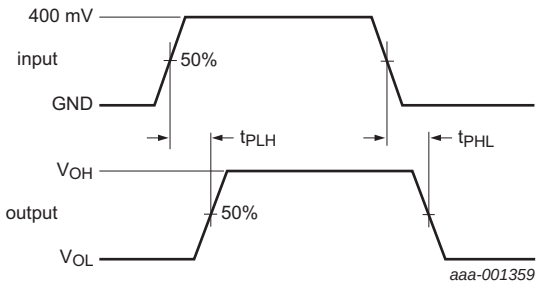
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Guaranteed by design.

[4] t_{en} is the same as t_{PZH}

[5] t_{dis} is the same as t_{PHZ}

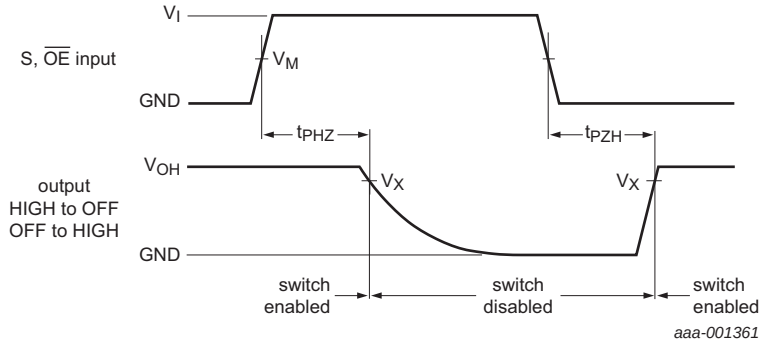
12.1 Waveform and test circuits



Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

$t_{sk(p)} = |t_{PHL} - t_{PLH}|$.

Fig 6. The data input to output propagation delay times and pulse skew times



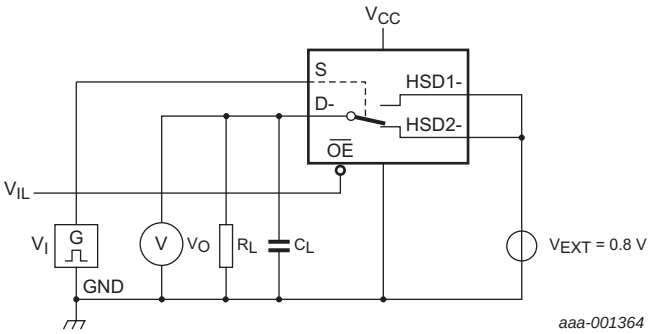
Measurement points are given in Table 10.

Logic level: V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

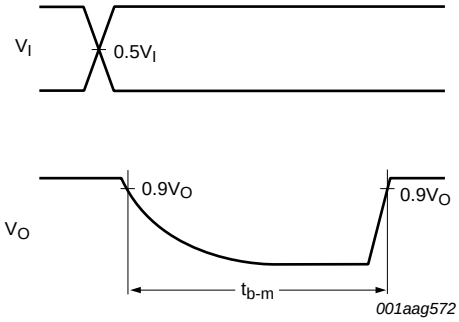
Fig 7. Enable and disable times

Table 10. Measurement points

Supply voltage	Input		Output
V_{CC}	V_M	V_I	V_X
3.0 V to 3.6 V	$0.5V_{CC}$	V_{CC}	$0.9V_{OH}$



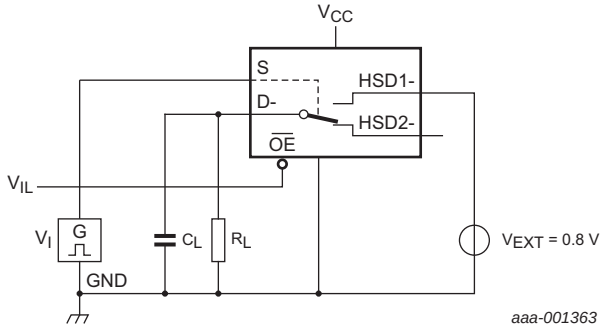
a. Test circuit.



b. Input and output measurement points

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 8. Test circuit for measuring break-before-make timing



Test circuit also applies for D+, HSD1+ and HSD2+.

Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance (should be equal to output impedance Z_o of the pulse generator).

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

V_I may be connected to S or $\overline{OE}$.

Fig 9. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
3.0 V to 3.6 V	V_{CC}	≤ 2.5 ns	5 pF	50 Ω

12.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics

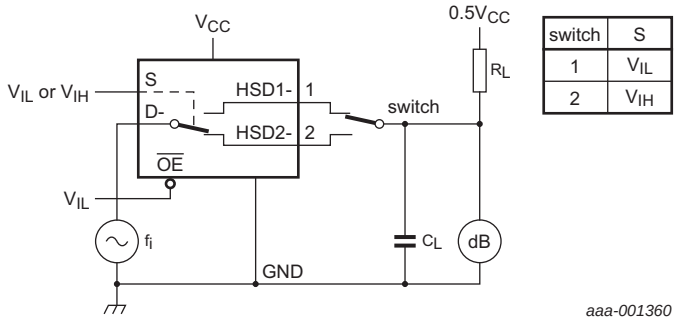
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); V_I = GND or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			Unit
				Min	Typ[2]	Max	
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; see Figure 10	[1]				
		C_L = 0 pF; V_{CC} = 3.0 V to 3.6 V		-	950	-	MHz
		C_L = 5 pF; V_{CC} = 3.0 V to 3.6 V		-	450	-	MHz
α_{iso}	isolation (OFF-state)	f_i = 240 MHz; R_L = 50 Ω; see Figure 11	[1]				
		V_{CC} = 3.0 V to 3.6 V		-	−30	-	dB
Xtalk	crosstalk	between switches; f_i = 240 MHz; R_L = 50 Ω; see Figure 12	[1]				
		V_{CC} = 3.0 V to 3.6 V		-	−30	-	dB

[1] f_i is biased at $0.5V_{CC}$.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

12.3 Test circuits

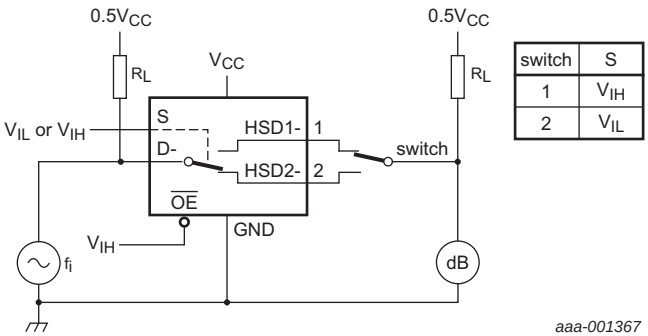


switch	S
1	V_{IL}
2	V_{IH}

Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads −3 dB.

Test circuit also applies for D+, HSD1+ and HSD2+.

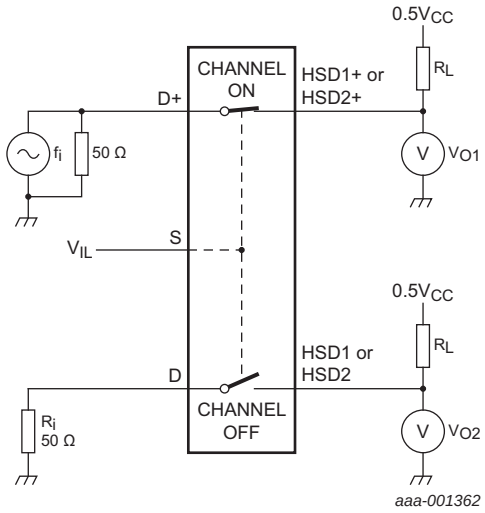
Fig 10. Test circuit for measuring the frequency response when channel is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Test circuit also applies for D+, HSD1+ and HSD2+.

Fig 11. Test circuit for measuring isolation (OFF-state)

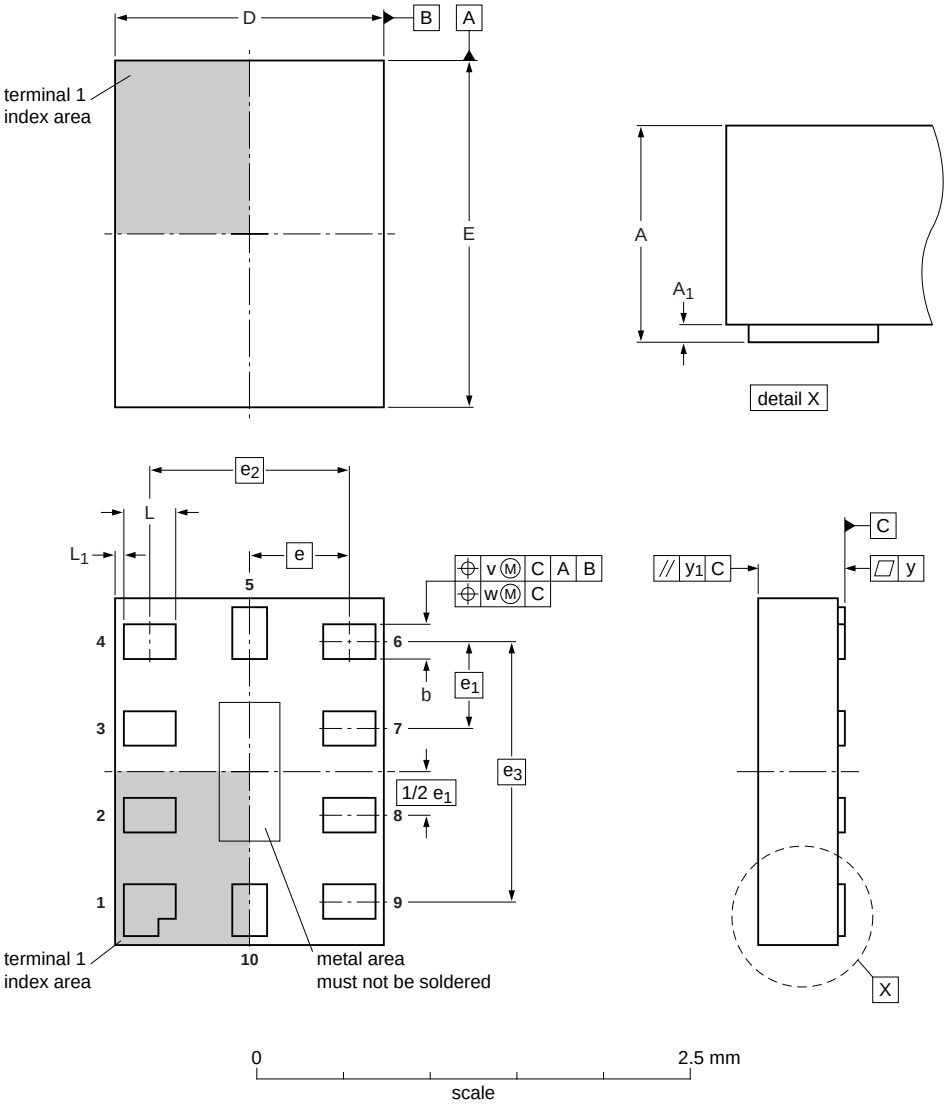


20 $\log_{10}$ (V_{O2}/V_{O1}) or 20 $\log_{10}$ (V_{O1}/V_{O2}).

Fig 12. Test circuit for measuring crosstalk between switches

13. Package outline

XQFN10U: plastic extremely thin quad flat package; no leads; 10 terminals; UTLP based; body 2 x 1.55 x 0.5 mm **SOT1049-2**



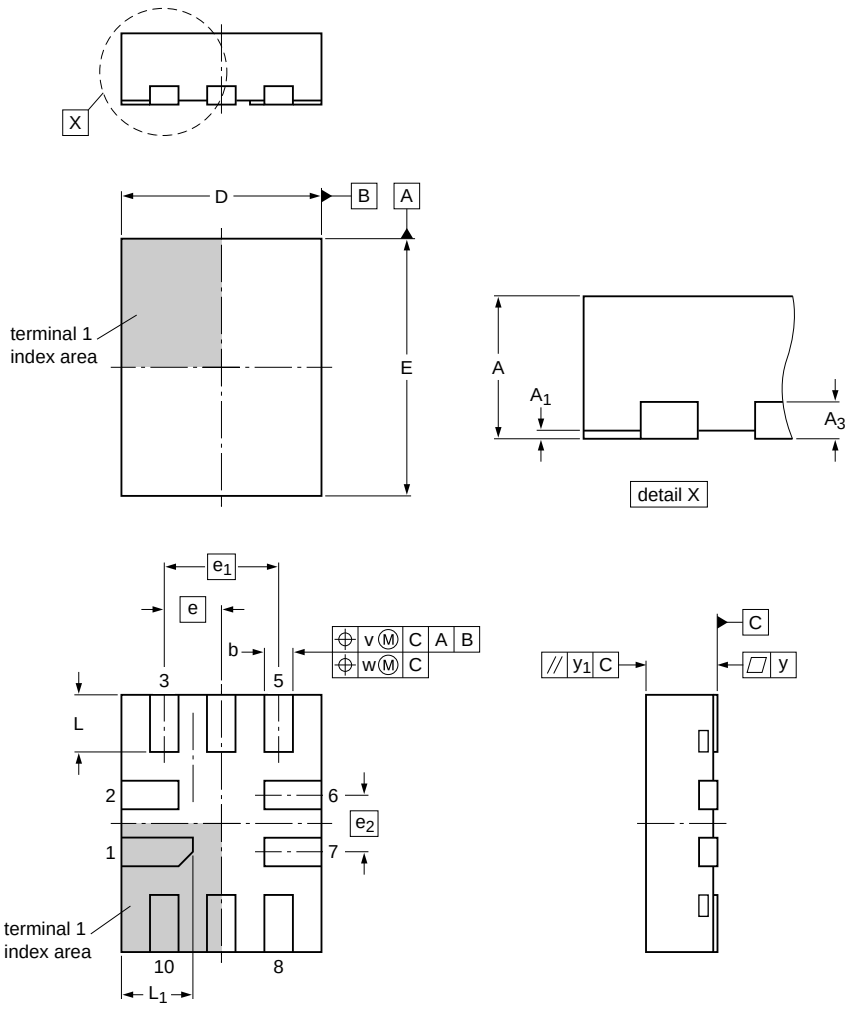
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	b	D	E	e	e_1	e_2	e_3	L	L_1	v	w	y	y_1
mm	max	0.50	0.05	0.30	1.65	2.1	0.58	0.5	1.16	1.5	0.4	0.15	0.1	0.05	0.1	0.05
	nom		0.03	0.23	1.55	2.0					0.3	0.08				
	min		0.00	0.15	1.45	1.9					0.2	0.00				

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1049-2	- - -	MO-255	- - -			~~08-04-22~~ 10-02-05

Fig 13. Package outline SOT1049-2 (XQFN10U)

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	1.5	1.9				0.45	0.55				
mm	nom			0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.3	1.7				0.35	0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	- - -	- - -	- - -		~~09-12-28~~ 09-12-29

Fig 14. Package outline SOT1160-1 (XQFN10)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX3DV42 v.1	20120103	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contact information

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

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