



NX3008CBKV

30 / 30 V, 400 / 220 mA N/P-channel Trench MOSFET

28 December 2022

Product data sheet

1. General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV

3. Applications

- Level shifter
- Power supply converter
- Loadswitch
- Switching circuits

4. Quick reference data

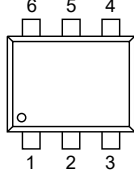
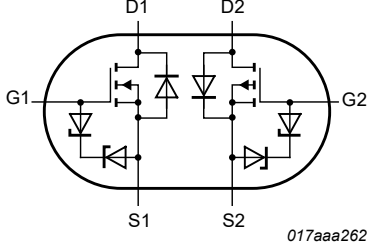
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	400	mA
TR2 (P-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-30	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-220	mA
TR1 (N-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 350\text{ mA}; T_j = 25\text{ °C}$	-	1	1.4	Ω
TR2 (P-channel), Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -200\text{ mA}; T_j = 25\text{ °C}$	-	2.8	4.1	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>SOT666</p>	 <p>017aaa262</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX3008CBKV	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT666

7. Marking

Table 4. Marking codes

Type number	Marking code
NX3008CBKV	AC

8. Limiting values

Table 5. Limiting values

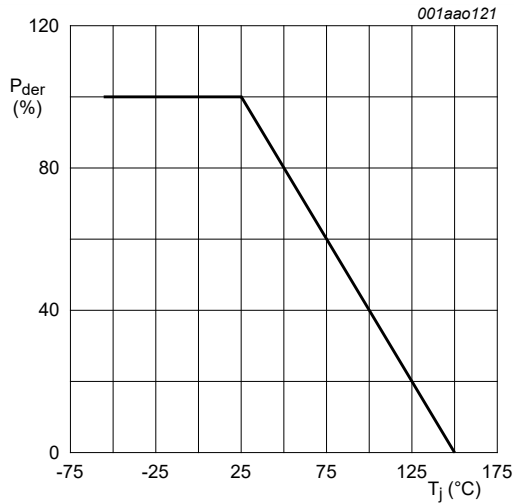
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1 (N-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	400	mA
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	260	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	1.6	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	330	mW
			[1]	-	390	mW
		$T_{sp} = 25\text{ °C}$		-	1090	mW
TR2 (P-channel)						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-220	mA
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-140	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-0.9	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	330	mW
			[1]	-	390	mW
		$T_{sp} = 25\text{ °C}$		-	1090	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	500	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
TR1 (N-channel), Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	400	mA
TR2 (P-channel), Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-220	mA
TR1 N-channel), ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V
TR2 (P-channel), ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

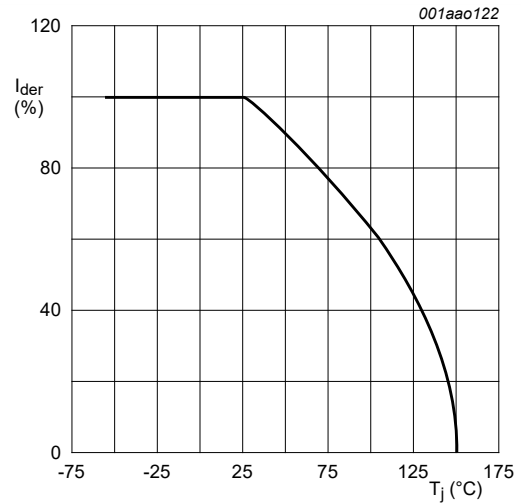
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[3] Measured between all pins.



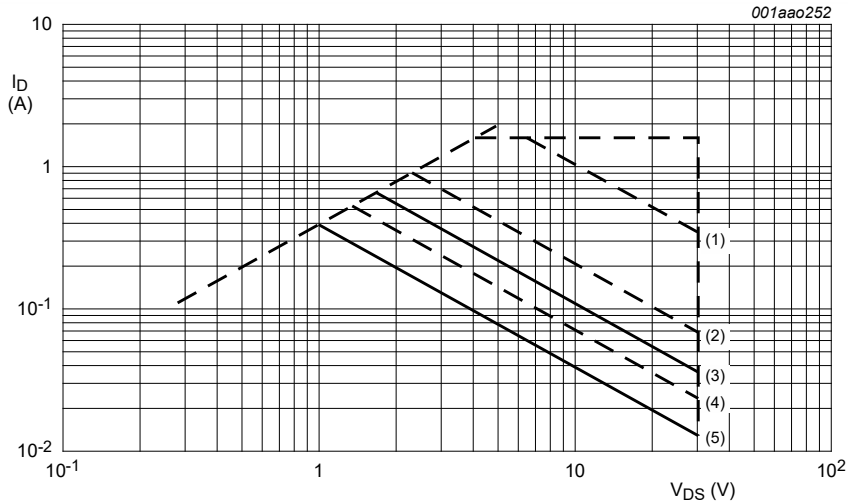
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}}$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



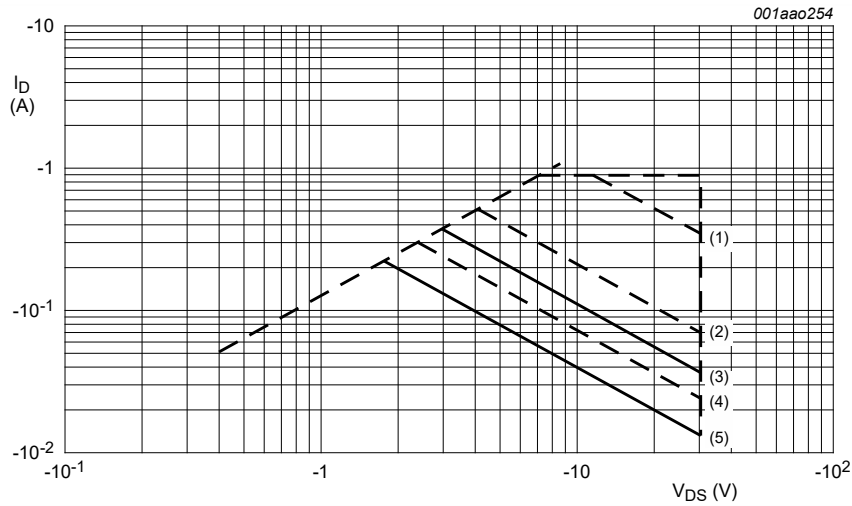
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature



- I_{DM} is a single pulse
- (1) $t_p = 1$ ms
 - (2) $t_p = 10$ ms
 - (3) DC; $T_{sp} = 25^\circ\text{C}$
 - (4) $t_p = 100$ ms
 - (5) DC; $T_{amb} = 25^\circ\text{C}$; 1 cm^2 drain mounting pad

Fig. 3. Safe operating area TR1 (N-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage



I_{DM} is a single pulse
 (1) $t_p = 1 \text{ ms}$
 (2) $t_p = 10 \text{ ms}$
 (3) DC; $T_{sp} = 25 \text{ }^\circ\text{C}$
 (4) $t_p = 100 \text{ ms}$
 (5) DC; $T_{amb} = 25 \text{ }^\circ\text{C}$; 1 cm^2 drain mounting pad

Fig. 4. Safe operating area TR2 (P-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage

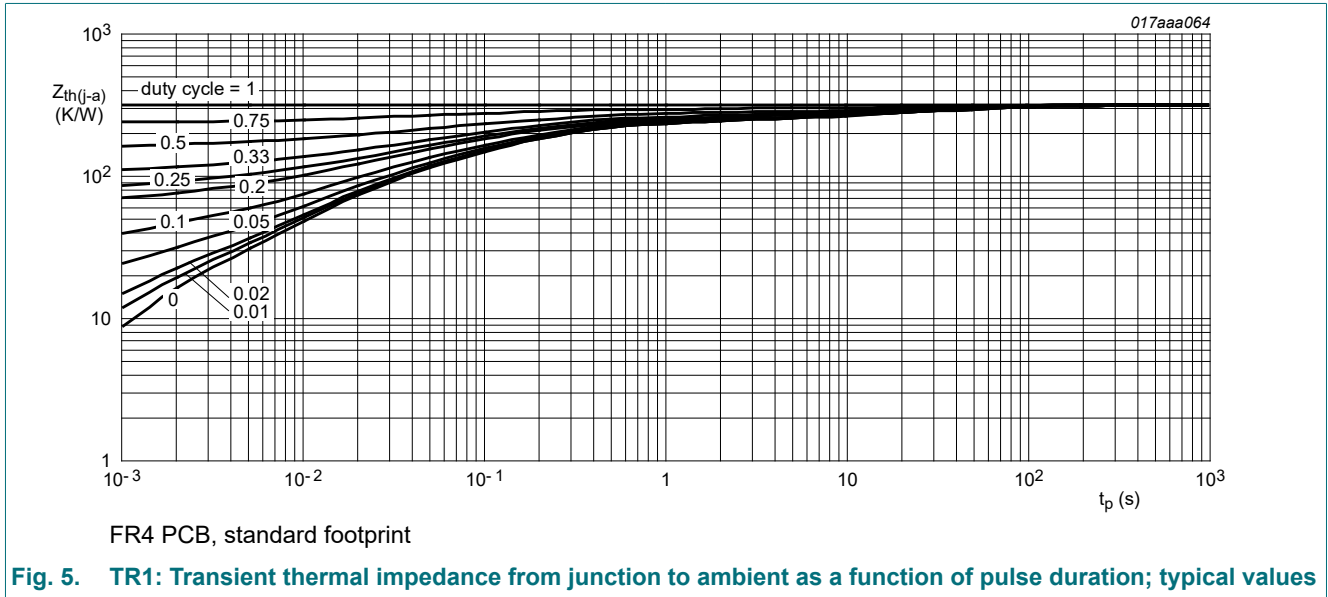
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (N-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
TR2 (P-channel)							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380	K/W
			[2]	-	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².



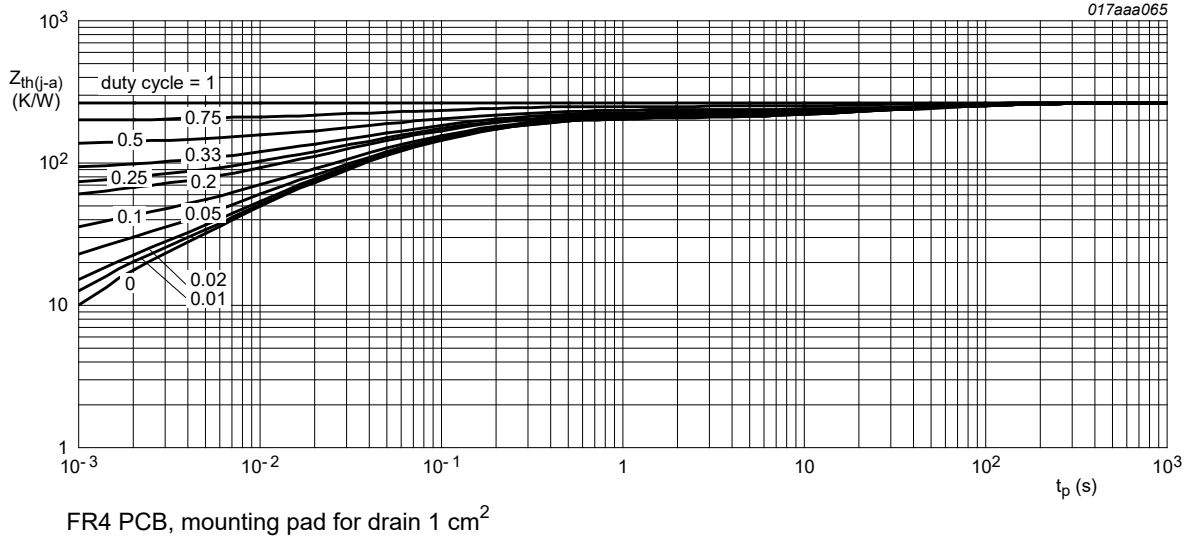


Fig. 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

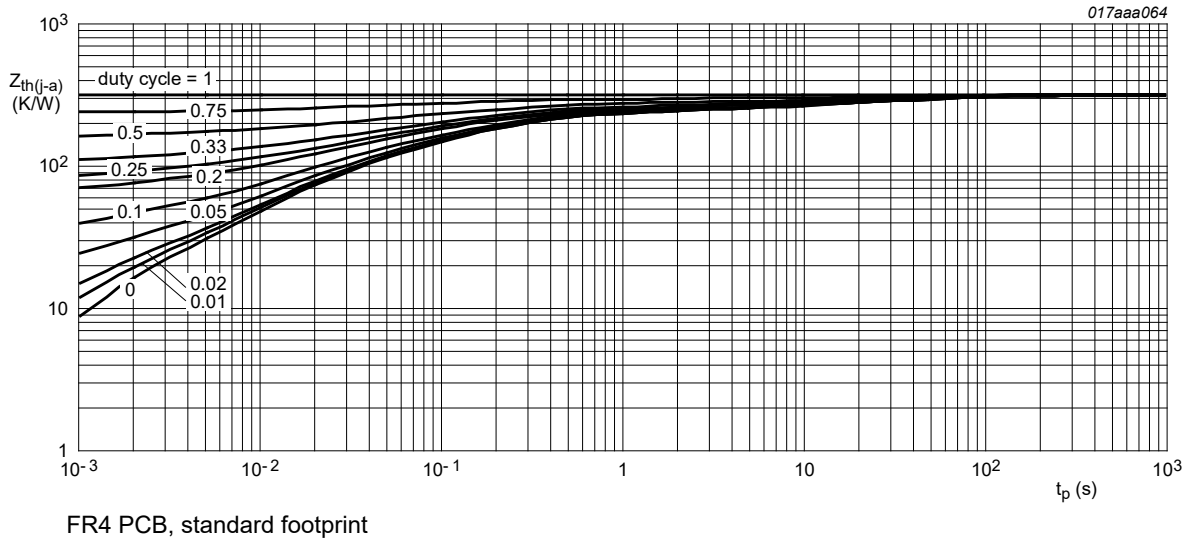


Fig. 7. TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

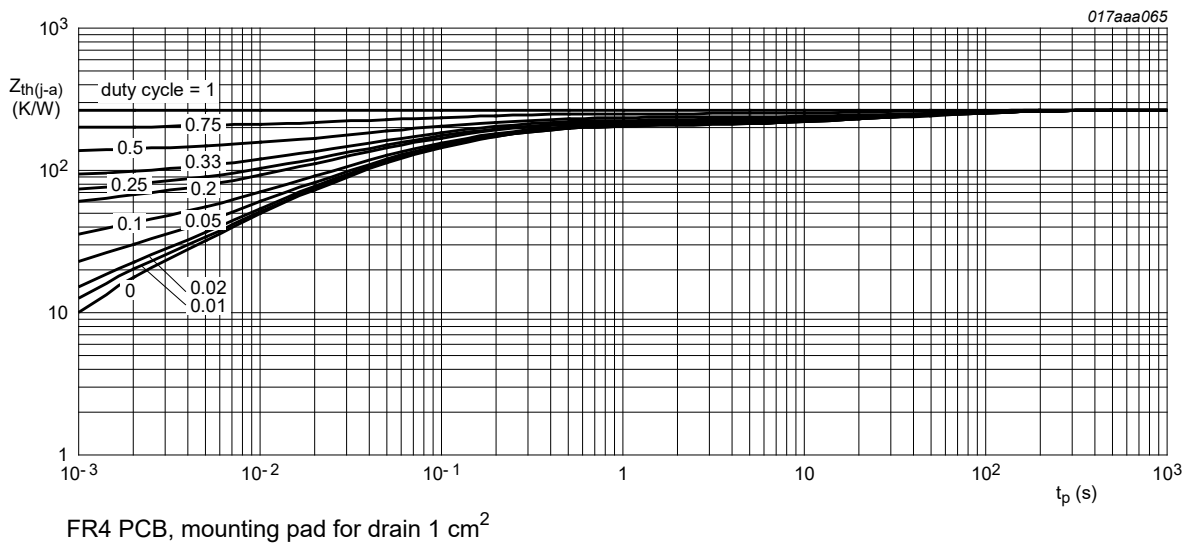


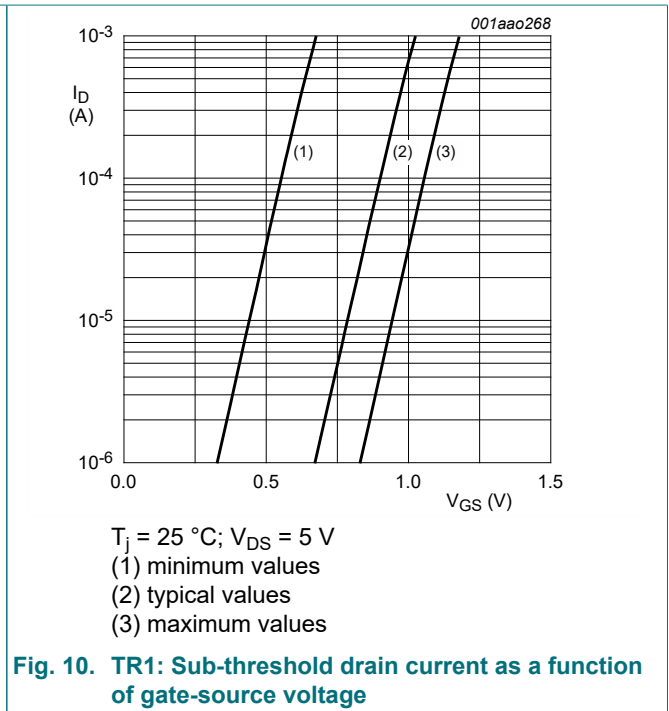
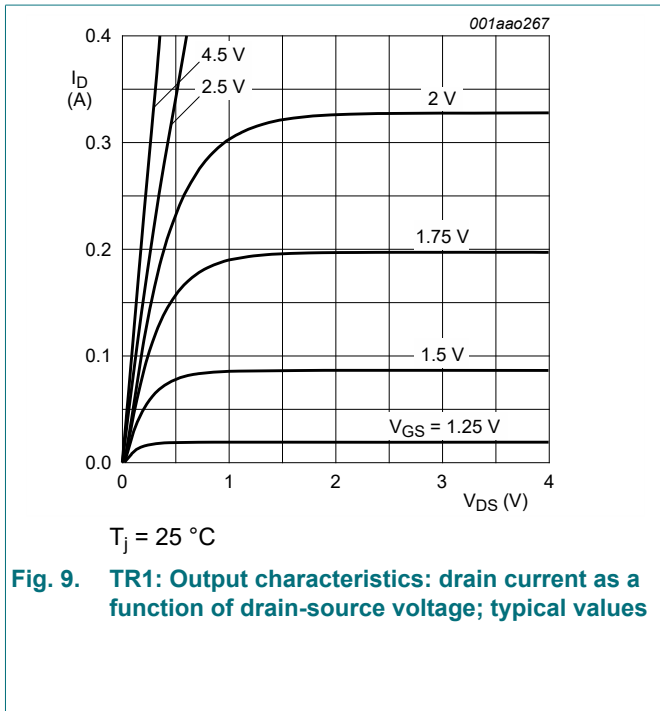
Fig. 8. TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

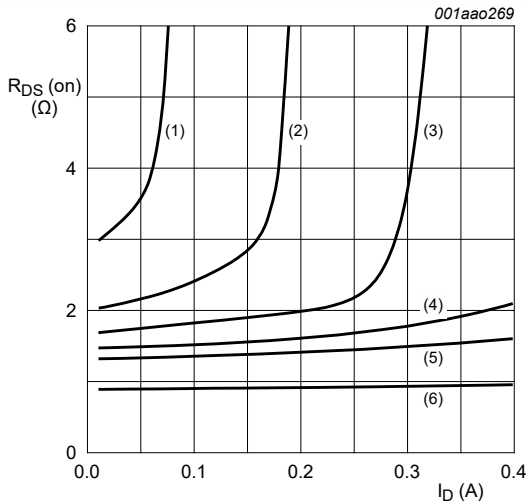
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1 (N-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	0.6	0.9	1.1	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.2	1	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.2	1	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	-	nA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	-	nA
		$V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	1	-	nA
		$V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	1	-	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 350 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1	1.4	Ω
		$V_{GS} = 4.5 V; I_D = 350 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	1.8	2.5	Ω
		$V_{GS} = 2.5 V; I_D = 200 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	1.4	2.1	Ω
		$V_{GS} = 1.8 V; I_D = 10 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2	2.8	Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V; I_D = 350 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	310	-	mS
TR2 (P-channel), Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	-0.6	-0.9	-1.1	V
I_{DSS}	drain leakage current	$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.2	-1	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.2	-1	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-10	-	nA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-10	-	nA
		$V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-1	-	nA
		$V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-1	-	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.8	4.1	Ω
		$V_{GS} = -2.5 V; I_D = -10 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	5.3	6.5	Ω
		$V_{GS} = -4.5 V; I_D = -200 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	5.3	7.8	Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V; I_D = -200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	160	-	mS
TR1 (N-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 V; I_D = 400 \text{ mA}; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$	-	0.52	0.68	nC
Q_{GS}	gate-source charge		-	0.17	-	nC
Q_{GD}	gate-drain charge		-	0.08	-	nC

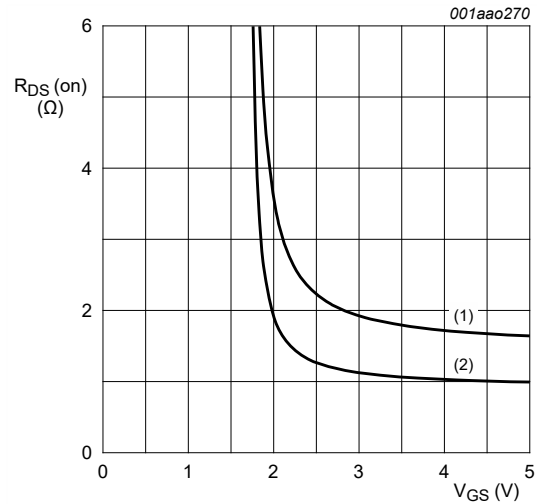
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	34	50	pF
C_{oss}	output capacitance		-	6.5	-	pF
C_{rss}	reverse transfer capacitance		-	2.2	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 250\ \Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 6\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	15	30	ns
t_r	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	69	138	ns
t_f	fall time		-	19	-	ns
TR2 (P-channel), Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -15\text{ V}; I_D = -200\text{ mA}; V_{GS} = -4.5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.55	0.72	nC
Q_{GS}	gate-source charge		-	0.23	-	nC
Q_{GD}	gate-drain charge		-	0.09	-	nC
C_{iss}	input capacitance	$V_{DS} = -15\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	31	46	pF
C_{oss}	output capacitance		-	6.5	-	pF
C_{rss}	reverse transfer capacitance		-	2.3	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -20\text{ V}; R_L = 250\ \Omega; V_{GS} = -4.5\text{ V}; R_{G(ext)} = 6\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	19	38	ns
t_r	rise time		-	30	-	ns
$t_{d(off)}$	turn-off delay time		-	65	130	ns
t_f	fall time		-	38	-	ns
TR1 (N-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = 350\text{ mA}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	0.47	0.85	1.2	V
TR2 (P-channel), Source-drain diode characteristics						
V_{SD}	source-drain voltage	$I_S = -200\text{ mA}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-0.47	-0.88	-1.2	V





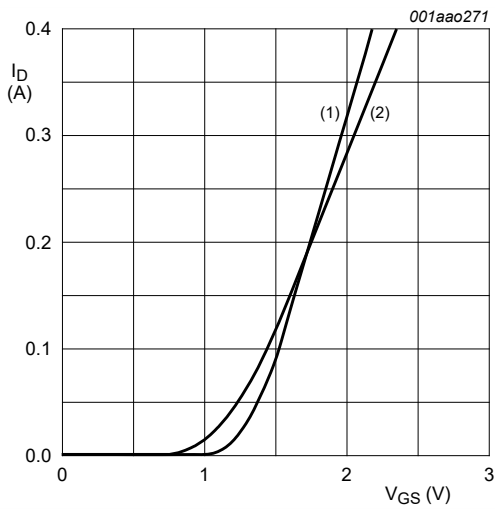
$T_j = 25\text{ }^\circ\text{C}$
 (1) $V_{GS} = 1.5\text{ V}$
 (2) $V_{GS} = 1.75\text{ V}$
 (3) $V_{GS} = 2.0\text{ V}$
 (4) $V_{GS} = 2.25\text{ V}$
 (5) $V_{GS} = 2.5\text{ V}$
 (6) $V_{GS} = 4.5\text{ V}$

Fig. 11. TR1: Drain-source on-state resistance as a function of drain current; typical values



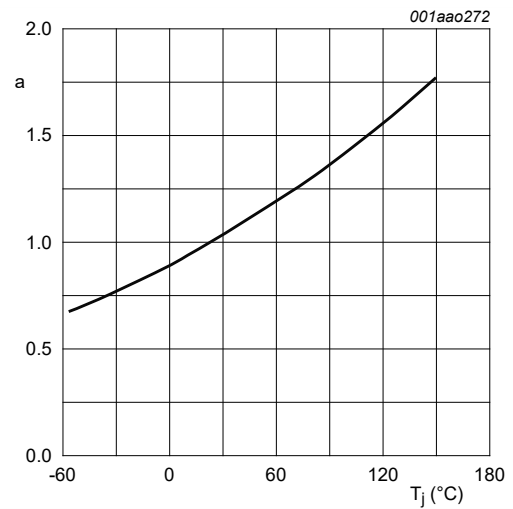
$I_D = 350\text{ mA}$
 (1) $T_j = 150\text{ }^\circ\text{C}$
 (2) $T_j = 25\text{ }^\circ\text{C}$

Fig. 12. TR1: Drain-source on-state resistance as a function of gate-source voltage; typical values



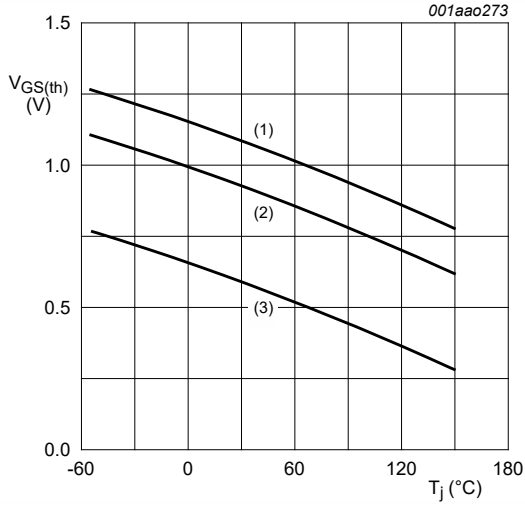
$V_{DS} > I_D \times R_{DS(on)}$
 (1) $T_j = 25\text{ }^\circ\text{C}$
 (2) $T_j = 150\text{ }^\circ\text{C}$

Fig. 13. TR1: Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

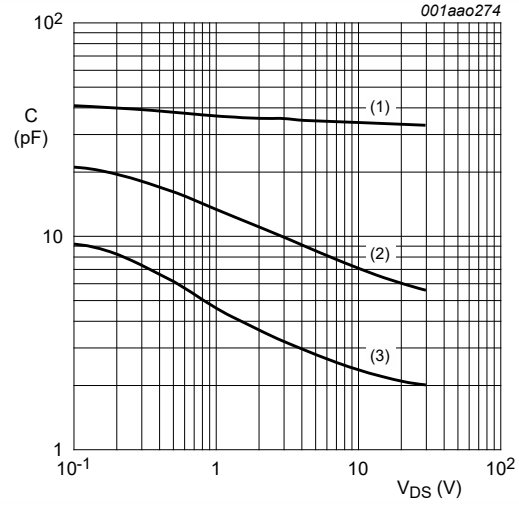
Fig. 14. TR1: Normalized drain-source on-state resistance as a function of junction temperature; typical values



$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

- (1) maximum values
- (2) typical values
- (3) minimum values

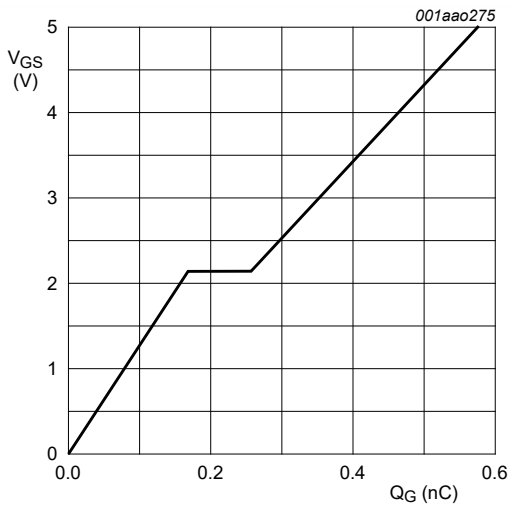
Fig. 15. TR1: Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

- (1) C_{iss}
- (2) C_{oss}
- (3) C_{rss}

Fig. 16. TR1: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 350 \text{ mA}; V_{DS} = 15 \text{ V}; T_{amb} = 25 \text{ °C}$

Fig. 17. TR1: Gate-source voltage as a function of gate charge; typical values

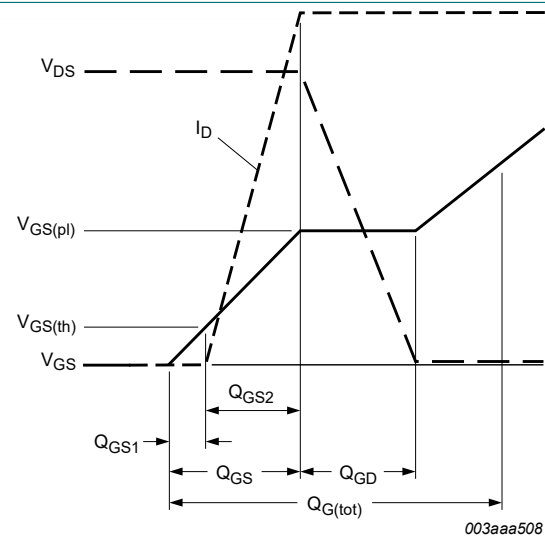
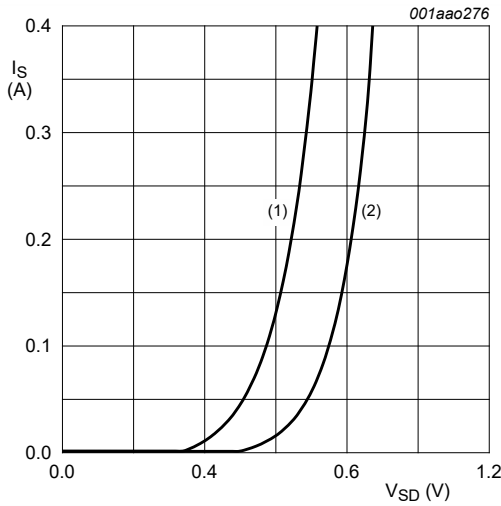
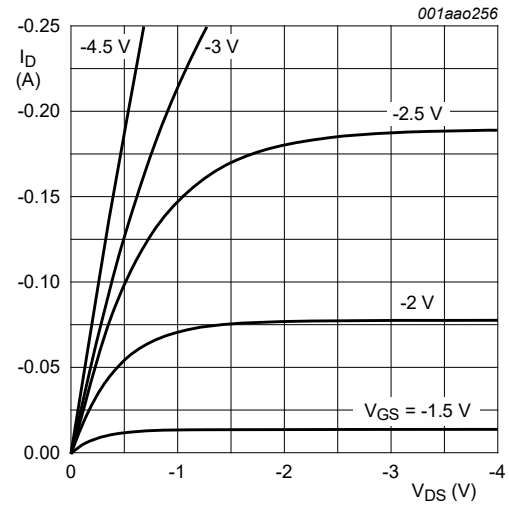


Fig. 18. Gate charge waveform definitions



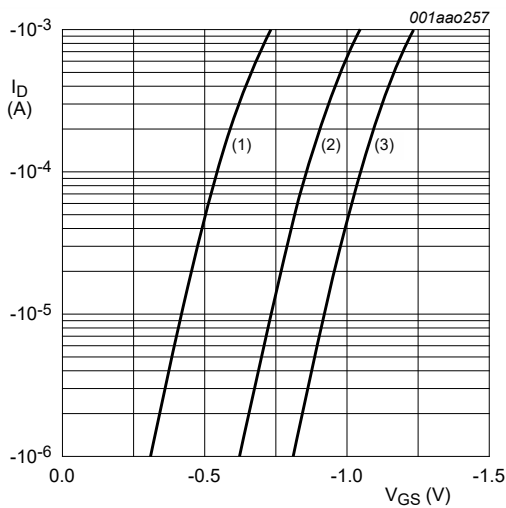
$V_{GS} = 0\text{ V}$
 (1) $T_j = 150\text{ °C}$
 (2) $T_j = 25\text{ °C}$

Fig. 19. TR1: Source current as a function of source-drain voltage; typical values



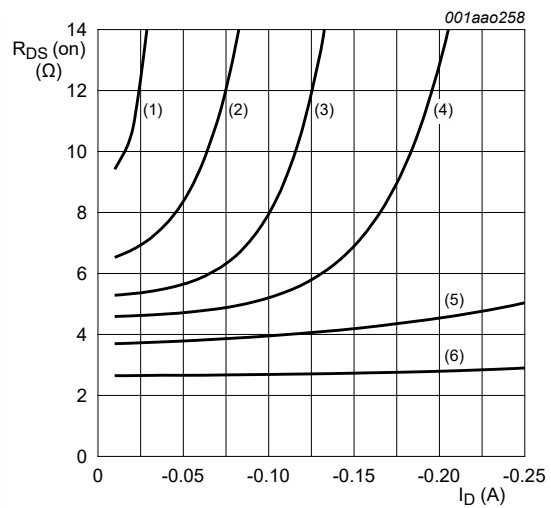
$T_j = 25\text{ °C}$

Fig. 20. TR2: Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25\text{ °C}; V_{DS} = -5\text{ V}$
 (1) minimum values
 (2) typical values
 (3) maximum values

Fig. 21. TR2: Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ °C}$
 (1) $V_{GS} = -1.75\text{ V}$
 (2) $V_{GS} = -2.0\text{ V}$
 (3) $V_{GS} = -2.25\text{ V}$
 (4) $V_{GS} = -2.5\text{ V}$
 (5) $V_{GS} = -3.0\text{ V}$
 (6) $V_{GS} = -4.5\text{ V}$

Fig. 22. TR2: Drain-source on-state resistance as a function of drain current; typical values

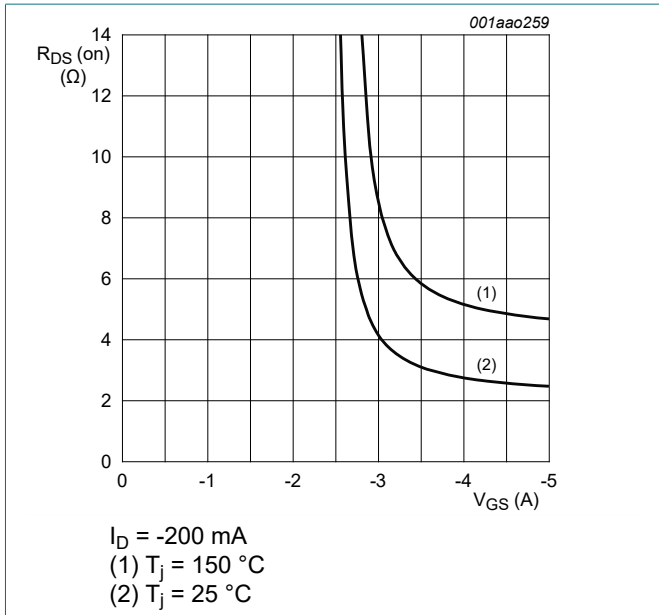


Fig. 23. TR2: Drain-source on-state resistance as a function of gate-source voltage; typical values

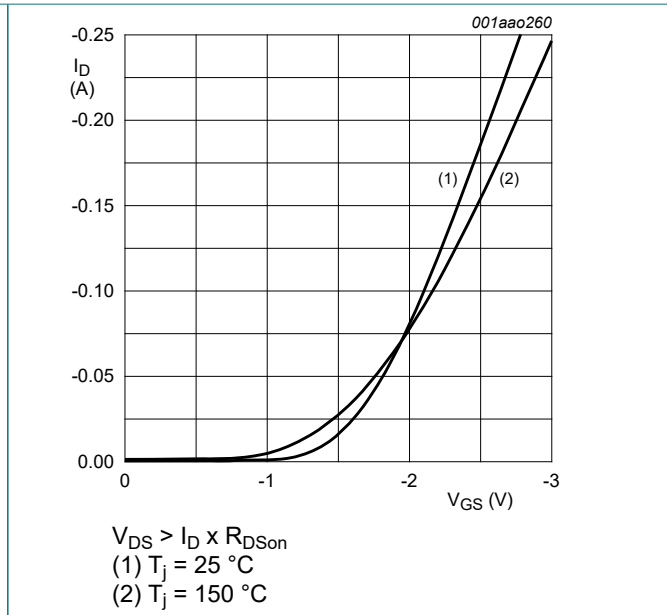


Fig. 24. TR2: Transfer characteristics: drain current as a function of gate-source voltage; typical values

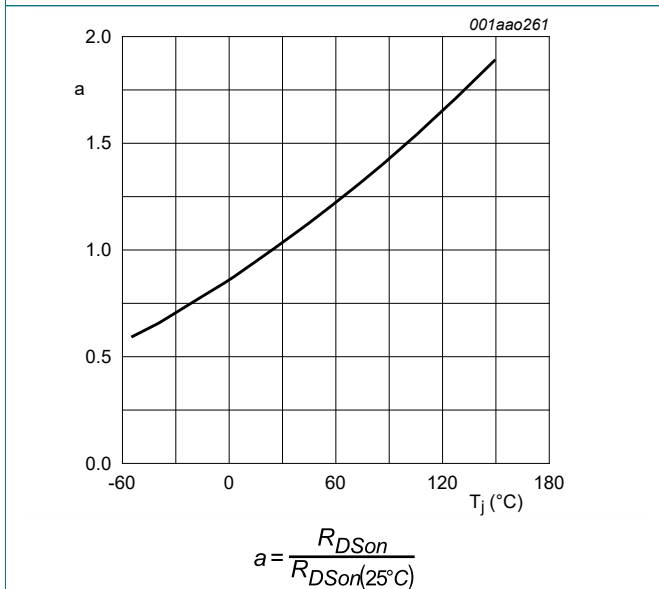


Fig. 25. TR2: Normalized drain-source on-state resistance as a function of junction temperature; typical values

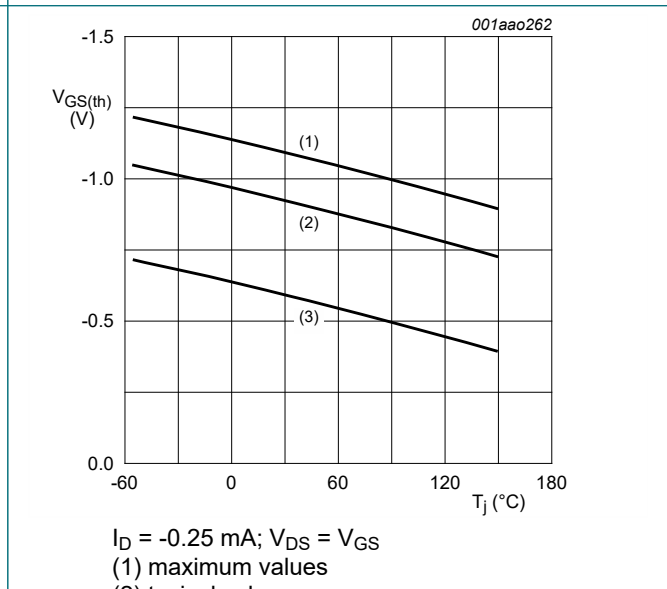
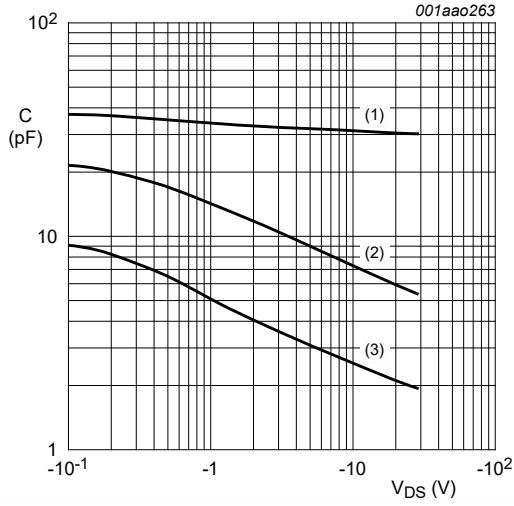


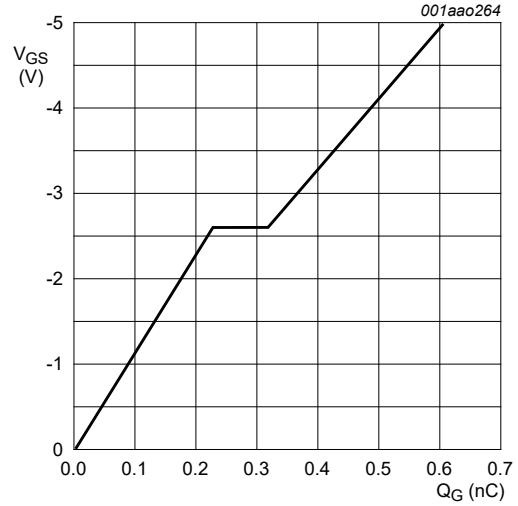
Fig. 26. TR2: Gate-source threshold voltage as a function of junction temperature



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

- (1) C_{iss}
- (2) C_{oss}
- (3) C_{rss}

Fig. 27. TR2: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = -200 \text{ mA}; V_{DS} = -15 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 28. Gate-source voltage as a function of gate charge; typical values

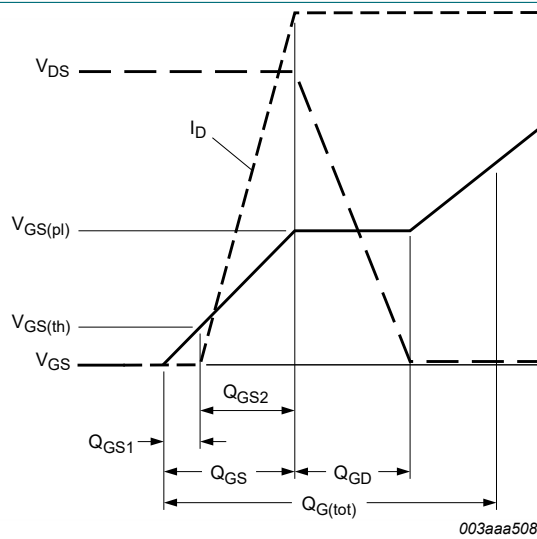
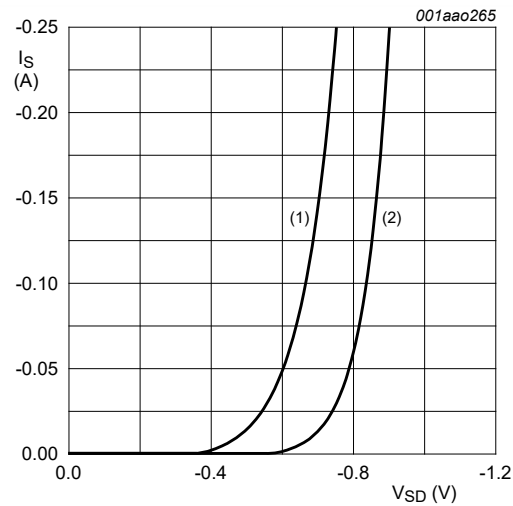


Fig. 29. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$
 (1) $T_j = 150 \text{ }^\circ\text{C}$
 (2) $T_j = 25 \text{ }^\circ\text{C}$

Fig. 30. TR2: Source current as a function of source-drain voltage; typical values

11. Test information

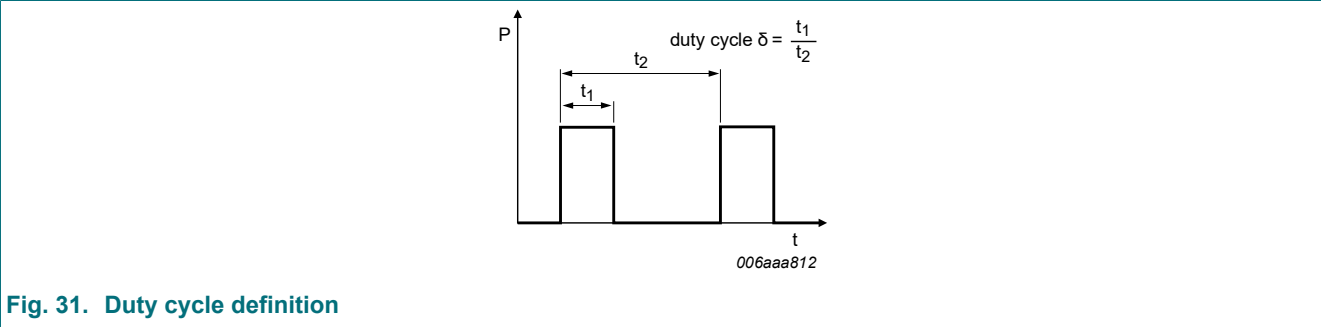


Fig. 31. Duty cycle definition

12. Package outline

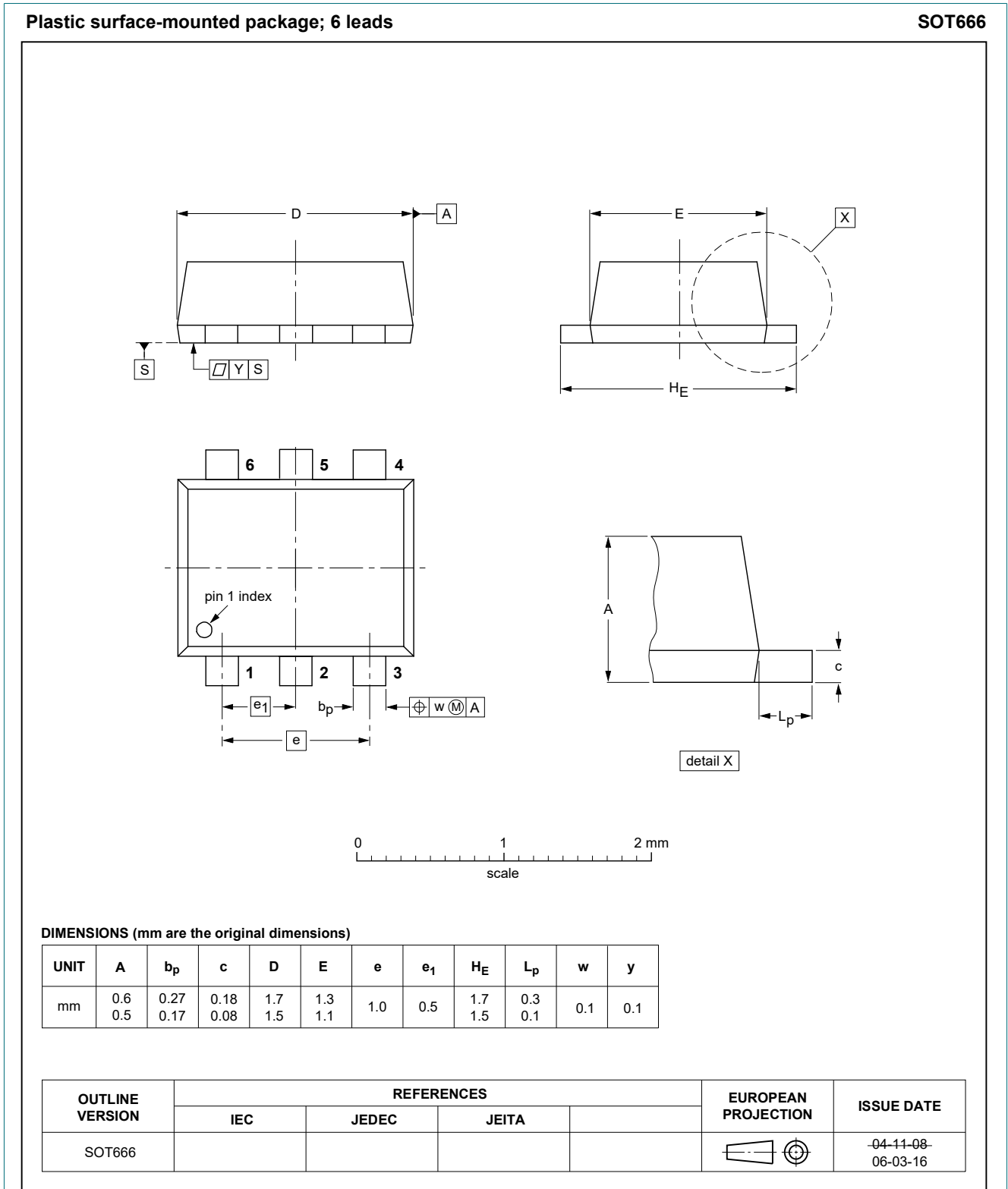


Fig. 32. Package outline SOT666

13. Soldering

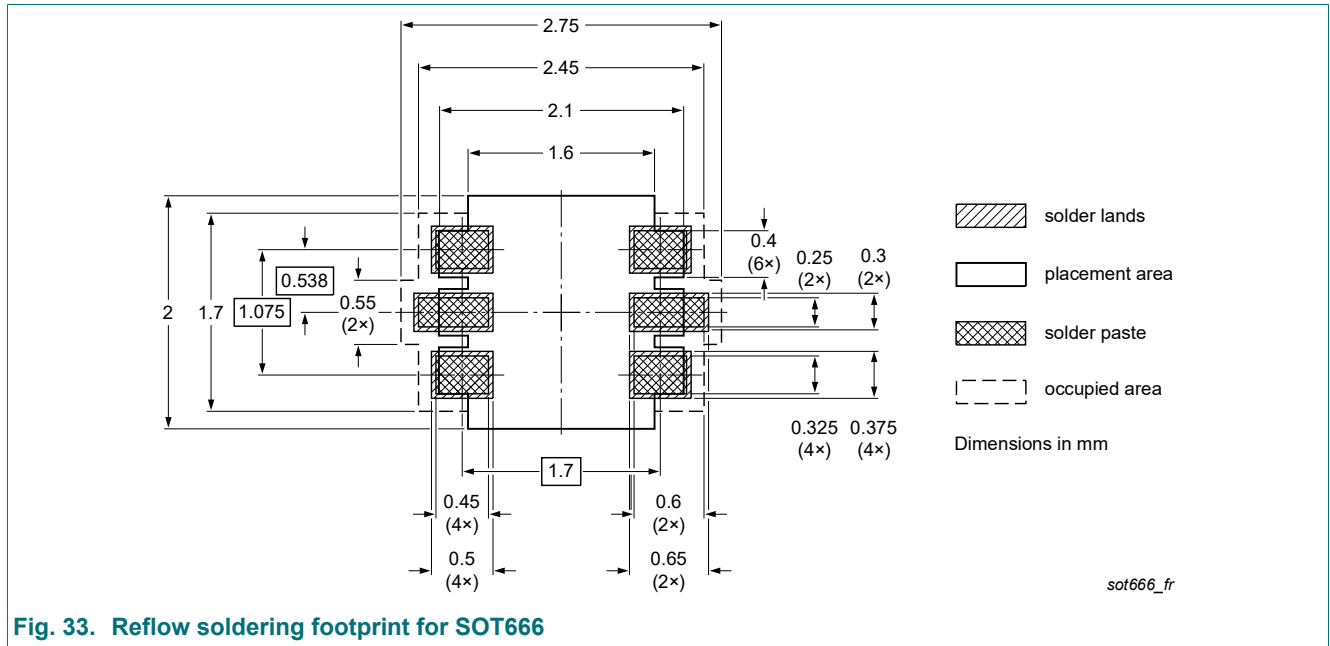


Fig. 33. Reflow soldering footprint for SOT666

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX3008CBKV v.2	20221228	Product data sheet	-	NX3008CBKV v.1
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia• Legal texts have been adapted to the new company name where appropriate• Product changed to non-automotive qualification			
NX3008CBKV v.1	20110729	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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