

# NTMS4704N

## Power MOSFET

30 V, 12.3 A, Single N-Channel, SO-8



ON Semiconductor®

<http://onsemi.com>

### Features

- Low  $R_{DS(on)}$
- Low Gate Charge
- Standard SO-8 Single Package
- Pb-Free Package is Available

### Applications

- Notebooks, Graphics Cards
- Synchronous Rectification
- High Side Switch
- DC-DC Converters

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	$I_D$ MAX
30 V	7.5 m $\Omega$ @ 10 V	12.3 A
	10 m $\Omega$ @ 4.5 V	

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

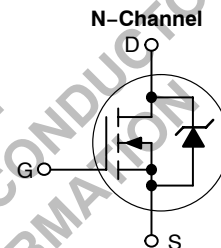
Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		$V_{DSS}$	30	V	
Gate-to-Source Voltage		$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	10	A
			$T_A = 85^\circ\text{C}$	7.3	
	$t \leq 10$ s	$T_A = 25^\circ\text{C}$	12.3		
Power Dissipation (Note 1)	Steady State	$P_D$	$T_A = 25^\circ\text{C}$	1.6	W
			$t \leq 10$ s	2.3	
Continuous Drain Current (Note 2)	Steady State	$I_D$	$T_A = 25^\circ\text{C}$	7.6	A
			$T_A = 85^\circ\text{C}$	5.4	
Power Dissipation (Note 2)		$P_D$	$T_A = 25^\circ\text{C}$	0.86	W
Pulsed Drain Current	$t_p = 10$ $\mu\text{s}$	$I_{DM}$	37	A	
Operating Junction and Storage Temperature		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		$I_S$	2.3	A	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 25$ V, $V_{GS} = 10$ V, $I_L$ Peak = 7.5 A, $L = 10$ mH, $R_G = 25$ $\Omega$ )		$E_{AS}$	200	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 secs)		$T_L$	260	$^\circ\text{C}$	

### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	80.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	55	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	145	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

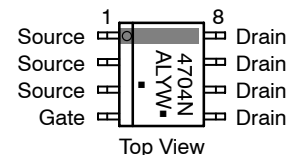
1. Surfaced mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surfaced mounted on FR4 board using the minimum recommended pad size.



### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8  
CASE 751  
STYLE 12



4704N = Device Code  
A = Assembly Location  
L = WaferLot  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4704NR2	SO-8	2500/Tape & Reel
NTMS4704NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMS4704N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			28		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1.0	$\mu\text{A}$
					50	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.0		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12.3\text{ A}$		7.5	9.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		10	12.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		20		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{iss}$			1225		pF
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 20\text{ V}$		580		
Reverse Transfer Capacitance	$C_{rss}$			125		
Total Gate Charge	$Q_{G(TOT)}$			12	17	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		1.6		
Gate-to-Source Charge	$Q_{GS}$			3.25		
Gate-to-Drain Charge	$Q_{GD}$			5.25		
Gate Resistance	$R_G$			1.8		$\Omega$

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$			8.2		ns
Rise Time	$t_r$	$V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 3.0\ \Omega$		5.4		
Turn-Off Delay Time	$t_{d(off)}$			28.4		
Fall Time	$t_f$			10.5		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$	$T_J = 25^\circ\text{C}$		0.75	1.0	V
			$T_J = 125^\circ\text{C}$		0.56		
Reverse Recovery Time	$t_{RR}$				35		ns
Charge Time	$t_a$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 2.3\text{ A}$			18		
Discharge Time	$t_b$				17		
Reverse Recovery Charge	$Q_{RR}$				33		nC

3. Pulse Test: pulse width = 300  $\mu\text{s}$ , duty cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

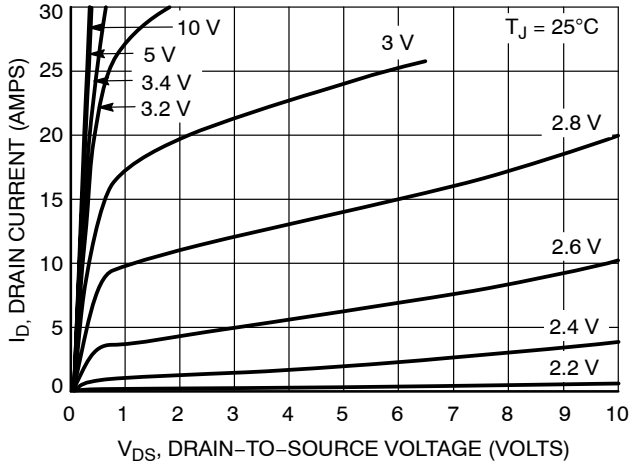


Figure 1. On-Region Characteristics

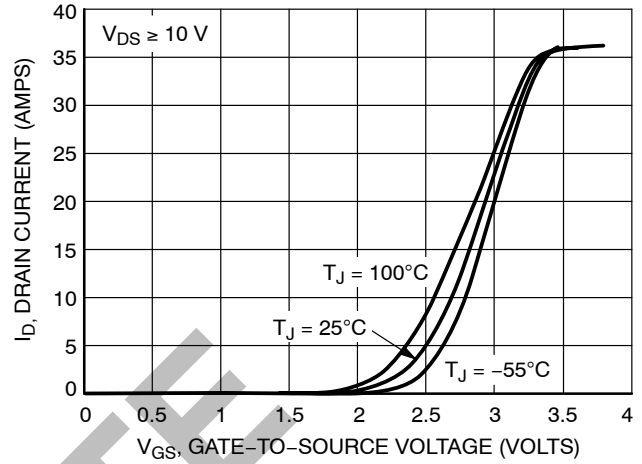


Figure 2. Transfer Characteristics

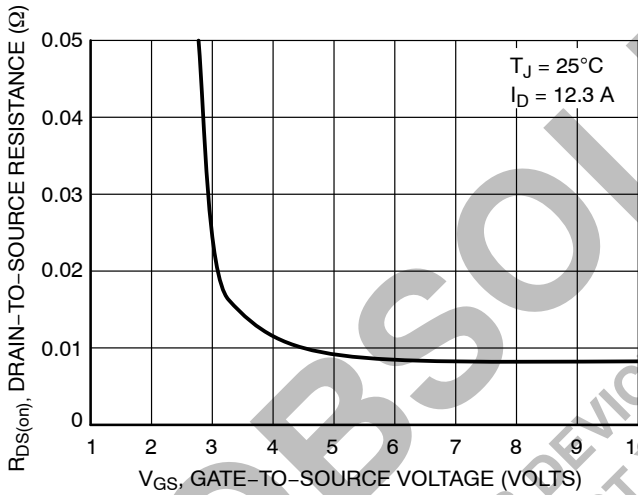


Figure 3. On-Resistance vs. Gate-to-Source Voltage

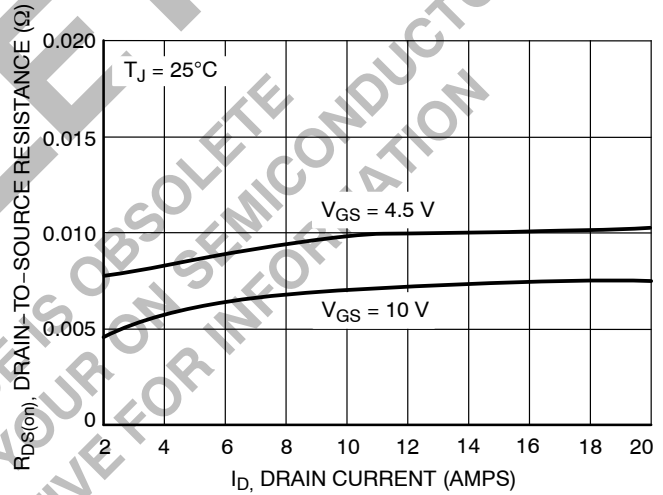


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

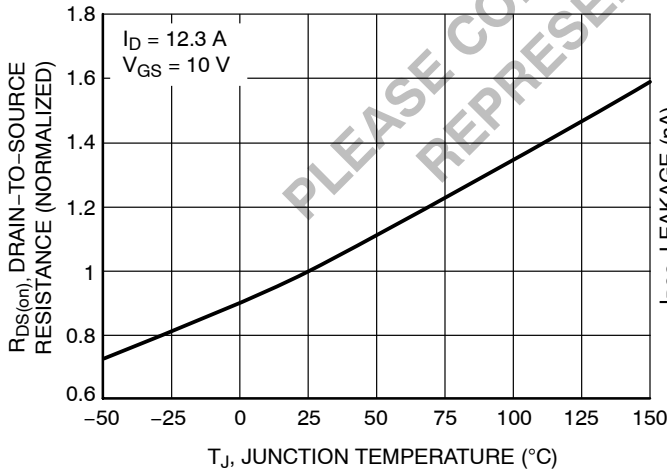


Figure 5. On-Resistance Variation with Temperature

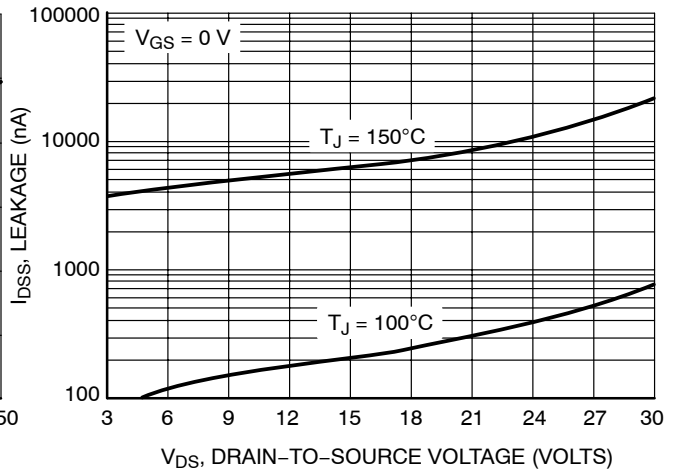


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NTMS4704N

## TYPICAL PERFORMANCE CURVES

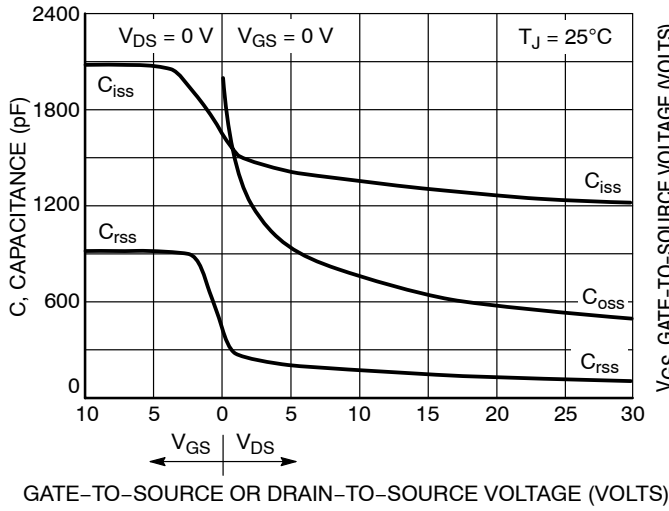


Figure 7. Capacitance Variation

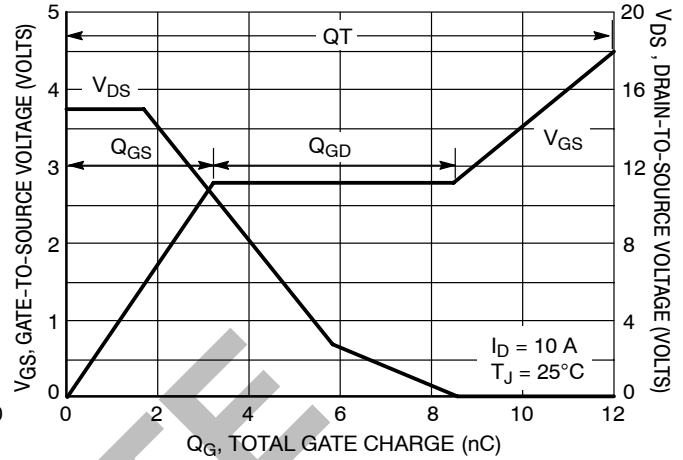


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

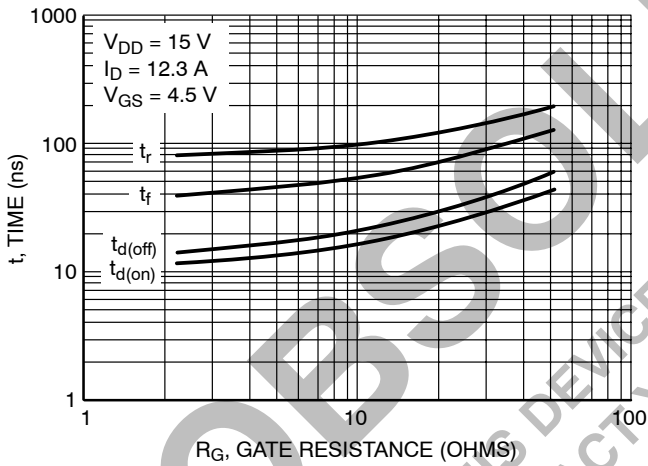


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

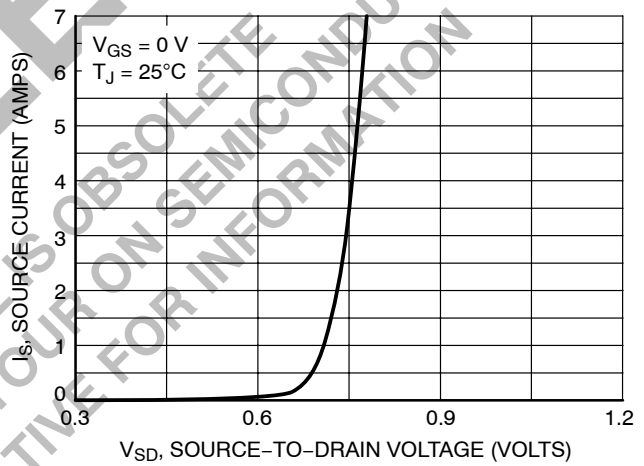
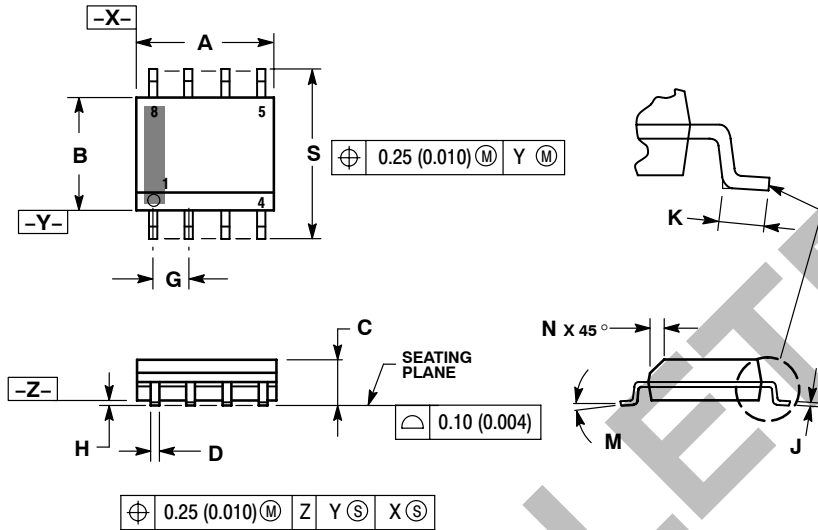


Figure 10. Diode Forward Voltage vs. Current

# NTMS4704N

## PACKAGE DIMENSIONS

SOIC-8  
CASE 751-07  
ISSUE AG

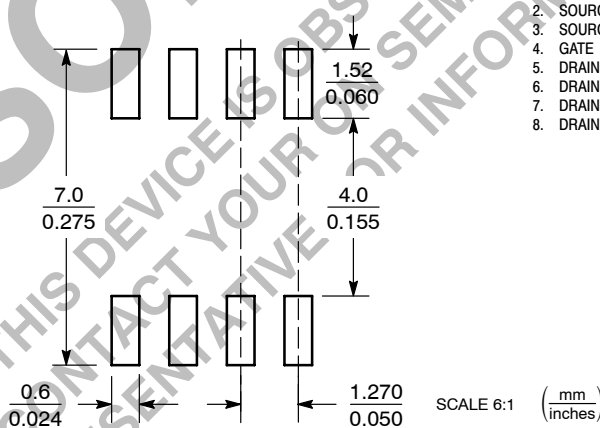


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



**STYLE 12:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:** Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative