

Dual N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
20	0.022 at V _{GS} = 4.5 V	4.8	1.8 nC
	0.028 at V _{GS} = 2.5 V	3.3	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

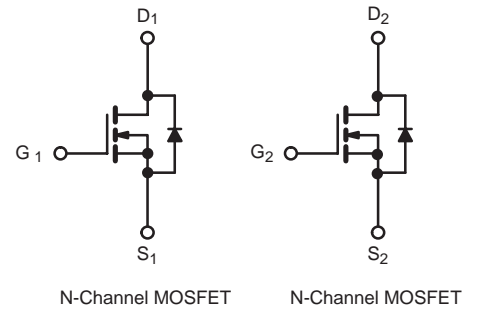
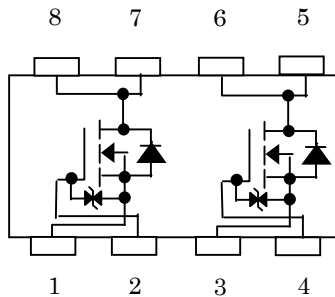
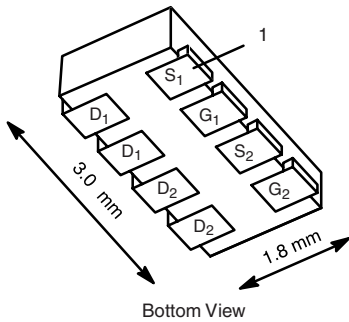


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch for Portable Applications
- DC/DC Converters

1206-8 ChipFET[®] (Dual)



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	20	V
Gate-Source Voltage		V _{GS}	± 12	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	4.8	A
	T _C = 70 °C		3	
	T _A = 25 °C		3.4 ^{b, c}	
	T _A = 70 °C		2.7 ^{b, c}	
Pulsed Drain Current		I _{DM}	15	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	1.17	
	T _A = 25 °C		0.95 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	1.4	W
	T _C = 70 °C		0.9	
	T _A = 25 °C		1.14 ^{b, c}	
	T _A = 70 °C		0.73 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 5 s	R _{thJA}	93	110	°C/W
Maximum Junction-to-Foot	Steady State	R _{thJF}	75	90	

Notes:

- T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- Maximum under steady state conditions is 150 °C/W.

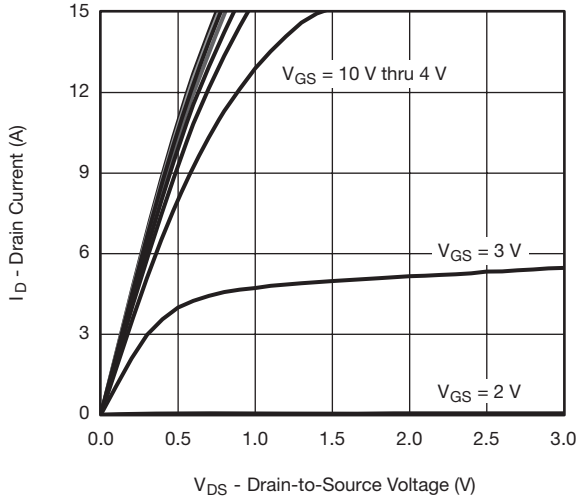
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		29		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.2	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	10			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 3.4\text{ A}$		0.017	0.022	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 3.0\text{ A}$		0.023	0.028	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 3.4\text{ A}$		10		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		235		μF
Output Capacitance	C_{oss}			45		
Reverse Transfer Capacitance	C_{rss}			16		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 3.4\text{ A}$		3.7	6	nC
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 3.4\text{ A}$		1.8	3	
Gate-Source Charge	Q_{gs}			0.74		
Gate-Drain Charge	Q_{gd}			0.42		
Gate Resistance	R_g	$f = 1\text{ MHz}$	1	5	10	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 5.6\text{ }\Omega$ $I_D \cong 2.7\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		10	20	ns
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			10	20	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 5.6\text{ }\Omega$ $I_D \cong 2.7\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		5	10	
Rise Time	t_r			15	30	
Turn-Off Delay Time	$t_{d(off)}$			10	20	
Fall Time	t_f			10	20	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			1.17	A
Pulse Diode Forward Current	I_{SM}				15	
Body Diode Voltage	V_{SD}	$I_S = 2.7\text{ A}, V_{GS} = 0\text{ V}$		0.85	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 2.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		10	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			4	10	nC
Reverse Recovery Fall Time	t_a			6		ns
Reverse Recovery Rise Time	t_b			4		

Notes:

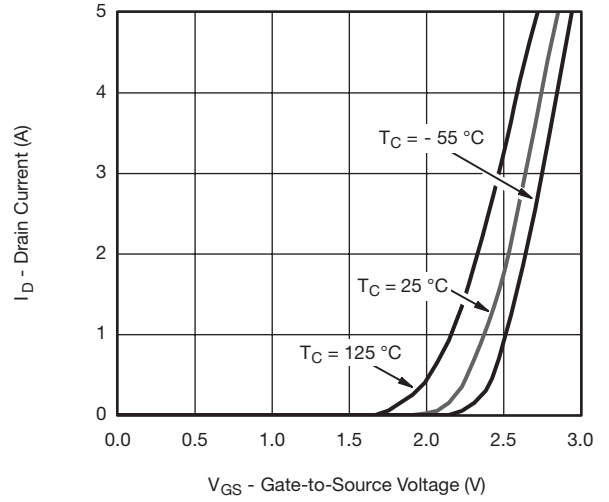
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

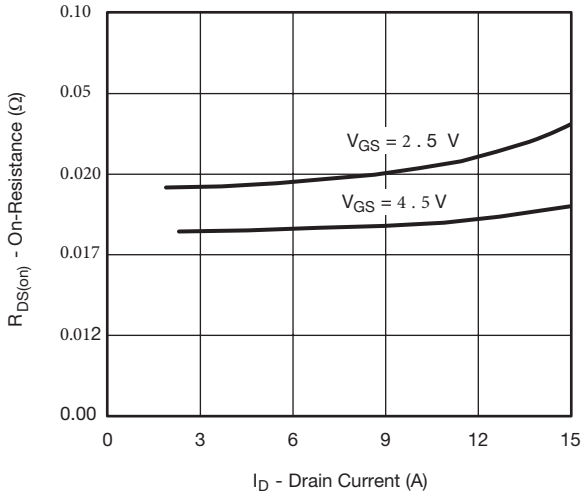
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



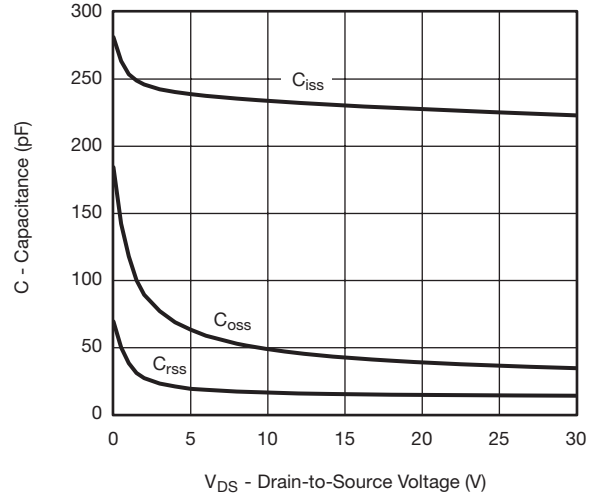
Output Characteristics



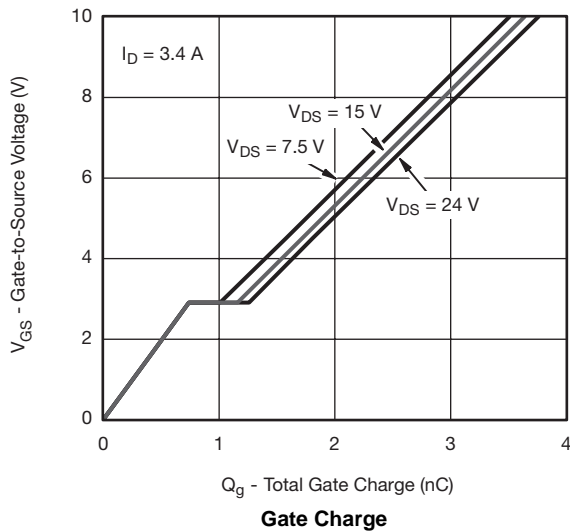
Transfer Characteristics



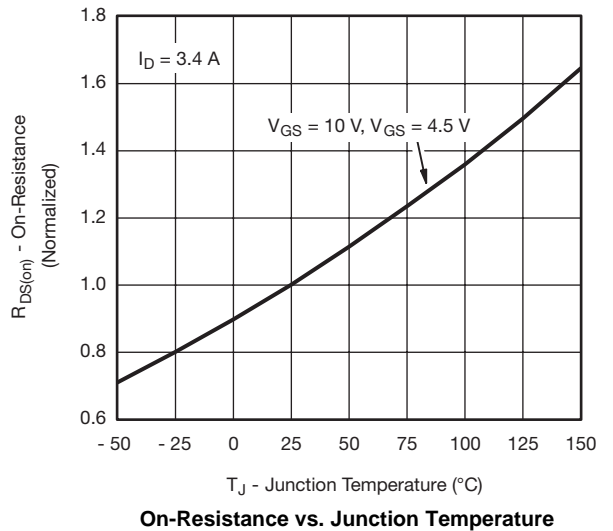
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

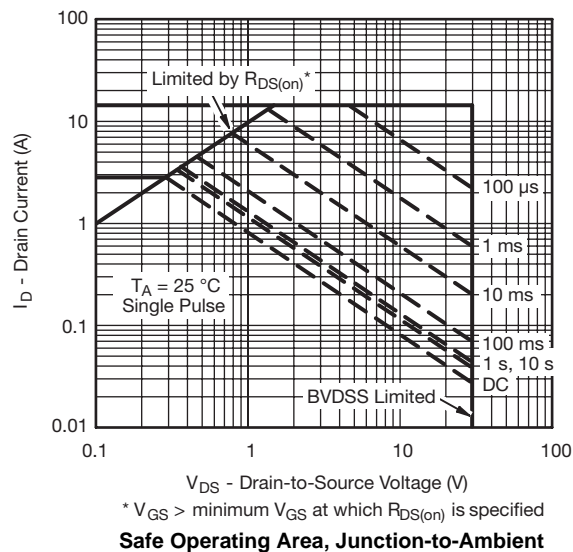
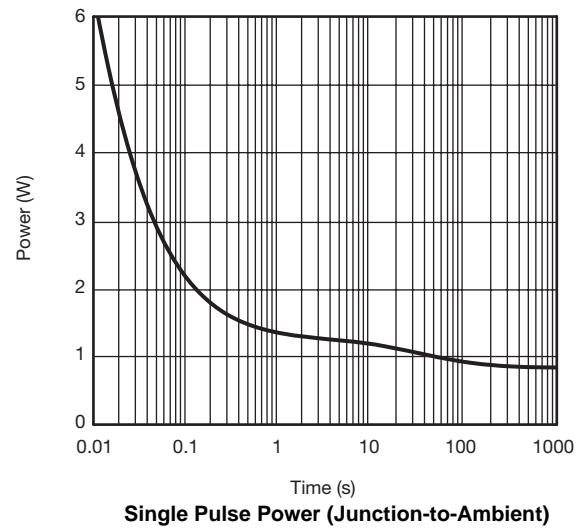
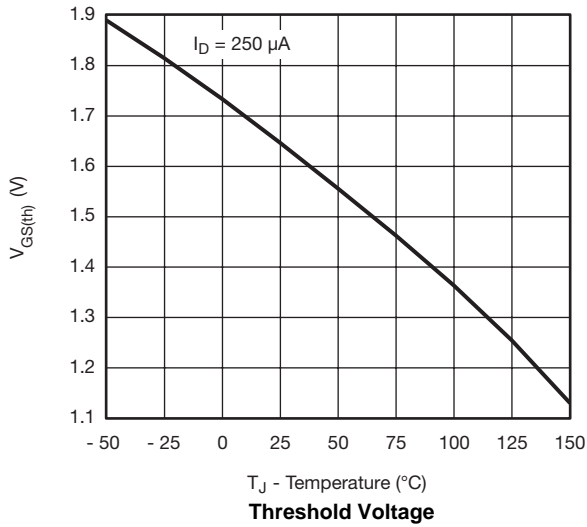
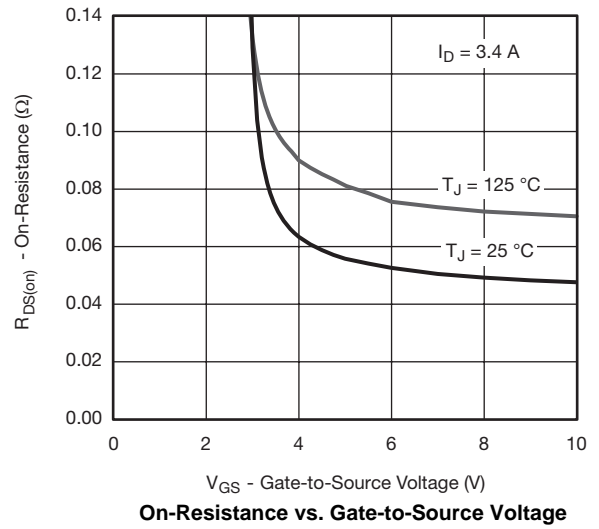
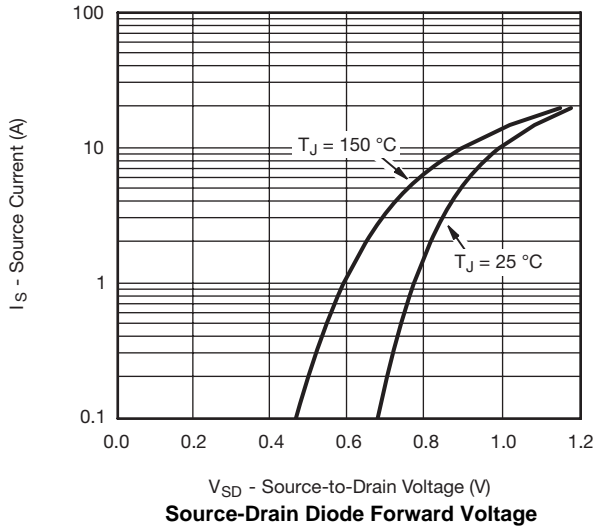


Gate Charge

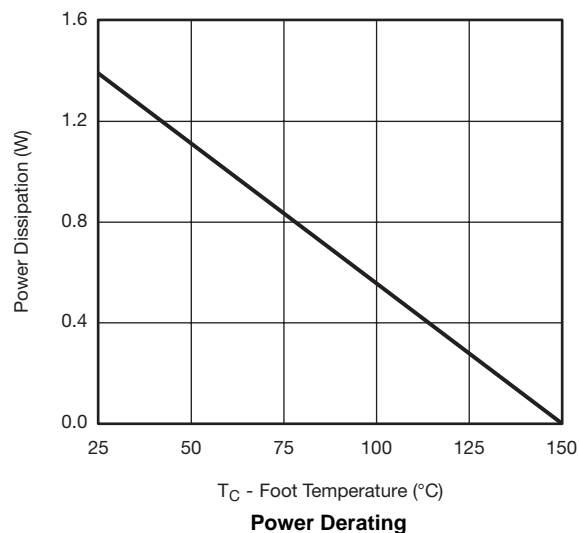
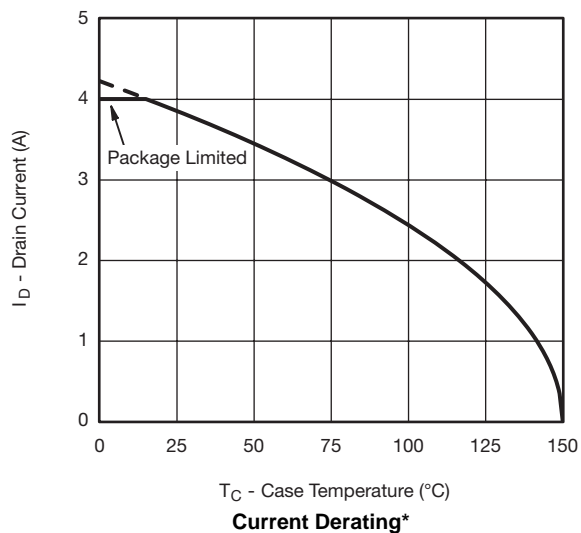


On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

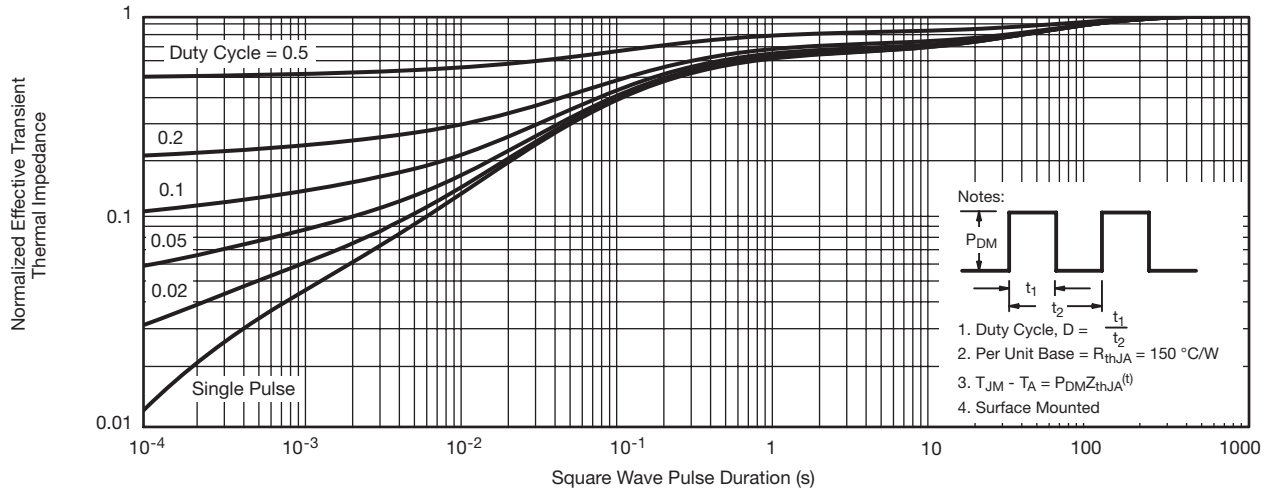


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

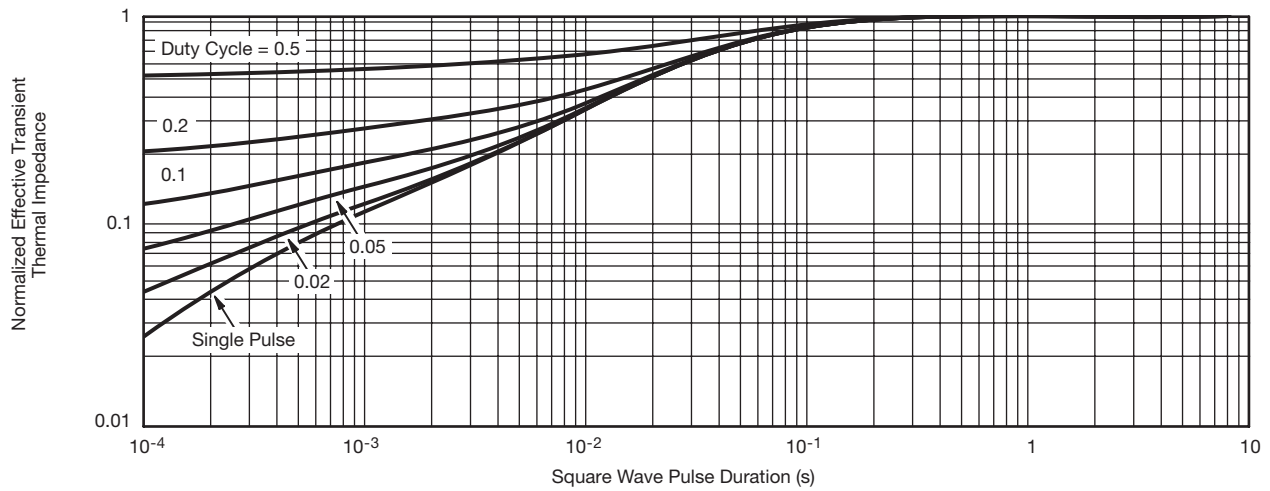


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

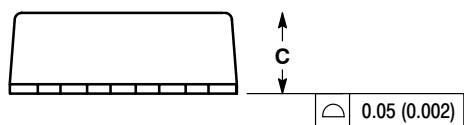
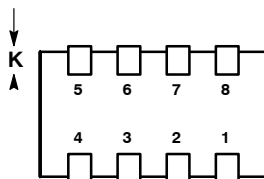
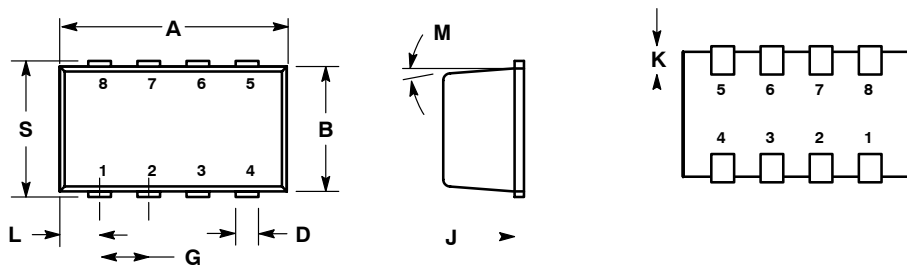


Normalized Thermal Transient Impedance, Junction-to-Foot

PACKAGE DIMENSIONS

ChipFET
CASE 1206A-03
ISSUE D

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.



STYLE 2:

2. GATE 1
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080

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