NCX8200

Audio jack configuration switch matrix

Rev. 1 — 15 May 2015 Product data sheet

1. General description

The NCX8200 is an advanced audio jack configuration switch matrix device that supports 3- and 4-pole connectors. It allows reconfiguration of the GND, microphone-bias contact to comply with the American Headset Jack (AHJ) and the Open Mobile Terminal Platform (OMTP) pinout. Furthermore, a GND sense path supports quasi-differential amplifier architectures. The device contains Human Body Model compliant ESD protection diodes rated 8 kV at all pins. The device can be operated from a supply in the range of 1.6 V to 3.6 V. It supports a broad variety of after-market headphones.

2. Features and benefits

- AHJ and OMTP headset jack pinout support
- Low supply current
- Sense path to GND for quasi differential amplifier configuration
- Low THD and noise microphone pass through channel
- Ultra low R_{DSon} of ground and sense switches
- High power supply ripple rejection
- ESD protection: HBM JEDEC JDS-001 Class 3B exceeds 8 kV
- Operating ambient temperature: −40 °C to +85 °C
- 1.22 mm × 1.22 mm × 0.5 mm WLCSP9 package

3. Applications

- Headphones with integrated microphone and remote control buttons

4. Ordering information

Table 1. Ordering information

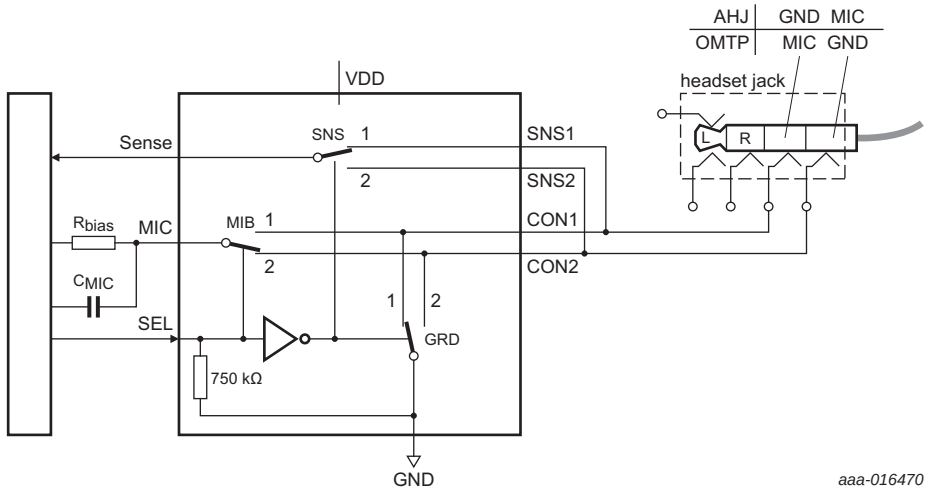
Type number	Package		
	Name	Description	Version
NCX8200UK	WLCSP9	wafer chip-scale package; 9 bumps; 1.22 × 1.22 × 0.5 mm	NCX8200UK

5. Marking

Table 2. Marking codes

Type number	Marking code
NCX8200UK	qx82

6. Functional diagram



Default configuration with SEL = L is AHJ-compliant in this example.

Fig 1. Simplified schematic

7. Pinning information

7.1 Pinning

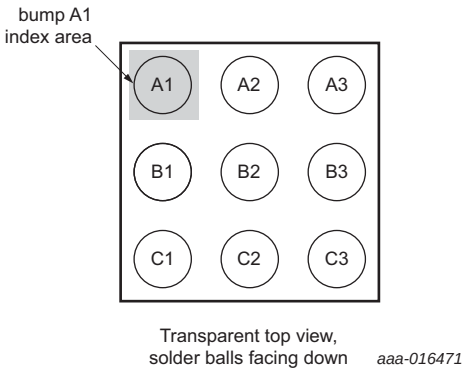


Fig 2. Pin configuration WLCSP9

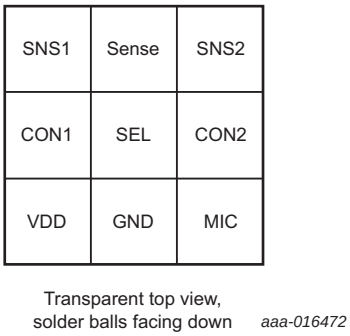


Fig 3. NCX8200 pinout, transparent top view

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
SNS1	A1	I/O	analog sense path 1 to headset jack GND
Sense	A2	I/O	analog sense path for GND sensing
SNS2	A3	I/O	analog sense path 2 to headset jack GND
CON1	B1	I/O	headset jack pin 1
SEL	B2	I	configuration select input: SEL = L: CON1 = GND, CON2 = MIC, Sense = SNS1 SEL = H: CON1 = MIC, CON2 = GND, Sense = SNS2
CON2	B3	I/O	headset jack pin 2
VDD	C1	power	core supply
GND	C2	ground	ground
MIC	C3	I/O	microphone bias connection audio codec side

8. Functional description

The basic application of the NCX8200 device is shown in Figure 1.

There is a 750 kW pull down resistor at SEL pin, for setting SEL default LOW.

If SEL is at low level, CON1 is connected to GND, the MIC channel is routed to CON2, and the Sense channel switches to SNS1. If SEL is at high level, CON2 is connected to GND, the MIC channel is routed to CON1, and the Sense channel switches to SNS2.

9. Application diagram

A capacitor of value not less than 1 μF, should be placed between VDD and GND for stable operation of the NCX8200. The bypass capacitor should be placed close to the device with low-ohmic connection from the power supply and GND connection.

SNS1 should be for sensing CON1 connection and SNS2 should be for sensing CON2 connection. In PCB design, CONx routes from the headset jack should be as low-ohmic as possible. SNSx sensing nodes should be as close to the headset jack as possible with low-ohmic connection, so that the star connection is recommended. The routes from sensing nodes to SNSx should be as low-ohmic as possible.

When VDD is not powered, all the FETs become open by default. Thus, the ground return path becomes floating. Noise might be heard if a speaker (with external powered amplified) is plugged in the audio jack. It is highly recommended when the audio jack detects a plug-in, the NCX8200 is kept powered until unplug.

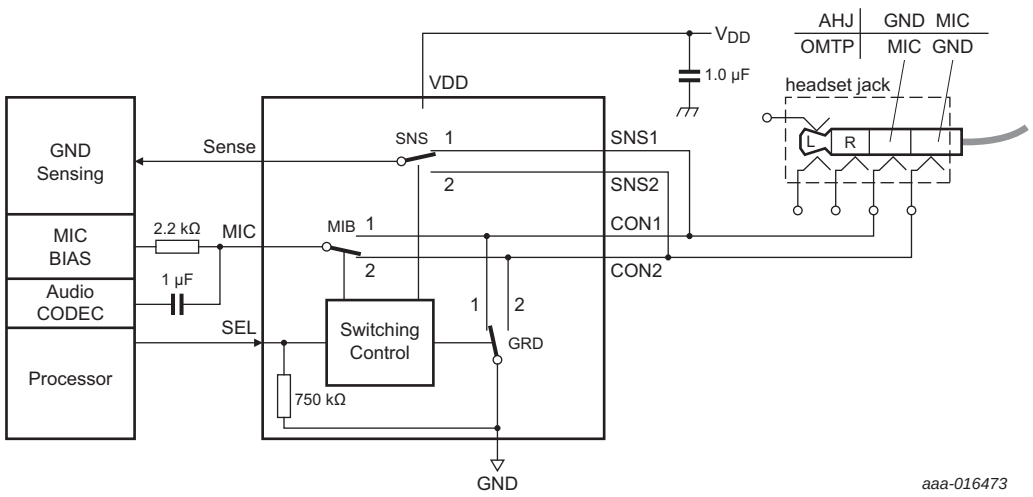


Fig 4. NCX8200 application diagram

10. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+3.6	V
$V_{I/O}$	input/output voltage	MIC, CON1, CON2, Sense, SNS1, SNS2	–0.5	V_{DD}	V
V_I	input voltage	SEL	–0.5	V_{DD} + 0.1	V
$I_{SW(GRD)}$	switch current	continuous current from CON1 or CON2 to GND	-	100	mA
$I_{SW(MIB)}$	switch current	continuous current from MIC to CON1 or CON2	-	50	mA
$I_{SW(SNS)}$	switch current	continuous current from Sense to SNS1 or SNS2	-	50	mA
$T_{j(max)}$	maximum junction temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation		-	530	mW

11. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		1.6	3.6	V
$V_{I/O}$	input/output voltage	MIC, CON1, CON2, Sense, SNS1, SNS2	–0.3	V_{DD}	V
V_I	input voltage	SEL	–0.3	V_{DD}	V
T_{amb}	ambient temperature		–40	+85	°C

12. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1][2]	75.5	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] Rely on the measurement data given for rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value may vary in applications using different layer stacks and layouts.

13. Static characteristics

Table 7. Static characteristics

At recommended operating conditions T_{amb} = −40 °C to +85 °C unless otherwise specified. Typical values are measured with V_{DD} = 3.0 V and T_{amb} = 25 °C. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital control						
V_{IH}	HIGH-level input voltage	SEL input	1.0	-	-	V
V_{IL}	LOW-level input voltage	SEL input	-	-	0.4	V
R_{pd}	pull-down Resistor	SEL input	-	750	-	kΩ
Current consumption						
I_{DD}	Quiescent current	V_{DD} = 3.0 V; T_{amb} = 25 °C	-	0.1	1	μA
		V_{DD} = 3.0 V; T_{amb} = 85 °C	-	-	5	μA
Microphone bias switch MIB						
$I_{S(MIB)}$	MIB Path leakage current	MIC; V_{MIC} = 850 mV; CONx open; SEL = H or L	-	-	1.5	μA
$R_{ON(MIB)}$	MIB switch-on resistance	I_O = 30 mA, V_I = 850 mV				
		V_{DD} = 1.8 V	-	1.6	2.5	Ω
		V_{DD} = 3.0 V	-	0.5	0.8	Ω
		V_{DD} = 3.6 V	-	0.46	0.7	Ω
$R_{ON(MIB\_flat)}$	MIB switch-on resistance flatness	I_O = 30 mA, 0.8 V < V_I < 1.2 V				
		V_{DD} = 1.8 V	-	-	5	Ω
		V_{DD} = 3.0 V	-	-	0.1	Ω
		V_{DD} = 3.6 V	-	-	0.1	Ω
C_S	input/output capacitance	MIC; CONx open; SEL = H or L	-	250	-	pF
THD	total harmonic distortion of the conducting MIB switch	R_S = R_L = 600 Ω, f_{AC} = 20 kHz, V_{AC} = 0.5 V_{PP}, V_{DC} = 1.7 V, V_{DD} = 3.0 V; SEL = H or L	-	0.005	-	%
PSRR	power supply ripple rejection ratio of the conducting MIB switch	R_S = R_L = 600 Ω, f = 217 Hz, V_{DD} = 3.0 V, V_{DC} = 2.1 V, V_{AC} = 0.3 V_{PP}; SEL = H or L	-	−80	-	dB
Ground switch GRD						
$R_{ON(GRD)}$	GRD switch on resistance	I_{ICONx} = 100 mA				
		V_{DD} = 1.8 V	-	70	120	mΩ
		V_{DD} = 3.0 V	-	60	90	mΩ
		V_{DD} = 3.6 V	-	57	82	mΩ
$R_{ON(GRD\_flat)}$	GRD switch-on resistance flatness	I_{ICONx} = 10 mA, V_{DD} = 1.8 V ~ 3.6 V	-	-	50	mΩ
		I_{ICONx} = 1 mA, V_{DD} = 1.8 V ~ 3.6 V	-	-	50	mΩ
PSRR	power supply ripple rejection ratio of the conducting GRD switch	V_S = 1 V, R_S = 8 Ω, V_{DD} = 3.0 V, V_{AC} = 0.3 V_{PP}, f = 217 Hz; SEL = H or L	-	−60	-	dB

Table 7. Static characteristics *…continued*

At recommended operating conditions T_{amb} = −40 °C to +85 °C unless otherwise specified. Typical values are measured with V_{DD} = 3.0 V and T_{amb} = 25 °C. Voltages are referenced to GND (ground = 0 V). …continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Sense switch SNS						
$R_{ON(SNS)}$	SNS switch on resistance	I_{Isense} = 30 mA, SNSx= 0 V				
		V_{DD} = 1.8 V	-	80	130	mΩ
		V_{DD} = 3.0 V	-	60	90	mΩ
		V_{DD} = 3.6 V	-	57	82	mΩ
$R_{ON(SNS\_flat)}$	SNS switch-on resistance flatness	I_{Isense} = 10 mA, SNSx = 0 V, V_{DD} = 1.8 V ~ 3.6 V	-	-	50	mΩ
		I_{Isense} = 1 mA, SNSx= 0 V, V_{DD} = 1.8 V ~ 3.6 V	-	-	50	mΩ
$I_{S(SNS\_OFF)}$	SNS switch leakage current	Sense; V_{sense} = 1 V				
		SEL = H; SNS1 =GND; SNS2 = OPEN	-	-	1	µA
		SEL = L; SNS1 = OPEN; SNS2 = GND	-	-	1	µA

13.1 Test circuit and graphs

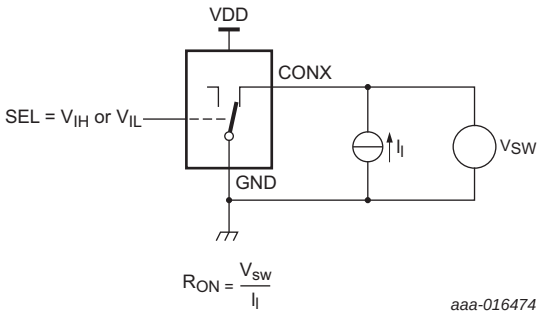


Fig 5. Test circuit for measuring ON resistance

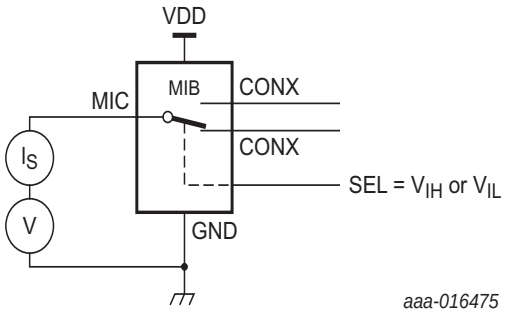
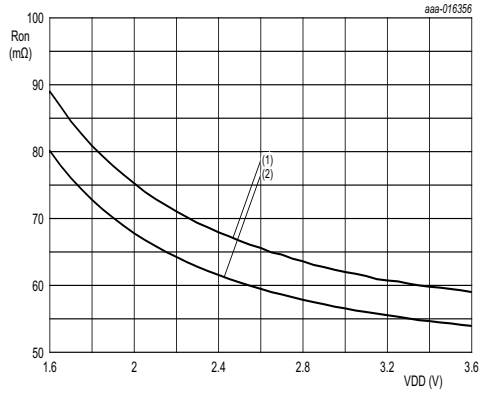


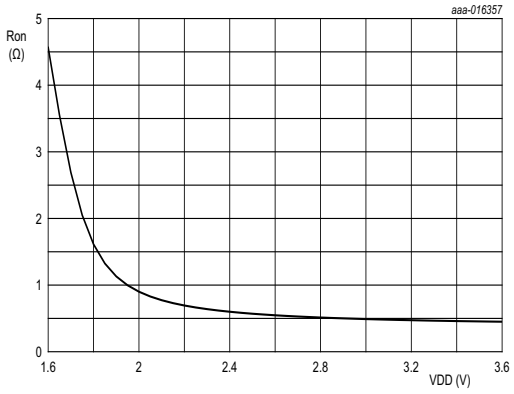
Fig 6. Test circuit for measuring leakage current



(1) SNS RON

(2) GRD RON

Fig 7. GRD and SNS channel ON resistance



MIB RON

Fig 8. MIB channel ON resistance

14. Dynamic characteristics

Table 8. Dynamic characteristics

At recommended operating conditions T_{amb} = −40 °C to +85 °C unless otherwise specified. Typical values are measured with V_{DD} = 3.0 V and T_{amb} = 25 °C. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max [1]	Unit
t_{ON}	Turn-ON Time	$V_{MIC} = V_{DD}$, V_{sense}= 0 V, R_L = 50 Ω, C_L = 35 pF	-	215	400	ns
t_{OFF}	Turn-OFF Time	$V_{MIC} = V_{DD}$, V_{sense}= 0 V, R_L = 50 Ω, C_L = 35 pF	-	35	120	ns
t_{BBM}	break-before-make time	$V_{MIC} = V_{DD}$, V_{sense}= 0 V, R_L = 50 Ω, C_L = 35 pF	70[1]	180	320	ns

[1] Guaranteed by design

14.1 Waveform

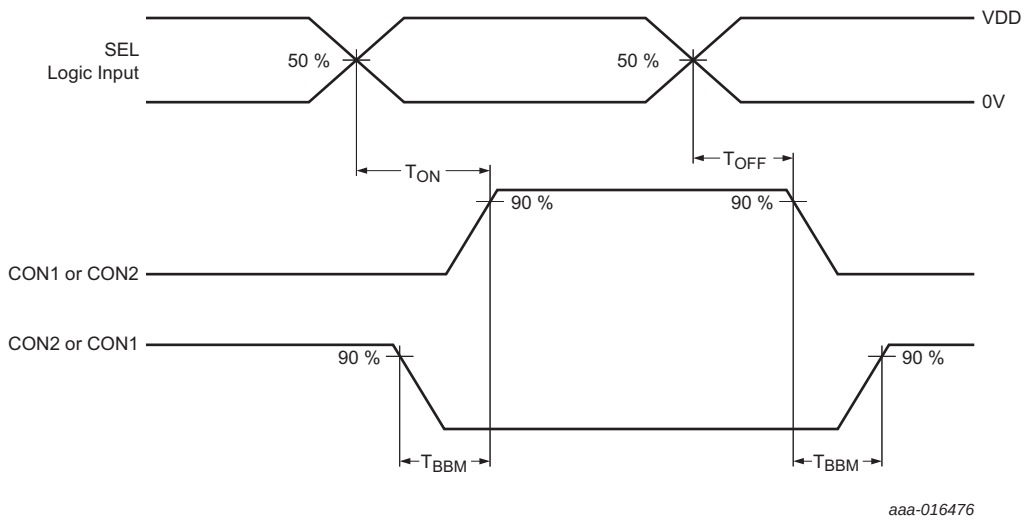
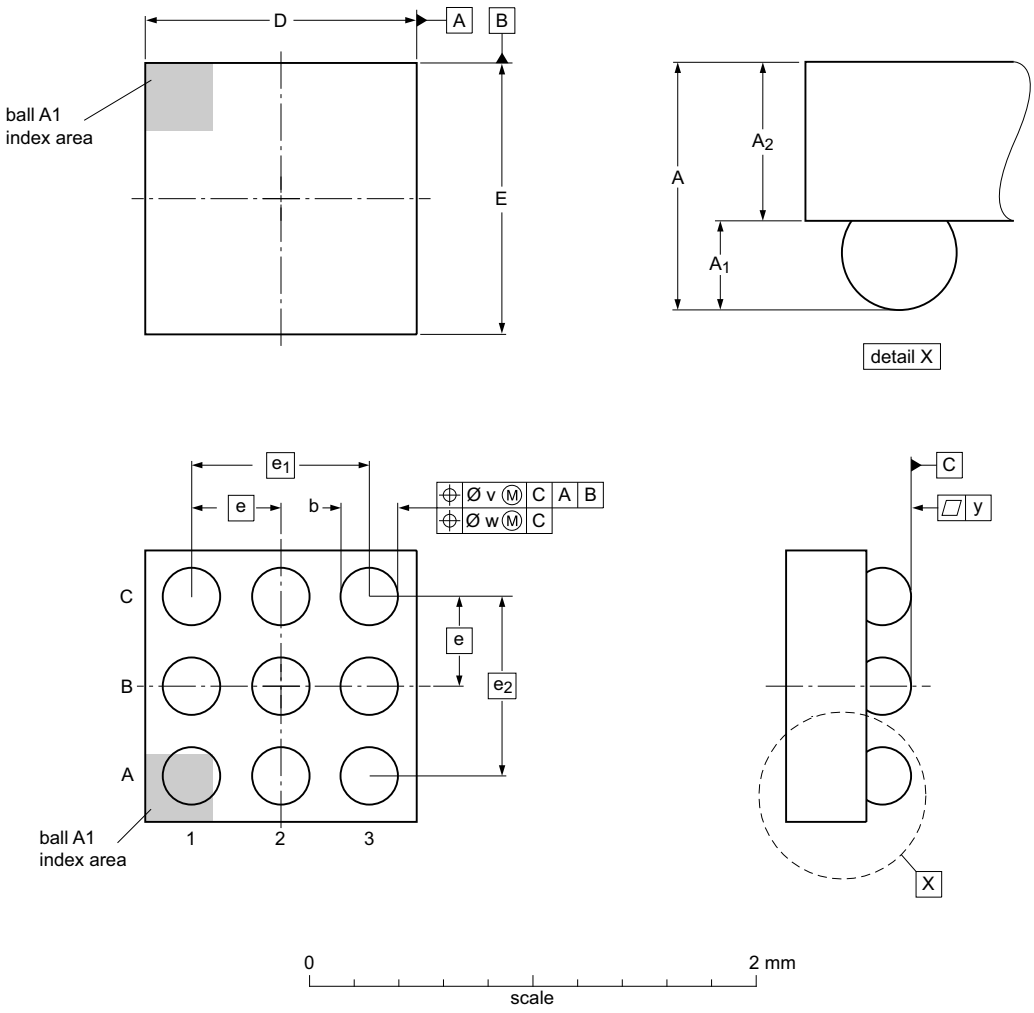


Fig 9. Turn-ON time and turn-OFF time

15. Package outline

WLCSP9: wafer chip-scale package; 9 bumps; 1.22 x 1.22 x 0.5 mm **NCX8200UK**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
	max	0.54	0.23	0.325	0.29	1.25	1.25						
mm	nom	0.50	0.20	0.300	0.26	1.22	1.22	0.4	0.8	0.8	0.05	0.015	0.03
	min	0.46	0.17	0.275	0.23	1.19	1.19						

ncx8200uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NCX8200UK						~~14-12-15~~ 14-12-16

Fig 10. Package outline NCX8200 (WLCSP9)

16. Abbreviations

Table 9. Abbreviations

Acronym	Description
THD	Total Harmonic Distortion
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NCX8200 v.1	20150515	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

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