

NCV8667

150 mA LDO Regulator with Enable, Reset and Early Warning

The NCV8667 is 150 mA LDO regulator with integrated reset and early warning functions dedicated for microprocessor applications. Its robustness allows NCV8667 to be used in severe automotive environments. Very low quiescent current as low as 28 μ A typical for NCV8667 makes it suitable for applications permanently connected to battery requiring very low quiescent current with or without load. The Enable function can be used for further decrease of quiescent current in shutdown mode to 1 μ A. The NCV8667 contains protection functions as current limit, thermal shutdown and reverse output current protection.

Features

- Output Voltage Options: 5 V
- Output Voltage Accuracy: $\pm 2\%$
- Output Current up to 150 mA
- Very Low Quiescent Current:
 - typ 28 μ A for Adjustable Early Warning Threshold Option
- Very Low Dropout Voltage
- Early Warning Threshold Accuracy: $\pm 10\%$ Over Temperature Range
- Enable Function (1 μ A Max Quiescent Current when Disabled)
- Microprocessor Compatible Control Functions:
 - Reset with Adjustable Power-on Delay
 - Early Warning
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features:
 - Current Limitation
 - Thermal Shutdown
 - Reverse Output Current
- These are Pb-Free Devices

Typical Applications

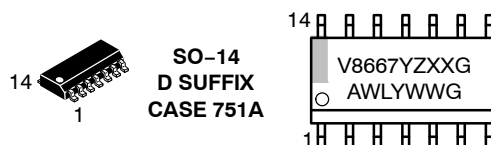
- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain



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MARKING DIAGRAMS



- Y = Timing and Reset Threshold Option*
- Z = Early Warning Option*
- XX = Voltage Option
5.0 V (XX = 50)
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*See Application Information Section.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

NCV8667

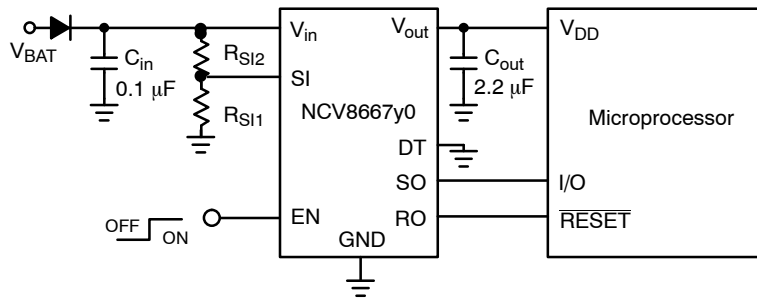
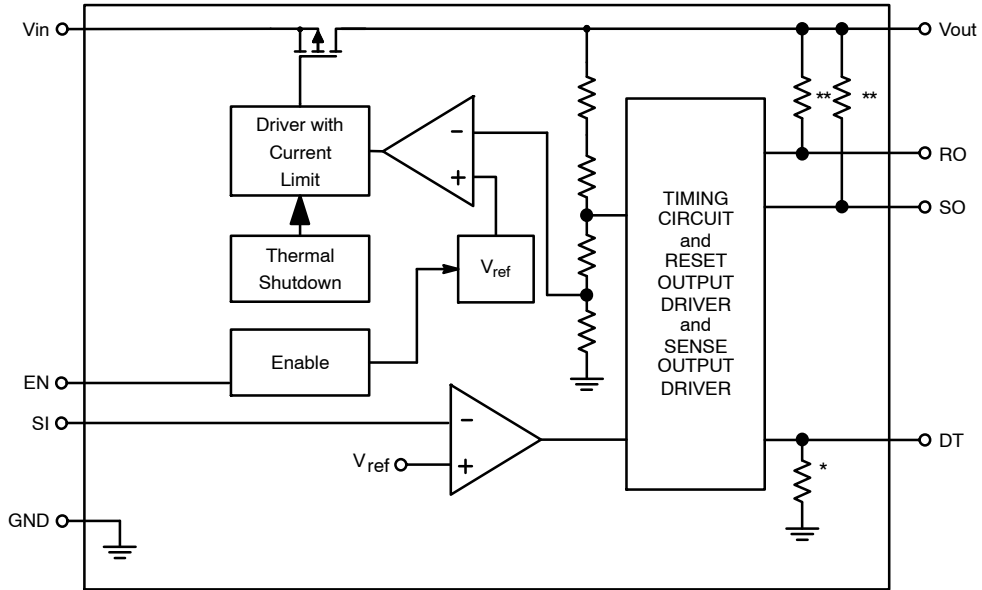


Figure 1. Application Circuit



*Pull-down Resistor (~150 kΩ) active only in Reset State.

** 5 V option only.

Figure 2. Simplified Block Diagram

NCV8667

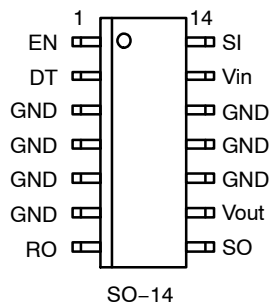


Figure 3. Pin Connections
(Top View)

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|------------------------|-----------|---|
| 1 | EN | Enable Input; low level disables the IC. |
| 2 | DT | Reset Delay Time Select. Short to GND or connect to V_{out} to select time. |
| 3, 4, 5, 6, 10, 11, 12 | GND | Power Supply Ground. |
| 7 | RO | Reset Output. 30 k Ω internal Pull-Up resistor connected to V_{out} . RO goes Low when V_{out} drops by more than 7% (typ.) from its nominal value. |
| 8 | SO | Early Warning Output. 30 k Ω internal Pull-Up resistor connected to V_{out} . It can be used to provide early warning of an impending reset condition. Leave open if not used. |
| 9 | V_{out} | Regulated Output Voltage. Connect 2.2 μ F capacitor with ESR < 100 Ω to ground. |
| 13 | V_{in} | Positive Power Supply Input. Connect 0.1 μ F capacitor to ground. |
| 14 | SI | Sense Input; If not used, connect to V_{out} . See Electrical Characteristics Table and Application Information sections for more information. |

ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Min | Max | Unit |
|---|--------------|------|-----------------|------|
| Input Voltage DC (Note 1) | V_{in} | -0.3 | 40 | V |
| Input Voltage Transient (Note 1) | V_{in} | - | 45 | V |
| Input Current | I_{in} | -5 | - | mA |
| Output Voltage (Note 2) | V_{out} | -0.3 | 5.5 | V |
| Output Current | I_{out} | -3 | Current Limited | mA |
| Enable Input Voltage DC | V_{EN} | -0.3 | 40 | V |
| Enable Input Voltage Transient | V_{EN} | - | 45 | V |
| Enable Input Current Range | I_{EN} | -1 | 1 | mA |
| DT (Reset Delay Time Select) Voltage | V_{DT} | -0.3 | 5.5 | V |
| DT (Reset Delay Time Select) Current | I_{DT} | -1 | 1 | mA |
| Reset Output Voltage | V_{RO} | -0.3 | 5.5 | V |
| Reset Output Current | I_{RO} | -3 | 3 | mA |
| Sense Input Voltage DC | V_{SI} | -0.3 | 40 | V |
| Sense Input Voltage Transient | V_{SI} | - | 45 | V |
| Sense Input Current | I_{SI} | -1 | 1 | mA |
| Sense Output Voltage | V_{SO} | -0.3 | 5.5 | V |
| Sense Output Current | I_{SO} | -3 | 3 | mA |
| Maximum Junction Temperature | $T_{J(max)}$ | -40 | 150 | °C |
| Storage Temperature | T_{STG} | -55 | 150 | °C |
| ESD Capability, Human Body Model (Note 3) | ESD_{HBM} | -2 | 2 | kV |
| ESD Capability, Machine Model (Note 3) | ESD_{MM} | -200 | 200 | V |
| Lead Temperature Soldering Reflow (SMD Styles Only) (Note 4) | T_{SLD} | - | 265 peak | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. 5.5 or ($V_{in} + 0.3$ V), whichever is lower
3. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|--|-------------------|-------|------|
| Thermal Characteristics, SO-14 (Note 5) | | | °C/W |
| Thermal Resistance, Junction-to-Air (Note 6) | $R_{\theta JA}$ | 94 | |
| Thermal Reference, Junction-to-Pin4 (Note 6) | $\Psi_{\psi JP4}$ | 18 | |

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
 6. Values based on copper area of 645 mm² (or 1 in²) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 7)

| Rating | Symbol | Min | Max | Unit |
|------------------------|----------|-----|-----|------|
| Input Voltage (Note 8) | V_{in} | 5.5 | 40 | V |
| Junction Temperature | T_J | -40 | 150 | °C |

7. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
 8. Minimum $V_{in} = 5.5$ V or ($V_{out} + V_{DO}$), whichever is higher.

ELECTRICAL CHARACTERISTICS $V_{in} = 13.2$ V, $V_{EN} = 3$ V, $V_{DT} = GND$, $V_{SI} = V_{out}$, R_{S11} & R_{S12} not used, $C_{in} = 0.1$ μ F, $C_{out} = 2.2$ μ F, for typical values $T_J = 25^\circ$ C, for min/max values $T_J = -40^\circ$ C to 150° C; unless otherwise noted. (Notes 9 and 10)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

REGULATOR OUTPUT

| | | | | | | |
|--|--|---------------------|----------------------|------------|---------------------|---------------------|
| Output Voltage (Accuracy %) | $V_{in} = 5.6$ V to 40 V, $I_{out} = 0.1$ mA to 100 mA $V_{in} = 5.8$ V to 16 V, $I_{out} = 0.1$ mA to 150 mA | V_{out} | 4.9 4.9 (-2 %) | 5.0 5.0 | 5.1 5.1 (+2%) | V |
| Output Voltage (Accuracy %) | $T_J = -40^\circ$ C to 125° C $V_{in} = 5.8$ V to 28 V, $I_{out} = 0$ mA to 150 mA | V_{out} | 4.9 (-2 %) | 5.0 | 5.1 (+2%) | V |
| Line Regulation | $V_{in} = 6$ V to 28 V, $I_{out} = 5$ mA | Reg _{line} | -20 | 0 | 20 | mV |
| Load Regulation | $I_{out} = 0.1$ mA to 150 mA | Reg _{load} | -40 | 10 | 40 | mV |
| Dropout Voltage (Note 11) | $I_{out} = 100$ mA $I_{out} = 150$ mA | V_{DO} | - | 225 300 | 450 600 | mV |
| Output Capacitor for Stability (Note 12) | $I_{out} = 0$ mA to 150 mA | C_{out} ESR | 2.2 0.01 | - - | 100 100 | μ F Ω |

DISABLE AND QUIESCENT CURRENTS

| | | | | | | |
|---|--|-----------|---|----|----------|---------|
| Disable Current | $V_{EN} = 0$ V, $T_J < 85^\circ$ C | I_{DIS} | - | - | 1 | μ A |
| Quiescent Current, $I_q = I_{in} - I_{out}$ | $I_{out} = 0.1$ mA, $T_J = 25^\circ$ C $I_{out} = 0.1$ mA to 150 mA, $T_J \leq 125^\circ$ C | I_q | - | 28 | 35 37 | μ A |

CURRENT LIMIT PROTECTION

| | | | | | | |
|-----------------------------|--------------------------------------|-----------|-----|---|-----|----|
| Current Limit | $V_{out} = 0.96 \times V_{out_nom}$ | I_{LIM} | 205 | - | 525 | mA |
| Short Circuit Current Limit | $V_{out} = 0$ V | I_{SC} | 205 | - | 525 | mA |

REVERSE OUTPUT CURRENT PROTECTION

| | | | | | | |
|-----------------------------------|-----------------------------------|----------------|---|---|-----|---|
| Reverse Output Current Protection | $V_{EN} = 0$ V, $I_{out} = -1$ mA | V_{out_rev} | - | 2 | 5.5 | V |
|-----------------------------------|-----------------------------------|----------------|---|---|-----|---|

PSRR

| | | | | | | |
|---|----------------------------|------|---|----|---|----|
| Power Supply Ripple Rejection (Note 12) | $f = 100$ Hz, $0.5 V_{pp}$ | PSRR | - | 60 | - | dB |
|---|----------------------------|------|---|----|---|----|

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
 10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
 11. Measured when output voltage falls 100 mV below the regulated voltage at $V_{in} = 13.2$ V.
 12. Values based on design and/or characterization.
 13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options.

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ELECTRICAL CHARACTERISTICS $V_{in} = 13.2\text{ V}$, $V_{EN} = 3\text{ V}$, $V_{DT} = \text{GND}$, $V_{SI} = V_{out}$, R_{SI1} & R_{SI2} not used, $C_{in} = 0.1\ \mu\text{F}$, $C_{out} = 2.2\ \mu\text{F}$, for typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to 150°C ; unless otherwise noted. (Notes 9 and 10)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

ENABLE

| | | | | | | |
|---|---|-------------------------------|----------|----------|----------|---------------|
| Enable Input Threshold Voltage Logic Low Logic High | | $V_{th(EN)}$ | – 2.5 | – – | 0.8 – | V |
| Enable Input Current Logic High Logic Low | $V_{EN} = 5\text{ V}$ $V_{EN} = 0\text{ V}$, $T_J < 85^\circ\text{C}$ | I_{EN_ON} I_{EN_OFF} | – – | 3 0.5 | 5 1 | μA |

DT (Reset Delay Time Select)

| | | | | | | |
|---|-----------------------|--------------|--------|--------|----------|---------------|
| DT Threshold Voltage Logic Low Logic High | | $V_{th(DT)}$ | – 2 | – – | 0.8 – | V |
| DT Input Current | $V_{DT} = 5\text{ V}$ | I_{DT} | – | – | 1 | μA |

RESET OUTPUT RO

| | | | | | | |
|--|--|-------------|--------------|----------|--------------|------------------|
| Output Voltage Reset Threshold (Note 13) | V_{out} decreasing $V_{in} > 5.5\text{ V}$ | V_{RT} | 90 | 93 | 96 | $\%V_{out}$ |
| Reset Hysteresis | | V_{RH} | – | 2.0 | – | $\%V_{out}$ |
| Maximum Reset Sink Current | $V_{out} = 4.5\text{ V}$, $V_{RO} = 0.25\text{ V}$ | I_{ROmax} | 1.75 | – | – | mA |
| Reset Output Low Voltage | $V_{out} > 1\text{ V}$, $I_{RO} < 200\ \mu\text{A}$ | V_{ROL} | – | 0.15 | 0.25 | V |
| Reset Output High Voltage | | V_{ROH} | 4.5 | – | – | V |
| Integrated Reset Pull Up Resistor | | R_{RO} | 15 | 30 | 50 | $\text{k}\Omega$ |
| Reset Delay Time (Note 13) | DT connected to GND DT connected to V_{out} | t_{RD} | 6.4 102.4 | 8 128 | 9.6 153.6 | ms |
| Reset Reaction Time (see Figure 29) | | t_{RR} | 16 | 25 | 38 | μs |

EARLY WARNING (SI and SO)

| | | | | | | |
|--|--|--------------|--------------|--------------|--------------|------------------|
| Sense Input Threshold (NCV8667y0) High Low | | $V_{SI(th)}$ | 1.25 1.20 | 1.33 1.25 | 1.40 1.33 | V |
| Sense Input Current (NCV8667y0) | $V_{SI} = 5\text{ V}$ | I_{SI} | –1 | 0.1 | 1 | μA |
| Integrated Sense Output Pull Up Resistor | | R_{SO} | 15 | 30 | 50 | $\text{k}\Omega$ |
| Sense Output Low Voltage | $V_{SI} < 1.2\text{ V}$, $I_{SO} < 200\ \mu\text{A}$, $V_{out} > 1\text{ V}$ | V_{SOL} | – | 0.15 | 0.25 | V |
| Sense Output High Voltage | | V_{SOH} | 4.5 | – | – | V |
| Maximum Sense Output Sink Current | $V_{out} = 4.5\text{ V}$, $V_{SI} < 1.2\text{ V}$, $V_{SO} = 0.25\text{ V}$ | I_{SOmax} | 1.75 | – | – | mA |
| SI High to SO High Reaction Time | V_{SI} increasing | t_{PSOLH} | – | 7 | 12 | μs |
| SI Low to SO Low Reaction Time | V_{SI} decreasing | t_{PSOHL} | – | 3.8 | 5.0 | μs |

THERMAL SHUTDOWN

| | | | | | | |
|--|--|----------|-----|-----|-----|------------------|
| Thermal Shutdown Temperature (Note 12) | | T_{SD} | 150 | 175 | 195 | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis (Note 12) | | T_{SH} | – | 25 | – | $^\circ\text{C}$ |

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.

10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

11. Measured when output voltage falls 100 mV below the regulated voltage at $V_{in} = 13.2\text{ V}$.

12. Values based on design and/or characterization.

13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options.

TYPICAL CHARACTERISTICS

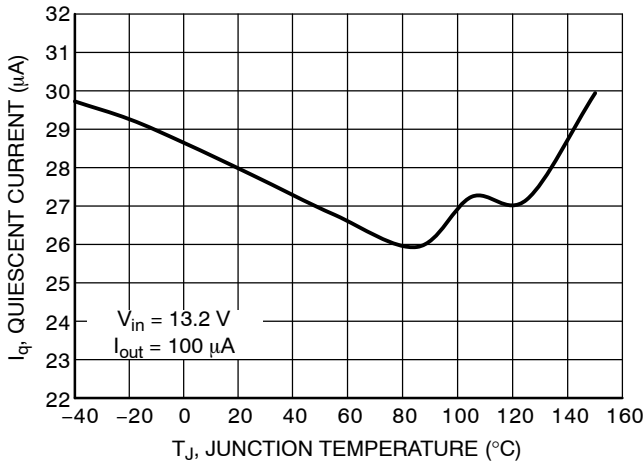


Figure 4. Quiescent Current vs. Temperature

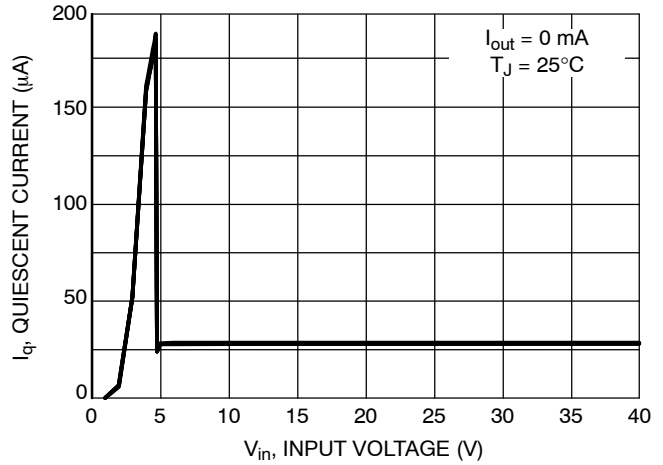


Figure 5. Quiescent Current vs. Input Voltage

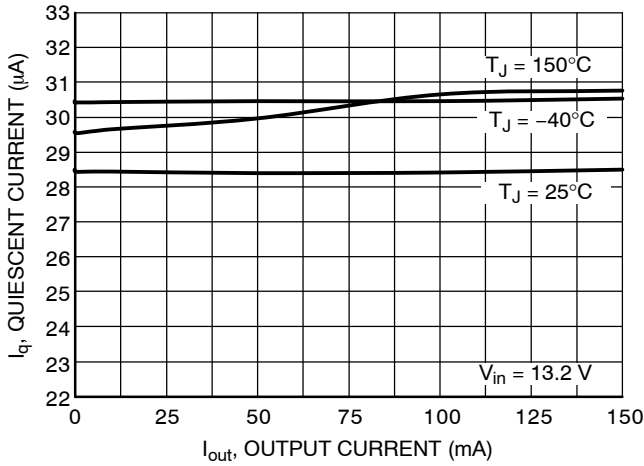


Figure 6. Quiescent Current vs. Output Current

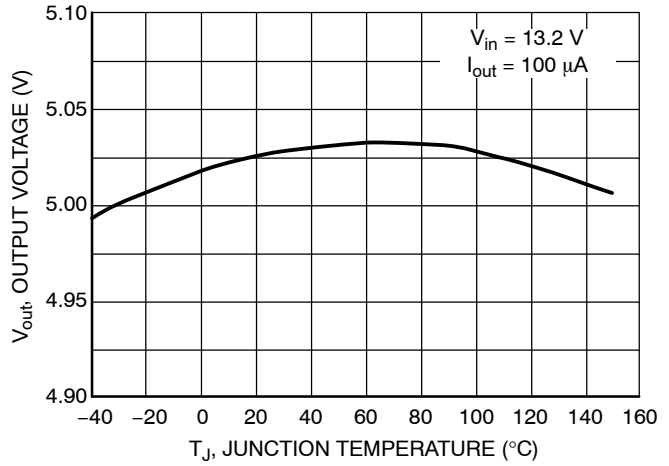


Figure 7. Output Voltage vs. Temperature

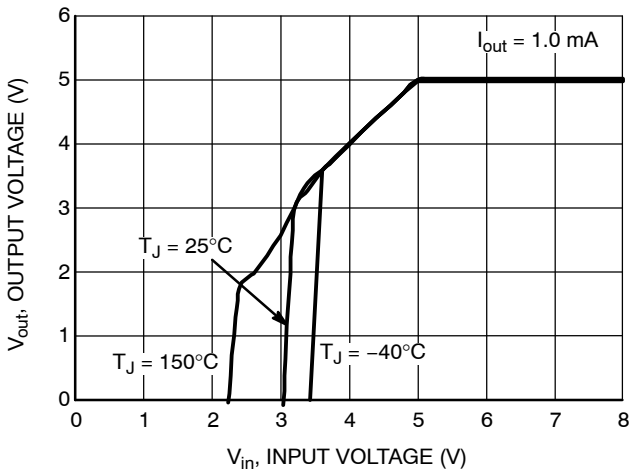


Figure 8. Output Voltage vs. Input Voltage

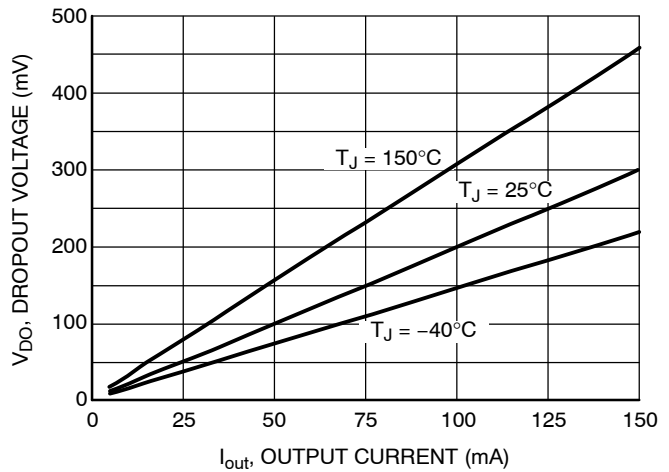


Figure 9. Dropout vs. Output Current

TYPICAL CHARACTERISTICS

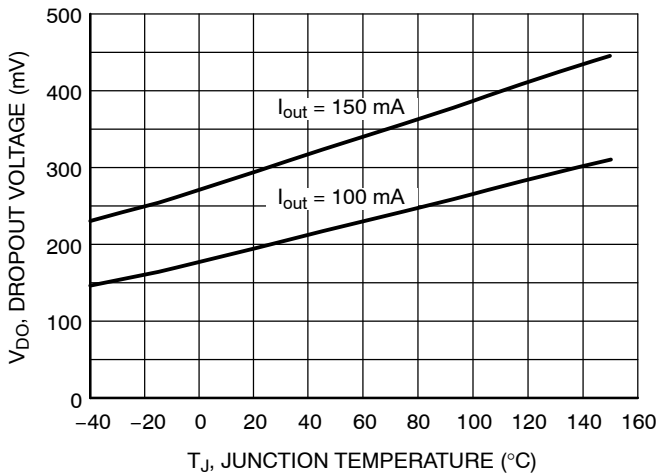


Figure 10. Dropout vs. Temperature

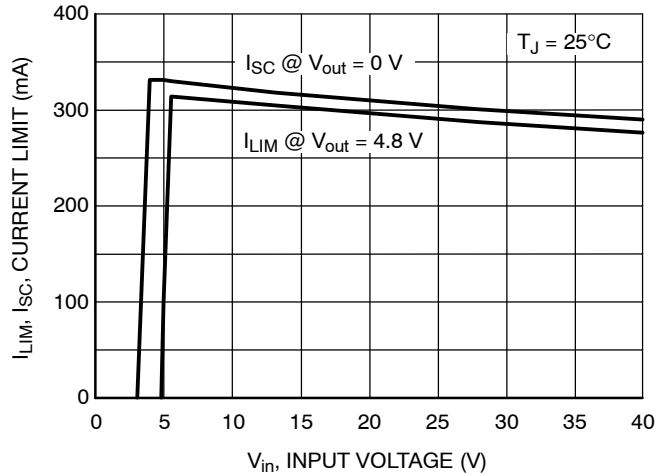


Figure 11. Output Current Limit vs. Input Voltage

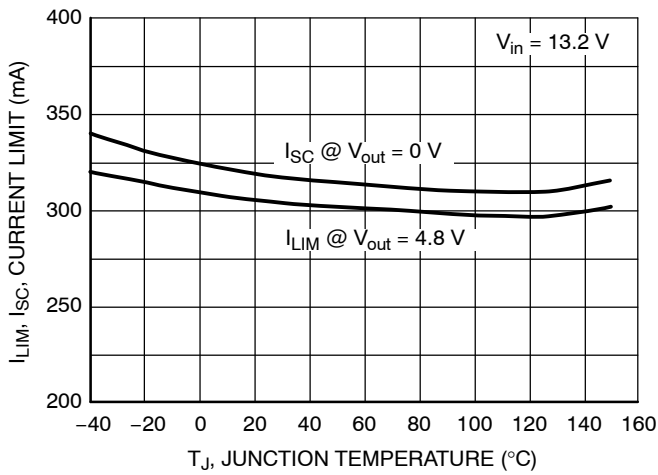


Figure 12. Output Current Limit vs. Temperature

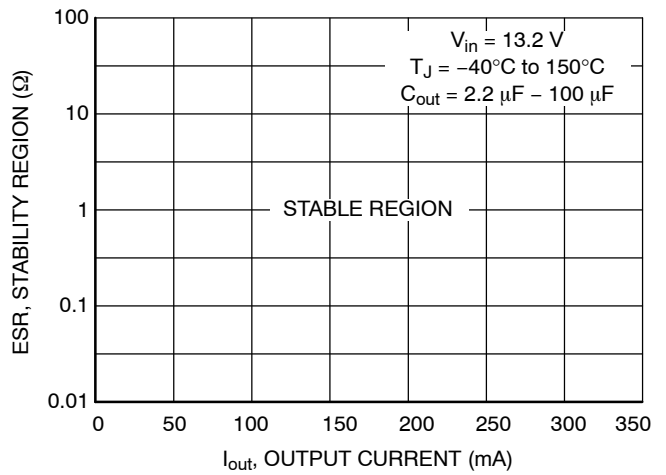


Figure 13. C_{out} ESR Stability vs. Output Current

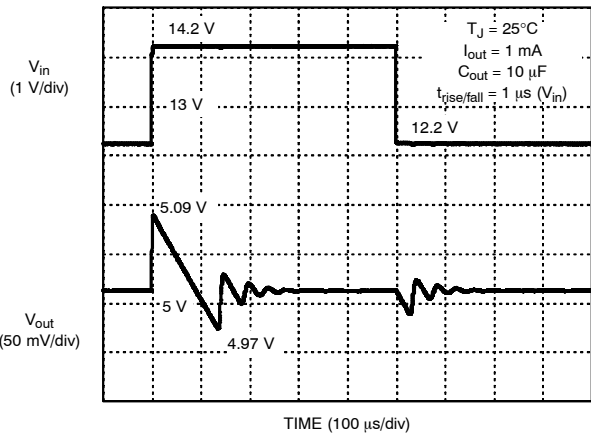


Figure 14. Line Transients

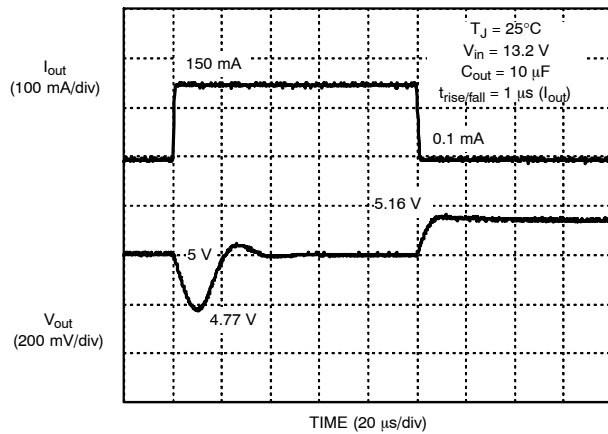


Figure 15. Load Transients

TYPICAL CHARACTERISTICS

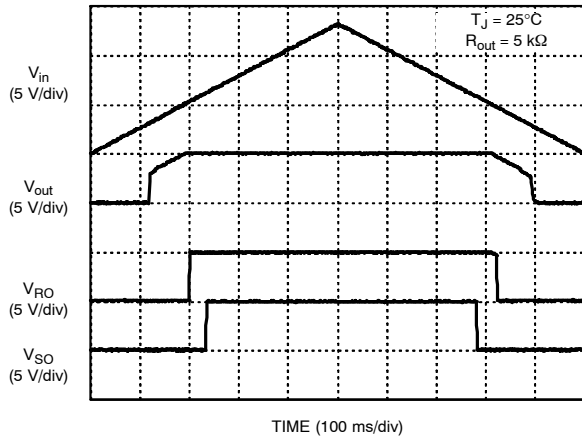


Figure 16. Power Up and Down Transient

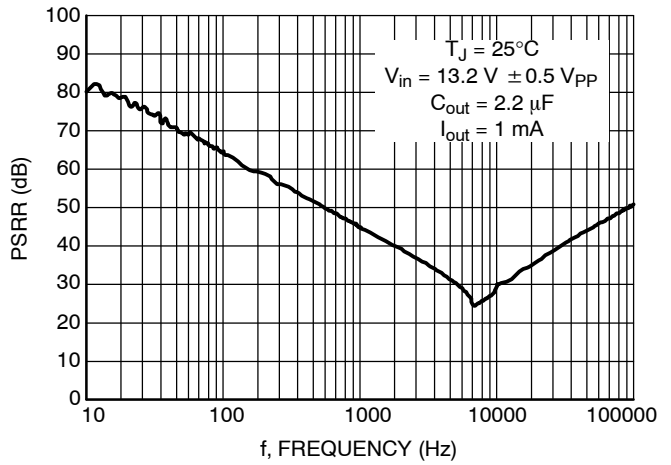


Figure 17. PSRR vs. Frequency

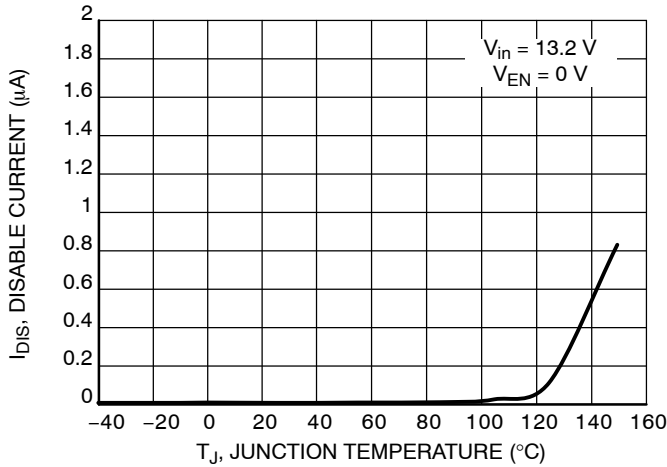


Figure 18. Disable Current vs. Temperature

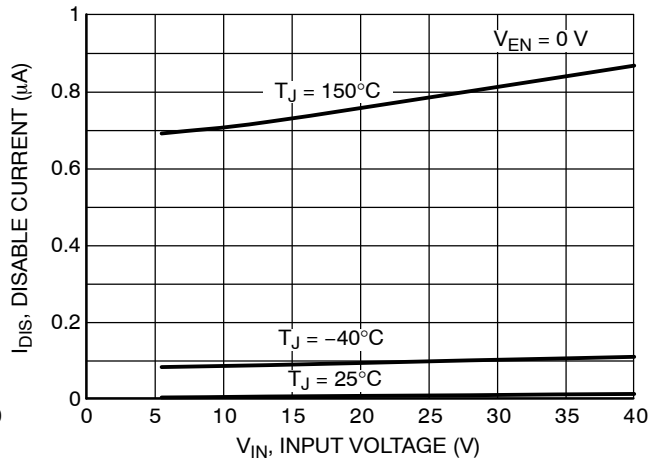


Figure 19. Disable Current vs. Input Voltage

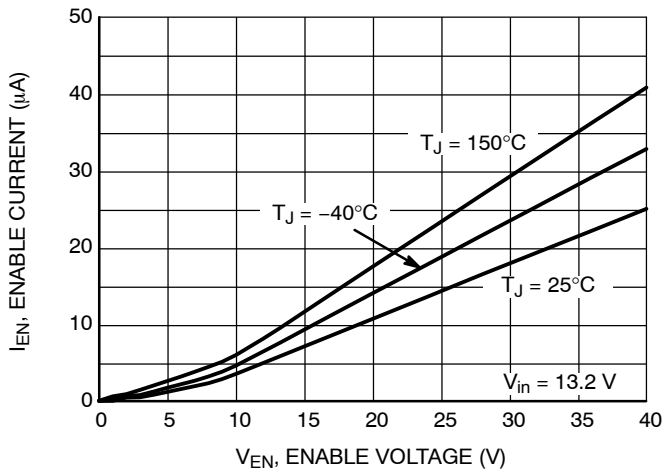


Figure 20. Enable Current vs. Enable Voltage

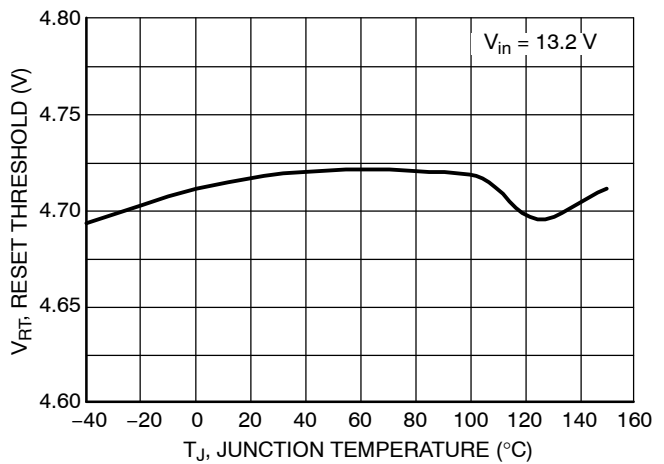


Figure 21. Reset Threshold vs. Temperature

TYPICAL CHARACTERISTICS

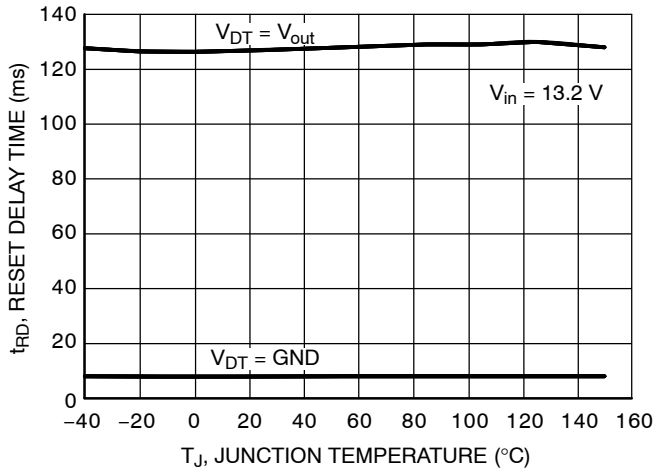


Figure 22. Reset Time vs. Temperature

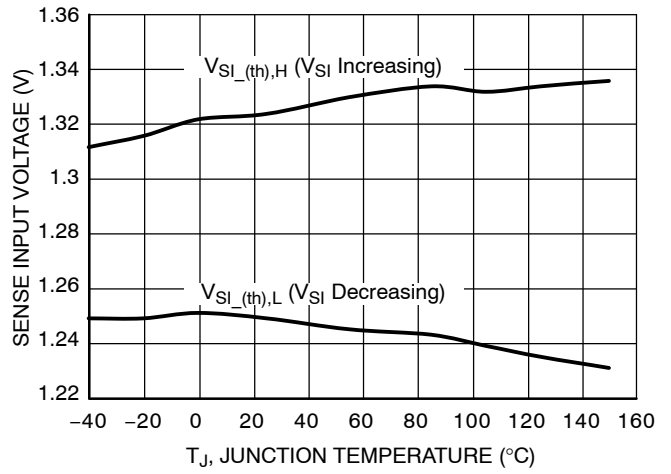


Figure 23. SI Threshold vs. Temperature

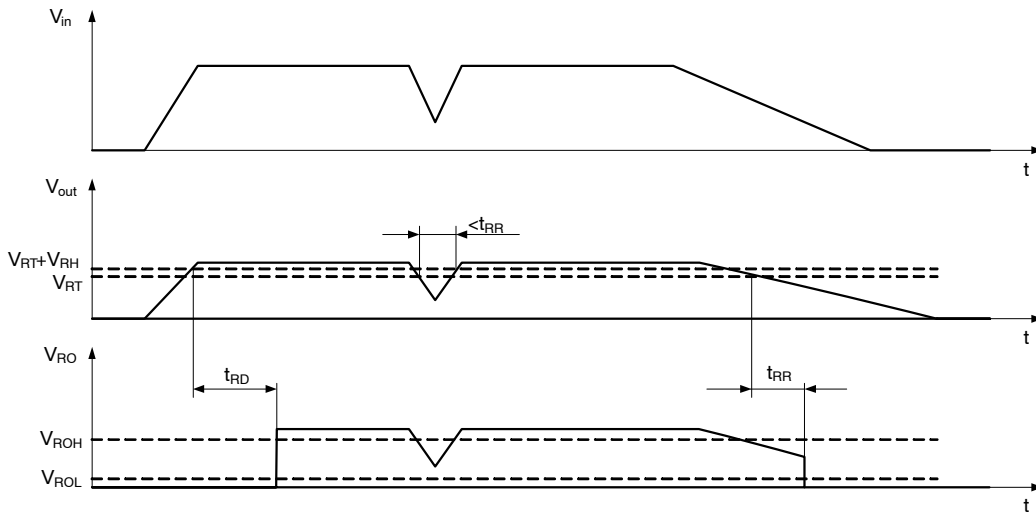


Figure 24. Reset Function and Timing Diagram

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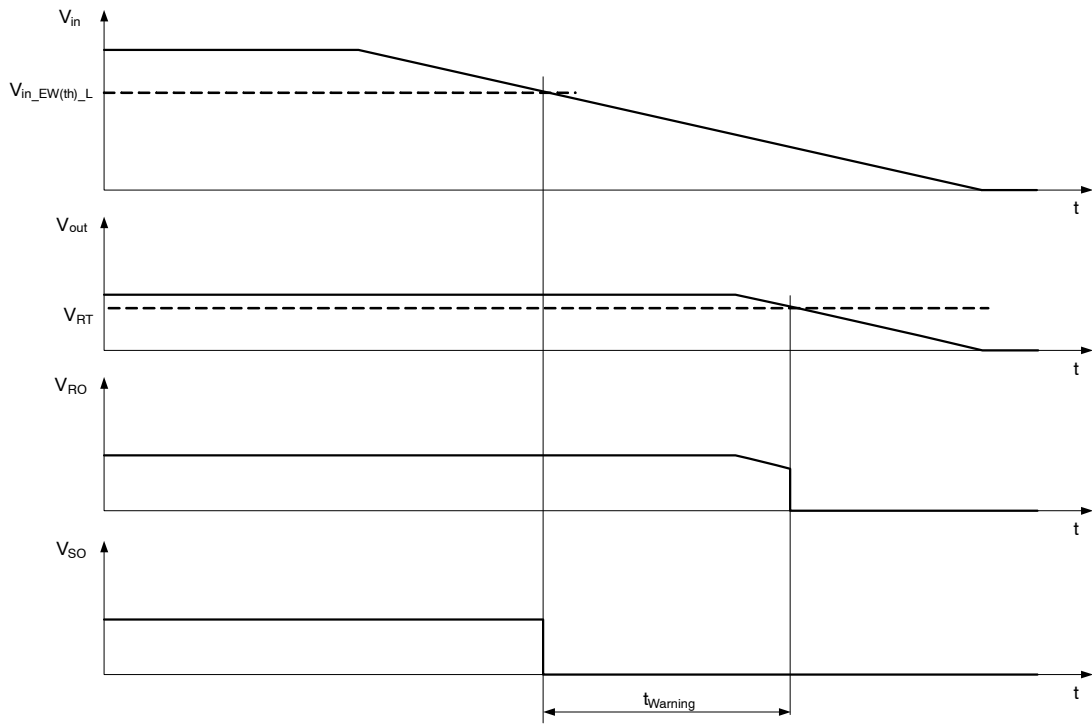


Figure 25. Input Voltage Early Warning Function Diagram

DEFINITIONS**General**

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent Current

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current.

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. It means that

the device is capable to supply minimum 200 mA without sending Reset signal to microprocessor.

Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8667 regulator is self-protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figures 4 to 25.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8667 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV8667 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs. Output Current is shown in Figure 13. The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load transient response.

Enable Operation

The Enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet.

Reset Delay Time Select

Selection of the NCV8667yz devices and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or OUT, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the slower Reset time (DT = GND condition). Times are in pairs and are highlighted in the chart below. Consult factory for availability. The Delay Time select (DT) pin is logic level controlled and provides Reset Delay time per the chart. Note the DT pin is sampled only when RO is low, and changes to the DT pin when RO is high will not effect the reset delay time.

Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 24. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V_{out} = 1.0 V. The Reset Output (RO) circuitry includes internal pull-up connected to the output (V_{out}) No external pull-up is necessary.

Reset signal is also generated in case when input voltage decreases below its minimum operating limit.

RESET DELAY AND RESET THRESHOLD OPTIONS

| Part Number | DT = GND Reset Time | DT = V _{out} Reset Time | Reset Threshold |
|-------------|------------------------|-------------------------------------|--------------------|
| NCV86671z | 8 ms | 128 ms | 93% |

NOTE: The timing values can be selected from following list: 8, 16, 32, 64, 128 ms. The reset threshold values can be selected from the following list: 90% and 93%. Contact factory for other timing combinations not included in the table.

Sense Input (SI)/Sense Output (SO) Voltage Monitor

An on-chip comparator is available to provide early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time (T_{WARNING}) to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor (SI). (See Figure 1) The values for R_{SI1} and R_{SI2} are selected for a typical threshold of 1.2 V on the SI pin according to Equations 1 and 2, where V_{in_EW(th)} is demanded value of input voltage at which Early Warning signal has to be generated. R_{SI2} is recommended to be selected in range of 100 kΩ to 1 MΩ. The higher are values of resistors R_{SI1} and R_{SI2} the lower is current flowing through the resistor divider, however this also increases a delay between Input voltage and SI input voltage caused by charging SI input capacitance with higher RC constant. The delay can be lowered by decreasing the resistors values with consequence of resistor divider current is increased.

$$V_{in_EW(th)} = 1.25 \left(1 + \frac{R_{SI1}}{R_{SI2}} \right) \quad (eq. 1)$$

$$R_{SI1} = R_{SI2} \left(\frac{V_{in_EW(th)}}{1.2} - 1 \right) \quad (eq. 2)$$

Sense Output

The Sense Output is from an open drain driver with an internal 30 kΩ pull up resistor to V_{out}. Figure 26 shows the SO Monitor timing waveforms as a result of the circuit depicted in Figure 1. If the input voltage decreases the output voltage decreases as well. If the SI input low threshold voltage is crossed it causes the voltage on the SO output goes low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. T_{WARNING} is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal.

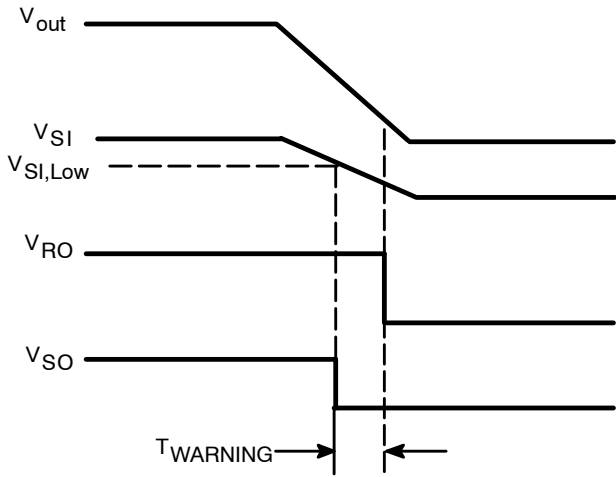


Figure 26. SO Warning Timing Diagram

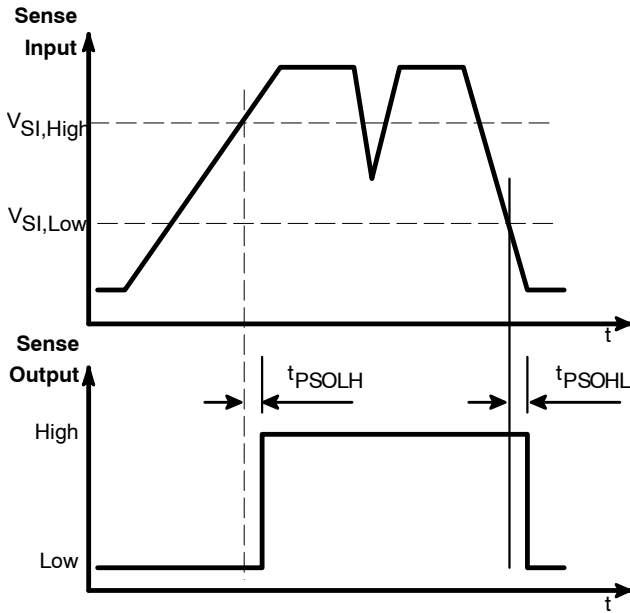


Figure 27. Sense Input to Sense Output Timing Diagram

Thermal Considerations

As power in the NCV8667 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration

on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8667 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8667 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (\text{eq. 3})$$

Since T_J is not recommended to exceed 150°C , then the NCV8667 soldered on 645 mm^2 , 1 oz copper area, FR4 can dissipate up to 1.33 W when the ambient temperature (T_A) is 25°C . See Figure 28 for R_{thJA} versus PCB area. The power dissipated by the NCV8667 can be calculated from the following equations:

$$P_D \approx V_{in}(I_q @ I_{out}) + I_{out}(V_{in} - V_{out}) \quad (\text{eq. 4})$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + (V_{out} \times I_{out})}{I_{out} + I_q} \quad (\text{eq. 5})$$

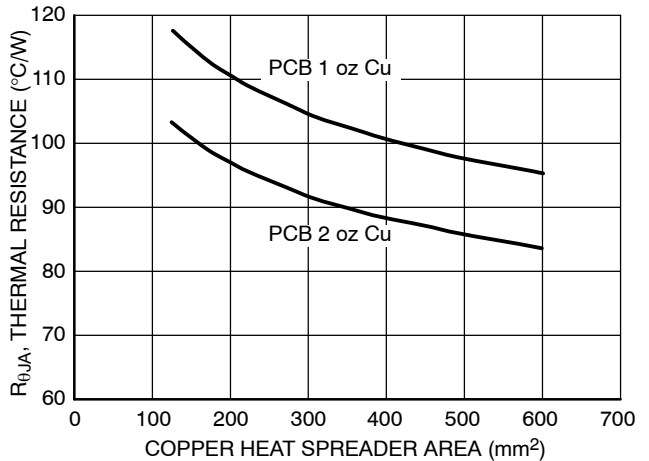


Figure 28. Thermal Resistance vs. PCB Copper Area

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8667 and make traces as short as possible.

ORDERING INFORMATION

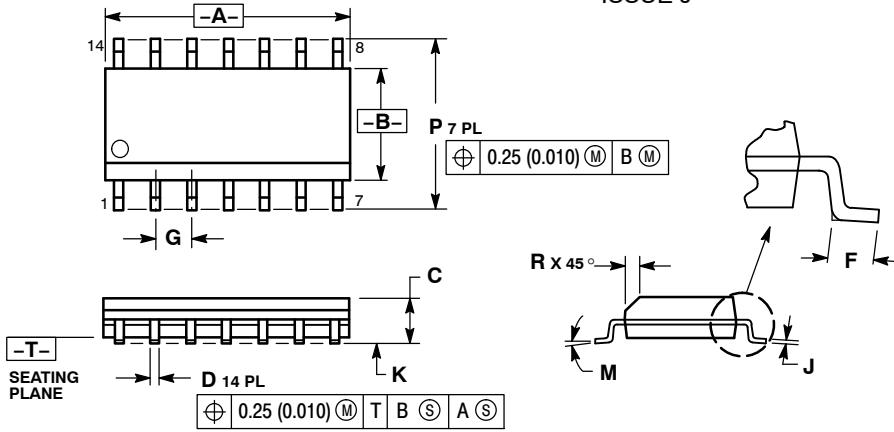
| Device | Output Voltage | Reset Delay Time DT = GND/V _{out} | Reset Threshold (Typ) | Marking | Package | Shipping† |
|------------------|----------------|---|-----------------------|------------|-----------------|--------------------|
| NCV866710D250R2G | 5.0 V | 8/128 ms | 93 % | V86671050G | SO-14 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

NCV8667

PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE J

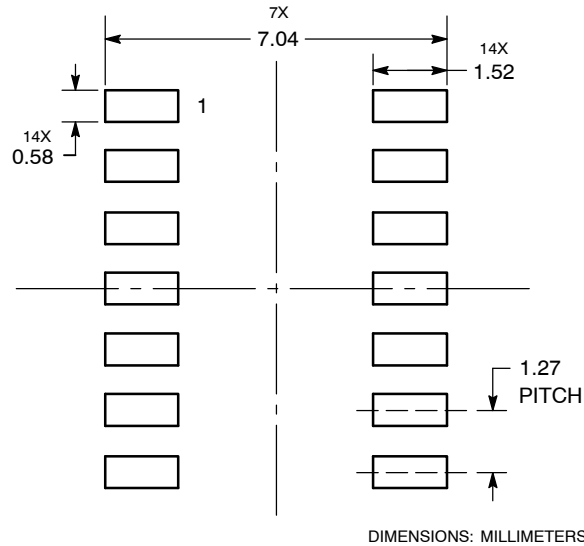


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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