# NCP81239, NCP81239A

# USB Power Delivery 4-Switch Buck Boost Controller

The NCP81239 USB Power Delivery (PD) Controller is a synchronous buck boost that is optimized for converting battery voltage or adaptor voltage into power supply rails required in notebook, tablet, and desktop systems, as well as many other consumer devices using USB PD standard and C−Type cables. The NCP81239 is fully compliant to the USB Power Delivery Specification when used in conjunction with a USB PD or C−Type Interface Controller. NCP81239 is designed for applications requiring dynamically controlled slew rate limited output voltage that require either voltage higher or lower than the input voltage. The NCP81239 drives 4 NMOSFET switches, allowing it to buck or boost and support the consumer and provider role swap function specified in the USB Power Delivery Specification which is suitable for all USB PD applications. The USB PD Buck Boost Controller operates with a supply and load range of 4.5 V to 32 V. NCP81239A is functionally same as NCP81239 except with different $I^2C$ address.

## Features

- Wide Input Voltage Range: from 4.5 V to 32 V
- Dynamically Programmed Frequency from 150 kHz to 1.2 MHz
- $I^2C$ Interface
- Real Time Power Good Indication
- Controlled Slew Rate Voltage Transitioning
- Feedback Pin with Internally Programmed Reference
- Support USBPD/QC2.0/QC3.0 Profile
- 2 Independent Current Sensing Inputs
- Over Temperature Protection
- Adaptive Non−Overlap Gate Drivers
- Filter Capacitor Switch Control
- Over−Voltage and Over−Current Protection
- Dead Battery Power Support
- 5 x 5 mm QFN32 Package

## ORDERING INFORMATION

| Device | Package | Shipping† | $I^2C$ Address |
|---|---|---|---|
| NCP81239MNTXG | QFN32 (Pb−Free) | 4000 / Tape & Reel | 74H |
| NCP81239AMNTXG | QFN32 (Pb−Free) | 4000 / Tape & Reel | 75H |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
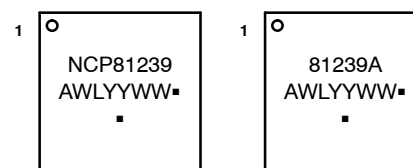
## ON Semiconductor®

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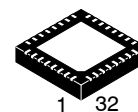
**QFN32 5x5, 0.5P**
**CASE 485CE**

### MARKING DIAGRAM

| | |
|---|---|
| 1 ○ NCP81239 AWLYYWW▪ ▪ | 1 ○ 81239A AWLYYWW▪ ▪ |

A     = Assembly Location
WL   = Wafer Lot
YY   = Year
WW  = Work Week
▪     = Pb−Free Package
(Note: Microdot may be in either location)

## Typical Application

- Notebooks, Tablets, Desktops
- All in Ones
- Monitors, TVs, and Set Top Boxes
- Consumer Electronics
- Car Chargers
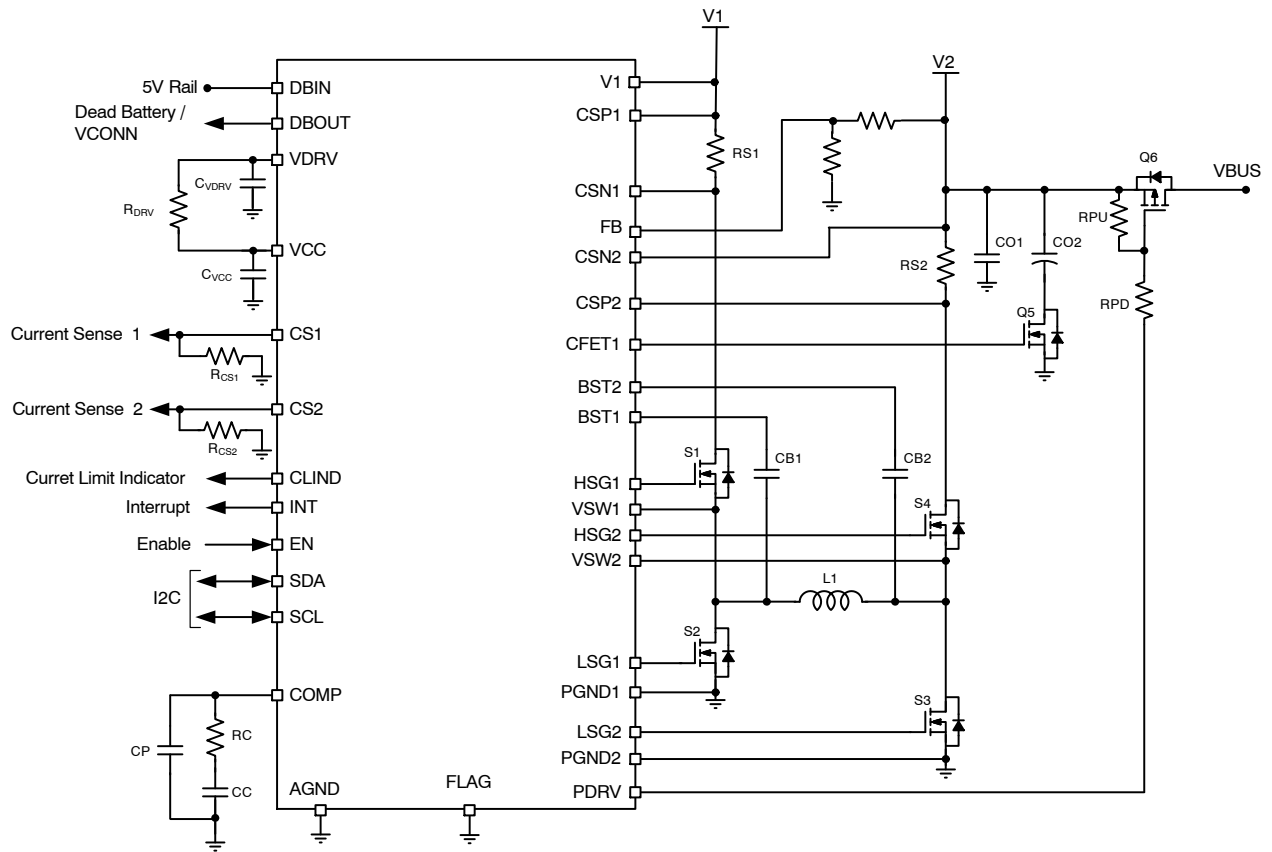- Docking Stations
- Power Banks

# NCP81239, NCP81239A
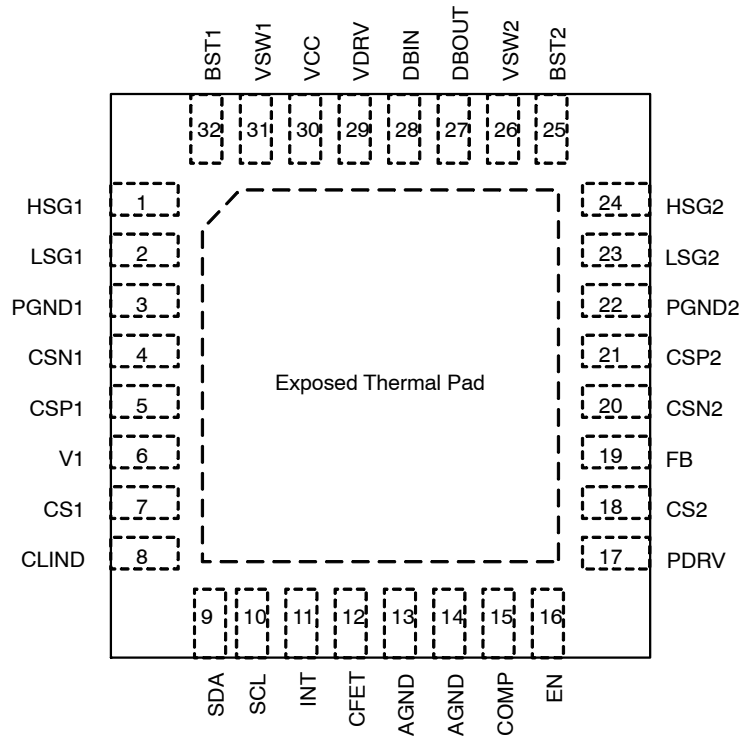


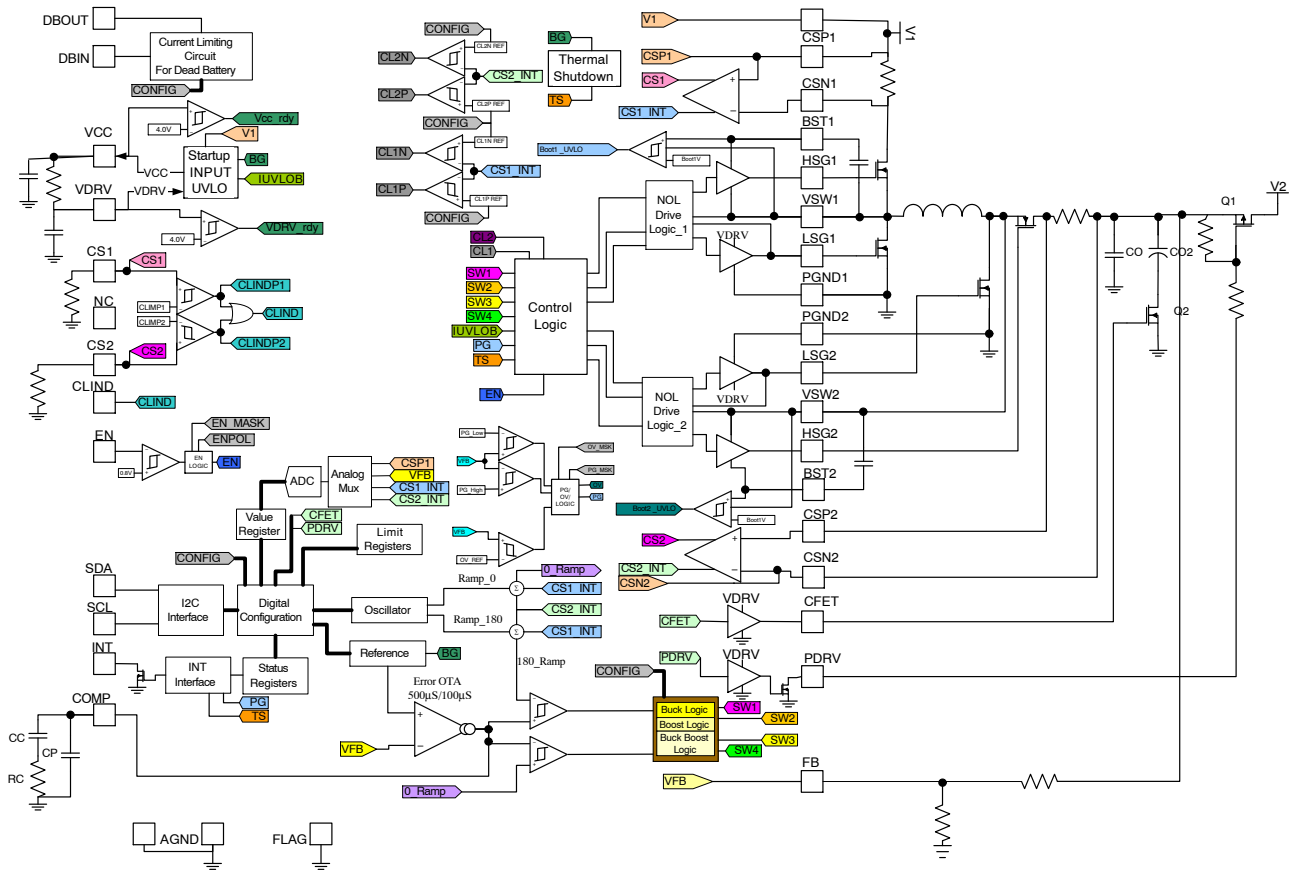Figure 1. Typical Application Circuit



Figure 2. Pinout

**Figure 3. Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin | Pin Name | Description |
|---|---|---|
| 1 | HSG1 | S1 gate drive. Drives the S1 N−channel MOSFET with a voltage equal to VDRV superimposed on the switch node voltage VSW1. |
| 2 | LSG1 | Drives the gate of the S2 N−channel MOSFET between ground and VDRV. |
| 3, 22 | PGND | Power ground for the low side MOSFET drivers. Connect these pins closely to the source of the bottom N−channel MOSFETs. |
| 4 | CSN1 | Negative terminal of the current sense amplifier. |
| 5 | CSP1 | Positive terminal of the current sense amplifier. |
| 6 | V1 | Input voltage of the converter |
| 7 | CS1 | Current sense amplifier output. CS1 will source a current that is proportional to the voltage across RS1 to an external resistor. CS1 voltage can be monitored with a high impedance input. Ground this pin if not used. |
| 8 | CLIND | Open drain output to indicate that the CS1 or CS2 voltage has exceeded the I2C programmed limit. |
| 9 | SDA | I2C interface data line. |
| 10 | SCL | I2C interface clock line. |
| 11 | INT | Interrupt is an open drain output that indicates the state of the output power, the internal thermal trip, and other I2C programmable functions. |
| 12 | CFET | Controlled drive of an external MOSFET that connects a bulk output capacitor to the output of the power converter. Necessary to adhere to low capacitance limits of the standard USB Specifications for power prior to USB PD negotiation. |
| 13−14 | AGND | The ground pin for the analog circuitry. |
| 15 | COMP | Output of the transconductance amplifier used for stability in closed loop operation. |

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin | Pin Name | Description |
|-----|----------|-------------|
| 16 | EN | Precision enable starts the part and places it into default configuration when toggled. |
| 17 | PDRV | The open drain output used to control a PMOSFET. |
| 18 | CS2 | Current sense amplifier output. CS2 will source a current that is proportional to the voltage across RS2 to an external resistor. CS2 voltage can be monitored with a high impedance input. Ground this pin if not used. |
| 19 | FB | Feedback voltage of the output, negative terminal of the gm amplifier. |
| 20 | CSN2 | Negative terminal of the current sense amplifier. |
| 21 | CSP2 | Positive terminal of the current sense amplifier. |
| 23 | LSG2 | Drives the gate of the S3 N−channel MOSFET between ground and VDRV. |
| 24 | HSG2 | S4 gate drive. Drives the S4 N−channel MOSFET with a voltage equal to VDRV superimposed on the switch node voltage VSW2. |
| 25 | BST2 | Bootstrapped Driver Supply. The BST2 pin swings from a diode voltage below VDRV up to a diode voltage below VOUT + VDRV. Place a 0.1 μF capacitor from this pin to VSW2. |
| 26 | VSW2 | Switch Node. VSW2 pin swings from a diode voltage drop below ground up to output voltage. |
| 27 | DBOUT | The output of the dead battery circuit which can also be used for the VCONN voltage supply. |
| 28 | DBIN | The dead battery input to the converter where 5 V is applied. A 1 μF capacitor should be placed close to the part to decouple this line. |
| 29 | VDRV | Internal voltage supply to the driver circuits. A 1 μF capacitor should be placed close to the part to decouple this line. |
| 30 | VCC | The VCC pin supplies power to the internal circuitry. The VCC is the output of a linear regulator which is powered from V1. Pin should be decoupled with a 1 μF capacitor for stable operation. |
| 31 | VSW1 | Switch Node. VSW1 pin swings from a diode voltage drop below ground up to V1. |
| 32 | BST1 | Driver Supply. The BST1 pin swings from a diode voltage below VDRV up to a diode voltage below V1 + VDRV. Place a 0.1 μF capacitor from this pin to VSW1. |
| 33 | THPAD | Center Thermal Pad. Connect to AGND externally. |

**Table 2. MAXIMUM RATINGS**
Over operating free−air temperature range unless otherwise noted

| Rating | Symbol | Min | Max | Unit |
|--------|--------|-----|-----|------|
| Input of the Dead Battery Circuit | DBIN | −0.3 | 5.5 | V |
| Output of the Dead Battery Circuit | DBOUT | −0.3 | 5.5 | V |
| Driver Input Voltage | VDRV | −0.3 | 5.5 | V |
| Internal Regulator Output | VCC | −0.3 | 5.5 | V |
| Output of Current Sense Amplifiers | CS1, CS2 | −0.3 | 3.0 | V |
| Current Limit Indicator | CLIND | −0.3 | VCC + 0.3 | V |
| Interrupt Indicator | INT | −0.3 | VCC + 0.3 | V |
| Enable Input | EN | −0.3 | 5.5 | V |
| I$^2$C Communication Lines | SDA, SCL | −0.3 | VCC + 0.3 | V |
| Compensation Output | COMP | −0.3 | VCC + 0.3 | V |
| V1 Power Stage Input Voltage | V1 | −0.3 | 32 V, 40 V (20 ns) | V |
| Positive Current Sense | CSP1 | −0.3 | 32 V, 40 V (20 ns) | V |
| Negative Current Sense | CSN1 | −0.3 | 32 V, 40 V (20 ns) | V |
| Positive Current Sense | CSP2 | −0.3 | 32 V, 40 V (20 ns) | V |
| Negative Current Sense | CSN2 | −0.3 | 32 V, 40 V (20 ns) | V |
| Feedback Voltage | FB | −0.3 | 5.5 | V |

## Table 2. MAXIMUM RATINGS

Over operating free−air temperature range unless otherwise noted

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| CFET Driver | CFET | −0.3 | VCC + 0.3 | V |
| Driver 1 and Driver 2 Positive Rails | BST1, BST2 | −0.3 V wrt/PGND −0.3 V wrt/VSW | 37 V, 40 V (20 ns) wrt/PGND 5.5 V wrt/VSW | V |
| High Side Driver 1 and Driver 2 | HSG1, HSG2 | −0.3 V wrt/PGND −0.3 V wrt/VSW | 37 V, 40 V (20 ns) wrt/GND 5.5 V wrt/VSW | V |
| Switching Nodes and Return Path of Driver 1 and Driver 2 | VSW1, VSW2 | −5.0 V | 32 V, 40 V (20 ns) | V |
| Low Side Driver 1 and Driver 2 | LSG1, LSG2 | −0.3 V | 5.5 | V |
| PMOSFET Driver | PDRV | −0.3 | 32 V, 40 V (20 ns) | V |
| Voltage Differential | AGND to PGND | −0.3 | 0.3 | V |
| CSP1−CSN1, CSP2−CSN2 Differential Voltage | CS1DIF, CS2DIF | −0.5 | 0.5 | V |
| PDRV Maximum Current | PDRVI | 0 | 10 | mA |
| PDRV Maximum Pulse Current (100 ms on time, with > 1 s interval) | PDRVIPUL | 0 | 200 | mA |
| Maximum VCC Current | VCCI | 0 | 80 | mA |
| Operating Junction Temperature Range (Note 1) | TJ | −40 | 150 | °C |
| Operating Ambient Temperature Range | TA | −40 | 100 | °C |
| Storage Temperature Range | TSTG | −55 | 150 | °C |
| Thermal Characteristics (Note 2) QFN 32 5mm x 5mm Maximum Power Dissipation @ TA = 25°C Maximum Power Dissipation @ TA = 85°C Thermal Resistance Junction−to−Air with Solder Thermal Resistance Junction−to−Case Top with Solder Thermal Resistance Junction−to−Case Bottom with Solder | PD PD RΘJA RΘJCT RΘJCB | | 4.1 2.1 30 1.7 2.0 | W W °C/W °C/W °C/W |
| Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free (Note 3) | RF | | 260 Peak | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The maximum package power dissipation limit must not be exceeded.
2. The value of ΘJA is measured with the device mounted on a 3in x 3in, 4 layer, 0.062 inch FR−4 board with 1.5 oz. copper on the top and bottom layers and 0.5 ounce copper on the inner layers, in a still air environment with TA = 25°C.
3. 60−180 seconds minimum above 237°C.

## Table 3. ELECTRICAL CHARACTERISTICS

(V1 = 12 V, $V_{out}$ = 1.0 V , $T_A$ = +25°C for typical value; −40°C < $T_A$ < 100°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| V1 Operating Input Voltage | V1 | | 4.5 | | 32 | V |
| VDRV Operating Input Voltage | VDRV | | 4.5 | 5 | 5.5 | V |
| VCC UVLO Rising Threshold | VCC$_{START}$ | | | 4.3 | | V |
| UVLO Hysteresis for VCC | VCCV$_{HYS}$ | Falling Hysteresis | | 300 | | mV |
| VDRV UVLO Rising Threshold | VDRV$_{START}$ | | | 4.3 | | V |
| UVLO Hysteresis for VDRV | VDRV$_{HYS}$ | Falling Hysteresis | | 300 | | mV |

**Table 3. ELECTRICAL CHARACTERISTICS**

(V1 = 12 V, $V_{out}$ = 1.0 V , $T_A$ = +25°C for typical value; −40°C < $T_A$ < 100°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VCC Output Voltage | VCC | With no external load | 4.5 | 5 | | V |
| VCC Drop Out Voltage | VCCDROOP | 30 mA load | | 150 | | mV |
| VCC Output Current Limit | IOUT$_{VCC}$ | VCC Loaded to 4.3 V | 80 | 97 | | mA |
| V1 Shutdown Supply Current | IVCC_SD | EN = 0 V, 4.3 V ≤ V1 ≤ 28 V | | 6.6 | 7.7 | mA |
| VDRIVE Switching Current Buck | IV1_SW | EN = 5 V, Cgate = 2.2 nF, VSW = 0 V, FSW = 600 kHz | | 15 | | mA |
| VDRIVE Switching Current Boost | IV1_SW | EN = 5 V, Cgate = 2.2 nF, VSW = 0 V, FSW = 600 kHz | | 15 | | mA |
| **Voltage Output** | | | | | | |
| Voltage Output Accuracy | FB | DAC_TARGET = 00110010<br>DAC_TARGET = 01111000<br>DAC_TARGET = 11001000 | 0.495<br>1.188<br>1.98 | 0.5<br>1.2<br>2.0 | 0.505<br>1.212<br>2.02 | V |
| Voltage Accuracy Over Temperature | VOUTERT | VFB ≥ 0.5 V<br>VFB < 0.5 V | −1.0<br>−5 | | 1.0<br>5 | %<br>mV |
| | VOUTER | $T_A$ = 25°C<br>VFB ≥ 0.5 V | −0.45 | | 0.45 | % |
| **Transconductance  Amplifier** | | | | | | |
| Gain Bandwidth Product | GBW | (Note 4) | | 5.2 | | MHz |
| Transconductance | GM1 | Default | | 500 | | μS |
| Max Output Source Current limit | GMSOC | | 60 | 80 | | μA |
| Max Output Sink Current  limit | GMSIC | | 60 | 80 | | μA |
| Voltage Ramp | Vramp | | | 1.4 | | V |
| **Internal BST Diode** | | | | | | |
| Forward Voltage Drop | VFBOT | $I_F$ = 10 mA, $T_A$ = 25°C | 0.35 | 0.46 | 0.55 | V |
| Reverse Bias Leakage Current | DIL | BST−VSW  = 5 V<br>$V_{SW}$ = 28 V, $T_A$ = 25°C | | 0.05 | 1 | μA |
| BST−VSW UVLO | BST1$_{UVLO}$ | Rising, Note 4 | | 3.5 | | V |
| BST−VSW Hysteresis | BST$_{HYS}$ | Note 4 | | 300 | | mV |
| **Oscillator** | | | | | | |
| Oscillator Frequency | FSW_0 | FSW = 000, default | 528 | 600 | 672 | kHz |
| | FSW_1 | FSW = 001 | 132 | 150 | 168 | kHz |
| | FSW_7 | FSW = 110 | 1056 | 1200 | 1344 | kHz |
| Oscillator Frequency Accuracy | FSWE | | −12 | | 12 | % |
| Minimum On Time | MOT | Measured at 10% to 90% of VCC | | 50 | | ns |
| Minimum Off  Time | MOFT | Measured at 90% to 10% of VCC | | 90 | | ns |
| **INT Thresholds** | | | | | | |
| Interrupt  Low Voltage | VINTI | IINT(sink) = 2 mA | | | 0.2 | V |
| Interrupt High Leakage Current | INII | 3.3 V | | 3 | 100 | nA |
| Interrupt Startup Delay | INTPG | Soft Start end to PG positive edge | | 2.1 | | ms |

4.  Ensured by design. Not production tested.

**Table 3. ELECTRICAL CHARACTERISTICS**
(V1 = 12 V, $V_{out}$ = 1.0 V , $T_A$ = +25°C for typical value; −40°C < $T_A$ < 100°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Interrupt Propagation Delay | PGI | Delay for power good in | | 3.3 | | ms |
| | PGO | Delay for power good out | | 100 | | ns |
| Power Good Threshold | PGTH | Power Good in from high | | 105 | | % |
| | PGTH | Power Good in from low | | 95 | | % |
| | PGTHYS | PG falling hysteresis | | 2.5 | | % |
| FB Overvoltage Threshold | FB_OV | | | 120 | | % |
| Overvoltage Propagation Delay | VFB_OVDL | | | 1 Cycle | | |
| **External Current Sense (CS1,CS2)** | | | | | | |
| Positive Current Measurement High | CS10 | CSP1−CSN1 or CSP2−CSN2 = 100 mV | | 500 | | μA |
| Transconductance Gain Factor | CSGT | Current Sense Transconductance Vsense = 1 mV to 100 mV | | 5 | | mS |
| Transconductance Deviation | CSGE | | −20 | | 20 | % |
| Current Sense Common Mode Range | CSCMMR | | 3 | | 32 | V |
| −3dB Small Signal Bandwidth | CSBW | VSENSE (AC) = 10 mVPP, RGAIN = 10 kΩ (Note 4) | | 30 | | MHz |
| Input Sense Voltage Full Scale | ISVFS | | | | 100 | mV |
| CS Output Voltage Range | CSOR | VSENSE = 100 mV Rset = 6k | 0 | | 3 | V |
| **External Current Limit (CLIND)** | | | | | | |
| Current Limit Indicator Output Low | CLINDL | Input current = 500 μA | | 5.6 | 100 | mV |
| Current Limit Indicator Output High | CLINDH | Input current = 500 μA | 4.0 | 5.0 | | V |
| **Internal Current Sense** | | | | | | |
| Internal Current Sense Gain for PWM | ICG | CSPx−CSNx = 100 mV | 9.2 | 9.8 | 10.5 | V/V |
| Positive Peak Current Limit Trip | PPCLT | INT_CL = 00 | 34 | 39 | 44 | mV |
| Negative Valley Current Limit Trip | NVCLT | INT_CL_NEG = 00 | 31 | 40 | 45 | mV |
| **Switching MOSFET Drivers** | | | | | | |
| HSG1 HSG2 Pullup Resistance | HSG_PU | BST−VSW = 4.5 V | | 2.8 | | Ω |
| HSG1 HSG2 Pulldown Resistance | HSG_PD | BST−VSW = 4.5 V | | 1.2 | | Ω |
| LSG1 LSG2 Pullup Resistance | LSG_PU | LSG −PGND = 2.5 V | | 3.3 | | Ω |
| LSG1 LSG2 Pulldown Resistance | LSG_PD | LSG −PGND = 2.5 V | | 0.9 | | Ω |
| HSG Falling to LSG Rising Delay | HSLSD | | | 15 | | ns |
| LSG Falling to HSG Rising Delay | LSHSD | | | 15 | | ns |

4. Ensured by design. Not production tested.

**Table 3. ELECTRICAL CHARACTERISTICS**

(V1 = 12 V, V$_{out}$ = 1.0 V , T$_A$ = +25°C for typical value; −40°C < T$_A$ < 100°C for min/max values unless noted otherwise)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CFET** | | | | | | |
| CFET Drive Voltage | CFETDV | | | VCC | | V |
| Source/Sink Current | CFETSS | CFET clamped to 2 V | | 2 | | μA |
| Pull Down Delay | CFETD | Measured at 10% to 90% of VCC | | 10 | | ms |
| CFET Pull Down Resistance | CFETR | Measured with 1 mA Pull up Current, after 10ms rising edge delay | | 1.3 | | kΩ |
| **Slew Rate/Soft Start** | | | | | | |
| Charge Slew Rate | SLEWP | Slew = 00, FB = 0.1 VOUT<br>Slew = 11, FB = 0.1 VOUT | | 0.6<br>4.8 | | mV/μs |
| Discharge Slew Rate | SLEWN | Slew = 00, FB = 0.1 VOUT<br>Slew = 11, FB = 0.1 VOUT | | −0.6<br>−4.8 | | mV/μs |
| Prebias Level | PBLV | FB=0.1VOUT | | 300 | | mV |
| **Dead Battery/VCONN** | | | | | | |
| Dead Battery Input Voltage Range | VDB | | 4.5 | 5 | 5.25 | V |
| Dead Battery Output Voltage | VIO | VDB = 5 V, Output Current 32 mA | 4 | 4.7 | 5 | V |
| Dead Battery Current Limit | DB_LIM | VDB = 5 V, V1 greater than 2 V | 29 | 57 | | mA |
| **Enable** | | | | | | |
| EN High Threshold Voltage | ENHT | EM_MASK = ENPU = ENPOL = 0 | | 798 | 820 | mV |
| EN Low Threshold Voltage | ENLT | | 640 | 665 | | mV |
| EN Pull Up Current | IEN_UP | EN = 0 V | | 5 | | μA |
| EN Pull Down Current | IEN_DN | EN = VCC | | 5 | | μA |
| **I²C Interface** | | | | | | |
| Voltage Threshold | I2CVTH | | 0.95 | 1 | 1.05 | V |
| Propagation Delay | I2CPD | (Note 4) | | 25 | | ns |
| Communication Speed | I2CSP | | | | 1 | MHz |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold | TSD | (Note 4) | | 151 | | °C |
| Thermal Shutdown Hysteresis | TSDHYS | (Note 4) | | 28 | | °C |
| **PDRV** | | | | | | |
| PDRV Operating Range | | | 0 | | 28 | V |
| PDRV Leakage Current | PDRV_IDS | FET OFF, VPDRV = 28 V | | 180 | | nA |
| PDRV Saturation Voltage | PDRV_VDS | ISNK = 10 mA | | 0.20 | | V |
| **Internal ADC** | | | | | | |
| Range | ADCRN | (Note 4) | 0 | | 2.55 | V |
| LSB Value | ADCLSB | (Note 4) | | 20 | | mV |
| Error | ADCFE | (Note 4) | | 1 | | LSB |

4. Ensured by design. Not production tested.

## APPLICATION INFORMATION

**Dual Edge Current Mode Control**

   When dual edge current mode control is used, two voltage ramps are generated that are 180 degrees out of phase. The inductor current signal is added to the ramps to incorporate current mode control. In Figure 4, the COMP signal from the compensation output interacts with two triangle ramps to generate gate signals to the switches from S1 to S4. Two ramp signals cross twice at midpoint within a cycle. When COMP is above the midpoint, the system will operate at

boost mode with S1 always on and S2 always off, but S3 and S4 turning on alternatively in an active switching mode. When COMP is below the midpoint, the system will operation at buck mode, with S4 always on and S3 always off, but S1 and S2 turning on alternatively in an active switching mode. The controller can switch between buck and boost mode smoothly based on the COMP signal from peak current regulation.
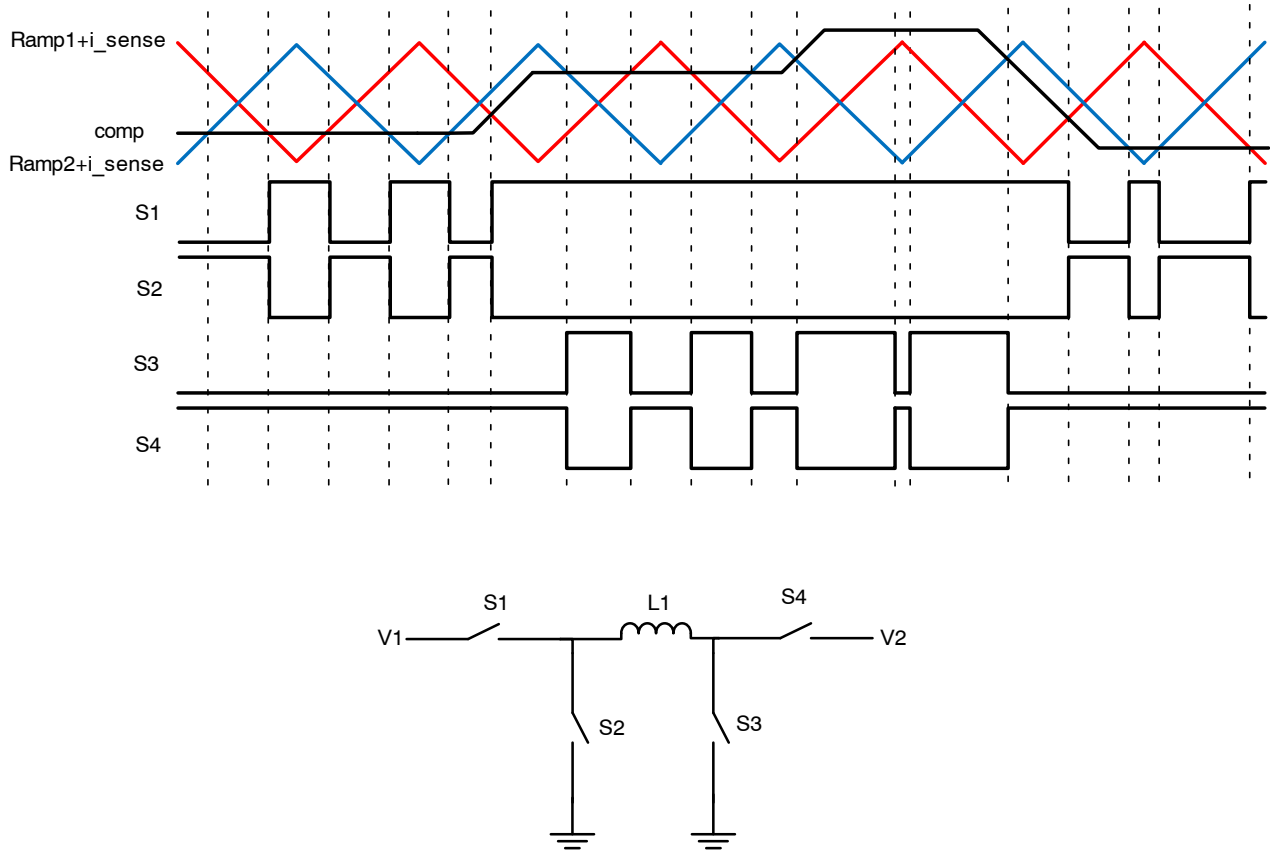


**Figure 4. Transitions for Dual Edge 4 Switch Buck Boost**

## Feedback and Output Voltage Profile

The feedback of the converter output voltage is connected to the FB pin of the device through a resistor divider. Internally FB is connected to the inverting input of the internal transconductance error amplifier. The non−inverting input of the gm amplifier is connected to the internal reference. The internal reference voltage is by default 0.5 V. Therefore a 10:1 resistor divider from the converter output to the FB will set the output voltage to 5 V in default. The reference voltage can be adjusted with 10 mV(default) or 5 mV steps from 0.1 V to 2.55 V through the voltage profile register (01H), which makes the continuous output voltage profile possible through an external resistor divider. For example, by default, if the external resistor divider has a 10:1 ratio, the output voltage profile will be able to vary from 1 V to 25.5 V with 100 mV steps.

**Table 4. VOLTAGE PROFILE REGISTER SETTINGS**

| dac_target (01h) | | | | | | | | Voltage Profile Hex Value | dac_target_lsb (03h, bit 4) | Reference Voltage (mV) |
|---|---|---|---|---|---|---|---|---|---|---|
| bit_8 | bit_7 | bit_6 | bit_5 | bit_4 | bit_3 | bit_2 | bit_1 | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H | 0 | Reserved |
| … | … | … | … | … | … | … | … | … | … | … |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09H | 1 | Reserved |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0AH | 0 | 100 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0AH | 1 | 105 |
| … | … | … | … | … | … | … | … | … | … | … |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32H | 0 | 500(Default) |
| … | … | … | … | … | … | … | … | … | … | … |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | C8H | 0 | 2000 |
| … | … | … | … | … | … | … | … | … | … | … |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFH | 0 | 2550 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFH | 1 | 2555 |

## Transconductance Voltage Error Amplifier

To maintain loop stability under a large change in capacitance, the NCP81239 can change the gm of the internal transconductance error amplifier from 87 μS to 1000 μS allowing the DC gain of the system to be increased more than a decade triggered by the adding and removal of the bulk capacitance or in response to another user input. The default transconductance is 500 μS.

**Table 5. AVAILABLE TRANSCONDUCTANCE SETTING**

| AMP_2 | AMP_1 | AMP_0 | Amplifier GM Value (μS) |
|---|---|---|---|
| 0 | 0 | 0 | 87 |
| 0 | 0 | 1 | 100 |
| 0 | 1 | 0 | 117 |
| 0 | 1 | 1 | 333 |
| 1 | 0 | 0 | 400 |
| 1 | 0 | 1 | 500 |
| 1 | 1 | 0 | 667 |
| 1 | 1 | 1 | 1000 |

## Programmable Slew Rate

The slew rate of the NCP81239 is controlled via the I$^2$C registers with the default slew rate set to 0.6 mV/μs (FB = 0.1 V2, assume the resistor divider ratio is 10:1) which is the slowest allowable rate change. The slew rate is used when the output voltage starts from 0 V to a user selected profile level, changing from one profile to another, or when the output voltage is dynamically changed. The output voltage is divided by a factor of the external resistor divider and connected to FB pin. The 9 Bit DAC is used to increase the reference voltage in 10 or 5 mV increments. The slew rate is decreased by using a slower clock that results in a longer time between voltage steps, and conversely increases by using a faster clock. The step

monotonicity depends on the bandwidth of the converter where a low bandwidth will result in a slower slew rate than the selected value. The available slew rates are shown in Table 6. The selected slew rate is maintained unless the

current limit is tripped; in which case the increased voltage will be governed by the positive current limit until the output voltage falls or the fault is cleared.
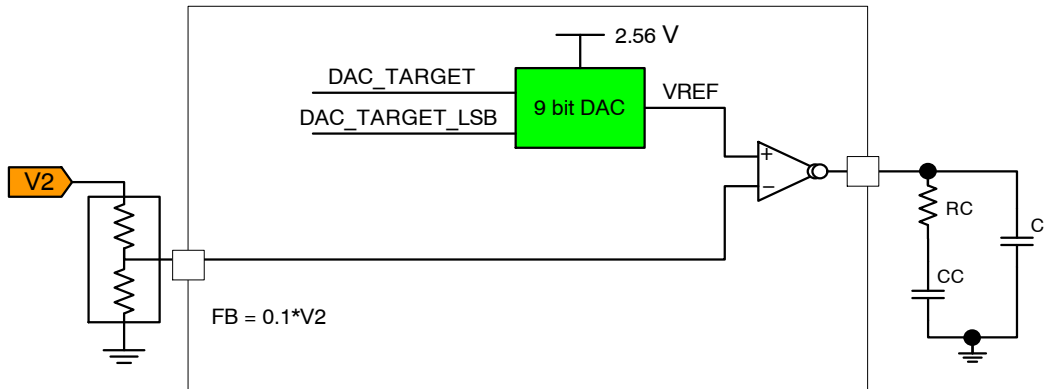


**Figure 5. Slew Rate Limiting Block Diagram and Waveforms**

**Table 6. SLEW RATE SELECTION**

| Slew Bits | Soft Start or Voltage Transition (FB = 0.1*V2) |
|---|---|
| Slew_0 | 0.6 mV/μs |
| Slew_1 | 1.2 mV/μs |
| Slew_2 | 2.4 mV/μs |
| Slew_3 | 4.9 mV/μs |

The discharge slew rate is accomplished in much the same way as the charging except the reference voltage is decreased rather than increased. The slew rate is maintained unless the negative current limit is reached. If the negative current limit is reached, the output voltage is decreased at the maximum rate allowed by the current limit (see the negative current limit section).

**Soft Start**

During a 0 V soft start, standard converters can start in synchronous mode and have a monotonic rising of output

voltage. If a prebias exists on the output and the converter starts in synchronous mode, the prebias voltage could be discharged. The NCP81239 controller ensures that if a prebias is detected, the soft start is completed in a non−synchronous mode to prevent the output from discharging. During softstart, the output rising slew rate will follow the slew rate register with default value set to 0.6 mV/μs (FB = 0.1*V2).

**Frequency Programming**

The switching frequency of the NCP81239 can be programmed from 150 kHz to 1.2 MHz via the I2C interface. The default switching frequency is set to 600 kHz. The switching frequency can be changed on the fly. However, it is a good practice to disable the part and then program to a different frequency to avoid transition glitches at large load current.

**Table 7. FREQUENCY PROGRAMMING TABLE**

| Name | Bit | Definition | Description |
|---|---|---|---|
| Freq1 | 03H [2:0] | Frequency Setting | 3 Bits that Control the Switching Frequency from 150 kHz to 1 MHz.<br>000: 600 kHz<br>001: 150 kHz<br>010: 300 kHz<br>011: 450 kHz<br>100: 750 kHz<br>101: 900 kHz<br>110: 1.2 MHz<br>111: Reserved |

## Current Sense Amplifiers

Internal precision differential amplifiers measure the potential between the terminal CSP1 and CSN1 or CSP2 and CSN2. Current flows from the input V1 to the output in a buck boost design. Current flowing from V1 through the switches to the inductor passes through $R_{SENSE}$. The external sense resistor, $R_{SENSE}$, has a significant effect on the function of current sensing and limiting systems and must be chosen with care. First, the power dissipation in the resistor should be considered. The system load current will cause both heat and voltage loss in $R_{SENSE}$. The power loss and voltage drop drive the designer to make the sense resistor as small as possible while still providing the input dynamic range required by the measurement. Note that input dynamic range is the difference between the maximum input signal and the minimum accurately measured signal, and is limited primarily by input DC offset of the internal amplifier. In addition, $R_{SENSE}$ must be small enough that $V_{SENSE}$ does not exceed the maximum input voltage 100 mV, even under peak load conditions.

The potential difference between CSPx and CSNx is level shifted from the high voltage domain to the low voltage VCC domain where the signal is split into two paths.

The first path, or external path, allows the end user to observe the analog or digital output of the high side current sense. The external path gain is set by the end user allowing the designer to control the observable voltage level. The voltage at CS1 or CS2 can be converted to 7 bits by the ADC and stored in the internal registers which are accessed through the I$^2$C interface.

The second path, or internal path, has internally set gain of 10 and allows cycle by cycle precise limiting of positive and negative peak input current limits.
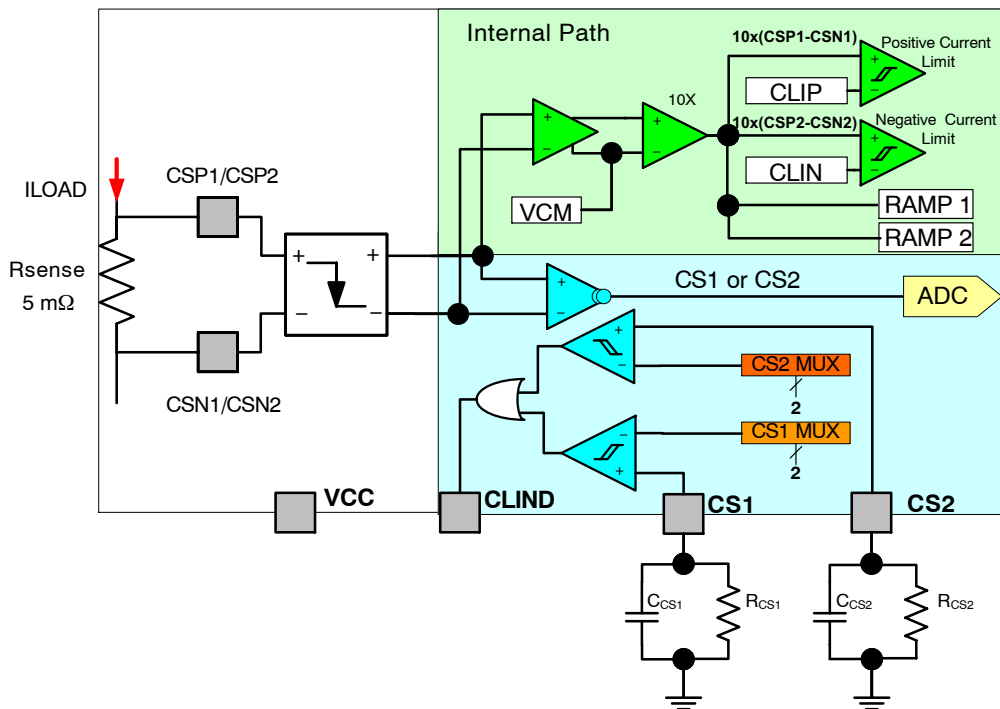


**Figure 6. Block Diagram and Typical Connection for Current Sense**

## Positive Current Limit Internal Path

The NCP81239 has a pulse by pulse current limiting function activated when a positive current limit triggers. CSP1/CSN1 will be the positive current limit sense channel.

When a positive current limit is triggered, the current pulse is truncated. In both buck mode and in boost mode the S1 switch is turned off to limit the energy during an over current event. The current limit is reset every switching cycle and waits for the next positive current limit trigger. In this way, current is limited on a pulse by pulse basis. Pulse by pulse current limiting is advantageous for limiting energy into a load in over current situations but are not up to the task of limiting energy into a low impedance short. To address the low impedance short, the NCP81239 does pulse by pulse current limiting for 2 ms known as Ilim timeout or until the output voltage falls below 300 mV, the controller will enter into fast stop. The NCP81239 remains in fast stop state with all switches driven off for 10 ms. Once the 10 ms has expired, the part is allowed to soft start to the previously programmed voltage and current level if the short circuit condition is cleared.

The internal current limits can be controlled via the I$^2$C interface as shown in Table 8.

**Table 8. INTERNAL PEAK CURRENT LIMIT**

| CLIN_1 | CLIN_0 | CLIM delta Value (mV) | CSP2−CSN2 (mV) | Current at RSENSE = 5 mΩ (A) |
|--------|--------|-----------------------|----------------|------------------------------|
| 0 | 0 | −400 | −40 (Default) | −8 |
| 0 | 1 | −250 | −25 | −5 |
| 1 | 0 | −150 | −15 | −3 |
| 1 | 1 | 0 | 0 | 0 |
| **CLIP_1** | **CLIP_0** | **CLIM delta Value (mV)** | **CSP1−CSN1 (mV)** | **Current at RSENSE = 5 mΩ (A)** |
| 0 | 0 | 380 | 38 (Default) | 7.6 |
| 0 | 1 | 230 | 23 | 4.6 |
| 1 | 0 | 110 | 11 | 2.2 |
| 1 | 1 | 700 | 70 | 14 |

**Negative Current Limit Internal Path**

Negative current limit can be activated in a few instances, including light load synchronous operation, heavy load to light load transition, output overvoltage, and high output voltage to lower output voltage transitions. CSP2/CSN2 will be the negative current limit sense channel.

During light load synchronous operation, or heavy load to light load transitions the negative current limit can be triggered during normal operation. When the sensed current exceeds the negative current limit, the S4 switch is shut off preventing the discharge of the output voltage both in buck mode and in boost mode if the output is in the power good range. Both in boost mode and in buck mode when a negative current is sensed, the S4 switch is turned off for the remainder of either the S4 or S2 switching cycle and is turned on again at the appropriate time. In buck mode, S4 is turned off at the negative current limit transition and turned on again as soon as the S2 on switch cycle ends. In boost mode, the S4 switch is the rectifying switch and upon negative current limit the switch will shut off for the remainder of its switching cycle. The internal negative current limits can be controlled via the I$^2$C interface as shown in Table 8.

**External Path (CS1, CS2, CLIND)**

The voltage drop across the sense resistors as a result of the load can be observed on the CS1 and CS2 pins. Both CS1, CS2 can be monitored with a high impedance input. An external series resistor can be added for additional filtering. The voltage drop is converted into a current by a transconductance amplifier with a typical GM of 5 mS. The final gain of the output is determined by the end users selection of the $R_{CS}$ resistors. The output voltage of the CS pin can be calculated from Equation 1. The user must be careful to keep the dynamic range below 3.0 V when considering the maximum short circuit current.

$$V_{CS} = (I_{LOAD\_MAX} * R_{SENSE} * Trans) * R_{CS} \rightarrow$$

$$\rightarrow 2.967 \text{ V} = (8.5 \text{ A} * 5 \text{ m}\Omega * 5 \text{ mS}) * 13.96 \text{ k}\Omega$$

$$R_{CS} = \frac{V_{CS}}{I_{LOAD} * R_{SENSE} * Trans} \rightarrow$$

$$\rightarrow 13.96 \text{ k}\Omega = \frac{2.967 \text{ V}}{8.5 \text{ A} * 5 \text{ m}\Omega * 5 \text{ mS}} \qquad \text{(eq. 1)}$$

The speed and accuracy of the dual amplifier stage allows the reconstruction of the input and output current signal, creating the ability to limit the peak current. If the user would like to limit the mean DC current of the switch, a capacitor can be placed in parallel with the $R_{CS}$ resistors. CS1, CS2 can be monitored with a high impedance input. An external series resistor can be added for additional filtering.

CS1, CS2 voltages are connected internally to 2 high speed low offset comparators. The comparators output can be used to suspend operation until reset or restart of the part depending on I$^2$C configuration. When the external CLIND flag is triggered, it indicates that one of the internal comparators has exceeded the preset limit (CSx_LIM). The default comparator setting is 250 mV which is a limit of 500 mA with a current sense resistor of 5 mΩ and an $R_{CS}$ resistor of 20 kΩ. The external current limit settings are shown in Table 9.

**Table 9. REGISTER SETTING FOR THE CLIM COMPARATORS**

| CLIMx_1 | CLIMx_0 | CSx_LIM (V) | Current at RSENSE = 5 mΩ RSET = 20 kΩ (A) | Current at RSENSE = 5 mΩ RSET = 10 kΩ (A) |
|---------|---------|-------------|-------------------------------------------|-------------------------------------------|
| 0 | 0 | 0.25 | .5 | 1 |
| 0 | 1 | 0.75 | 1.5 | 3 |
| 1 | 0 | 1.5 | 3 | 6 |
| 1 | 1 | 2.5 | 5 | 10 |

## Overvoltage Protection (OVP)

When the divided output voltage is 120% (typical) above the internal reference voltage for greater than one switching cycle, an OV fault is set. During an overvoltage fault, S1 is driven off, S2 is driven on, and S3 and S4 are modulated to discharge the output voltage while preventing the inductor current from going beyond the I$^2$C programmed negative current limit.
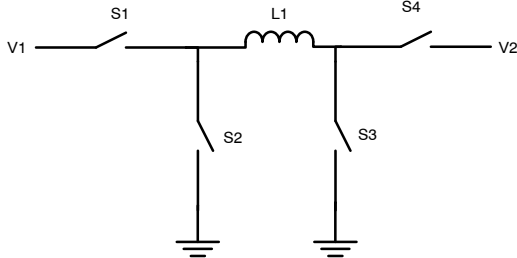


**Figure 7. Diagram for OV Protection**

During overvoltage fault detection the switching frequency changes from its I$^2$C set value to 50 kHz to reduce the power dissipation in the switches and prevent the inductor from saturating. OVP is disabled during voltage changes to ensure voltage changes and glitches during slewing are not falsely reported as faults. The OV faults are reengaged 1 ms after completion of the soft start.

When the output voltage profile is set below 100 mV, it is easy to trigger OVP falsely. So it is better for one to avoid using output voltage profile under 100 mV. When 0 V output voltage is needed, one can pull EN pin low with external circuit or write to EN registers (00h) through I$^2$C to disable NCP81239. Setting output voltage profile to 0 via I$^2$C is not recommended.
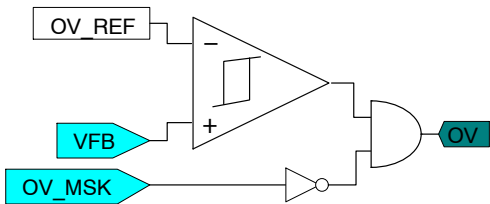


**Figure 8. OV Block Diagram**

**Table 10. OVERVOLTAGE MASKING**

| OV_MSK | Description |
|---|---|
| 0 | OV Action and Indication Unmasked |
| 1 | OV Action and Indication Masked |

## Power Good Monitor (PG)

NCP81239 provides two window comparators to monitor the internal feedback voltage. The target voltage window is ±5% of the reference voltage (typical). Once the feedback voltage is within the power good window, a power good indication is asserted once a 3.3 ms timer has expired. If the feedback voltage falls outside a ±7% window for greater than 1 switching cycle, the power good register is reset. Power good is indicated on the INT pin if the I$^2$C register is set to display the PG state. During startup, INT is set until the feedback voltage is within the specified range for 3.3 ms.
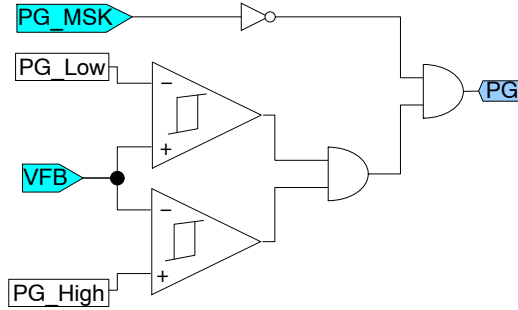


**Figure 9. PG Block Diagram**

**Table 11. POWER GOOD MASKING**

| PG_MSK | Description |
|---|---|
| 0 | PG Action and Indication Unmasked |
| 1 | PG Action and Indication Masked |

## Thermal Shutdown

The NCP81239 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown threshold (typically 150°C), all MOSFETs will be driven to the off state, and the part will wait until the temperature decreases to an acceptable level. The fault will be reported to the fault register and the INT flag will be set unless it is masked. When the junction temperature drops below 125°C (typical), the part will discharge the output voltage to Vsafe 0 V.

## CFET Turn On

The CFET is used to engage the output bulk capacitance after successful negotiations between a consumer and a provider. The USB Power Delivery Specification requires that no more than 30 μF of capacitance be present on the VBUS rail when sinking power. Once the consumer and provider have completed a power role swap, a larger capacitance can be added to the output rail to accommodate a higher power level. The bulk capacitance must be added in such a way as to minimize current draw and reduce the voltage perturbation of the bus voltage. The NCP81239 incorporates a right drive circuit that regulates current into the gate of the MOSFET such that the MOSFET turns on slowly reducing the drain to source resistance gradually. Once the transition from high to low has occurred in a controlled way, a strong pulldown driver is used to ensure normal operation does not turn on the power N−MOSFET engaging the bulk capacitance. The CFET must be activated through the I$^2$C interface where it can be engaged and disengaged. The default state is to have the CFET disengaged.

# NCP81239, NCP81239A
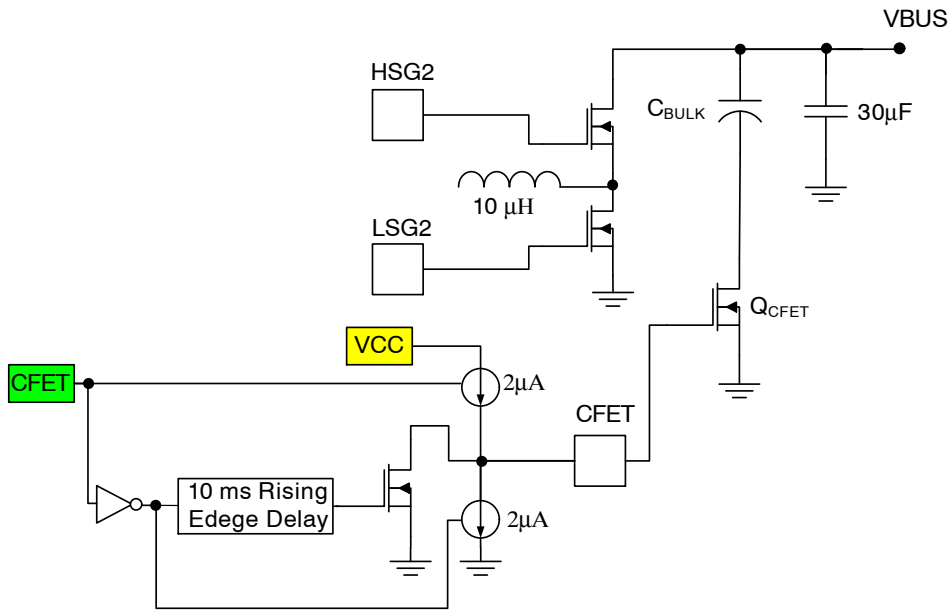


**Figure 10. CFET Drive**

**Table 12. CFET ACTIVATION TABLE**

| CFET_0 | Description |
|--------|-------------|
| 0 | CFET Drive Pulldown |
| 1 | CFET Drive Pull Up |

**PFET Drive**

The PMOS drive is an open drain output used to control the turn on and turn off of PMOSFET switches at a floating potential. The external PMOS can be used as a cutoff switch, enable for an auxiliary power supply, or a bypass switch for a power supply. The RDSon of the pulldown NMOSFET is typically 20 Ω allowing the user to quickly turn on large PMOSFET power channels.
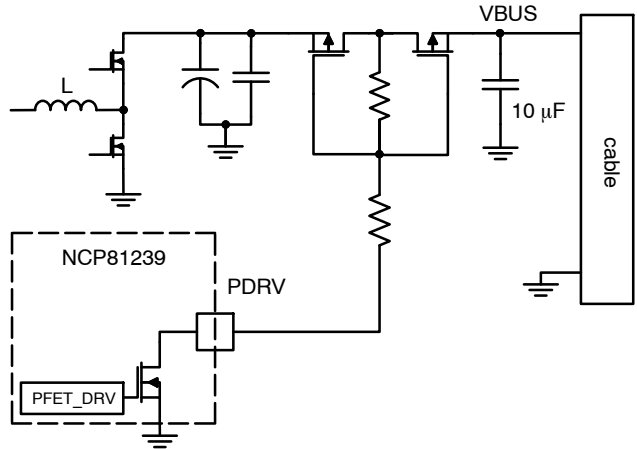


**Figure 11. PFET Drive**

**Table 13. PFET ACTIVATION TABLE**

| PFET_DRV | Description |
|----------|-------------|
| 0 | NFET OFF (Default) |
| 1 | NFET ON |

**Analog to Digital Converter**

The analog to digital converter is a 7−bit A/D which can be used as an event recorder, an input voltage sampler, output voltage sampler, input current sampler, or output current sampler. The converter digitizes real time data during the sample period. The internal precision reference is used to provide the full range voltage; in the case of V1(input voltage), or FB (with 10:1 external resistor divider) the full range is 0 V to 25.5 V. The V1 is internally divided down by 10 before it is digitized by the ADC, thus the range of the measurement is 0 V−2.55 V, same as FB. The resolution of the V1 and FB voltage is 20 mV at the analog mux, but since the voltage is divided by 10 output voltage resolution will be 200 mV. When CS1 and CS2 are sampled, the range is 0 V−2.55 V. The resolution will be 20 mV in the CS monitoring case. The actual current can be calculated by dividing the CS1 or CS2 values with the factor of Rsense × 5mS × RCSx, the total gain from the current input to the external current monitoring outputs.
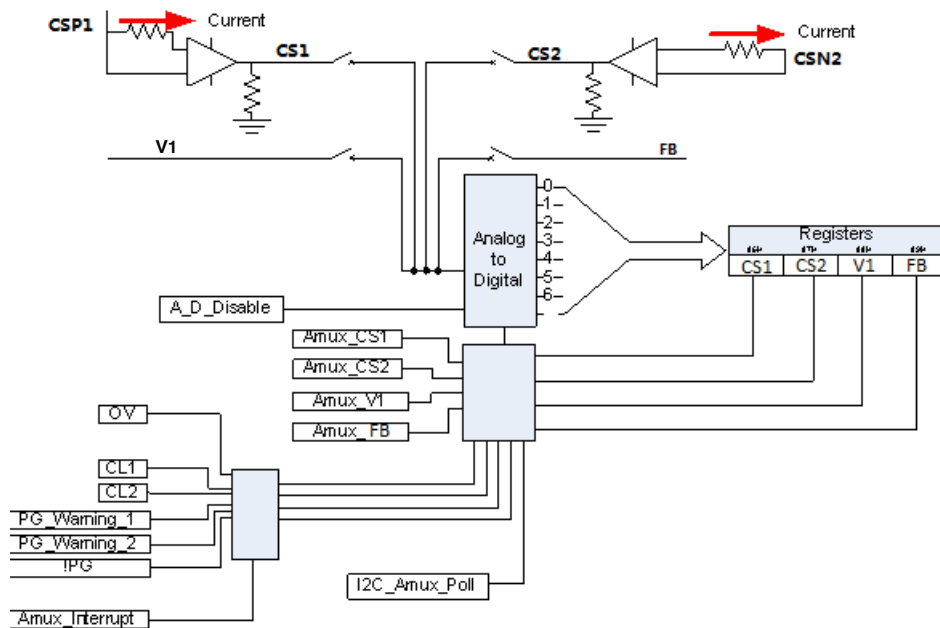


**Figure 12. Analog to Digital Converter**

**Table 14. ADC BYTE**

|  | MSB | 5 | 4 | 3 | 2 | 1 | LSB |
|---|---|---|---|---|---|---|---|
| DATA | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Table 15. REGISTER SETTING FOR ENABLING DESIRED ADC BEHAVIOUR**

| ADC_1 | ADC_0 | Description |
|---|---|---|
| 0 | 0 | Set Amux to VFB |
| 0 | 1 | Sets Amux to V1 |
| 1 | 0 | Set Amux to CS2 |
| 1 | 1 | Set Amux to CS1 |

**Table 16. REGISTER SETTING FOR ADC TRIGGER MANNER**

| ADC Trigger | Description |
|---|---|
| 00 | Trigger a 1xread by a fault condition (Default) |
| 01 | Trigger a 1xread |
| 10 | Trigger a continuous read |

## Interrupt Control

The interrupt controller continuously monitors internal interrupt sources, generating an interrupt signal when a system status change is detected. Individual bits generating interrupts will be set to 1 in the INTACK register (I$^2$C read only registers), indicating the interrupt source. All interrupt sources can be masked by writing 1 in register INTMSK. Masked sources will never generate an interrupt request on the INT pin. The INT pin is an open drain output. A non−masked interrupt request will result in the INT pin being driven high. Figure 13 illustrates the interrupt process.
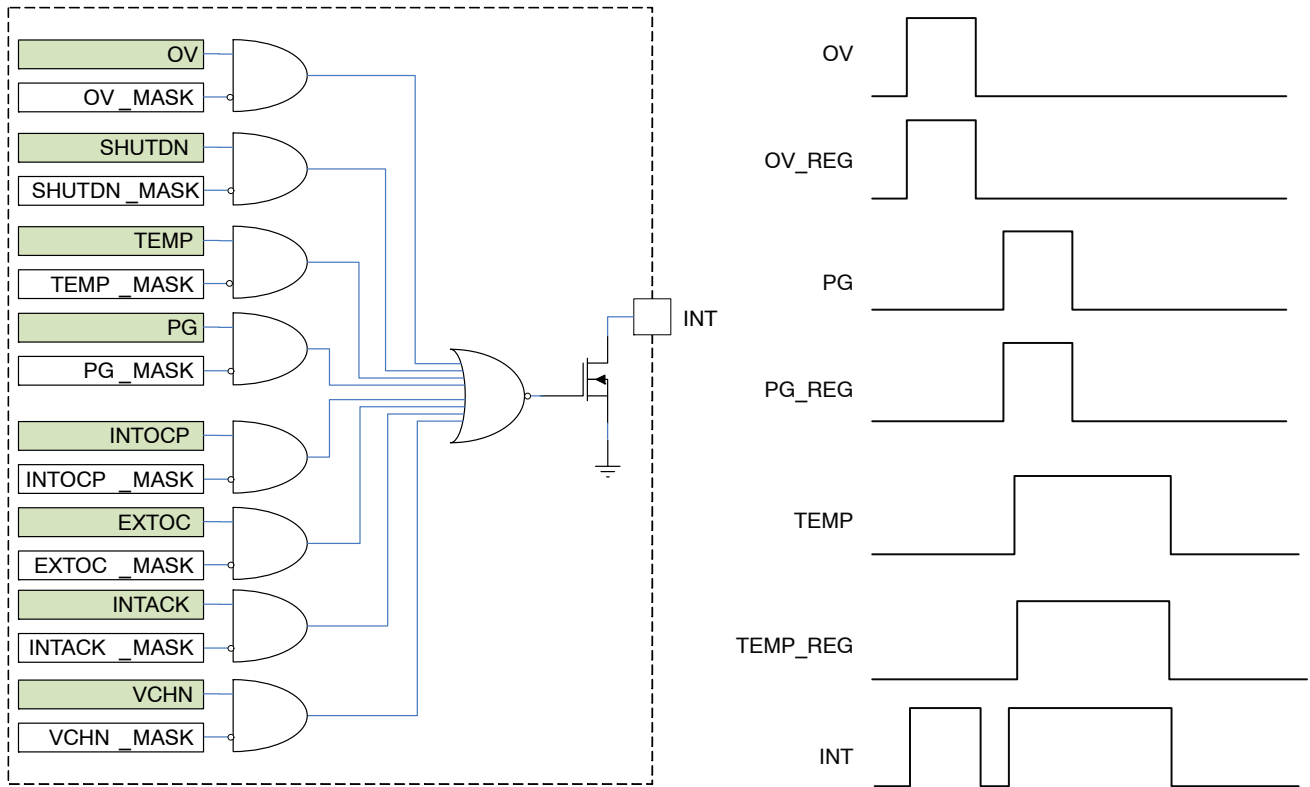


**Figure 13. Interrupt Logic**

### Table 17. INTERPRETATION TABLE

| Interrupt Name | Description |
|---|---|
| OV | Output Over Voltage |
| Shutdown | Shutdown Detection (EN=low) |
| TEMP | IC Thermal Trip |
| PG | Power Good Trip Thresholds Exceeded |
| INTOCP | Internal Current Limit Trip |
| EXTOC | External Current Trip from CLIND |
| VCHN | Output Negative Voltage Change |
| INTACK | I2C ACK signal to the host |

### I$^2$C Address

NCP81239 and NCP81239A are functionally same but have different factory I$^2$C addresses. NCP81239 address is set to 74h, NCP81239A is set to 75h.

### Table 18. I$^2$C ADDRESS

| I$^2$C Address | Hex | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|
| NCP81239 | 0x74 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| NCP81239A | 0x75 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |

## I²C Interface

The I²C interface can support 5 V TTL, LVTTL, 2.5 V and 1.8 V interfaces with two precision SCL and SDA comparators with 1 V thresholds shown in Figure 14. The part cannot support 5 V CMOS levels as there can be some ambiguity in voltage levels.

## I²C Compatible Interface

The NCP81239 can support a subset of I²C protocol as detailed below. The NCP81239 communicates with the external processor by means of a serial link using a 400 kHz up to 1.2 MHz I²C two−wire interface protocol. The I²C interface provided is fully compatible with the Standard, Fast, and High−Speed I²C modes. The NCP81239 is not intended to operate as a master controller; it is under the control of the main controller (master device), which controls the clock (pin SCL) and the read or write operations through SDA. The I²C bus is an addressable interface (7−bit addressing only) featuring two Read/Write addresses.
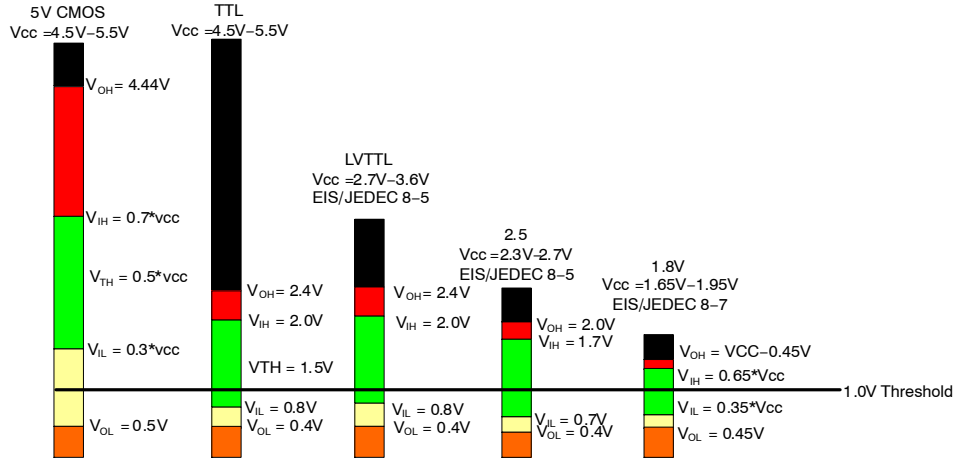


**Figure 14. I²C Thresholds and Comparator Thresholds**

## I2C Communication Description

The first byte transmitted is the chip address (with the LSB bit set to 1 for a Read operation, or set to 0 for a Write operation). Following the 1 or 0, the data will be:

- In case of a Write operation, the register address (@REG) pointing to the register for which it will be written is followed by the data that will written in that location. The writing process is auto−incremental, so the first data will be written in @REG, the contents of @REG are incremented, and the next data byte is placed in the location pointed to @REG + 1..., etc.

- In case of a Read operation, the NCP81239 will output the data from the last register that has been accessed by the last write operation. Like the writing process, the reading process is auto−incremental.
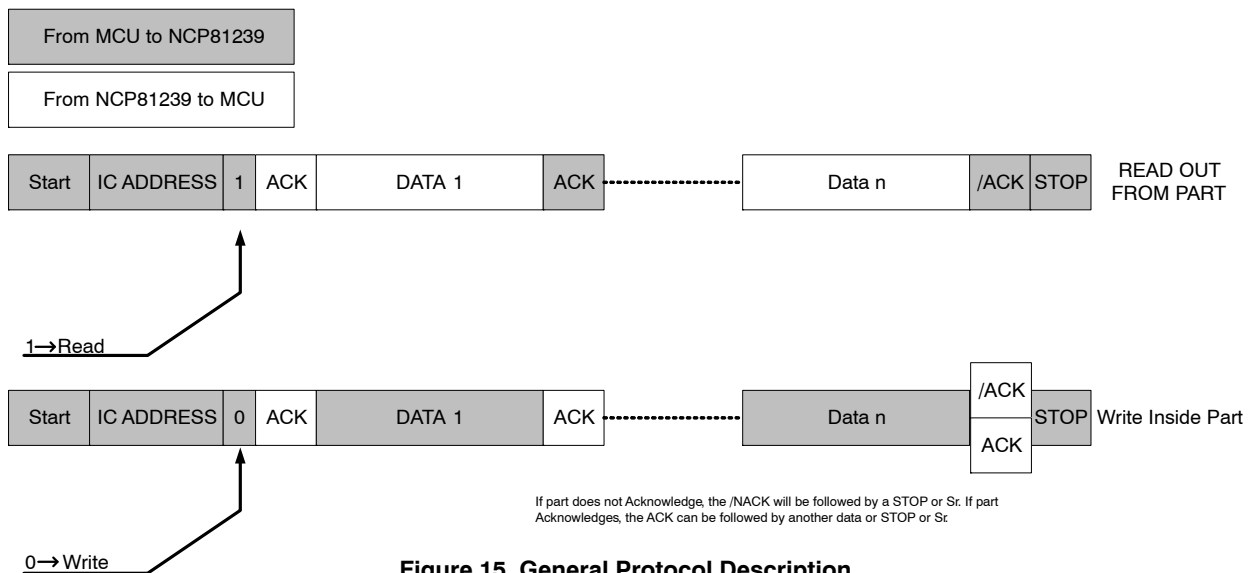


**Figure 15. General Protocol Description**

**Read Out from Part**

The master will first make a "Pseudo Write" transaction with no data to set the internal address register. Then, a stop then start or a repeated start will initiate the Read transaction from the register address the initial Write transaction was pointed to:
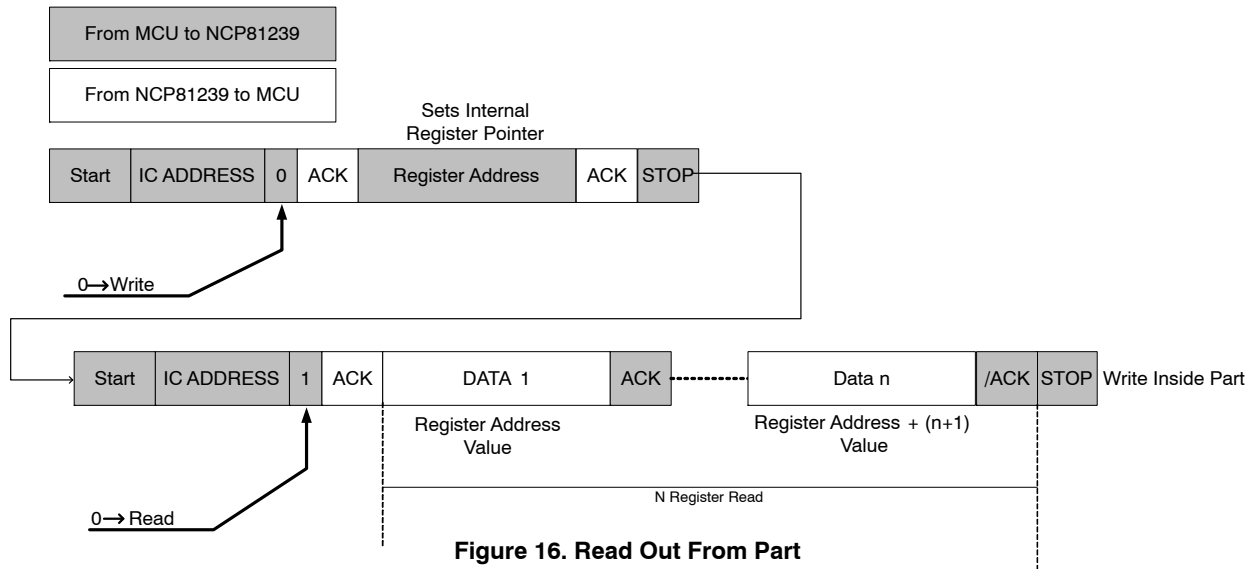


**Figure 16. Read Out From Part**
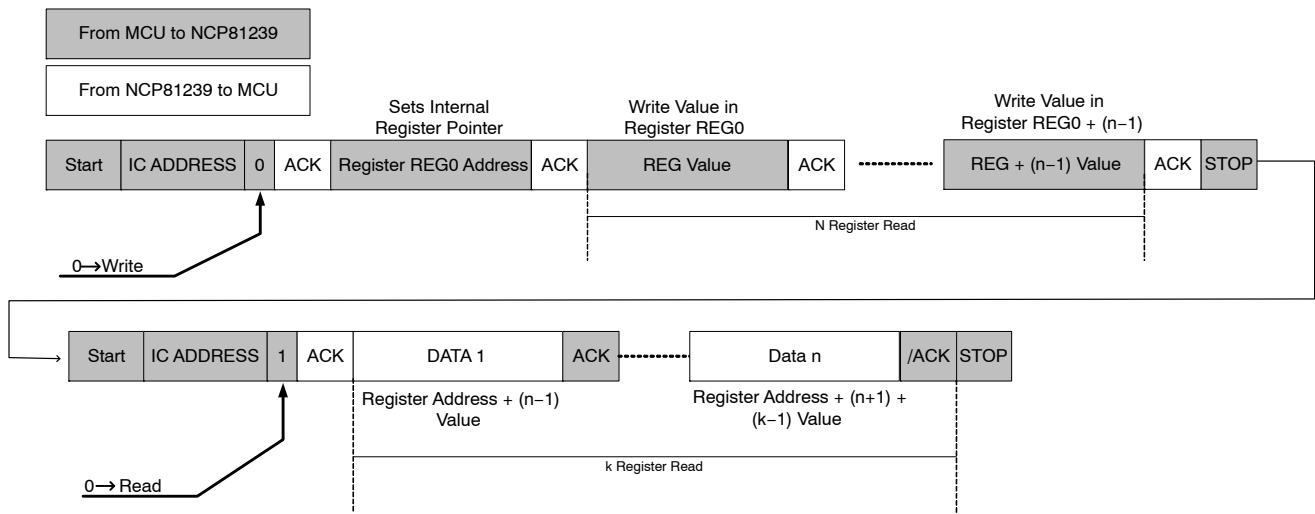


**Figure 17. Write Followed by Read Transaction**

**Write In Part**

Write operation will be achieved by only one transaction. After the chip address, the MCU first data will be the internal register desired to access, the following data will be the data written in Reg, Reg + 1, Reg + 2, ..., Reg +n.
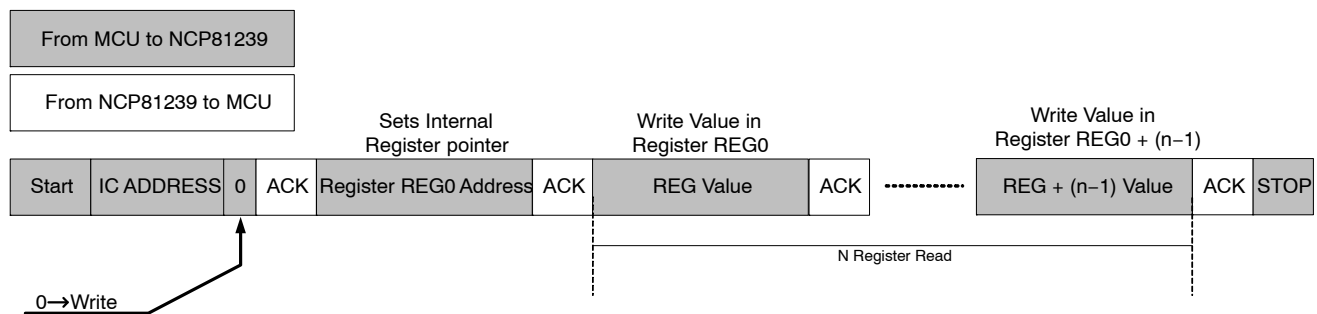


**Figure 18. Write in n Registers**

## PACKAGE OUTLINE

**QFN32 5x5, 0.5P**
CASE 485CE
ISSUE O
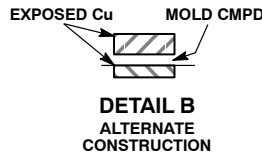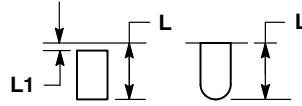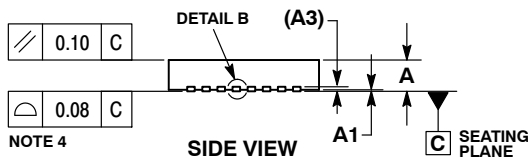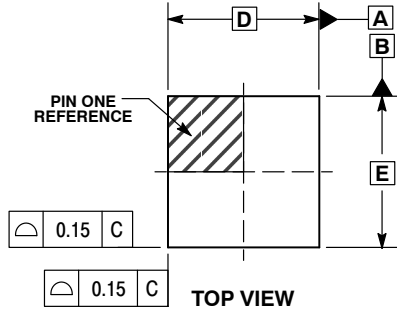
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

**PIN ONE REFERENCE**

0.15 C

0.15 C

**TOP VIEW**

0.10 C

**DETAIL B**

(A3)

0.08 C

NOTE 4

**SIDE VIEW**

A1

**SEATING PLANE**

**DETAIL A**
**ALTERNATE CONSTRUCTIONS**

L1   L   L

**DETAIL A**

**EXPOSED Cu**   **MOLD CMPD**

**DETAIL B**
**ALTERNATE CONSTRUCTION**

| DIM | MILLIMETERS | |
|-----|-----|-----|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 5.00 BSC | |
| D2 | 3.40 | 3.60 |
| E | 5.00 BSC | |
| E2 | 3.40 | 3.60 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

**DETAIL A**

D2   K

E2

8   17

1   24

32   25

32X L

32X b

e

e/2

| 0.10 Ⓜ C A-B B |
|---|
| 0.05 Ⓜ C NOTE 3 |

**BOTTOM VIEW**
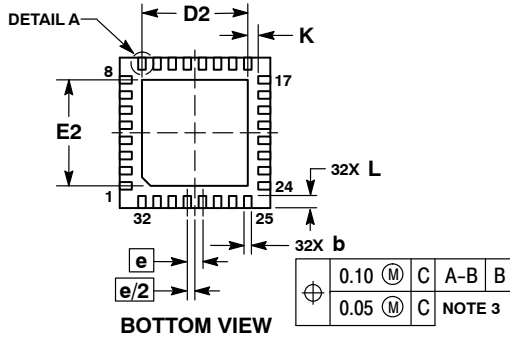
**RECOMMENDED SOLDERING FOOTPRINT***

5.30

3.70

32X
0.62

3.70

5.30

0.50
PITCH

32X
0.30

DIMENSIONS: MILLIMETERS
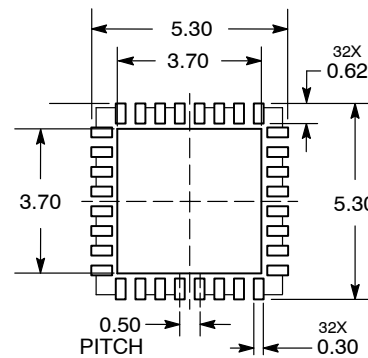
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

◊

**NCP81239/D**