NCP5339

Integrated Driver & MOSFETs

The NCP5339 integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a 6 mm x 6 mm 40−pin QFN package. The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP5339 integrated solution greatly reduce package parasitics and board space compared to a discrete component solution.

Features

- 3−State 5 V PWM Logic
- Capable of Switching Frequencies up to 1 MHz
- Zero Current Detection for Improving Light Load Efficiency
- Internal Bootstrap Schottky Diode
- Undervoltage Lockout of VCIN
- Disable Pin Disables Both Driver Outputs
- Internal Thermal Warning / Thermal Shutdown Functionality
- These are Pb−free Devices

Typical Applications

- Servers and Desktops
- Graphics Cards
- Telecom

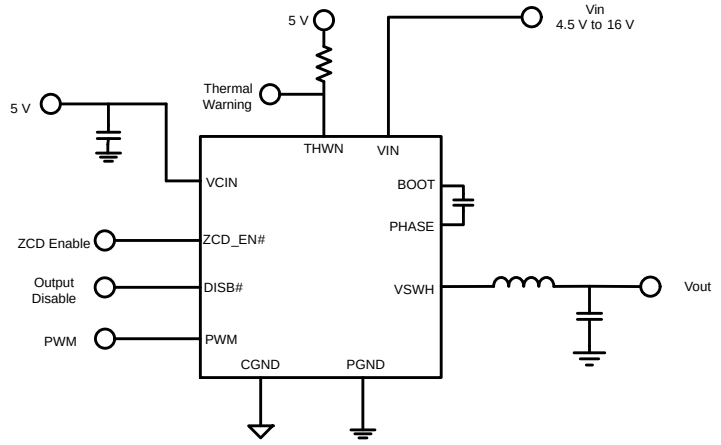

Figure 1. Application Schematic

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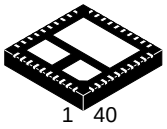
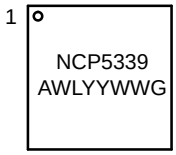


QFN40 6x6, 0.5P
CASE 485CM

MARKING DIAGRAM



NCP5339	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5339MNTXG	QFN−40 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

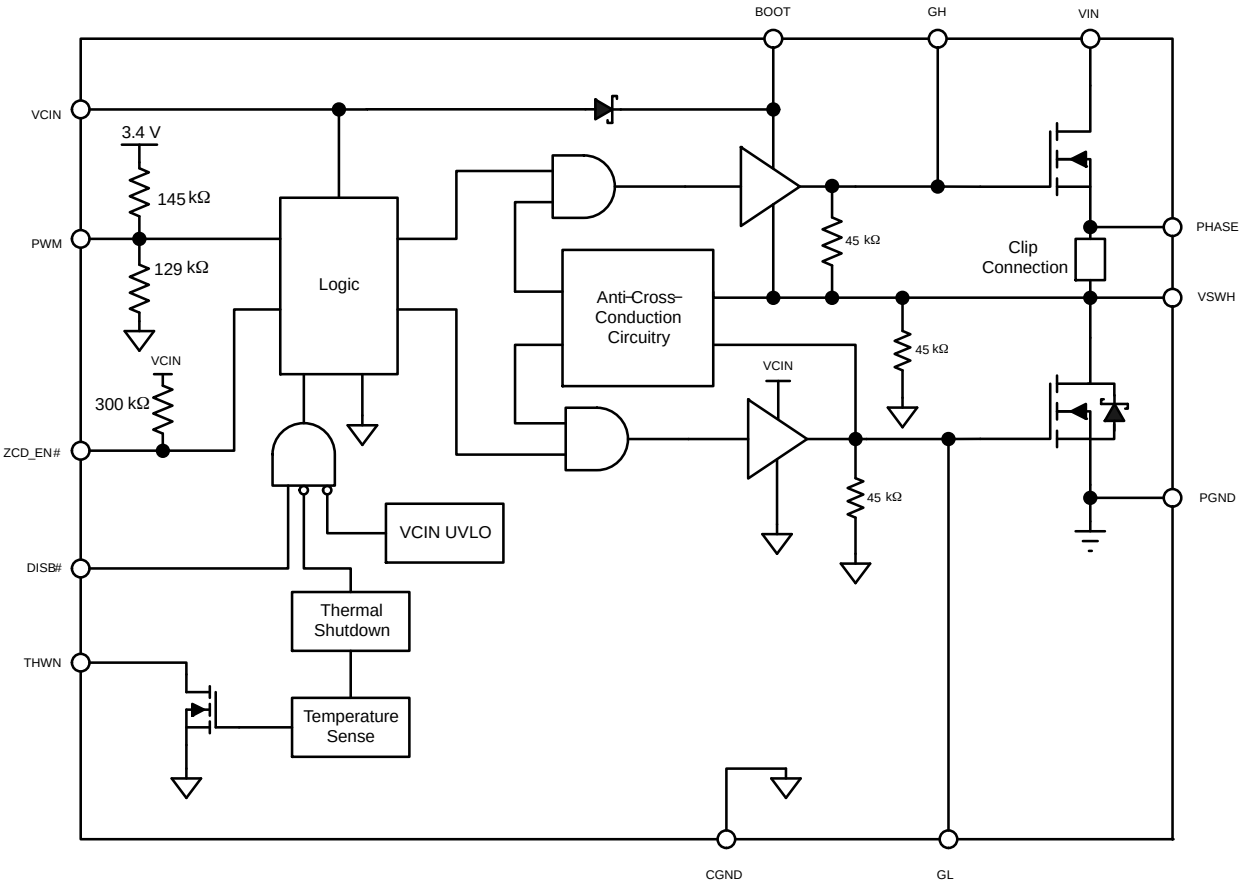
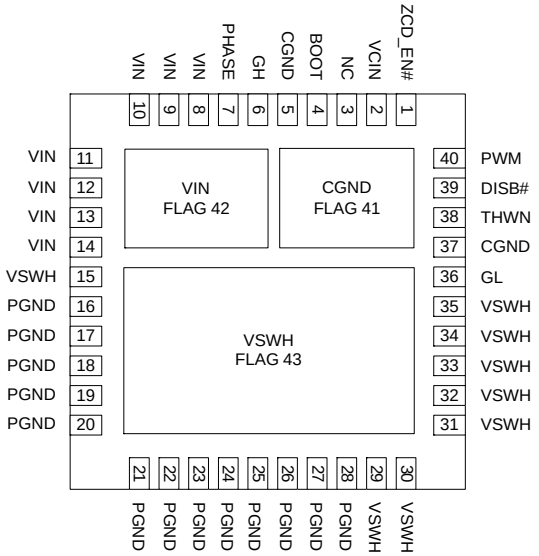


Figure 2. Simplified Block Diagram



(Top View)

Figure 3. Pin Connections

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	ZCD_EN#	Enable Zero Current Detection. When the voltage on this pin is low, the NCP5339 will enter zero current detection mode. Otherwise, the NCP5339 will be in PWM mode. There is a 300 kΩ pull−up resistor to VCIN.
2	VCIN	Control Input Voltage. Provides power to the driver IC logic and power to the GL driver.
3	NC	No Connect. There is no connection to any IC die.
4	BOOT	Bootstrap Voltage. This provides power to the GH driver. Place a high frequency ceramic capacitor of 0.1 μF to 1.0 μF from this pin to PHASE.
5, 37, FLAG 41	CGND	Control Signal Ground
6	GH	High−Side FET Gate Access
7	PHASE	Connection to the source of the high−side MOSFET. Place a high frequency ceramic capacitor of 0.1 μF to 1.0 μF from this pin to BOOT pin.
8−14, FLAG 42	VIN	Input Voltage
15, 29−35, FLAG 43	VSWH	Switch Node Output
16−28	PGND	Power Ground
36	GL	Low−Side FET Gate Access
38	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver die reaches T_{THWN}, this pin is pulled low. Driver operation is not disabled until the driver die temperature reaches T_{THDN}. Driver operation is resumed once the driver die temperature falls below the T_{THDN} hysteresis level.
39	DISB#	Output Disable Pin. When the voltage on this pin is low, GH and GL is pulled low.
40	PWM	PWM Drive Logic. This is a 3−state input: PWM = High → GH is high, GL is low. PWM = Mid → GH is low, GL goes low after $t_{holdoff}$. PWM = Low → GH is low, GL is high (ZCD_EN# = High). GH is low, GL is high for t_{blank} and then goes low when zero current is detected (ZCD_EN# = Low). There are internal PWM resistors that bias this pin to 2.2 V (mid−state) if the pin is left floating.

Table 2. ABSOLUTE MAXIMUM RATINGS (All Signals Referenced to CGND unless noted otherwise)

Pin Symbol	Pin Name	Min	Max	Unit
VCIN	Control Input Voltage	−0.3	6.5	V
VIN	Power Input Voltage (Note 1)	−0.3	25 to PGND	V
BOOT	Bootstrap Voltage	−0.3 to VSWH	35 40 (< 50 ns) 6.5 to VSWH	V
VSWH	Switch Node Output (Note 1)	−0.3 to PGND −5 to PGND (< 10 ns)	25 to PGND 30 to PGND (< 10 ns)	V
GH	High−Side FET Gate Access	−0.3 to VSWH	6.5 to VSWH	V
GL	Low−Side FET Gate Access	−0.3	6.5	V
ZCD_EN#	Zero Current Detection	−0.3	6.5	V
PWM	PWM Drive Logic	−0.3	6.5	V
DISB#	Output Disable	−0.3	6.5	V
THWN	Thermal Warning	−0.3	6.5	V
Continuous Output Current	Output Current, Fsw = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1.2 V (Note 2)	−	50	A
Peak Output Current (Note 3)	Output Current, Fsw = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1.2 V (Note 2)	−	80	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. During switching of the MOSFETs, high transient voltages can appear on these pins. It is important to keep these transients within the Maximum Ratings range.
2. Output current ratings are based on using a 3.0″ x 3.0″ PCB, 8 layers, board design, T_A = 25°C, natural convection.
3. Peak output current is applied for 10 ms.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 3. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient (Note 4)	θ_{JA}	24.6	°C/W
Thermal Characterization Parameter, Junction−to−Board (Note 4)	ψ_{JB}	0.3	°C/W
Thermal Characterization Parameter, Junction−to−Top (Note 4)	ψ_{JC}	0.5	°C/W
Operating Junction Temperature Range	T_J	−40 to 150	°C
Storage Temperature Range	T_S	−55 to 150	°C
Moisture Sensitivity Level	MSL	3	

4. JESD51−7 board (2s2p, 1 oz. Cu thickness), 0 LFM.

Table 4. OPERATING RANGES

Rating	Symbol	Min	Typ	Max	Unit
Control Input Voltage	VCIN	4.5	5	5.5	V
Input Voltage	VIN	4.5	12	16	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS
(VCIN = 5 V, VIN = 12 V, T_A = −40°C to +125°C, unless otherwise noted.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CURRENT						
VCIN Current (normal mode)	–	DISB# = 5 V, PWM = switching (0 V to 5 V), FSW = 400 kHz	–	18	30	mA
VCIN Current (shutdown mode)	–	DISB# = GND, ZCD_EN# = VCIN	–	1	–	μA
UNDERVOLTAGE LOCKOUT (VCIN)						
UVLO Rising	V_{UVLO}	VCIN rising	3.8	4.35	4.5	V
UVLO Hysteresis	HYS_{UVLO}	UVLO rising threshold – UVLO falling threshold	150	200	250	mV
BOOTSTRAP DIODE						
Forward Voltage	–	Forward bias current = 2 mA	0.1	0.3	0.6	V
PWM INPUT						
PWM Input Voltage High	V_{PWM_HI}		3.7	–	–	V
PWM Input Voltage Mid−State	V_{PWM_MID}		1.3	–	3.0	V
PWM Input Voltage Low	V_{PWM_LO}		–	–	0.7	V
Tri−State Shutdown Holdoff Time	$t_{holdoff}$			300		ns
PWM Input Resistance	–			68		kΩ
PWM Input Bias Voltage	–			2.2		V
OUTPUT DISABLE						
Output Disable Input Voltage High	$V_{DISB\#\_HI}$		2.0	–	–	V
Output Disable Input Voltage Low	$V_{DISB\#\_LO}$		–	–	0.8	V
Output Disable Hysteresis	$HYS_{DISB\#}$	$V_{DISB\#\_HI} - V_{DISB\#\_LO}$	–	300	–	mV
Enable Delay Time (Note 5)	–	DISB# rising, PWM = 0 V, GL rising to 10%	–	25	–	μs
Output Disable Propagation Delay	–	DISB# falling, PWM = 0 V, GL falling to 90%	–	20	40	ns
ZERO CROSS DETECT						
Zero Cross Detect High	$V_{ZCD\_EN\#\_HI}$		2.0	–	–	V
Zero Cross Detect Low	$V_{ZCD\_EN\#\_LO}$		–	–	0.8	V
Zero Cross Detect Threshold	–	ZCD_EN# = 0 V	–	−3	–	mV
ZCD Blanking + Debounce Timer	t_{blank}		–	350	–	ns
THERMAL WARNING/SHUTDOWN						
Thermal Warning Temperature (Note 5)	T_{THWN}	Temperature at driver IC	–	150	–	°C
Thermal Warning Hysteresis (Note 5)	HYS_{THWN}		–	15	–	°C
Thermal Shutdown Temperature (Note 5)	T_{THSD}	Temperature at driver IC	–	180	–	°C
Thermal Shutdown Hysteresis (Note 5)	HYS_{THSD}		–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Guaranteed by design and/or characterization. This parameter is not tested in production.

TYPICAL CHARACTERISTICS

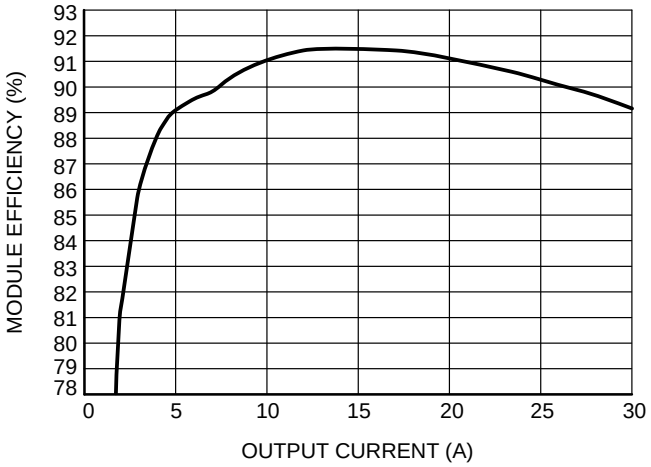


Figure 4. Module Efficiency vs. Current (Vin = 12 V, Vout = 1.2 V, Natural Air Convection, Inductor = 0.15 μH, Output measured at VSW)

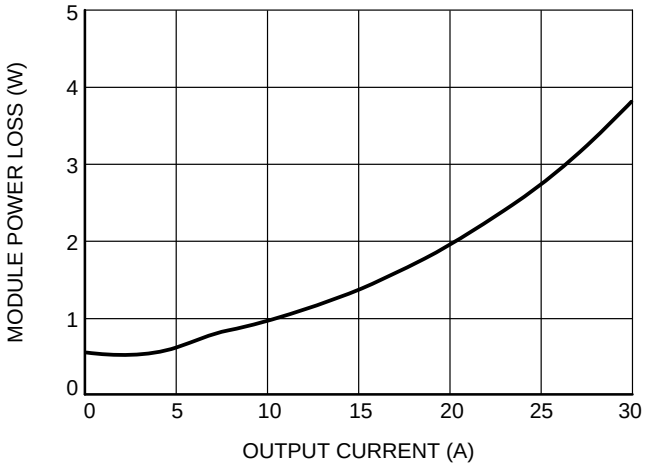


Figure 5. Module Power Loss vs. Current (Vin = 12 V, Vout = 1.2 V, Natural Air Convection)

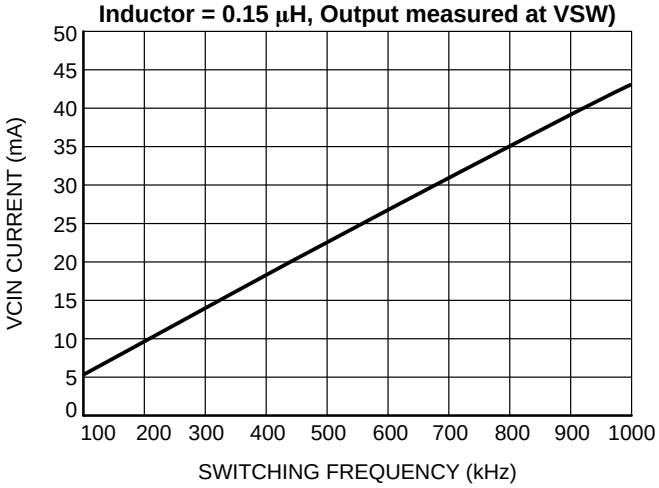


Figure 6. Driver Supply Current vs. Frequency (VCIN = 5 V, Ta = 25°C)

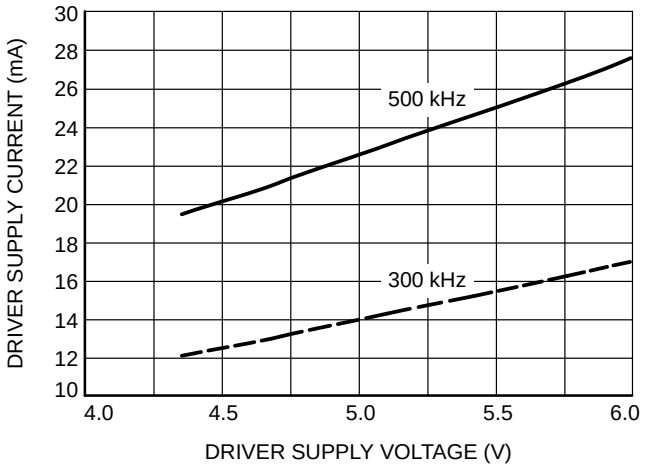


Figure 7. Driver Supply Current vs. Driver Supply Voltage (Ta = 25°C)

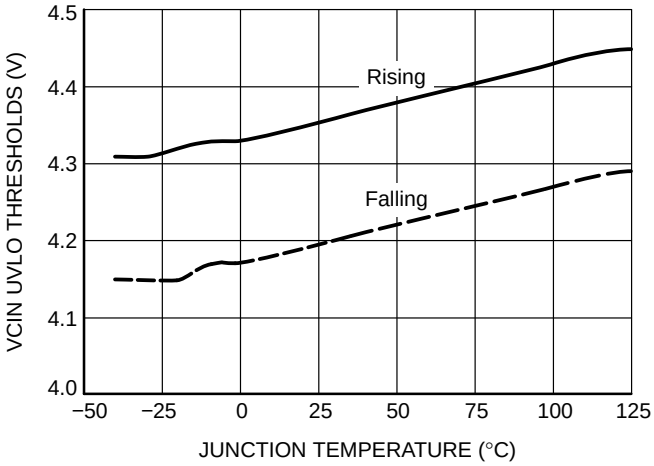


Figure 8. VCIN UVLO vs. Temperature (VCIN = 5 V, Ta = 25°C)

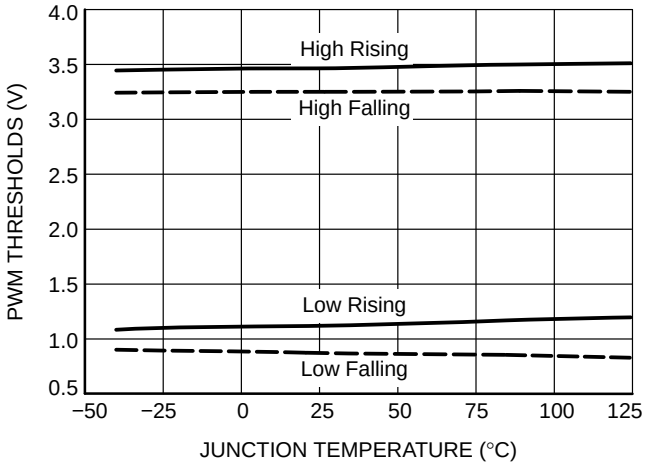


Figure 9. PWM Thresholds vs. Temperature (VCIN = 5 V, Ta = 25°C)

TYPICAL CHARACTERISTICS

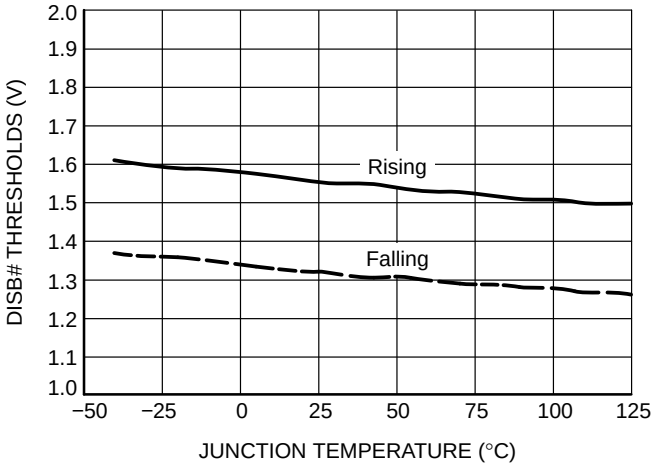


Figure 10. DISB# Threshold vs. Temperature (VCIN = 5 V, Ta = 25°C)

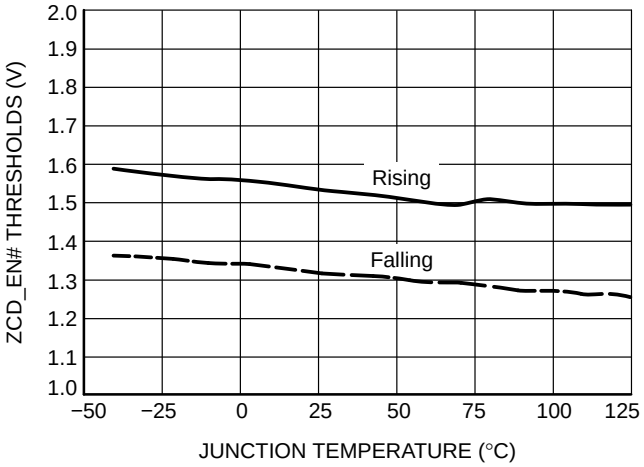


Figure 11. ZCD_EN# Threshold vs. Temperature (VCIN = 5 V, Ta = 25°C)

APPLICATIONS INFORMATION

Theory of Operation

The NCP5339 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. It consists of a MOSFET driver die and two MOSFET dies, one acting as the control MOSFET (high−side FET) and the other acting as the synchronous MOSFET (low−side FET). A single PWM input signal is all that is required to properly drive the high−side and low−side MOSFETs.

VCIN Undervoltage Lockout (UVLO)

The VCIN pin is monitored by an Undervoltage Lockout circuit. While VCIN is below UVLO Rising threshold (4.35 V, typical), the outputs of the MOSFET driver, GH and GL, are floating. The internal pull−down resistors connected to GH and GL keep the MOSFETs in the off−state. When VCIN is greater than UVLO Rising threshold, the driver can be enabled by pulling DISB# high. There is a hysteresis of 200 mV (typical) on VCIN UVLO.

Enabling/Disabling the Driver (DISB#)

The DISB# pin is used to disable the GH and GL outputs of the MOSFET driver. When DISB# is low, the driver is disabled, pulling both gates of the MOSFETs low. This prevents power transfer from VIN to the output. The driver is enabled by pulling DISB# into a logic−high state (as long as VCIN is greater than UVLO Rising threshold). When the driver is enabled, the states of GH and GL are determined by the signal on the PWM pin. See Table 6 for the UVLO/DISB# logic table.

Every time DISB# changes from a low−state to a high−state, the driver undergoes an auto−calibration cycle for the zero current detect threshold. This auto−calibration cycle typically takes 25 μs to complete. The driver outputs will not respond to the PWM input signal until the auto−calibration cycle is completed.

Table 6. UVLO/DISB# Logic Table

UVLO	DISB#	GH, GL Outputs
L	X	GH = Low, GL = Low
H	L	GH = Low, GL = Low
H	H	Normal PWM Operation (See X)
H	Open	GH = Low, GL = Low

Low−Side Driver

The low−side driver is designed to drive a ground−referenced low−$R_{DS(on)}$ N−Channel MOSFET, the synchronous MOSFET in a buck converter. The voltage supply for the low−side driver is internally connected to the VCIN and CGND pins. The driver turns on the low−side MOSFET with the charge stored in the VCIN capacitor. So, it is important to place the VCIN capacitor close to the VCIN and CGND pins to minimize the parasitics in this loop. A multi−layer ceramic capacitor greater than 1 μF should be used.

High−Side Driver

The high−side driver is designed to drive a floating low−$R_{DS(on)}$ N−channel MOSFET, the control MOSFET in a buck converter. The gate voltage for the high−side driver is developed by a bootstrap circuit referenced to the VSWH pin (switch node).

The bootstrap circuit is comprised of the internal Schottky diode and an external capacitor. When the NCP5339 is starting up, the VSWH pin is held at ground, allowing the bootstrap capacitor to charge up to VCIN through the bootstrap diode (See Figure 1). When the PWM input is driven high, the high−side driver will turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the VSWH pin rises. When the high−side MOSFET is fully turned on, the switch node will settle to VIN and the BST pin will settle to VIN + VCIN (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge−storage capacitor (C_{BST}) and an integrated diode to provide current to the high−side driver. A multi−layer ceramic capacitor with a value greater than 100 nF should be used as the bootstrap capacitor.

Overlap Protection Circuit

It is important to avoid cross−conduction of the two MOSFETs, which could result in a decrease in the power conversion efficiency or damage to the device.

The NCP5339 prevents cross−conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non−overlap time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). See Figure 12.

When the PWM input is driven high, the gate of the low−side MOSFET (GL) goes low after a propagation delay, $tpdl_{GL}$. The time it takes for the low−side MOSFET to turn off is dependent on the total charge on the low−side MOSFET gate. The NCP5339 monitors the pre−driver voltage of both MOSFETs and VSWH to determine the conduction status of the MOSFETs. Once the low−side MOSFET is turned off, an internal timer will delay the turn−on of the high−side MOSFET, $tpdh_{GH}$.

Likewise, when the PWM input pin goes low, the gate of the high−side MOSFET (GH) goes low after a propagation delay, $tpdl_{GH}$. The time to turn off the high−side MOSFET is dependent on the total gate charge of the high−side MOSFET. A timer is triggered once the high−side MOSFET stops conducting, to delay the turn−on of the low−side MOSFET, $tpdh_{GL}$.

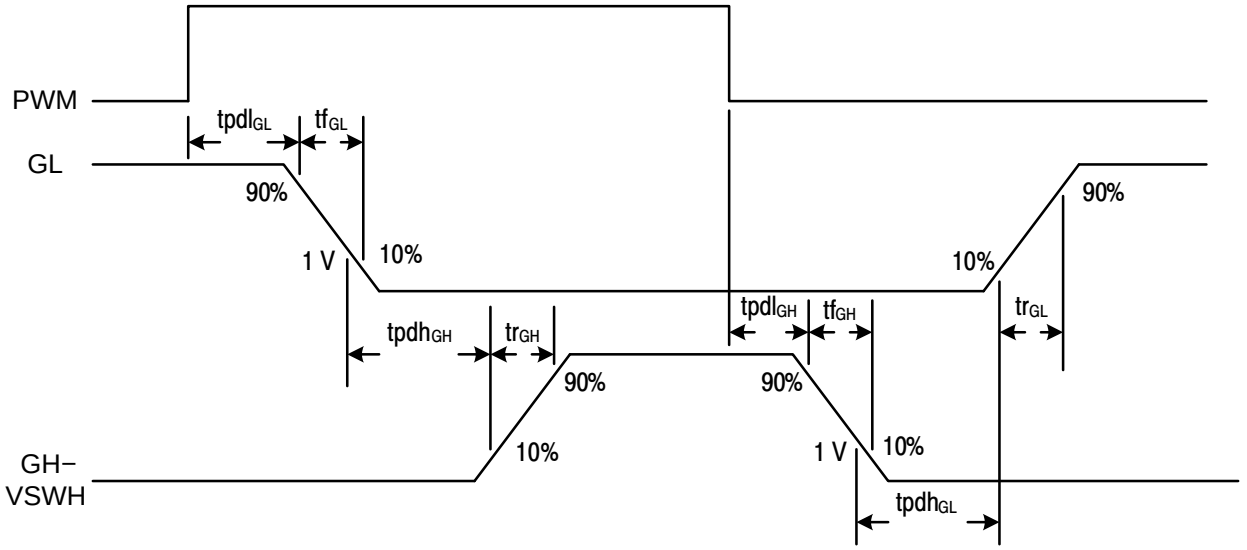


Figure 12. MOSFET Gate Timing Diagram

PWM Mid−State

The NCP5339 can be placed into a high−impedance state, where both high−side and low−side MOSFETs are in the off−state. This state is commonly used in multi−phase applications that allow phase shedding. A phase can be turned off by placing the NCP5339 from that phase into PWM mid−state. The phase can quickly be turned back on by having PWM exit mid−state. When the voltage on PWM is within the V_{PWM_MID} voltage range, both GH and GL are pulled low after a hold−off time (See Figure 13).

- When transitioning from a PWM low state to mid−state, GL goes from high to low after $t_{holdoff}$. GH is already low due to the prior PWM low state.
- When transitioning from a PWM high state to mid−state, GH goes from high to low without delay. After GH is pulled low, GL goes high for $t_{holdoff}$.

There are internal resistors at the PWM input that biases the voltage on PWM to be at mid−state when the voltage at the pin is otherwise floating.

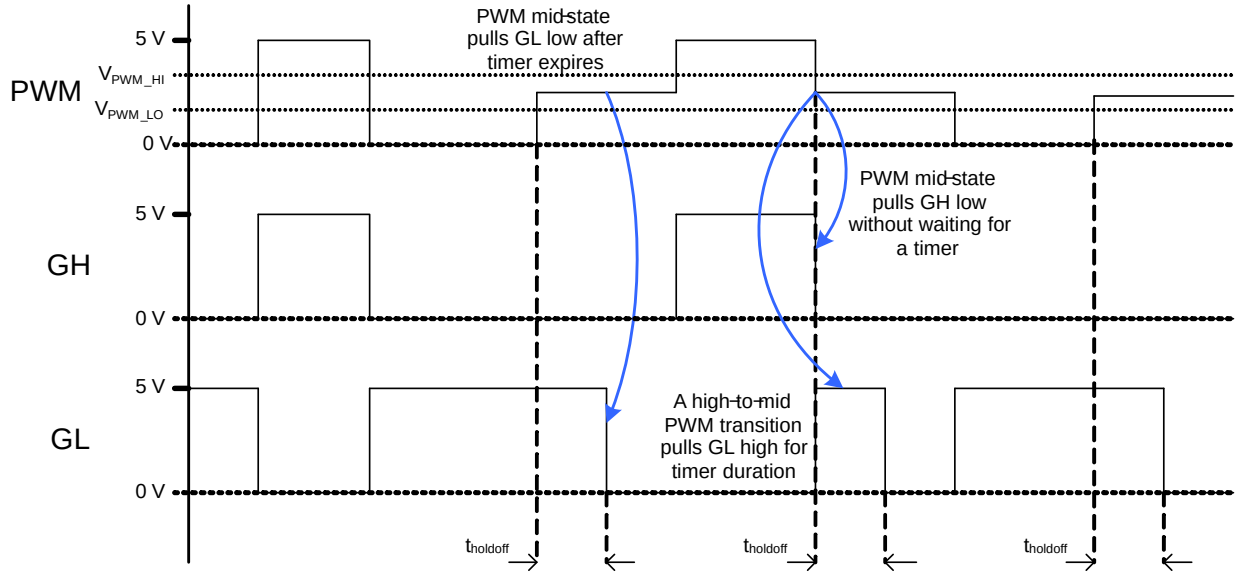


Figure 13. PWM Tri−State Behavior

Zero Current Detect

When operating under light load conditions, the current ripple through the inductor can cause a buck converter to partially operate with negative current. This can have a noticeable impact on converter efficiency as the negative current discharges the output capacitors. The zero current detect feature in the NCP5339 automatically turns off the low−side MOSFET before the inductor current goes negative. This causes the converter to operate under discontinuous conduction mode and improves the efficiency during light load conditions.

The ZCD_EN# pin is a logic input pin with an active 300 kΩ pull−up resistance to VCIN.

When ZCD_EN# is set high, the NCP5339 will operate in normal PWM mode.

When ZCD_EN# is set low, zero cross detect (ZCD) is enabled, see Figure 14. The high−side driver responds to PWM in the same manner as in normal PWM mode. When PWM is high, GH goes high after the non−overlap delay. When PWM is low, GL goes high after the non−overlap delay, and stays high for the duration of the ZCD blanking timer. Once this timer expires, VSWH is monitored for zero cross detection, pulling GL low after VSWH is detected to be at or above the ZCD threshold voltage.

The ZCD threshold undergoes an auto−calibration cycle every time DISB# is brought from low to high. This auto−calibration cycle typically takes 25 µs to complete. During the auto−calibration cycle, GH and GL are pulled low and do not respond to PWM signals.

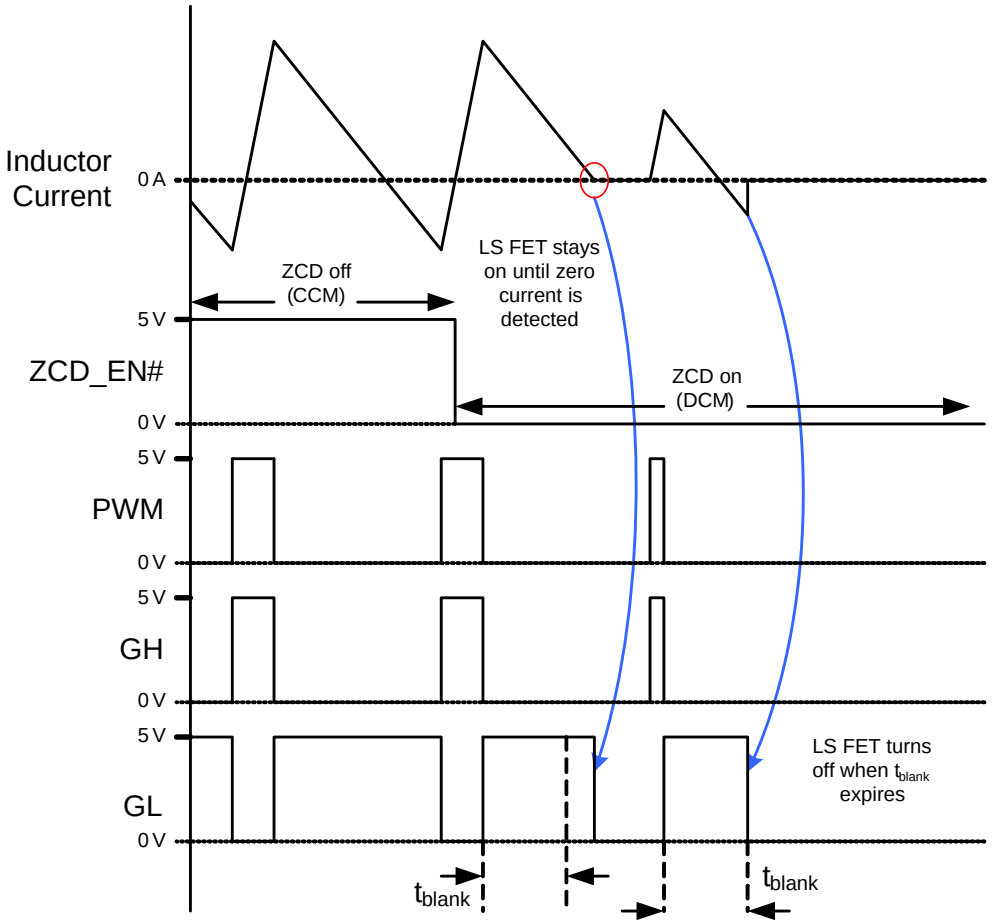


Figure 14. Zero Current Detect Behavior

Prebias Startup

There are conditions that could allow a converter to start up when there is a pre−existing voltage at the output. Turning off a converter and then quickly turning it back on is an example of this. There are controllers that, when a prebias startup is recognized, will want to start the power stage without discharging the output capacitors. To allow for a prebias startup, the GL control of the NCP5339 has the following behavior when it is first enabled:

1. If on startup, ZCD_EN# is low and PWM is low or mid, GL is low. Need a PWM transition (mid−to−high−to−low, low−to−high−to−low or mid−to−low) to get GL to go high.
2. If on startup, ZCD_EN# is high and PWM is mid, GL is low. Need a PWM transition to low to get GL to go high.
3. If on startup, ZCD_EN# is high and PWM is low, GL is high. No prebias condition.

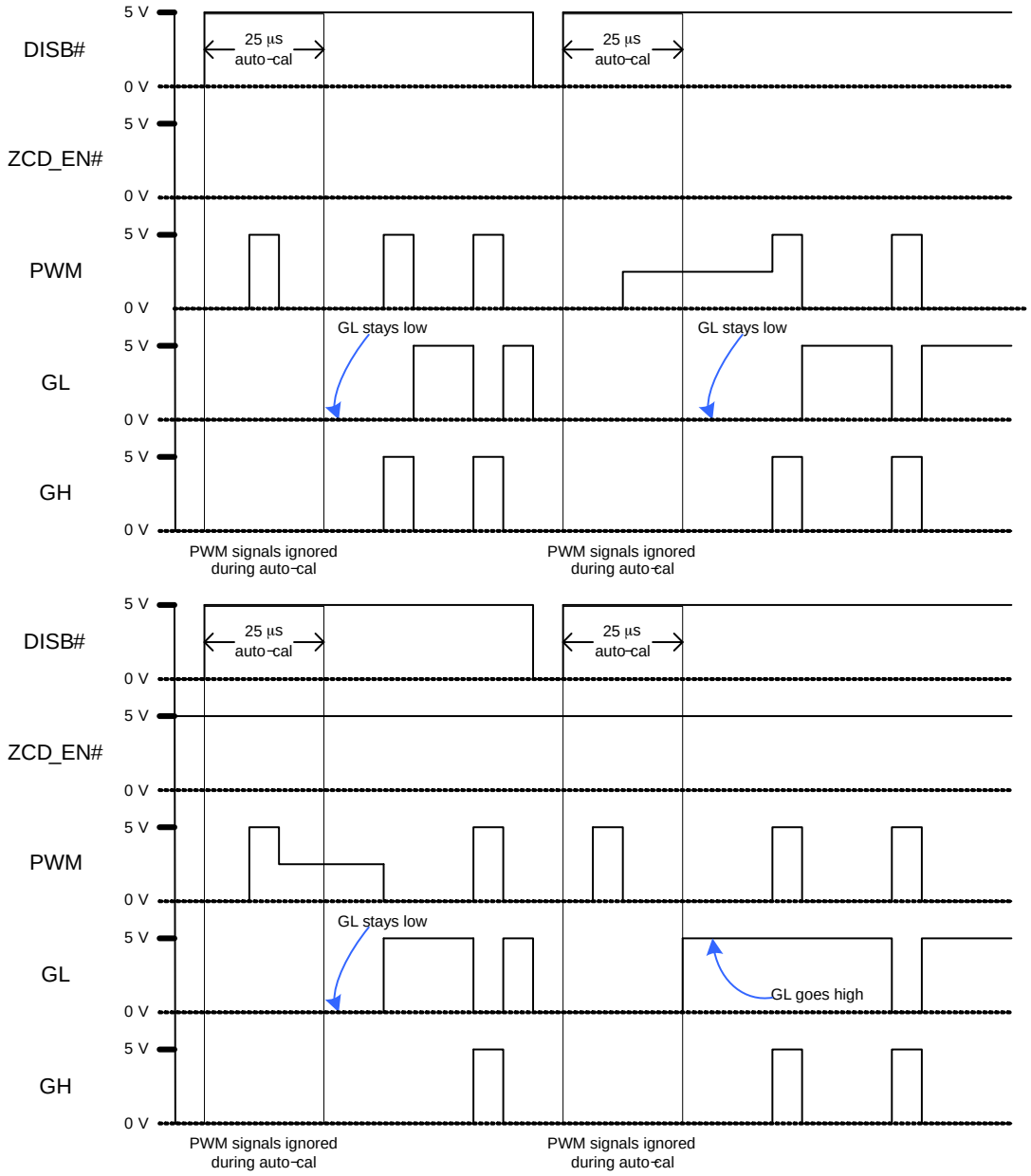


Figure 15. Prebias Startup
(Top figure: ZCD_EN# = High, Bottom figure: ZCD_EN# = Low)

Thermal Warning / Thermal Shutdown

The THWN pin is an open−drain output. The temperature sensor is on the die of the MOSFET driver. When the temperature of the driver reaches 150°C, the THWN pin is pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops below 135°C, the THWN pin is released. If the driver temperature exceeds 180°C, the part enters thermal shutdown and turns off both MOSFETs. Once the temperature falls below 155°C, the part resumes normal operation. The THWN pin has a maximum current capability of 30 mA.

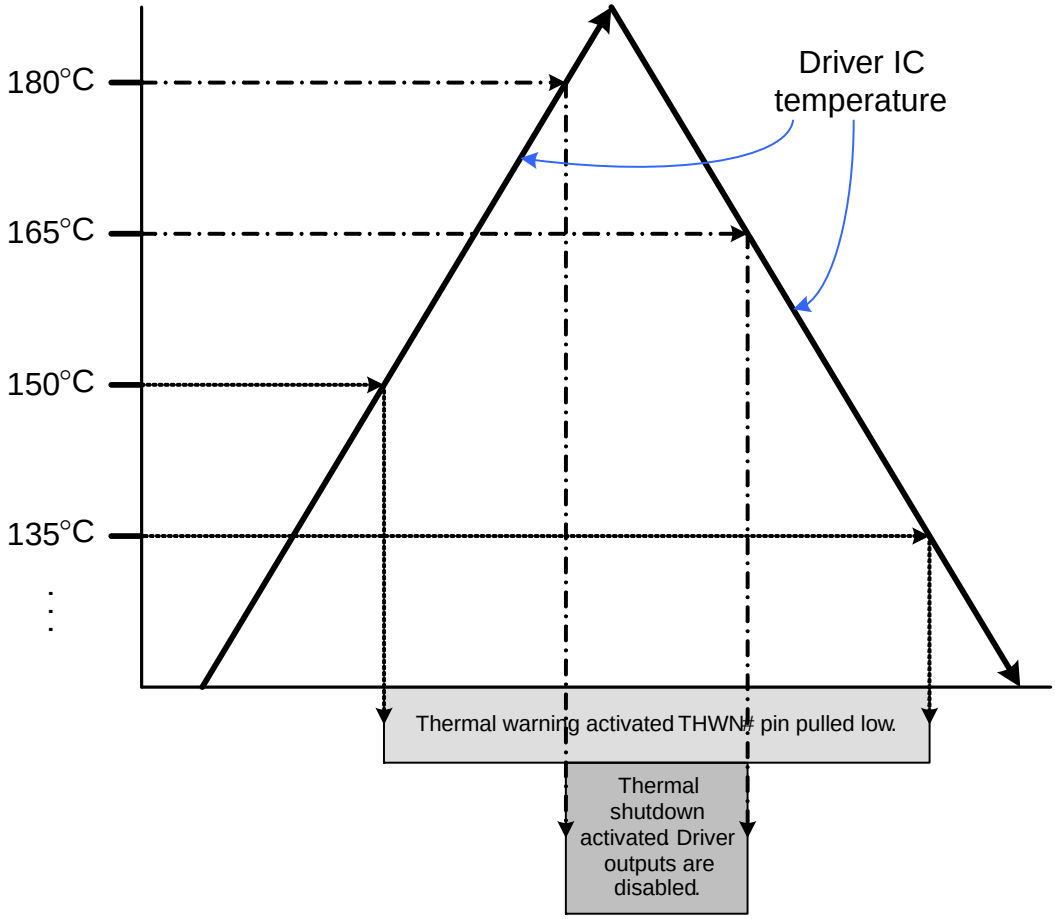
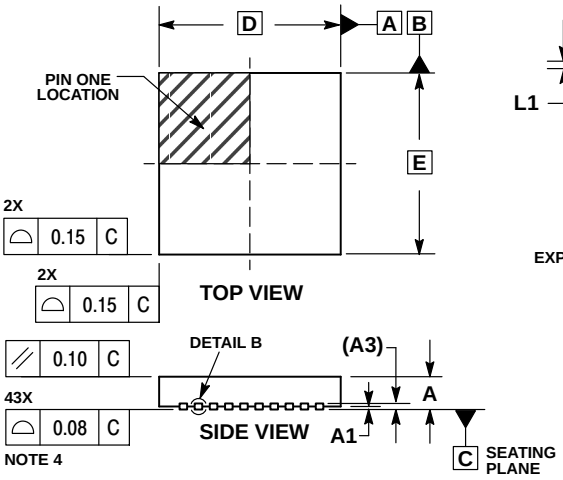
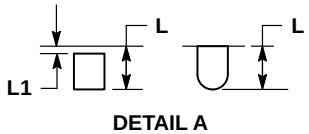


Figure 16. Thermal Warning/Thermal Shutdown Behavior

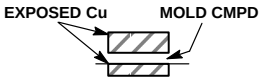
PACKAGE DIMENSIONS

QFN40 6x6, 0.5P
CASE 485CM
ISSUE O





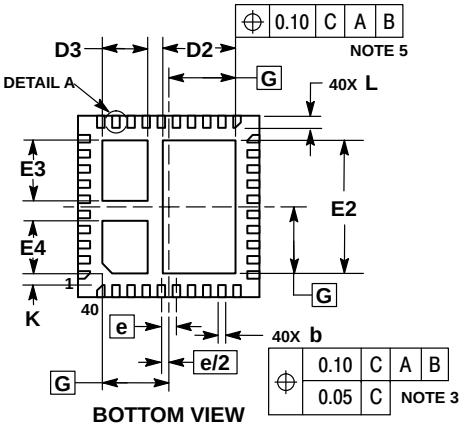
DETAIL A
ALTERNATE CONSTRUCTIONS

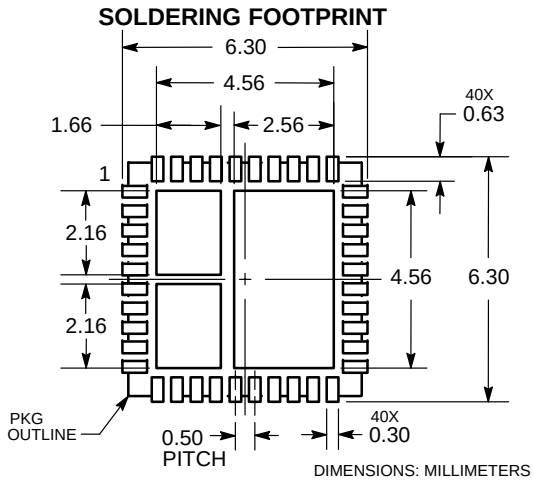


DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.30	2.50
D3	1.40	1.60
E	6.00 BSC	
E2	4.30	4.50
E3	1.90	2.10
E4	1.64	1.84
e	0.50 BSC	
G	2.20 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15





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