Power Factor Controller, High-Efficiency, Enhanced for Lighting

NCL2801

The 8−pin PFC controller NCL2801 is designed to drive PFC boost stages. It is based on an innovative ***V***alley **C**ount **F**requency **F**old−back (**VCFF**) method. The circuit classically operates in **Cr**itical conduction **M**ode (**CrM**) for high load values. When the load decreases a Discontinuous Conduction Mode DCM is forced by forcing a dead time which, by construction corresponds to a fixed number of valleys. The lower the output power, the higher the number of valleys corresponding to the dead time. After DCM works down to 6th valley switching and if the load continues to decrease, a dead time is continuously added to the 6th valley. The end of additional dead time is synchronized with the drain voltage valley. The maximum switching period is limited to 36.5 μs. **VCFF** maximizes the efficiency during DCM and light load. In particular, the stand−by losses are reduced to a minimum. Like in **FCCrM** controllers, internal circuitry allows near−unity power factor even when the switching frequency is reduced. Housed in a SO−8 package, the circuit also incorporates the features necessary for robust and compact PFC stages, with few external components.

General Features

- Near−Unity Power Factor
- Critical Conduction Mode (CrM)
- Valley Count Frequency Fold−Back (VCFF)
- Peak Current Control Mode to Maintain a Proper Current Shaping in VCFF Mode
- Fast Line / Load Transient Compensation (***D***ynamic ***R***esponse ***E***nhancer) Option
- Brown−out Detection
- Two−level Line Feed−Forward (HL&LL)
- Valley Turn−on (No Valley Hoping by Construction)
- High Drive Capability: −500 mA / +800 mA
- V_{CC} Range: from 10.5 V to 27 V
- Low Start−up Consumption for :
- [*C*]& [*D*] Option: Low V_{CC} Start−up Level (12.5 V)
  [*A*]& [*B*] Option: High V_{CC} Start−up Level (17.0 V)
  [*E*]& [*F*] Option: High V_{CC} Start−up Level (10.5 V)
- This is a Pb−Free Device

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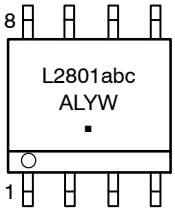
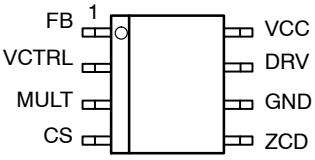
SOIC−8
CASE 751

MARKING DIAGRAMS



L2801abc = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information on page 25 of this data sheet.

Safety Features

- Thermal Shutdown
- Non−latching, Over−Voltage Protection (3 Prog Levels)
- Over Current Limitation
- Low Duty−Cycle Operation if the Bypass Diode is Shorted
- Open Ground Pin Fault Monitoring
- Pin CS shorted to GND or open Monitoring
- Pin ZCD open tested before controller starts
- Controller not allowed to start if MULT pin is left open

Typical Applications

- PC Power Supplies
- Lighting Ballasts (LED, Fluorescent)
- Flat TV
- All Off Line Appliances Requiring Power Factor Correction
  Several product configurations coded with three letters (L_1,L_2, L_3) marked on the package will be available

Table 1. NCL2801 1ST LETTER CODING OF PRODUCT VERSIONS

L_1	Soft OVP (% of V_{REF})	Fast OVP (% of V_{REF})
A	Disabled	112.5
B	Disabled	110.0
C (default)	105.0	107.0

1. The NCL2801 SO8 package is marked $L_1L_2L_3$

Table 2. NCL2801 2ND LETTER CODING OF PRODUCT VERSIONS

L2	VCC Startup Level (V)	DRE (After Startup)	DRE (During Startup)
A	17.0	NO	YES
B	17.0	YES	YES
C	12.5	NO	YES
D (default)	12.5	YES	YES
E	10.5	NO	YES
F	10.5	YES	YES

2. The NCL2801 SO8 package is marked $L_1L_2L_3$

Table 3. NCL2801 3RD LETTER CODING OF PRODUCT VERSIONS

L_3	Brown−in & Brown−out	Line Range Detection w/ 2−level Line Feed−Forward
A (default)	YES	YES
B	YES	NO
C	NO	YES
D	NO	NO

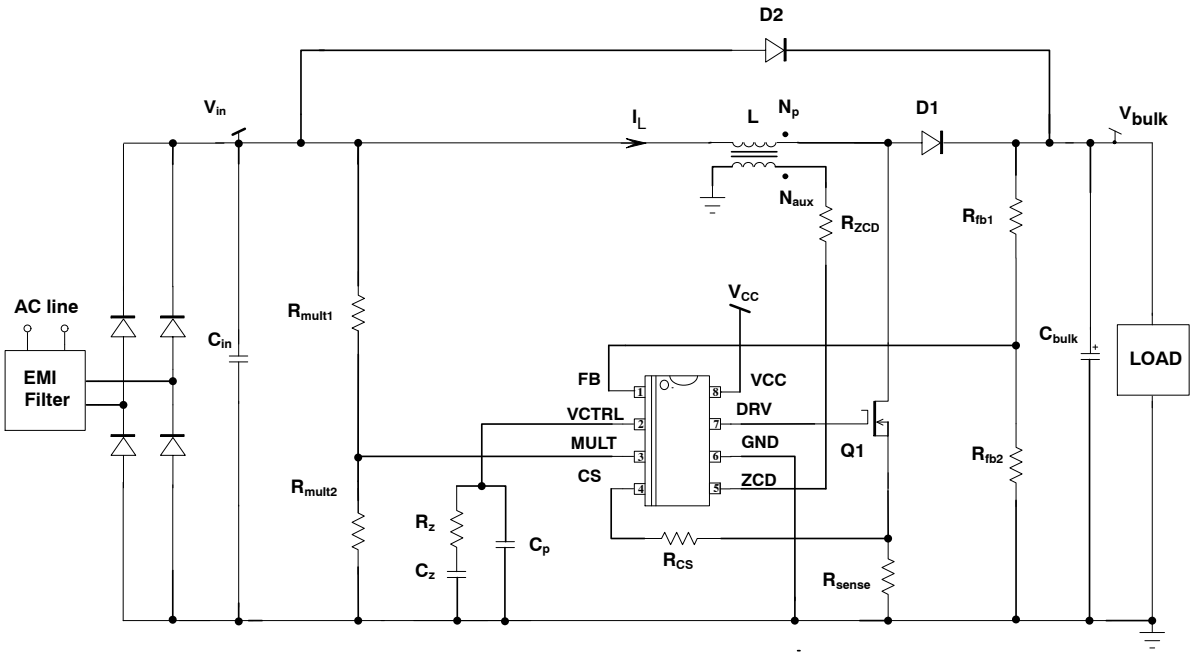


Figure 1. NCL2801 Application Schematic

Table 4. NCL2801 3RD LETTER CODING OF PRODUCT VERSIONS

Pin Number	Name	Function
1	FB	This pin receives a portion of the PFC output voltage for the regulation and the optional Dynamic Response Enhancer (DRE) that drastically speeds−up the loop response when the output voltage drops below 95.5 % of the desired output level. FB pin voltage V_{FB} is also the input signal for the (non−latching) Over−Voltage (OVP). The UVP comparator prevents operation as long as FB pin voltage is lower than V_{UVPH} internal voltage reference. A SOFTOVP comparator gradually reduces the duty−ratio when FB pin voltage exceeds 105% of V_{REF} (option dependent). If despite of this, the output voltage still increases, the driver is immediately disabled by fast OVP if the output voltage exceeds x% of the desired level (option dependent).. A 250−nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidently left open.
2	VCTRL	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. VCTRL pin is internally pulled down when the circuit is off so that when it starts operation, the power increases slowly to provide a soft−start function. VCTRL pin must not be controlled or pulled down externally. Pulled to GND if BO and at startup (pseudo−soft start). Just a switch.
3	MULT	Multiplier input pin. This pin receives a scaled down rectified mains voltage by the means of a resistor voltage divider connected between Vin and GND. .
4	CS	This pin senses the MOSFET current in order to end the on−time when the current reaches the control value or the maximum current limit. Just before startup, the value of the resistance between CS pin and GND pin is sensed for determining the VCTRL value of the CrM to DCM threshold.
5	ZCD	This pin uses the auxiliary winding voltage to determine the inductor current zero crossing.
6	GND	Connect this pin to the PFC stage ground.
7	DRV	The high−current capability of the totem pole gate drive (−0.5/+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
8	VCC	This pin is the positive supply of the IC. The circuit starts to operate when VCC exceeds 17.0 V ([*A*] & [*B*] Versions) or 12.5 V ([*C*] & [*D*] Versions) or 10.5 V ([*E*] & [*F*] Options) and turns off when VCC goes below 10.0 V (typ) for [*C*] & [*D*] Options and below 9.0 V (typ) for [*A*] & [*B*] &[*E*] & [*F*] Options. After start−up, the operating range is 10.0 V (or 9 V depending on option) up to 27 V.

Table 5. MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
FB	1	Feedback Pin	−0.3, +9	V
VCTRL	2	$V_{CONTROL}$ pin	−0.3, $V_{ctrl,max}$ (Note 3)	V
MULT	3	Multiplier Input pin	−0.3, +9	V
CS	4	CS Pin	−0.3, +9	V
ZCD	5	ZCD Pin	−0.3, VCC+0.3	V
DRV	7	Driver Voltage Driver Current	−0.3, V_{DRV} (Note 3) −500, +800	V mA
VCC	8	Power Supply Input	−0.3, + 27	V
P_D $R_{\theta ja}$		Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A=70°C Thermal Resistance Junction to Air	300 180	mW °C/W
T_J		Operating Junction Temperature Range	−40 to + 125	°C
$T_{J,max}$		Maximum Junction Temperature	150	°C
$T_{S,max}$		Storage Temperature Range	−65 to 150	°C
$T_{L,max}$		Lead Temperature (Soldering, 10s)	300	°C
MSL		Moisture Sensitivity Level	1	−
		ESD Capability, HBM model (Note 4)	> 2000	V
		ESD Capability, Machine Model (Note 4)	> 200	V
		ESD,CDM	1000	V

3. "$V_{ctrl,max}$" is the VCTRL pin clamp voltage. "V_{DRV}" is the DRV clamp voltage ($V_{DRVhigh}$) if V_{CC} is higher than ($V_{DRVhigh}$). "V_{DRV}" is V_{CC} otherwise.
4. This device(s) contains ESD protection and exceeds the following tests: Human Body Model 2000 V per JEDEC Standard JESD22−A114E Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
5. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V, T_J = −40°C to +125°C, unless otherwise specified) (Note 6)

Symbol	Rating	Min	Typ	Max	Unit
START−UP AND SUPPLY CIRCUIT					
$V_{CC,on}$	Start−Up Threshold, V_{CC} increasing: [*E*] & [*F*] Versions [*C*] & [*D*] Versions [*A*] & [*B*] Versions	9.75 11.6 15.6	10.5 12.50 16.7	11.25 13.4 18.00	V V V
$V_{CC,off}$	Minimum Operating Voltage, V_{CC} falling [*C*] & [*D*] Versions [*A*] & [*B*] & [*E*] & [*F*]	9.3 8.4	10.0 9.0	10.7 9.6	V V
$V_{CC,rst}$	Voltage at which IC completely restarts ICC drops to ~ $I_{CC,start}$ (Min and Max values are guaranteed by functional testing)	6.50	7.2	7.80	V
$V_{CC,hyst}$	Hysteresis ($V_{CC,on} - V_{CC,off}$) [*E*] & [*F*] Versions [*C*] & [*D*] Versions [*A*] & [*B*] Versions	0.75 1.25 6.00	1.6 2.5 7.7	3.0 3.75 10	V V V
$I_{CC,start}$	Start−Up Current, V_{CC} = 9.4 V, below startup voltage	0	10	60	μA
$I_{CC,op1}$	Operating Consumption, no switching.	0	0.4	1.00	mA
$I_{CC,op2}$	Operating Consumption, 50−kHz switching, no load on DRV pin	1.0	2.00	3.00	mA
GATE DRIVE					
t_R	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	15	30	90	ns
t_F	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	10	20	50	ns
R_{OH}	Source resistance @ 200 mV under High VCC	4	10	20	Ω
R_{OL}	Sink resistance @ 200mV above Low VCC	2	7	15	Ω
$V_{DRV,low}$	DRV pin level for V_{CC} = $V_{CC,off}$ + 200 mV (10−kΩ resistor between DRV and GND) [*A*] & [*B*] & [*E*] & [*F*] [*C*] & [*D*] Versions	8.6 9.6	9.2 10	10 11	V V
$V_{DRV,high}$	DRV pin level at V_{CC} = 27 V (R_L = 33 kΩ & C_L = 1 nF)	10	12	14	V
$V_{DRV,L}$	Maximum DRV voltage while forcing zero at DRV pin and injecting 10 mA into DRV pin @ V_{CC} = 12 V	0	100	200	mV
REGULATION BLOCK					
V_{REF}	Feedback Voltage Reference	2.45	2.50	2.55	V
I_{EA}	Error Amplifier Current Capability (source and sink)	15	20	25	μA
G_{EA}	Error Amplifier Gain	110	200	290	μS
$V_{ctrl,max}$ $V_{ctrl,min}$	*VCTRL* pin Voltage (V_{ctrl}): − @ V_{FB} = 2 V (OTA is sourcing 20 μA) − @ V_{FB} = 3 V (OTA is sinking 20 μA)	4.4 0.4	4.5 0.5	4.6 0.6	 V
CURRENT SENSE BLOCK					
$V_{CS\_OCP(th)}$	Current Sense Voltage Reference for option w/o line level detection [**B]&[**D] Options At $t_{LEB,OCP}$	0.97	1.07	1.19	V
$V_{CS\_OVS(th)}$	Current Sense Overstress Voltage Reference for option w/o line level detection [**B]&[**D] Options At $t_{LEB,OVS}$	1.45	1.60	1.78	V
$V_{CS\_OCP\_LL(th)}$	Current Sense Voltage Reference when Low Line is detected [**A]&[**C] Options At $t_{LEB,OCP}$	0.97	1.07	1.19	V
$V_{CS\_OVS\_LL(th)}$	Current Sense Overstress Voltage Reference when Low Line is detected [**A]&[**C] Options At $t_{LEB,OVS}$	1.45	1.60	1.78	V

Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V, T_J = −40°C to +125°C, unless otherwise specified) (Note 6)

Symbol	Rating	Min	Typ	Max	Unit
$V_{CS\_OCP\_HL(th)}$	Current Sense Voltage Reference when High Line is detected [**A]&[**C] Options At $t_{LEB,OCP}$**	0.53	0.58	0.66	V
$V_{CS\_OVS\_HL(th)}$	Current Sense Overstress Voltage Reference when High Line is detected [**A]&[**C] Options At $t_{LEB,OVS}$	0.79	0.87	0.97	V
$t_{LEB,OCP}$	Leading edge Blanking Time for current control	125	200	275	ns
$t_{LEB,OVS}$	Leading edge Blanking Time for Overstress	50	100	150	ns
t_{OCP}	Over−Current Protection Delay from V_{CS}>$V_{CS(th)}$ to DRV low Test: V_{CS} > V_{CS} + 100 mV	10	40	200	ns
$t_{WDG(OS)}$	Watch Dog Timer in “OverStress” Situation	400	800	1200	μs
ZERO CURRENT DETECTION BLOCK					
$V_{CL(pos)}$	ZCD positive clamp (V_{CC} = 12 V, I_{ZCD} = 5 mA)	12.6	12.9	13.2	V
$V_{ZCD(th)H}$	Zero Current Detection, V_{ZCD} rising	675	750	825	mV
$V_{ZCD(th)L}$	Zero Current Detection, V_{ZCD} falling	200	250	300	mV
$V_{ZCD(hyst)}$	Hysteresis of the Zero Current Detection Comparator	375	500	625	mV
$I_{ZCD,bias}$	ZCD pin input leakage current	0	250	500	nA
t_{ZCD}	(V_{ZCD} < $V_{ZCD(th)L}$) to (DRV high)	20	80	200	ns
t_{SYNC}	Minimum ZCD Pulse Width (Guaranteed by Design)	–	60	–	ns
t_{WDG}	Watch Dog Timer If no ZCD detected	80	200	320	μs
$I_{ZCD,pu}$	Pull−up current source to detect ZCD open pin At startup only	0.85	1	1.15	μA
$V_{REF,ZCD,open}$	Voltage reference to test ZCD pin short during startup	150	200	250	mV
MULTIPLIER					
K_{mult}	Multiplier Gain (Note 2) for option w/o line level detection [**B]&[**D] Options	0.34	0.38	0.42	1/V
$K_{mult,HL}$	Multiplier Gain (Note 2) when High Line is detected [**A]&[**C] Options	0.22	0.24	0.28	1/V
$K_{mult,LL}$	Multiplier Gain (Note 2) when Low Line is detected [**A]&[**C] Options	0.72	0.80	0.88	1/V
$K_{mult,Ratio}$	Ration between $K_{mult,LL}$ and $K_{mult,HL}$ [**A]&[**C] Options	2.9	3.3	3.7	
K_{offset}	K_{offset}.V_{ton} voltage added at the multiplier output [**A]&[**C] Options (w/ Line Detection)	0.10	0.140	0.20	
K_{offset_nld}	K_{offset}.V_{ton} voltage added at the multiplier output [**B]&[**D] Options (w/o Line Detection)	0.040	0.075	0.12	
I_{mult_pd}	Current pull−down on Mult pin	200	280	350	nA
V_{mult_max}	Maximum MULT pin voltage Controller disabled if MULT pin voltage goes above this threshold	2.88	3.2	3.52	V
MAXIMUM ON−TIME					
$t_{ON,max,A,2}$	@ V_{CTRL} = 4.50 V	26	30	36	μs
$t_{ON,max,A,1}$	@ V_{CTRL} = 0.55 V	3.6	5	6.9	μs

Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V, T_J = −40°C to +125°C, unless otherwise specified) (Note 6)

Symbol	Rating	Min	Typ	Max	Unit
R_{CS} VALUE IDENTIFICATION REFERENCE VOLTAGES					
I_{RCS}	Internal current sourced by CS pin into a 1% R_{CS} resistor just before the startup generates a voltage drop V_{CS}	0.96	1.0	1.04	mA
$V_{RCS,REF,1}$	Internal voltage reference for identifying the R_{CS} resistor value CS pin is said shorted to GND if $V_{CS} < V_{RCS,REF,1}$	20	50	100	mV
$V_{RCS,REF,2}$	Internal voltage reference for identifying the R_{CS} resistor value R_{CS} = 150 Ω if $_{RCS,REF,1} < V_{CS} < V_{RCS,REF,2}$	180	230	280	mV
$V_{RCS,REF,3}$	Internal voltage reference for identifying the R_{CS} resistor value R_{CS} = 330 Ω if $V_{RCS,REF,2} < V_{CS} < V_{RCS,REF,3}$	400	460	530	mV
$V_{RCS,REF,4}$	Internal voltage reference for identifying the R_{CS} resistor value R_{CS} = 620 Ω if $V_{RCS,REF,3} < V_{CS} < V_{RCS,REF,4}$	720	790	880	mV
$V_{RCS,REF,5}$	Internal voltage reference for identifying the R_{CS} resistor value R_{CS} = 1000 Ω if $V_{RCS,REF,4} < V_{CS} < V_{RCS,REF,5}$ CS pin open if $V_{CS} > V_{RCS,REF,5}$ RCS open do not allow the controller to start	1190	1300	1400	mV
FREQUENCY FOLDBACK THRESHOLDS & HYSTERESIS					
$V_{CTRL,th,12,1000}$	V_{CTRL} threshold for valley1 to valley2 forcing @R_{CS} = 1000 Ω	1.971	2.19	2.409	V
$V_{CTRL,th,23,\ 1000}$	V_{CTRL} threshold for valley2 to valley3 forcing @R_{CS} = 1000 Ω	1.647	1.83	2.013	V
$V_{CTRL,th,34,\ 1000}$	V_{CTRL} threshold for valley3 to valley4 forcing @R_{CS} = 1000 Ω	1.332	1.48	1.628	V
$V_{CTRL,th,45,\ 1000}$	V_{CTRL} threshold for valley4 to valley5 forcing @R_{CS} = 1000 Ω	1.008	1.12	1.232	V
$V_{CTRL,th,56,\ 1000}$	V_{CTRL} threshold for valley5 to valley6 forcing @R_{CS} = 1000 Ω	0.693	0.77	0.847	V
$V_{CTRL,th,65,\ 1000}$	V_{CTRL} threshold for valley6 to valley5 forcing @R_{CS} = 1000 Ω	1.008	1.12	1.232	V
$V_{CTRL,th,54,\ 1000}$	V_{CTRL} threshold for valley5 to valley4 forcing @R_{CS} = 1000 Ω	1.332	1.48	1.628	V
$V_{CTRL,th,43,\ 1000}$	V_{CTRL} threshold for valley4 to valley3 forcing @R_{CS} = 1000 Ω	1.647	1.83	2.013	V
$V_{CTRL,th,32,\ 1000}$	V_{CTRL} threshold for valley3 to valley2 forcing @R_{CS} = 1000 Ω	1.971	2.19	2.409	V
$V_{CTRL,th,21,\ 1000}$	V_{CTRL} threshold for valley2 to valley1 forcing @R_{CS} = 1000 Ω	2.286	2.54	2.794	V
$V_{CTRL,hyst,\ 1000}$	V_{CTRL} hysteresis when changing forced valley @R_{CS} = 1000 Ω	300	356	420	mV
$V_{CTRL,th,12,620}$	V_{CTRL} threshold for valley1 to valley2 forcing @R_{CS} = 620 Ω	1.647	1.830	2.013	V
$V_{CTRL,th,23,\ 620}$	V_{CTRL} threshold for valley2 to valley3 forcing @R_{CS} = 620 Ω	1.413	1.570	1.727	V
$V_{CTRL,th,34,\ 620}$	V_{CTRL} threshold for valley3 to valley4 forcing @R_{CS} = 620 Ω	1.170	1.300	1.430	V
$V_{CTRL,th,45,\ 620}$	V_{CTRL} threshold for valley4 to valley5 forcing @R_{CS} = 620 Ω	0.927	1.030	1.133	V
$V_{CTRL,th,56,\ 620}$	V_{CTRL} threshold for valley5 to valley6 forcing @R_{CS} = 620 Ω	0.693	0.770	0.847	V
$V_{CTRL,th,65,\ 620}$	V_{CTRL} threshold for valley6 to valley5 forcing @R_{CS} = 620 Ω	0.927	1.030	1.133	V
$V_{CTRL,th,54,\ 620}$	V_{CTRL} threshold for valley5 to valley4 forcing @R_{CS} = 620 Ω	1.170	1.300	1.430	V
$V_{CTRL,th,43,\ 620}$	V_{CTRL} threshold for valley4 to valley3 forcing @R_{CS} = 620 Ω	1.413	1.570	1.727	V
$V_{CTRL,th,32,\ 620}$	V_{CTRL} threshold for valley3 to valley2 forcing @R_{CS} = 620 Ω	1.647	1.830	2.013	V
$V_{CTRL,th,21,\ 620}$	V_{CTRL} threshold for valley2 to valley1 forcing @R_{CS} = 620 Ω	1.890	2.100	2.310	V
$V_{CTRL,hyst,\ 620}$	V_{CTRL} hysteresis when changing forced valley @R_{CS} = 620 Ω	200	267	320	mV
$V_{CTRL,th,12,\ 330}$	V_{CTRL} threshold for valley1 to valley2 forcing @R_{CS} = 330 Ω	1.332	1.480	1.628	V
$V_{CTRL,th,23,\ 330}$	V_{CTRL} threshold for valley2 to valley3 forcing @R_{CS} = 330 Ω	1.170	1.300	1.430	V
$V_{CTRL,th,34,\ 330}$	V_{CTRL} threshold for valley3 to valley4 forcing @R_{CS} = 330 Ω	1.008	1.120	1.232	V
$V_{CTRL,th,45,\ 330}$	V_{CTRL} threshold for valley4 to valley5 forcing @R_{CS} = 330 Ω	0.846	0.940	1.034	V

Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V, T_J = −40°C to +125°C, unless otherwise specified) (Note 6)

Symbol	Rating	Min	Typ	Max	Unit
$V_{CTRL,th,56,\ 330}$	V_{CTRL} threshold for valley5 to valley6 forcing @R_{CS} = 330 Ω	0.693	0.770	0.847	V
$V_{CTRL,th,65,\ 330}$	V_{CTRL} threshold for valley6 to valley5 forcing @R_{CS} = 330 Ω	0.846	0.940	1.034	V
$V_{CTRL,th,54,\ 330}$	V_{CTRL} threshold for valley5 to valley4 forcing @R_{CS} = 330 Ω	1.008	1.120	1.232	V
$V_{CTRL,th,43,\ 330}$	V_{CTRL} threshold for valley4 to valley3 forcing @R_{CS} = 330 Ω	1.170	1.300	1.430	V
$V_{CTRL,th,32,\ 330}$	V_{CTRL} threshold for valley3 to valley2 forcing @R_{CS} = 330 Ω	1.332	1.480	1.628	V
$V_{CTRL,th,21,\ 330}$	V_{CTRL} threshold for valley2 to valley1 forcing @R_{CS} = 330 Ω	1.494	1.660	1.826	V
$V_{CTRL,hyst,\ 330}$	V_{CTRL} hysteresis when changing forced valley @R_{CS} = 330 Ω	120	178	230	mV
$V_{CTRL,th,12,150}$	V_{CTRL} threshold for valley1 to valley2 forcing @R_{CS} = 150 Ω	1.008	1.120	1.232	V
$V_{CTRL,th,23,\ 150}$	V_{CTRL} threshold for valley2 to valley3 forcing @R_{CS} = 150 Ω	0.927	1.030	1.133	V
$V_{CTRL,th,34,\ 150}$	V_{CTRL} threshold for valley3 to valley4 forcing @R_{CS} = 150 Ω	0.846	0.940	1.034	V
$V_{CTRL,th,45,\ 150}$	V_{CTRL} threshold for valley4 to valley5 forcing @R_{CS} = 150 Ω	0.774	0.860	0.946	V
$V_{CTRL,th,56,\ 150}$	V_{CTRL} threshold for valley5 to valley6 forcing @R_{CS} = 150 Ω	0.693	0.770	0.847	V
$V_{CTRL,th,65,\ 150}$	V_{CTRL} threshold for valley6 to valley5 forcing @R_{CS} = 150 Ω	0.774	0.860	0.946	V
$V_{CTRL,th,54,\ 150}$	V_{CTRL} threshold for valley5 to valley4 forcing @R_{CS} = 150 Ω	0.846	0.940	1.034	V
$V_{CTRL,th,43,\ 150}$	V_{CTRL} threshold for valley4 to valley3 forcing @R_{CS} = 150 Ω	0.927	1.030	1.133	V
$V_{CTRL,th,32,\ 150}$	V_{CTRL} threshold for valley3 to valley2 forcing @R_{CS} = 150 Ω	1.008	1.120	1.232	V
$V_{CTRL,th,21,\ 150}$	V_{CTRL} threshold for valley2 to valley1 forcing @R_{CS} = 150 Ω	1.089	1.210	1.331	V
$V_{CTRL,hyst,\ 150}$	V_{CTRL} hysteresis when changing forced valley @R_{CS} = 150 Ω	35	89	135	mV
SWITCHING CYCLE DEAD TIME					
t_{ADT}	Dead time added after 6th valley Vctrl = 0.50 V Vctrl = 0.77 V	14 0	20 0.1	– 0.4	µs µs
FEED−BACK OVER AND UNDER−VOLTAGE PROTECTIONS (OVP)					
$R_{softOVP,C}$	Ratio (Soft OVP Threshold, V_{FB} rising) over V_{REF} (Options [C**])	103.5	105	106.5	%
$R_{softOVP(HYST)}$	Ratio (Soft OVP Hysteresis) over V_{REF} .	0.8	1.3	3.2	%
$R_{fastOVP,A}$	Ratio (Fast OVP Threshold, V_{FB} rising) over V_{REF} (Options [A**])	108.5	112.5	116.5	%
$R_{fastOVP,B}$	Ratio (Fast OVP Threshold, V_{FB} rising) over V_{REF} (Option [B**])	106.1	110	113.9	%
$R_{fastOVP,C}$	Ratio (Fast OVP Threshold, V_{FB} rising) over V_{REF} (Option [C**])	103.2	107	110.8	%
$R_{fastOVP(HYST)}$	Ratio (Fast OVP Hysteresis) over V_{REF}	3.0	4.0	5.7	%
$I_{B,FB}$	FB pin pull−down Current @ V_{FB} = V_{OVP} and V_{FB} = V_{UVP} Pulls down the FB pin in case the pin is open (solder failure)	50	200	450	nA
DYNAMIC RESPONSE ENHANCER (DRE)					
R_{DRE}	Ratio (DRE Threshold, V_{FB} falling) over V_{REF}	94.0	95.7	97.5	%
$R_{DRE(HYST)}$	Ratio (DRE Hysteresis) over V_{REF}	0.8	2.0	3.0	%
$I_{VCTRL,Startup}$	Current measured out of VCTRL pin (DRE current source minus max OTA current) @ VFB=1V (PFCOK=0 ⇔ Startup)	80	100	120	µA
$I_{VCTRL,1,Steady}$	Current measured out of VCTRL pin (DRE current source minus max OTA current) @ VFB=1V (PFCOK=1 ⇔ Steady State) [*B*], [*D*], [*F*] Product Options	160	200	240	µA
UNDER VOLTAGE PROTECTION / DISABLE					
V_{UVPH}	UVP Threshold, V_{FB} increasing	380	450	520	mV
V_{UVPL}	UVP Threshold, V_{FB} decreasing	150	200	250	mV

Table 6. ELECTRICAL CHARACTERISTICS (Conditions: VCC = 18 V, T_J = −40°C to +125°C, unless otherwise specified) (Note 6)

Symbol	Rating	Min	Typ	Max	Unit
$V_{UVP(HYST)}$	UVP Hysteresis	200	250	300	mV
BROWN−OUT PROTECTION AND LINE FEED FORWARD					
V_{BOH}	Brown−In Threshold, V_{mains} increasing Note: $V_{line,BOH,rms}$ = 74, 80, 87 V assuming $1/K_m$ = 144	725	787	860	mV
V_{BOL}	Brown−Out Threshold, V_{mains} decreasing Note: $V_{line,BOL,rms}$ = 64, 72, 78 V assuming $1/K_m$ = 144	634	709	770	mV
$V_{BO(HYST)}$	Brown−Out Comparator Hysteresis	50	75	130	mV
$t_{BO(blank)}$	Brown−Out Blanking Time	36	50	67	ms
$I_{VCTRL(BO)}$	VCTRL pin sink current during BO condition	20	30	42	μA
V_{HL}	Comparator Threshold for Line Range Detection V_{MULT} rising Note: $V_{line,HL,rms}$ = 157,165,174 V assuming $1/K_m$ = 144	1.543	1.625	1.706	V
V_{LL}	Comparator Threshold for Line Range Detection V_{MULT} falling Note: $V_{line,HL,rms}$ = 137,145,152 V assuming $1/K_m$ = 144	1.350	1.422	1.493	V
$V_{HL(hyst)}$	Comparator Hysteresis for Line Range Detection	37	218	300	mV
$t_{HL(blank)}$	Blanking Time for Line Range Detection (must stay below $V_{LL}$for 25 ms before changing to LL)	13	25	43	ms
THERMAL SHUTDOWN					
T_{LIMIT}	Thermal Shutdown Threshold	150	–	–	°C
H_{TEMP}	Thermal Shutdown Hysteresis	–	50	–	°C

6. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.
7. In CrM mode, $G_{mult} = V_{CS(th)}/[(V_{CTRL}-0.5)*(1.5/4.0)*V_{MULT}]$, $V_{CS(th)}$ is the CS pin voltage threshold at which DRV pin goes low (end of on−time). K_{offset} is set to zero in test mode, otherwise the formula is more complex.

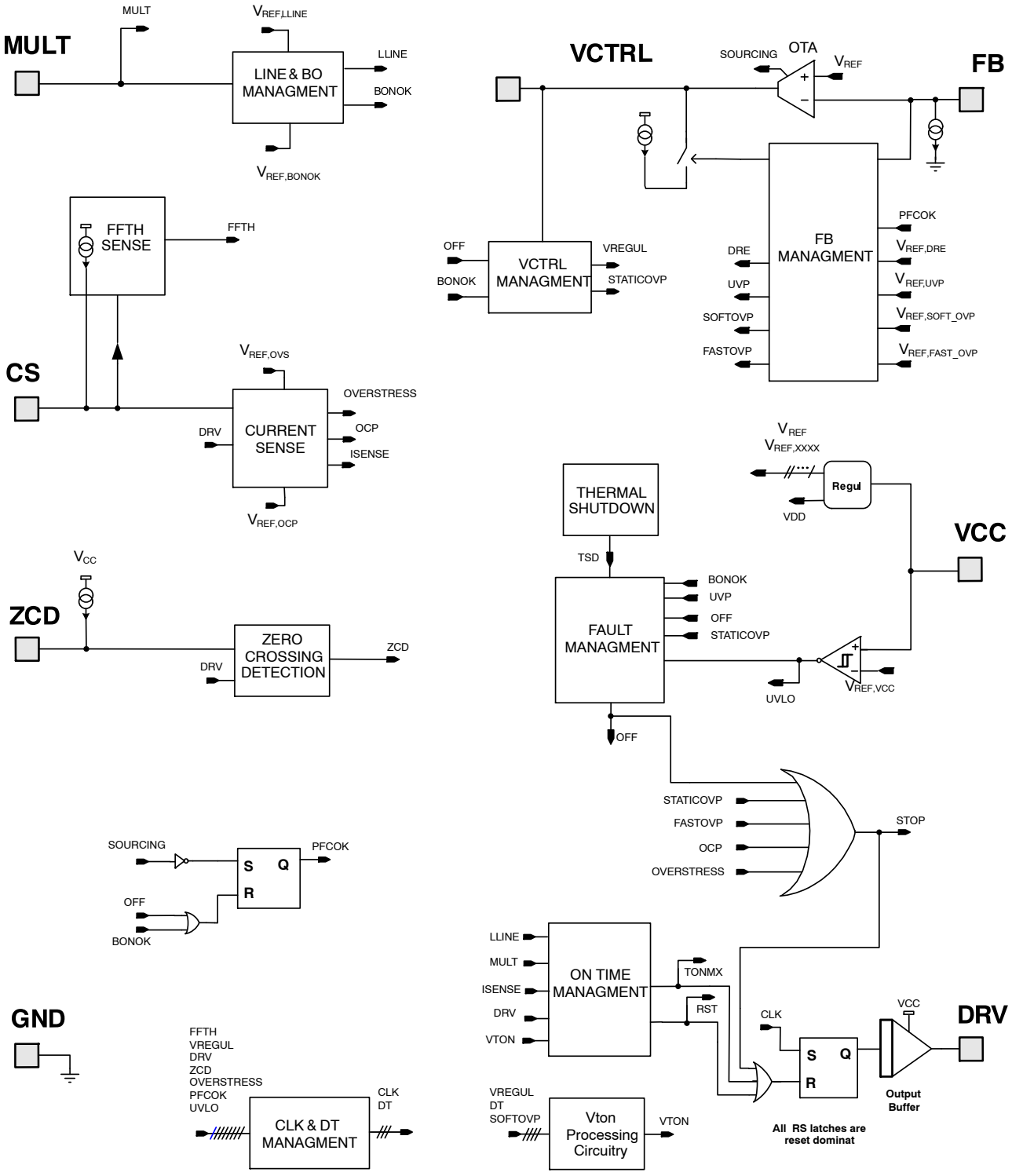


Figure 2. NCL2801 Block Diagram (SOURCING Flag is High When OTA Sources Current, if Sourcing Less Than 1nA SOURCING Flag Goes Low)

DETAILED OPERATING DESCRIPTION

Introduction

NCL2801 is designed for working with LED Lighting applications coping with high ripple voltage on bulk capacitor and providing optimized line current THD and good efficiency. In addition, it incorporates protection features for robust operation. More generally, NCL2801 is ideal in systems where cost−effectiveness, reliability, low line current THD, low stand−by power and high efficiency are key requirements:

- Valley Count Frequency Fold−back: NCL2801 is designed to drive PFC boost stages in so−called *V*alley *C*ount *F*requency *F*old−back (*VCFF*). In high load current condition, the circuit classically operates in *Cr*itical conduction *M*ode (*CrM*) also called 1st valley switching. When output power is decreasing, if a threshold is reached (determined by sensing the CS pin impedance during initial power up), a dead time based on a number of valleys is added. The number of valleys will increase, each time a dead time window (based on V_{CTRL} value) is entered. By construction, this counting process will avoid valley hoping during the mains voltage period. If the output power continues decreasing and the 6th valley is reached, extra “analog” dead time will be added based on a voltage ramp (see Figure 4). On−time will be synchronized with a valley. A timer will clamp the total switching period to not exceed 36.5 μs (the switching frequency will never go under about 27.4 kHz). The switching frequency depends on output voltage, input voltage, and boost inductor value, and increases as the load power increases. Hysteresis and added to the VCTRL control windows to avoid valley hopping during steady state conditions. *VCFF* maximizes the efficiency at both nominal and light load. Similarly to *FCCrM* controllers, an internal circuitry allows near−unity power factor even when the switching frequency is reduced.
- Low Start−up Current: The start−up consumption of the circuit is minimized to allow the use of high impedance start−up resistors to precharge the V_{CC} capacitor. Also, the minimum value of the UVLO hysteresis is 6 V to avoid the need for large V_{CC} capacitors and help shorten the start−up time without the need for excessive dissipation in the start−up circuit. The [*C*] & [*D*] version is preferred in applications where the circuit is fed by an external power source (from an auxiliary power supply or from a downstream converter). After start−up, the high V_{CC} maximum rating allows a large operating range from 10.5 V up to 27 V.
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer): Since PFC stages exhibit low loop bandwidth, abrupt changes in the load or input voltage (e.g. at start−up) may cause excessive over or under−shoot. This circuit limits possible deviations from the regulation level as follows:
  - NCL2801 linearly decays the power delivery to zero when the output voltage exceeds the soft OVP limit (105% of V_{REF}) for option [C**]). Soft OVP feature is disabled on options [A**] &[B**]. If this soft OVP is too smooth and the output continues to rise, the circuit immediately (priority to Fast OVP) interrupts the power delivery when the output voltage is 112.5 % above its desired level (Fast OVP) for options [A**]. Options [B**] & [C**] are providing lower Fast OVP thresholds. Fast OVP threshold is higher than Soft OVP threshold for option [C**].
  - While disabled on options [*A*], [*C*] and [*E*] after startup time, NCL2801 has a DRE (Dynamic Response Enhancer) circuitry on options [*B*], [*D*]&[*F*] which dramatically speeds−up the regulation loop when the output voltage goes below 95.5 % of its regulation level. The DRE function is enabled only after the PFC stage has started−up to allow normal soft−start operation to occur. For all the product options, the DRE is active during the start−up phase to accelerate the start−up (VCTRL pin voltage is brought at its higher value by the by half of the 200−μA DRE current source which charges the capacitors of the compensation network)
- Soft−OVP / Fast−OVP (Over Voltage Protection) There are cases (for example during an high−load to low−load rapid transition) were the bulk capacitor voltage goes up very rapidly above the voltage regulation level triggering Over−Voltage protection. When the bulk capacitor voltage V_{bulk} reaches typically 105% of its nominal value, the Soft−OVP protection is triggered, causing the duty−ratio to decrease gradually down to zero. As a consequence, Vbulk decreases and when Vbulk reaches the low level of Soft−OVP threshold (typically 103% of nominal Vbulk) the protection is released and the voltage regulation loop takes−over .If Vbulk rises faster and reaches the Fast−OVP threshold (typically 107% of nominal Vbulk), the switching is instantaneously stop (DRV signal is disabled). As a consequence, Vbulk decreases and when the low level of Fast−OVP threshold is reached (typically 103% of nominal Vbulk) the protection is released and the voltage regulation loop takes−over. Soft−OVP has only one level and can be disabled dependent on product option. Three Fast_OVP levels are available by product options : typically 107, 110 and 112% of nominal Vbulk. The 112% option is well suited for applications using a low value bulk capacitor were the two−times mains frequency Vbulk

ripple voltage is high (in this case Soft−OVP is disabled)

- Safety Protections: Permanently monitoring the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over−stress makes the PFC stage extremely robust and reliable. In addition to the OVP protection, the following methods of protection are provided :
  - Maximum Current Limit: The circuit senses the MOSFET current and turns off the power switch if the set current limit is exceeded. In addition, the circuit enters a low duty−cycle operation mode when the current reaches 150% of the current limit as a result of the inductor saturation or a short of the bypass diode.
  - Thermal Shutdown: An internal thermal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C (50°C hysteresis).
- Output Stage Totem Pole: NCL2801 incorporates a −0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

NCL2801 Operation Modes

As mentioned, NCL2801 PFC controller implements a ***V***alley ***C***ount ***F***requency ***F***old−back (***VCFF***) where:

- The circuit operates in classical ***Cr***itical conduction ***M***ode (***CrM***) when output power is high and VCTRL pin voltage greater than a threshold ($V_{CTRL,th,12}$ for V_{CTRL} decreasing and $V_{CTRL,th,21}$ for V_{CTRL} increasing) which value is determined by the value the resistance R_{CS} placed between CS pin and top of Rsense which bottom is connected to GND (R_{sense} being negligible versus R_{CS}, it is the R_{CS} value which is sensed). R_{CS} value is sensed just before the startup phase (see Table 6).
- When the output power decreases the NCL2801 reduces the operating frequency by means of increasing valley number count up to 6 valleys (the number of valleys between end of inductor demagnetization and power MOSFET turn−on determines the dead time value). After counting is done, the power MOSFET turns on at drain voltage valley. When 6th valley is reached and V_{CTRL} voltage stays under 0.77 V, an extra “analog” dead time is added based on a voltage ramp (see Figure 4). The added analog dead time t_{ADT} is based on 0.77 V minus V_{CTRL} value. t_{ADT} will be equal to zero when (0.5 V−V_{CTRL}) = 0 V and will increase monotonically versus V_{CTRL} decreases while V_{CTRL} is under the 0.77 V threshold corresponding to $V_{CTRL,th,56}$. The analog dead time added tADT will equal typically 20 μs when VCTRL=0.5 V.
- When additional “analog” dead time is added, the power MOSFET turn−on will, by default, be synchronized with the falling edge of ZCD signal (valley turn−on) and there will be possible, upon request, of no valley synchronization for the on−time start. The total dead−time (number of valleys and extra dead−time) will not exceed 36.5 μs (A timer will be clamping the dead time).
- When the output power increases, the extra ”analog” dead−time plus number of valleys dead time will decrease ,according in which VCTRL pin voltage window VCTRL pin voltage is, down to 1st valley switching which is the CrM mode. The VCTRL pin voltage window in which VCTRL pin voltage is will be detected with comparators having an hysteresis to avoid valley hopping due to VCTRL pin voltage ripple.
- It will be the responsibility of the application designer not to allow a VCTRL pin voltage ripple (at 2 times the mains frequency) greater than the hysteresis of VCTRL windows.
- Valley hopping can lead to audible noise. The NCL2801 avoids this activity by locking the operating valley before turning on the MOSFET during steady state operation.

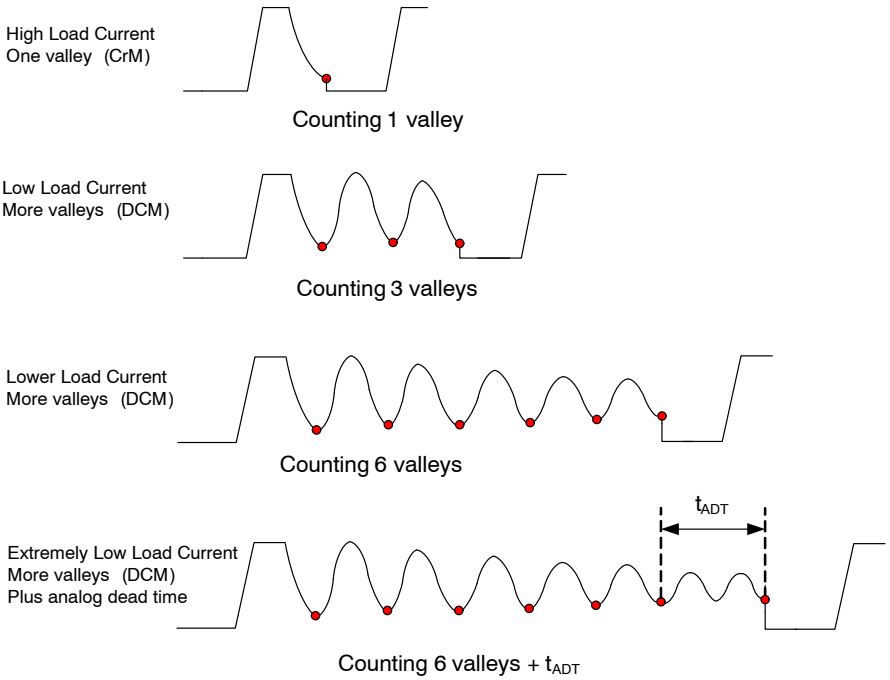


Figure 3. Valley Switching Operation in CrM and DCM Modes Seen Through Power MOSFET Drain Voltage

As illustrated in Figure 3, under high load conditions, the boost stage is operating in CrM (only one valley is counted before turning on the power MOSFET). The second example shows a DCM state of operation where 3 valleys have been counted before turning on the power MOSFET. The third example shows a DCM state with lower output power than the previous one where 5 valleys have been counted before turning on the power MOSFET.The fourth example shows how additional dead time is added after 6th valley.

Valley Count Frequency Foldback (VCFF)

The turn−on of the power MOSFET is synchronized with the valley of the power MOSFET drain voltage signal by the means of counting the falling edges of the ZCD signal until the counter reaches the number of valleys set by the window in which the VCTRL pin voltage is (see Figure 4). The 3−bit counter allows to work “Valley synchronized” up to 6 valleys. When the 6th valley is reached, and V_{CTRL} is lower than 0.770 V ($V_{CTRL,th,56}$ = 0.770 V whatever frequency foldback threshold setting), an additional analog dead time will be added to the 6 valleys dead time and there will be valley synchronization turn−on of the power MOSFET (ADT_nosync = 0 by default) based on falling edge of ZCD signal. The total dead−time (number of valleys and extra analog dead−time) will not exceed 36.5 μs. As a result of this timer the minimum switching frequency will not go under 27.4 kHz.

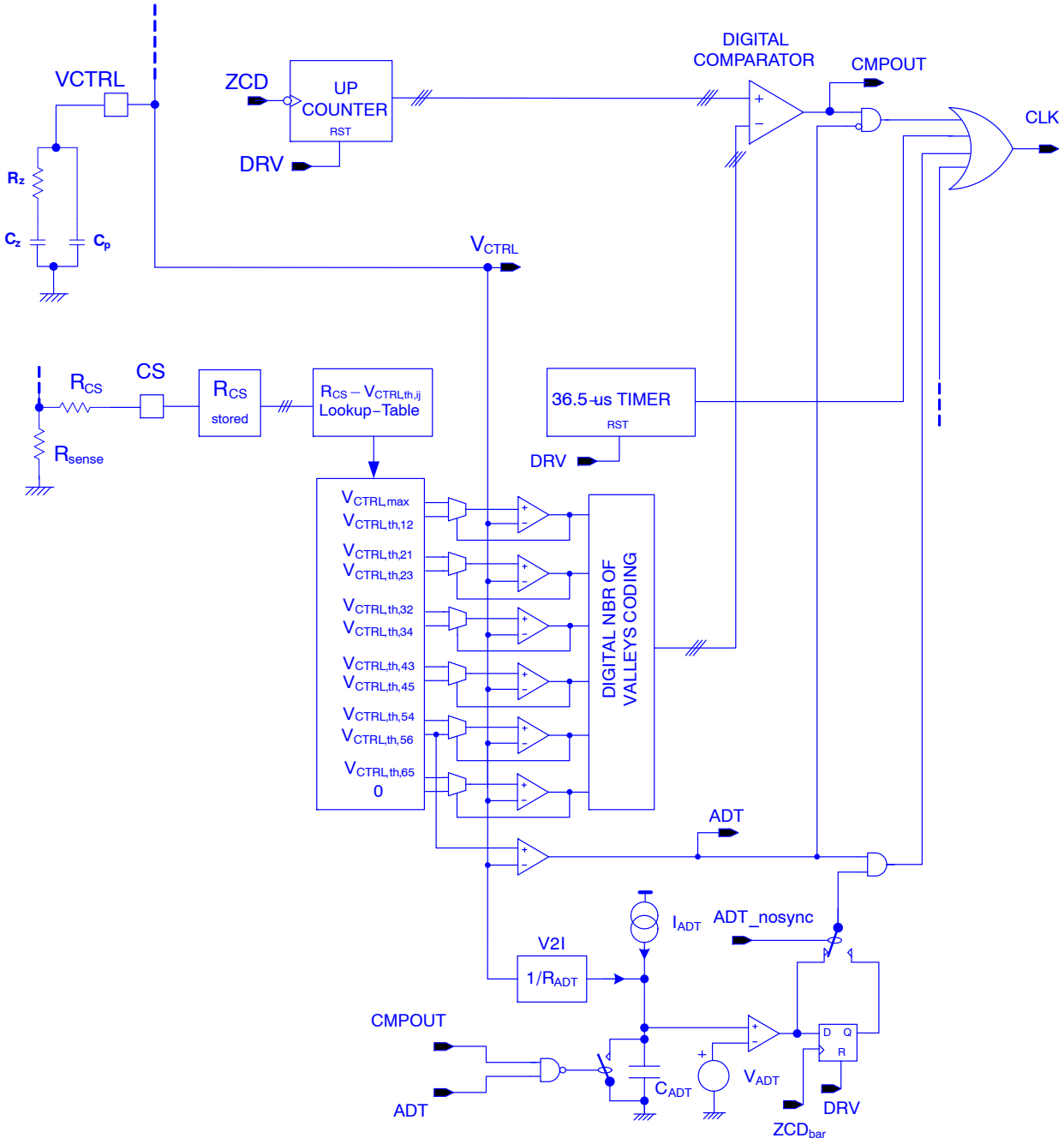


Figure 4. Valley Count Turn−on Block Diagram

This Valley Counting (VC) method avoids “valley hoping” during the half period of mains voltage which is on other designs, the cause of undesired mains current ringing glitches due to the excitation of the input EMI filter by a dead time discontinuity. The NCL2801 circuitry acts so that the PFC controller transitions from the n valley to (n+1) valley or from the n valley to (n−1) and stays on this valley number is long as the VCTRL pin voltage stays in a the voltage window corresponding to this valley number. If no demagnetization is sensed the power MOSFET will be turned−on after a watchdog timing of 200−μs.

The system relies on the counting of ZCD pulses to determine dead−time periods. Should the ZCD pulses diminish in voltage so that the event timing can’t be used, an internal copy of the last reliable first−to−second falling edge timing is substituted for the natural ZCD ring. The substitute timing for a second falling edge is allowed 1us beyond the recorded value before being asserted. The substitute timing for the third falling edge and afterward is allowed 250 ns beyond the recorded value before a ZCD pulse is asserted.

The NCL2801 PFC controller, depending on the application power output which is correlated with the

VCTRL pin voltage level, starts adding a dead−time t_{DT}. The system adjusts the on−time t_{ON} (by means of peak current control) versus t_{DT} (see Figure 5) and consequently the output power in order to ensure that the instantaneous mains current remains in phase with the mains instantaneous voltage (creating a unity PF).

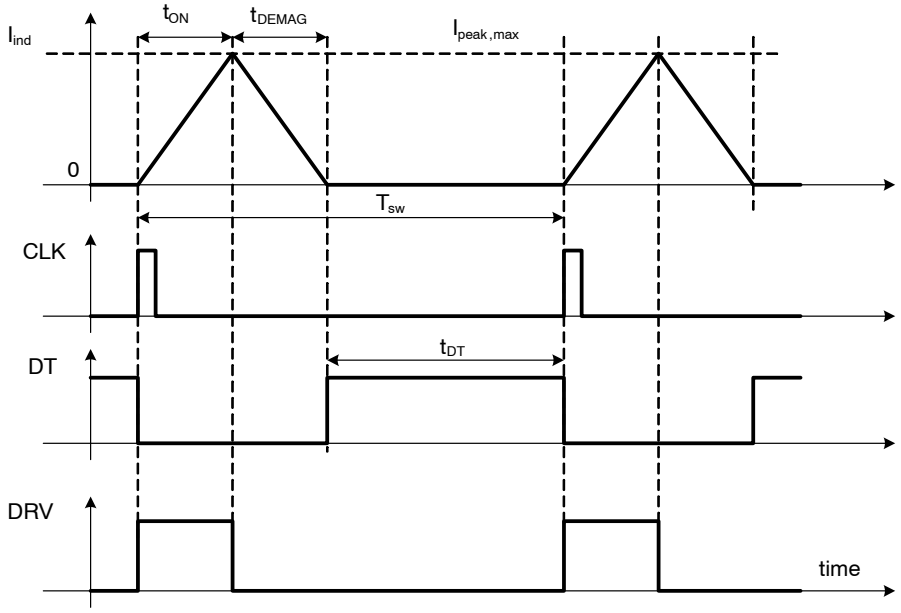


Figure 5. NCL2801 Clock, Dead Time and t_{ON} waveforms

When the output power is at the maximum available for a given application and the inductor peak current limitation is not triggering, VCTRL pin voltage (V_{CTRL}), is above the frequency foldback threshold ($V_{CTRL,th,21}$) making the controller to work in CrM mode. When output power decreases V_{CTRL} will go under the frequency foldback threshold ($V_{CTRL,th,12}$) and DCM mode will be forced by adding dead time as explained before.

Adding dead−time will naturally decrease the switching frequency, hence the FF (standing for Frequency Foldback) which is part of the name VCFF.

The switching frequency in DCM mode is given by the following equation..

$$F_{SW,DCM} = \frac{1}{t_{DT} + t_{ON} + t_{DEMAG}} \qquad \text{(eq. 1)}$$

The value of the external resistor placed between CS pin and R_{sense} will determine the value of the VCTRL pin voltage frequency foldback threshold.

CrM−DCM Threshold

For a given application, R_{sense} and R_{mult} divider ratio of the resistors bridge connected to MULT pin are set such as the maximum power is given just under to the maximum VCTRL pin voltage V_{CTRL} which is 4.5 V. Zero ouput power will be supplied for V_{CTRL}=0.5 V

For adjusting at which V_{CTRL} value the transition from CrM to DCM mode will happen, the resistance value between CS pin and GND will be sensed before start−up and its value stored digitally (see Figure 6). The sensed resistance is equal to R_{CS} plus R_{sense}, but because R_{sense} value is much lower than R_{CS}, it is the R_{CS} value which will be sensed.

This resistor sense will be done after $V_{CC,on}$ level is reached and just before the controller starts switching in order to avoid any noise perturbation the sensing (see Figure 6). The I_{RCS} 1−mA (+/− 4%) current source, active when RCS flag is high will generate a voltage drop through R_{CS} (+/−1%) resistor and this voltage drop will be compared to internal voltage references to identify which is the R_{CS} resistor value and set the internal frequency foldback settings.

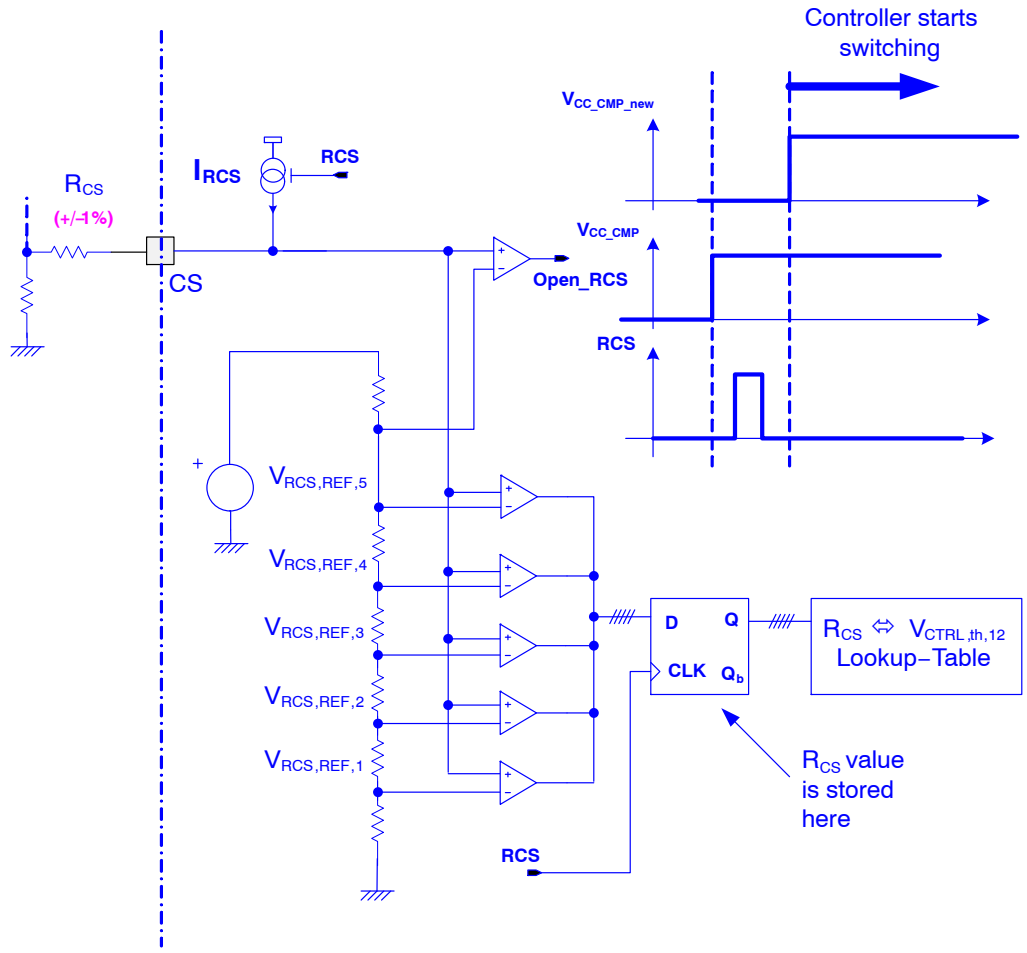


Figure 6. RCS Sensing Method And Schematic

Table 7.

R_{CS} (Ω)	$V_{CTRL,th,12}$ (V)
1000	2.19
620	1.83
330	1.48
150	1.12

gives the digital code used in Figure 6 corresponding to the R_{CS} resistor value which in turn will be used to set the CrM to DCM threshold (when output power is decreasing).

There will be a different DCM to CrM threshold than CrM to DCM making an hysteresis to avoid valley hopping (see Table 7 and Figure 4).

During this R_{CS} identification phase which main purpose is to setting the the frequency foldback thresholds and number of valley for dead time, if it happen that V_{CS} voltage is greater than $V_{RCS,REF,5}$ an OPEN CS pin fault will be triggered and latched disabling the startup of the controller, the fault will be released if VCC pin voltage falls unders $V_{CC,rst}$. On the other hand if it happen that V_{CS} voltage is lower than $V_{RCS,REF,1}$ a SHORT CS pin fault will be triggered and latched disabling the startup of the controller, the fault will be released if VCC pin voltage falls unders $V_{CC,rst}$.

DCM_n−DCM_{n+1} and DCM_{n+1}−DCM_n Transition Hysteresis

As explained before, DCM mode is driven by the number of valleys counted before the power MOSFET turns on.

As shown in Figure 7**,** the forced number of valleys, shown in the Y−axis, depends on 5 VCTRL pin voltage windows,

the X−Axis representing the VCTRL pin voltage. In order to avoid valley hopping due to VCTRL pin voltage ripple, we have included an hysteresis. We can clearly see in Figure

7 that the V_{CTRL} hysteresis voltage is defined by: $V_{CTRL,hyst} = V_{CTRL,th43} - V_{CTRL,th,34}$ and more generally by $V_{CTRL,hyst} = V_{CTRL,th,ij} - V_{CTRL,th,ji}$. If VCTRL pin peak−to−peak ripple voltage stays under $V_{CTRL,hyst}$ there will be no valley hopping.

$V_{CTRL,hyst}$ can be calculated for each frequency foldback option determined by R_{CS} value from the thresholds specified in Table 7. While the hysteresis between two adjacent valley numbers is constant for one frequency foldback option, it decreases for options having a lower CrM to DCM V_{CTRL} threshold. This should not be a problem as the two times mains frequency ripple also decreases when VCTRL pin voltage decreases which results from output power decrease. We can also mention looking at Figure 7 and the specified frequency foldback thresholds of Table 7 that $V_{CTRL,th,56}$ which is the V_{CTRL} threshold at which we force counting 6 valleys, has always the same value. This threshold is also called $V_{CTRL,ADT}$ because when VCTRL pin voltage falls under this threshold, an analog dead−time starts to be added to the dead−time determined by counting 6 valleys. The lower VCTRL pin voltage goes under $V_{CTRL,ADT}$ threshold, the more analog dead time is added. An example on how the analog dead time can be added is shown in the circuit of Figure 4 and the correspond power MOSFET drain voltage is shown in Figure 3.

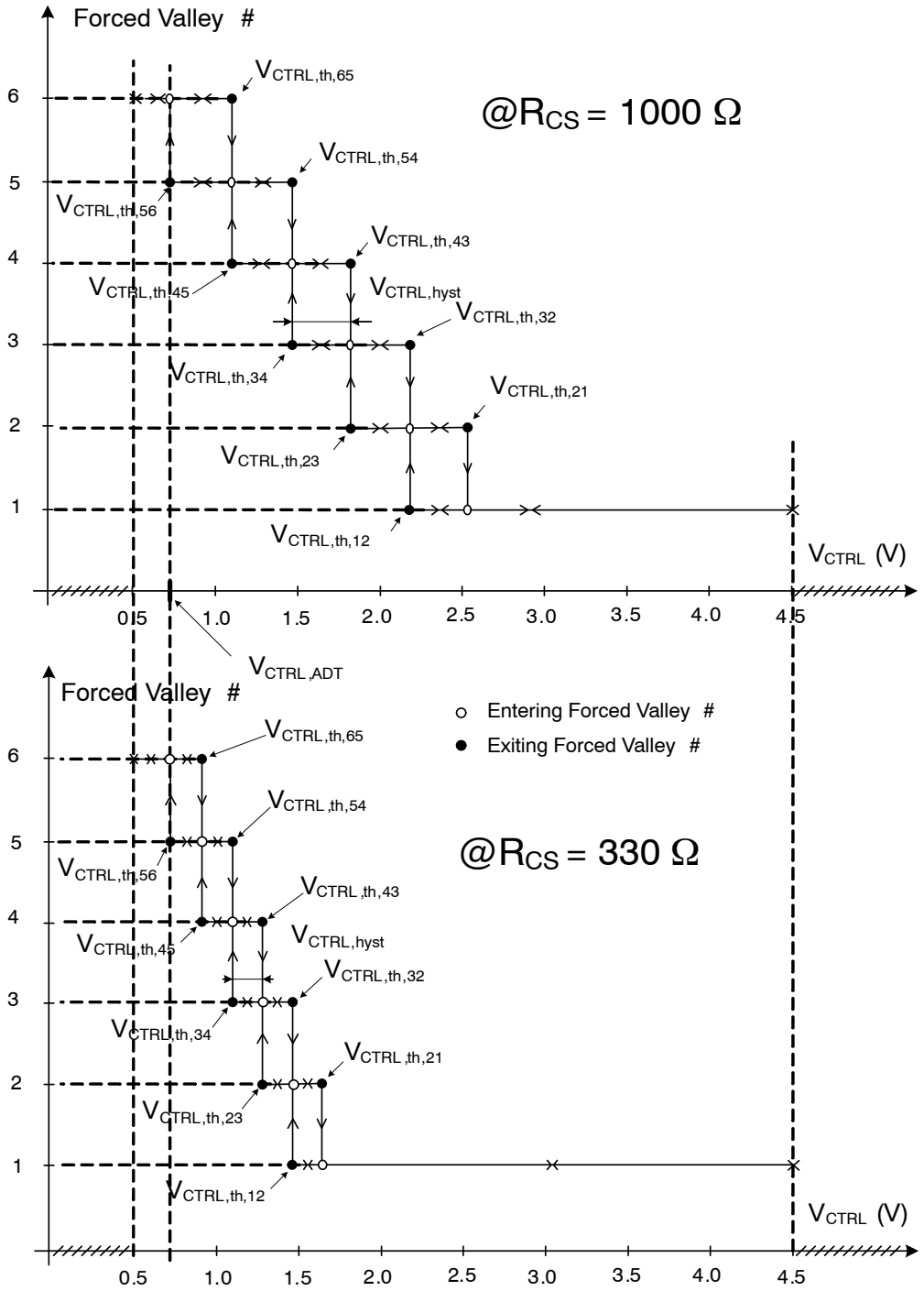


Figure 7. Forced Valley Number versus VCTRL Pin Voltage For a Two Different RCS Values of the Mandatory List {150 Ω, 330 Ω, 620 Ω, 1000 Ω}

NCL2801 On−time Modulation and V_{TON} Processing Circuit

Let's analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is *on*. The slope is (V_{in}/L) where L is the coil inductance. At the end of the on−time (t_1), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is (t_2). In some cases, the system enters then the dead−time (t_3) that lasts until the next clock is generated.

One can show that the ac line current is given by:

$$I_{in} = V_{in}\frac{t_1(t_1 + t_2)}{2TL} \quad \text{(eq. 2)}$$

Where

$$T = t_1 + t_2 + t_3 \quad \text{(eq. 3)}$$

is the switching period and V_{in} is the ac line rectified voltage.

In light of this equation, we immediately note that I_{in} is proportional to V_{in} if $[t_1.(t_1+t_2)/T]$ is a constant.

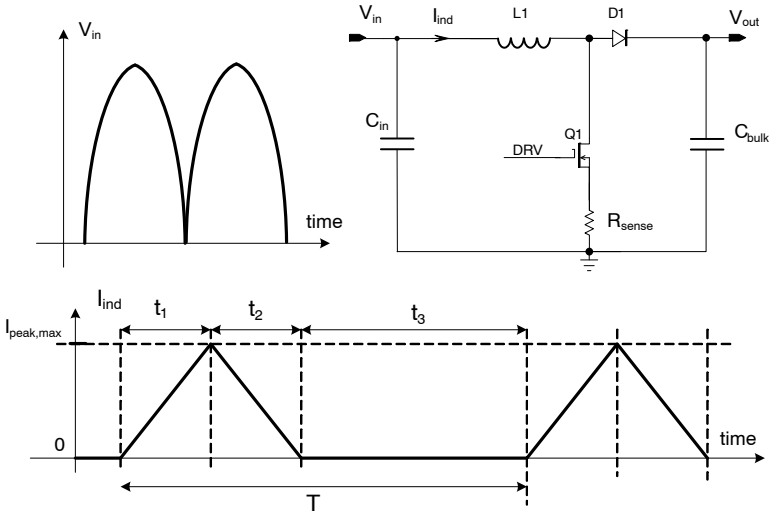


Figure 8. PFC boost converter and Inductor Current in DCM

NCL2801 operates in current control mode. As portrayed by Figure 8 & Figure 10, the MOSFET on−time t_1 results from a current control mode circuitry which is using a dedicated circuitry monitoring V_{ctrl} and dead−time t_3 ensuring $[t_1.(t_1+t_2)/T]$ is constant and as a result making I_{in} proportional to V_{in} (PF=1)

On−time t_1, also called t_{ON}, has a high value clamp called $t_{ON,max}$, generated by an internal circuitry. This 30−μs clamp value is given for maximum VCTRL pin voltage (V_{CTRL}=4.5 V) but reduces down to 5 μs when VCTRL pin voltage reaches 0.5 V which is its minimum value.

The input current is then proportional to the input voltage. Hence, the ac line current is properly shaped.

One can note that this analysis is also valid in the CrM case. This condition is just a particular case of this functioning where (t_3=0), which leads to ($t_1+t_2=T$) and ($V_{ton}=V_{regul}$). That is why the NCL2801 automatically adapts to the conditions and transitions from **DCM_n to DCM_{n+1} and DCM_{n+1} to DCM_n** without power factor degradation and without discontinuity in the power delivery.

This analysis while carried−out for constant on−time architecture is also valid for the current control architecture of the NCL2801 because at steady state, what results from a current control is a constant on−time.

Current Control Mode & THD Enhancer

In order for the mains current to have very good THD, the Current Control Mode depicted in Figure 10 mode is preferred.

To improve the mains current THD, an offset voltage is added to the multiplier output (see Figure 9).

The added offset is equal to $K_{offset}.V_{ton}$

The role of this offset is to add on−time and this added on−time will be very beneficial close to line zero crossing where, without this offset, the inductor peak current is low and comparable to the inductor negative peak current resulting to zero line current. Adding this offset greatly reduces the time width during which the line current is equal to zero (line voltage cross−over distortion) and by doing improve the line current THD.

A traditional scheme, where the inductor current during on−time multiplied by R_{sense} is compared to a scaled down rectified mains voltage V_{in} multiplied by V_{ton} is used. What may sound strange is the V_{ton}, but V_{ton} is equal to V_{regul} when in CrM.

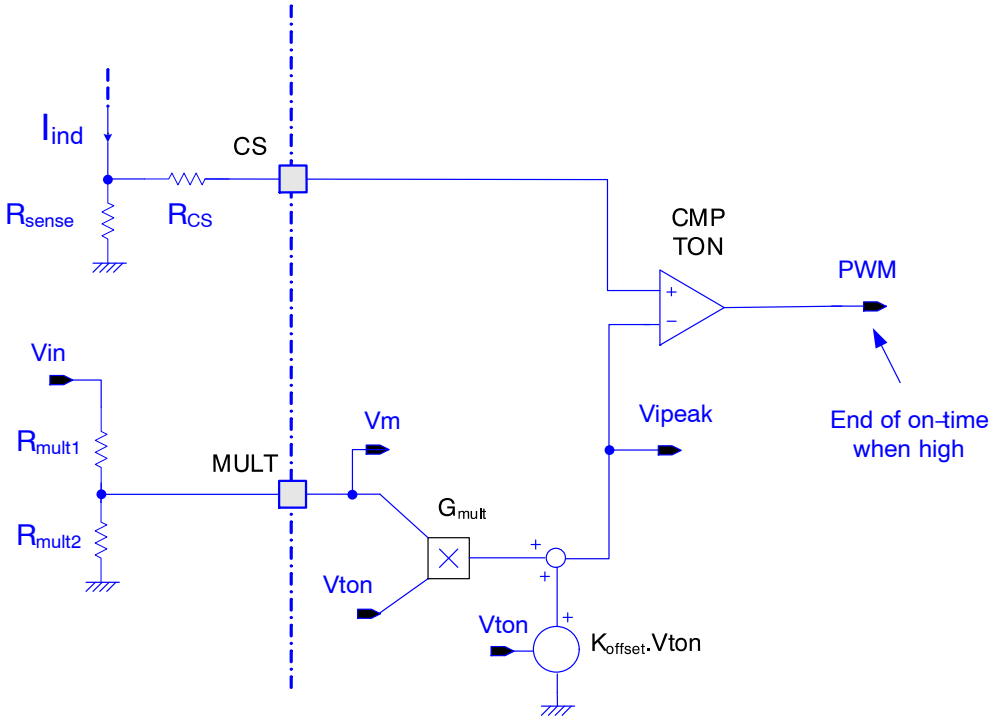


Figure 9. Simplified Current Control Circuit (Max On−Time and Blanking Not Shown)

$$V_{regul} = (V_{VCTRL} - 0.5V)\frac{1.5V}{4.0V} \quad \text{(eq. 4)}$$

The range of V_{regul} is equal to 1.5 V and V_{regul} operates between 0 V and 1.5 V.

The range of V_{CTRL} is equal to 4.0 V and V_{CTRL} operates between 0.5 V and 4.5 V.

In DCM mode, the Vton input of the multiplier is modified thanks to the Vton processing block in order to maintain the mains current proportional to the mains voltage.

It can be demonstrated that the maximum peak inductor current is given by the following equation

$$I_{ind,peak,max} = \frac{V_{ipeak,max}}{R_{sense}} = \frac{\left(K_m K_{mult}\sqrt{2}\,V_{mains,rms} + K_{offset}\right)\cdot V_{TON}}{R_{sense}} \quad \text{(eq. 5)}$$

From $I_{ind,peak,max}$, assuming we are in CrM we can get the rms line current by :

$$I_{mains,rms} = \frac{V_{ind,peak,max}}{2\sqrt{2}} = \frac{\left(K_m K_{mult}\sqrt{2}\,V_{mains,rms} + K_{offset}\right)\cdot V_{TON}}{2\sqrt{2}\,R_{sense}} \quad \text{(eq. 6)}$$

Then,

$$P_{mains,rms} = \frac{(K_m K_{mult}\sqrt{2}\,V^2_{mains,rms} + K_{offset}V_{mains,rms})\cdot V_{TON}}{2\sqrt{2}\,R_{sense}} \quad \text{(eq. 7)}$$

To better see the effect of K_{offset} on $P_{mains,rms}$ the previous equation can be re−written as follows

$$P_{mains,rms} = \frac{K_m K_{mult} V^2_{mains,rms} V_{TON}}{2R_{sense}} + \frac{K_{offset} V_{mains,rms} V_{TON}}{2\sqrt{2}\,R_{sense}} \quad \text{(eq. 8)}$$

In both previous equations K_{mult} is the multiplier gain and K_m is given by the following:

$$K_m = \frac{R_{mult2}}{R_{mult1} + R_{mult2}} \quad \text{(eq. 9)}$$

It is important to mention that in CrM mode so particularly at max output power, V_{TON}=V_{regul}.

The multiplier gain, for product options having no line level detection ([**B]&[**D] has a value which does not vary versus V_{mains} value.

For product options having line level detection ([**A]&[**C], the multiplier gain has an High Line value ($K_{mult,HL}$) and a Low Line value ($K_{mult,LL}$). These two line

level dependent multiplier gain values act as a two−level line feed forward.

NCL2801 Maximum on−time

In order to avoid the on−time to go too high close to line voltage zero crossing, a V_{CTRL} dependent maximum on time circuitry has been added. The on−time limiting values are linearly depending on VCTRL pin voltage as follows:

30−μs @V_{CTRL} = 4.5 V and 5−μs @V_{CTRL} = 0.55 V

NCL2801 Regulation Block and Output Voltage Control

A trans−conductance error amplifier (OTA) with access to its inverting input (FB pin) and to its output pin (VCTRL pin) is provided. It features a typical trans−conductance gain of 200 μS and a maximum current capability of +/−20 μA. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the OTA inverting input (pin FB). Bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. However, it is high enough so that the pin remains in low state if the pin is not connected.

The output of the error amplifier is brought to pin VCTRL for external loop compensation. Typically a type−2 network is applied between pin VCTRL and ground, to set the regulation bandwidth below about 20 Hz and to provide a decent phase boost.

The swing of the error amplifier output is limited within an operating range:

- It is forced above a voltage drop (V_F) by a dedicated circuitry.
- It is clamped not to exceed 4.0 V + the same V_F voltage drop.

The V_F value is 0.5 V typically.

The regulated output voltage V_{bulk} uses an internal reference voltage V_{REF} = 2.5 V.

The regulated V_{bulk} voltage (its average value in case of important ripple) will be equal to V_{REF} multiplied by the dividing factor given by the resistor bridge placed between V_{bulk} and FB pin, resulting for example in V_{bulk} = 395 V.

Given the low bandwidth of the regulation loop, abrupt variations of the load, may result in excessive over or under−shoot. Over−shoot is limited by the Over−Voltage Protection (OVP) connected to FB pin (Feedback).

Optionally, NCL2801 embeds a "**D**ynamic **R**esponse **E**nhancer" circuitry (**DRE**) that limits under−shoots. The DRE works during startup phase by injecting current into the VCTRL pin which rises VCTRL pin voltage and allows more current to charge the bulk capacitor. After the startup phase, when internal PFCOK flag goes high, the DRE is disabled on some options, but is enabled in other product options. For the product options where the DRE is enabled, an internal comparator monitors the FB pin voltage (V_{FB}) and when V_{FB} is lower than 95.5% of its nominal value, it connects the 220−μA current source to VCTRL pin in order to speed−up the charge of the compensation network. Effectively this appears as a 10x increase in the loop gain.

The circuit also detects overshoot using the Soft OVP circuitry and immediately reduces the power delivery when the output voltage exceeds a value which is product option dependent.

The error **O**perational **T**ransconductance **A**mplifier OTA and the OVP and DRE comparators share the same input information. Based on the typical value of their parameters and if $V_{bulk,nom}$ is the bulk nominal voltage value (e.g., 400 V), we can deduce:

- Output Regulation Level: $V_{bulk,nom}$
- Output DRE Level: $V_{bulk,dre}$ = 95.5%.$V_{bulk,nom}$
- Output Soft OVP Level: $V_{bulk,sovp}$ = X%.$V_{bulk,nom}$
- Output Fast OVP level: $V_{bulk,fovp}$ = Y%.$V_{bulk,nom}$

NOTE: Note: X% and Y% are product option dependent

Current Sense and Current Control

The power MOSFET current I_{ind} is sensed during the on−time phase by the resistor R_{sense} inserted between the MOSFET source and ground (see Figure 10). The voltage $R_{sense}.I_{ind}$ after a proper leading edge blanking ($t_{LEB,OCP}$ and $t_{LEB,OVS}$) starting from the power MOSFET rising edge drive signal (DRV) is compared to internal over−current protection (OCP) and overstress protection (OVS) internal references (namely $V_{CS(th)}$ *and* $V_{CS,OVS(th)}$) which when triggered ends the on−time for OCP or stops the switching during 800 us for OVS. The voltage $R_{sense}.I_{ind}$ is also low−pass filtered (R=20 kΩ, C=20 pF see Figure 10), leading edge blanked and compared to the multiplier output voltage to generate the end of the on−time which is typical of a current mode control (see Figure 10).

In order to improve the THD of the mains current, a Vton dependent offset at the output of the multiplier and a TONMAX processing block have been added (see Figure 10).

Vton is one of the inputs of the multiplier for helping improve THD in DCM mode (Frequency Foldback).

Vton is equal to Vregul which is proportional to the VCTRL pin voltage when in CrM mode.

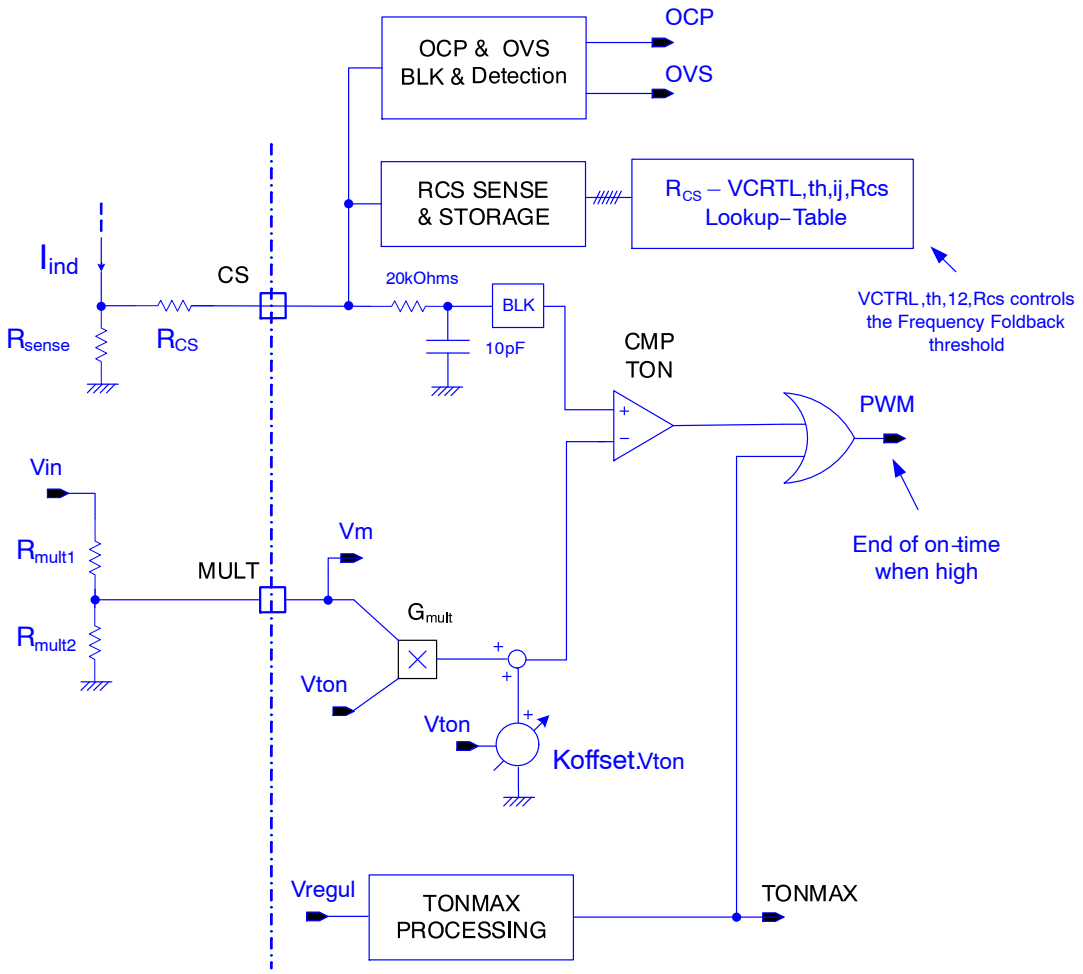


Figure 10. PWM Circuit Showing Current Control Mode With a New MULT Pin

Zero Current Detection (ZCD)

The ZCD pin features a classical and robust ZCD detection based on sensing the auxiliary winding voltage as shown in Figure 11. The ZCD pin voltage is clamped high at V_{CC} plus a diode V_f (0.7 V) and clamped low at minus a diode Vf (−0.7 V) and then compared to ZCD thresholds voltages $V_{ZCD,th,H}$ and $V_{ZCD,th,L}$ (see Table 6).

When no signal is received that triggers the ZCD comparator to indicate the end of inductor demagnetization, an internal 200−μs watchdog timer initiates the next drive pulse.

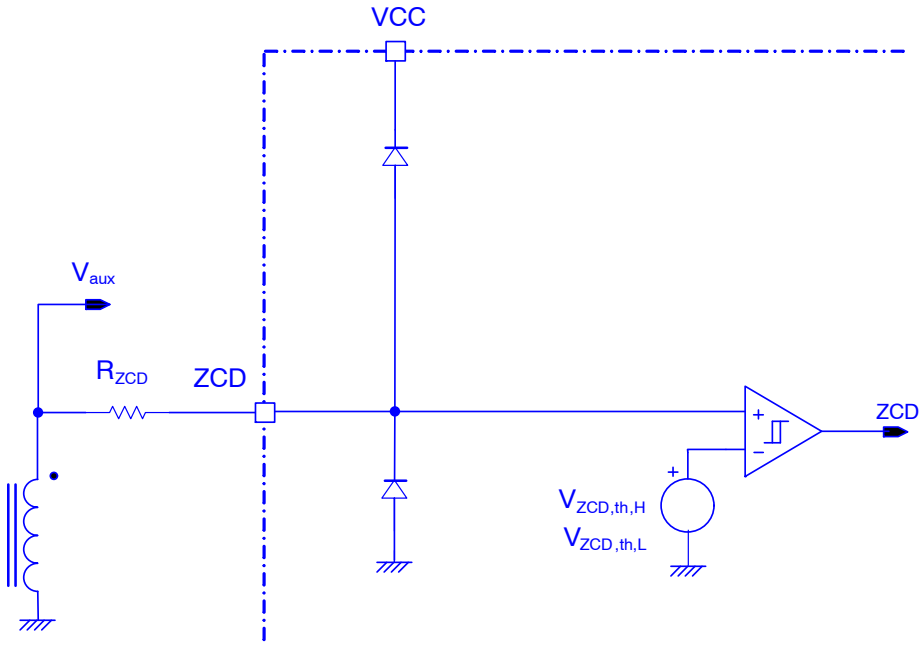


Figure 11. Zero Current Detection (ZCD) Circuitry

Brown−Out Detection) – (Options [A], [**B])**

Thanks to the line voltage scaled−down by K_m and rectified available on MULT−pin (V_m) a Brown−Out feature is available on options [**A], [**B].

$$V_m(t) = K_m \cdot V_{in}(t) \quad \text{(eq. 10)}$$

With

$$K_m = \frac{R_{mult2}}{R_{mult1} + R_{mult2}} \quad \text{(eq. 11)}$$

The V_{MULT} voltage is sensed and when eventually V_{MULT} falls under Brown−out internal reference voltage V_{BOL} for 50 ms, BONOK flag will be set to 1. After BONOK flag is set to 1, drive is not disabled, instead, a 30−μA current source ($I_{VCTRL(BO)}$) is applied to VCTRL pin to gradually reduce V_{CTRL}. As a result, the circuit only stops pulsing when the STATICOVP function is activated. At that moment, the circuit stops switching. This method limits any risk of false triggering.

The input of the PFC stage has some impedance that leads to some sag of the input voltage when the input current is large. If the PFC stage suddenly stops while a high current is drawn from the mains, the abrupt decay of the current may make the input voltage rise and the circuit detect a correct line level. Instead, the gradual decrease of V_{CTRL} avoids a line current discontinuity and limits the risk of false triggering.

The line voltage ($V_{line,BO,H}$) at which the controller starts switching which can be called **brown−in** and is given by the following equation:

$$V_{line,BO,H} = V_{line,Brown-in} = \frac{V_{BOH}}{K_m \sqrt{2}} \quad \text{(eq. 12)}$$

The line voltage ($V_{line,BO,L}$) at which the controller starts reducing on−time until it stops switching which can be called **brown−out** and is given by:

$$V_{line,BO,L} = V_{line,Brown-in} = \frac{V_{BOL}}{K_m \sqrt{2}} \quad \text{(eq. 13)}$$

It has to be reminded that while changing K_m by changing the R_{mult} resistors dividing ratio can help to shift up or down the line brown−in and brown−out levels, K_m determines also the internal gain of the controller, together with R_{sense} and K_{mult} (multiplier gain), so care must be taken at adjusting R_{sense} accordingly to the K_m adjustment.

Line Level Detection and 2−Level Line Feed−Forward− (Options [A], [**C])**

For product options [**A], [**C], the line level detection (High Line or Low Line) feature together with a two−level line feed forward is activated and operates as described here after.

MULT pin voltage V_{MULT} is used to sense the line voltage and apply a two−level line feed−forward.

The V_{MULT} voltage is compared to a V_{HL} internal voltage reference. If V_{MULT} exceeds V_{HL}, the circuit detects a High−Line state (LLINE flag is set to 0) and the multiplier gain is set to value corresponding to High Line which is $K_{mult,HL}$. Once this occurs, if V_{MULT} remains below V_{LL} for 25 ms, the circuit detects a Low−Line state ($V_{HL(hyst)}$ hysteresis) and the multiplier gain is set to $K_{mult,LL}$.

At startup, the circuit is in High−Line state (LLINE flag is set to 0) and then V_{MULT} will be used to determine the High−Line or Low−Line state.

The line range detection circuit allows more optimal loop gain control for universal (wide input mains) applications by adjusting the multiplier gain value versus line voltage status (High Line or Low Line).

For the options [**B], [**D], no line feedforward action is taken based on the line level and the multiplier gain remains set at K_{mult} whatever line level.

The High Line and Low Line thresholds, respectively $V_{line,HL}$ and $V_{line,LL}$ are given by the following equations:

$$V_{line,HL,rms} = \frac{V_{HL}}{K_m \sqrt{2}} \quad \text{(eq. 14)}$$

$$V_{line,LL,rms} = \frac{V_{LL}}{K_m \sqrt{2}} \quad \text{(eq. 15)}$$

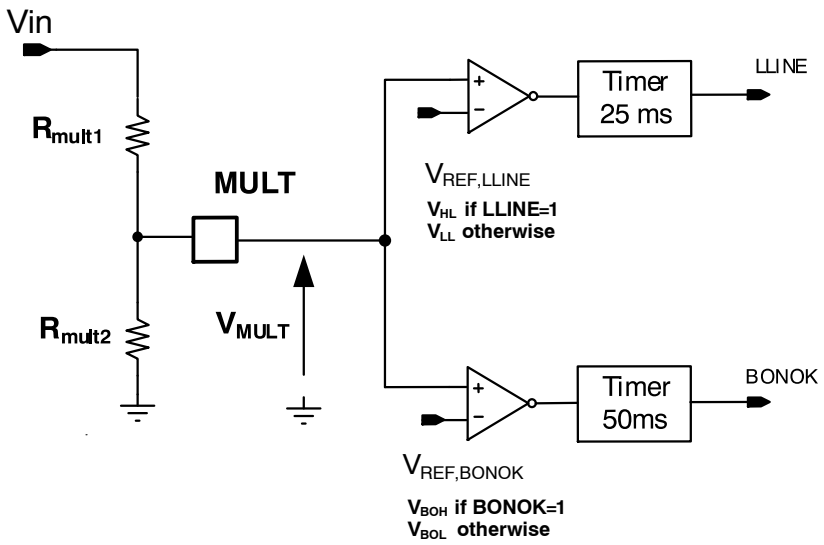


Figure 12. Input Line Sense and Brown−out Monitoring

Thermal Shut−Down (TSD)

An internal circuitry sensing the silicon temperature disables the circuit gate drive and keeps the power switch off when the junction temperature exceeds 150°C. The output stage is then enabled once the temperature drops below about 100°C (50°C hysteresis).

The temperature shutdown remains active as long as the circuit is not reset, that is, as long as V_{CC} is higher than a reset threshold.

Output Drive Section

The output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. Its high current capability (−500 mA/+800 mA) allows it to effectively drive high gate charge power MOSFET.

OFF Mode

As previously mentioned, the circuit turns off when one of the following faults is detected:

- Incorrect feeding of the circuit (“UVLO” high when V_{CC}<$V_{CC(off)}$, $V_{CC(off)}$).
- Excessive die temperature detected by the thermal shutdown
- STATICOVP (see Figure 2)

Generally speaking, the circuit turns off when the conditions are not proper for desired operation. In this mode, the controller stops operating. The major part of the circuit sleeps and its consumption is minimized.

More specifically, when the circuit is in OFF state:

- The drive output is kept low
- All the blocks are off except:
  - The UVLO circuitry that keeps monitoring the V_{CC} voltage and controlling the start−up current source accordingly.
  - The TSD (thermal shutdown)
- V_{ctrl} is grounded so that when the fault is removed, the device starts−up under the soft start mode.
- The internal “PFCOK” signal is grounded.
- The output of the “V_{ton} processing block” is grounded

Failure detection

When manufacturing a power supply, elements can be accidently shorted or improperly soldered. Such failures can also happen to occur later on because of the components fatigue or excessive stress, soldering defaults or external interactions. In particular, adjacent pins of controllers can be shorted; a pin can be grounded or badly connected. Such open/short situations are generally required not to cause fire, smoke or hazardous conditions. NCL2801 integrate functions that ease meeting this requirement. Among them, we can list:

- Fault of the GND connection
  If the GND pin is not connected, internal circuitry detects it and if such a fault is detected for 200 μs, the circuit stops operating.
- Fault of the FB connection
  If the FB pin is left open because for example of bad

soldering, an internal pull down current source pulls down the FB voltage under the UVP threshold and the controller is turned off.

- Detection the ZCD pin improper connection
  If the ZCD pin is floating or shorted to GND it is detected by internal circuitry and the circuit stops operating.
- Boost or bypass diode short

The controller addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty−cycle operation until the fault is gone.

Table 8. NCL2801 ORDERING TABLE

Ordering Part No.	Soft OVP	Fast OVP (%)	V_{CC} Start (V)	DRE (after start)	DRE (during start)	Brown Out	Line Range Detect	Package	Shipping
NCL2801CDADR2G	X	107	12.5	X	X	X	X	SOIC−8 (Pb−Free)	2500/Tape & Reel
NCL2801CDBDR2G	X	107	12.5	X	X	X			
NCL2801CFADR2G	X	107	10.5	X	X	X	X		

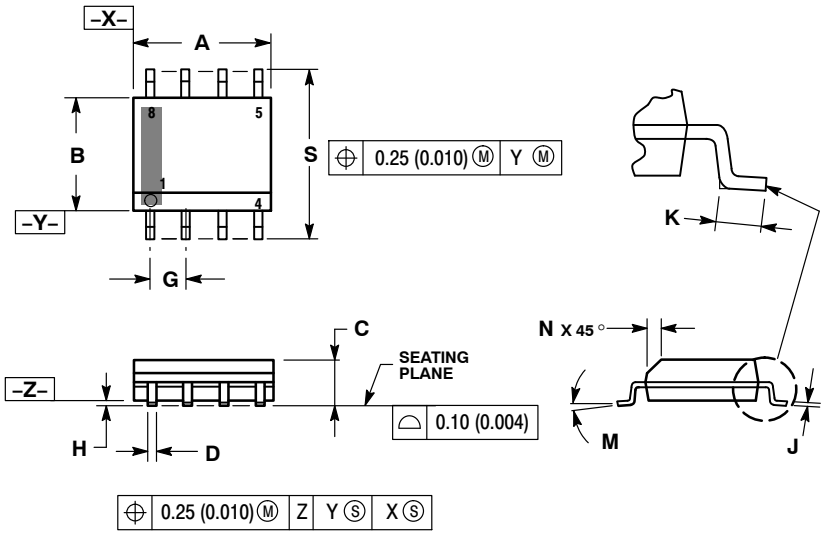
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

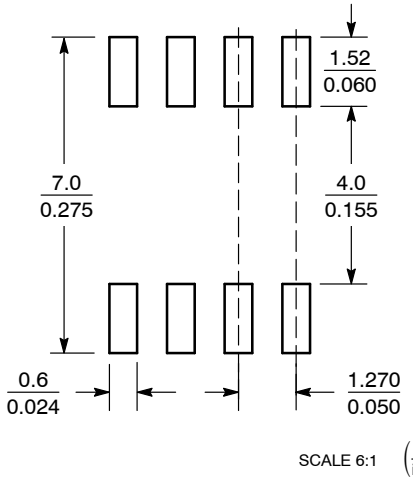
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

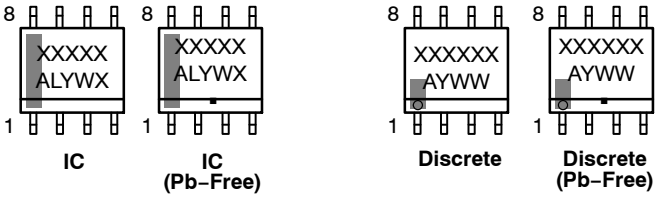
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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