NB4N855S

3.3 V, 1.5 Gb/s Dual AnyLevel™ to LVDS Receiver/Driver/Buffer/ Translator

ON Semiconductor®

http://onsemi.com

Description

NB4N855S is a clock or data Receiver/Driver/Buffer/Translator capable of translating AnyLevel input signal (LVPECL, CML, HSTL, LVDS, or LVTTL/LVCMOS) to LVDS. Depending on the distance, noise immunity of the system design, and transmission line media, this device will receive, drive or translate data or clock signals up to 1.5 Gb/s or 1.0 GHz, respectively. This device is pin−for−pin plug in compatible to the SY55855V in a 3.3 V applications.

The NB4N855S has a wide input common mode range of GND + 50 mV to V_{CC} − 50 mV. This feature is ideal for translating differential or single−ended data or clock signals to 350 mV typical LVDS output levels.

The device is offered in a small 10 lead MSOP package. NB4N855S is targeted for data, wireless and telecom applications as well as high speed logic interface where jitter and package size are main requirements.

Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Guaranteed Input Clock Frequency up to 1.0 GHz
- Guaranteed Input Data Rate up to 1.5 Gb/s
- 490 ps Maximum Propagation Delay
- 1.0 ps Maximum RMS Jitter
- 180 ps Maximum Rise/Fall Times
- Single Power Supply; V_{CC} = 3.3 V ±10%
- Temperature Compensated TIA/EIA−644 Compliant LVDS Outputs
- GND + 50 mV to V_{CC} − 50 mV V_{CMR} Range
- Pb−Free Package is Available

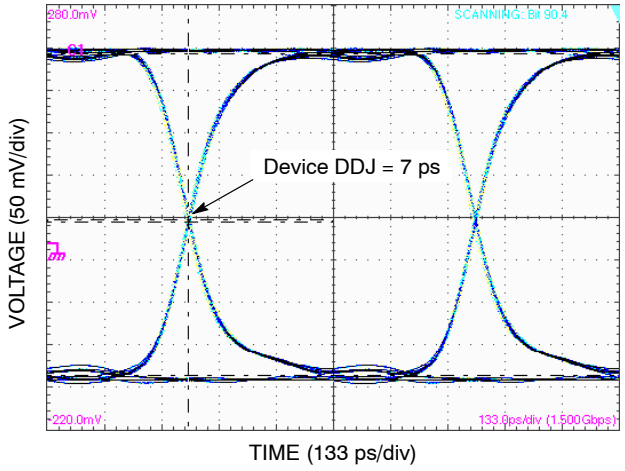
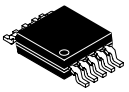
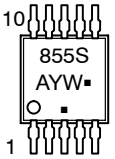


Figure 1. Typical Output Waveform at 1.5 Gb/s with K28.5 (V_{INPP} = 100 mV, Input Signal DDJ = 24 ps)



Micro−10
M SUFFIX
CASE 846B

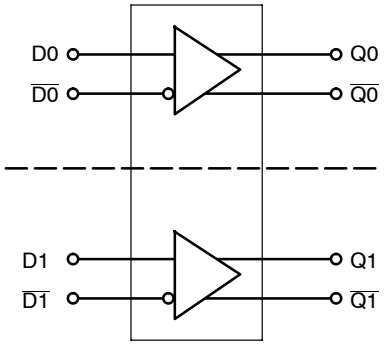
MARKING DIAGRAM*



A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.



Functional Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

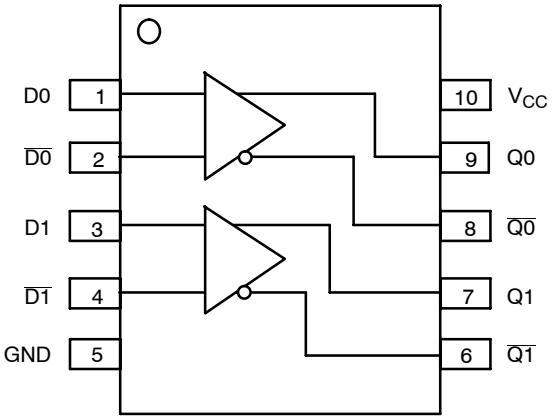


Figure 2. Pin Configuration and Block Diagram (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	D0	LVPECL, CML, LVCMOS, LVTTL, LVDS	Noninverted Differential Clock/Data D0 Input.
2	$\overline{D0}$	LVPECL, CML, LVCMOS, LVTTL, LVDS	Inverted Differential Clock/Data $\overline{D0}$ Input.
3	D1	LVPEL, CML, LVDS LVCMOS, LVTTL	Noninverted Differential Clock/Data D1 Input.
4	$\overline{D1}$	LVPECL, CML, LVDS LVCMOS LVTTL	Inverted Differential Clock/Data $\overline{D1}$ Input.
5	GND	–	Ground. 0 V.
6	$\overline{Q1}$	LVDS Output	Inverted $\overline{Q1}$ output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
7	Q1	LVDS Output	Noninverted Q1 output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
8	$\overline{Q0}$	LVDS Output	Inverted $\overline{Q0}$ output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
9	Q0	LVDS Output	Noninverted Q0 output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
10	V_{CC}	–	Positive Supply Voltage.

Table 2. ATTRIBUTES

Characteristics		Value	
Moisture Sensitivity (Note 1)		Pb Pkg	Pb−Free Pkg
	Micro−10	Level 1	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 1 kV	
Transistor Count		281	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		3.8	V
V_I	Positive Input	GND = 0 V	$V_I = V_{CC}$	3.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		35 70	mA mA
I_{OSC}	Output Short Circuit Current Line−to−Line (Q to $\overline{Q}$) Line−to−End (Q or $\overline{Q}$ to GND)	 Q or $\overline{Q}$ to GND Q to $\overline{Q}$	 Continuous Continuous	 12 24	mA
T_A	Operating Temperature Range	Micro−10		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 2)	0 lfpm 500 lfpm	Micro−10 Micro−10	177 132	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	1S2P (Note 4)	Micro−10	40	°C/W
T_{sol}	Wave Solder Pb Pb−Free	<3 Sec @ 248°C <3 Sec @ 260°C		265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 1S2P (1 signal, 2 power).

Table 4. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS V_{CC} = 3.0 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Note 3)		40	53	mA
DIFFERENTIAL INPUTS DRIVEN SINGLE−ENDED (Figures 10 and 12)					
V_{th}	Input Threshold Reference Voltage Range (Note 4)	GND +100		V_{CC} − 100	mV
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	GND		V_{th} − 100	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 11 and 13)					
V_{IHD}	Differential Input HIGH Voltage	100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{CC} − 100	mV
V_{CMR}	Input Common Mode Range (Differential Configuration)	GND + 50		V_{CC} − 50	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	100		V_{CC}	mV
LVDS OUTPUTS (Note 5)					
V_{OD}	Differential Output Voltage	250		450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States (Note 6)	0	1.0	25	mV
V_{OS}	Offset Voltage (Figure 9)	1125		1375	mV
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States (Note 6)	0	1.0	25	mV
V_{OH}	Output HIGH Voltage (Note 7)		1425	1600	mV
V_{OL}	Output LOW Voltage (Note 8)	900	1075		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Dx/$\overline{Dx}$ at the DC level within V_{CMR} and output pins loaded with R_L = 100 Ω across differential.
4. V_{th} is applied to the complementary input when operating in single−ended mode.
5. LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 8.
6. Parameter guaranteed by design verification not tested in production.
7. V_{OH}max = V_{OS}max + ½ V_{OD}max.
8. V_{OL}max = V_{OS}min − ½ V_{OD}max.

Table 5. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V; (Note 9)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPMIN}$) $f_{in} \le 1.0$ GHz (Figure 3) $f_{in} = 1.5$ GHz	230 200	350 300		230 200	350 300		230 200	350 300		mV
f_{DATA}	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s
t_{PLH}, t_{PHL}	Differential Input to Differential Output Propagation Delay	330	410	490	330	410	490	330	410	490	ps
t_{SKEW}	Duty Cycle Skew (Note 10) Within −Device Skew (Note 11) Device to Device Skew (Note 12)		8 10 20	45 35 100		8 10 20	45 35 100		8 10 20	45 35 100	ps
t_{JITTER}	RMS Random Clock Jitter (Note 13) f_{in} = 1.0 GHz f_{in} = 1.5 GHz Deterministic Jitter (Note 14) f_{DATA} = 622 Mb/s f_{DATA} = 1.5 Gb/s f_{DATA} = 2.488 Gb/s Crosstalk Induced Jitter (Note 15)		0.5 0.5 6 7 10 20	1 1 15 20 25 40		0.5 0.5 6 7 10 20	1 1 15 20 25 40		0.5 0.5 6 7 10 20	1 1 15 20 25 40	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 16)	100		V_{CC}− GND	100		V_{CC}− GND	100		V_{CC}− GND	mV
t_r t_f	Output Rise/Fall Times @ 250 MHz Q, $\overline{Q}$ (20% − 80%)	50	110	180	50	110	180	50	110	180	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Measured by forcing $V_{INPPMIN}$ with 50% duty cycle clock source and V_{CC} − 1400 mV offset. All loading with an external R_L = 100 Ω across "D" and "$\overline{D}$" of the receiver. Input edge rates 150 ps (20%−80%).
10. See Figure 7 differential measurement of $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform @ 250 MHz.
11. The worst case condition between Q0/$\overline{Q0}$ and Q1/$\overline{Q1}$ from either D0/$\overline{D0}$ or D1/$\overline{D1}$, when both outputs have the same transition.
12. Skew is measured between outputs under identical transition @ 250 MHz.
13. RMS jitter with 50% Duty Cycle clock signal.
14. Deterministic jitter with input NRZ data at PRBS 2^{23}−1 and K28.5.
15. Crosstalk Induced Jitter is the additive Deterministic jitter to channel one with channel two active both running at 622 Gb/s PRBS 2^{23} −1 as an asynchronous signals.
16. Input voltage swing is a single−ended measurement operating in differential mode.

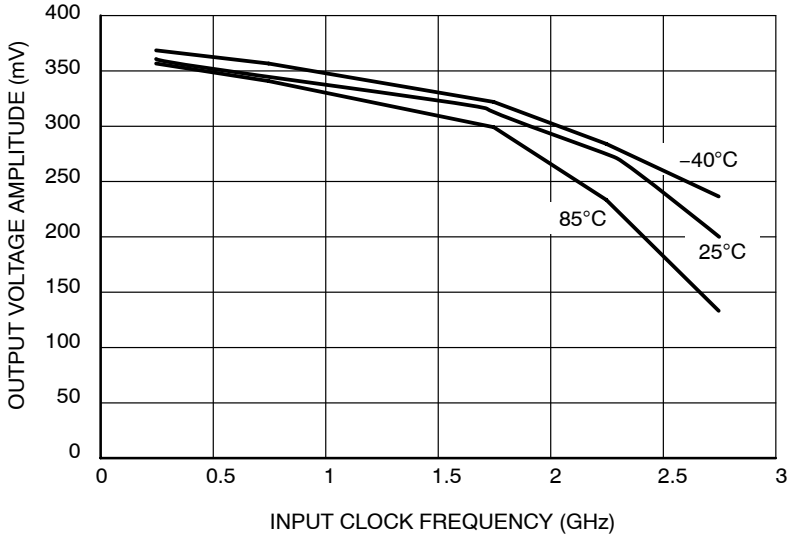


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) and Temperature (@ V_{CC} = 3.3 V)

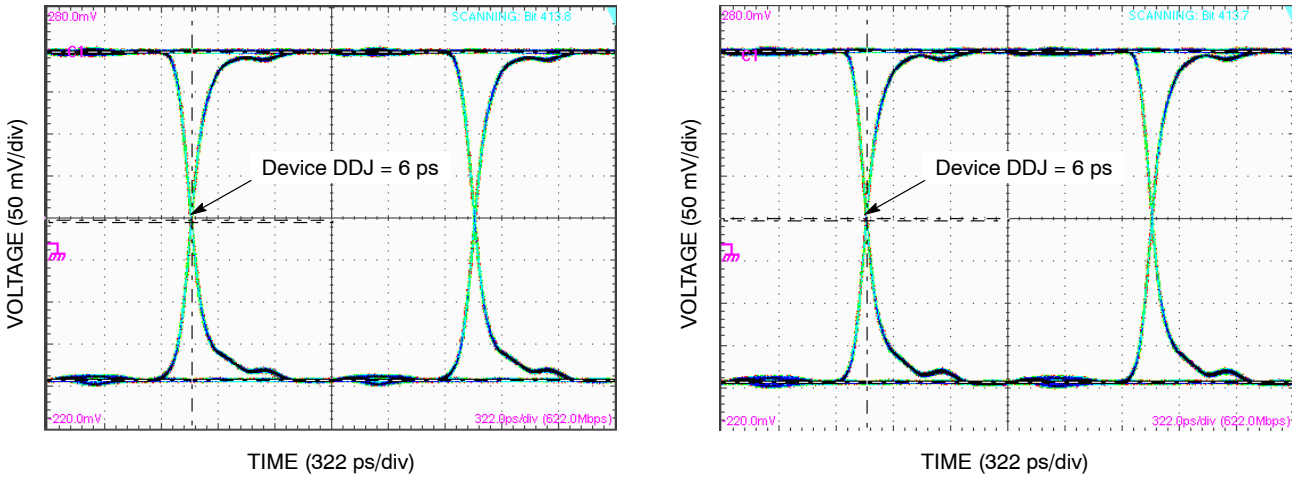


Figure 4. Typical Output Waveform at 1.5 Gb/s with 2^{23-1} (V_{INPP} = 100 mV (left) & V_{INPP} = 400 mV (right), Input Signal DDJ = 24 ps)

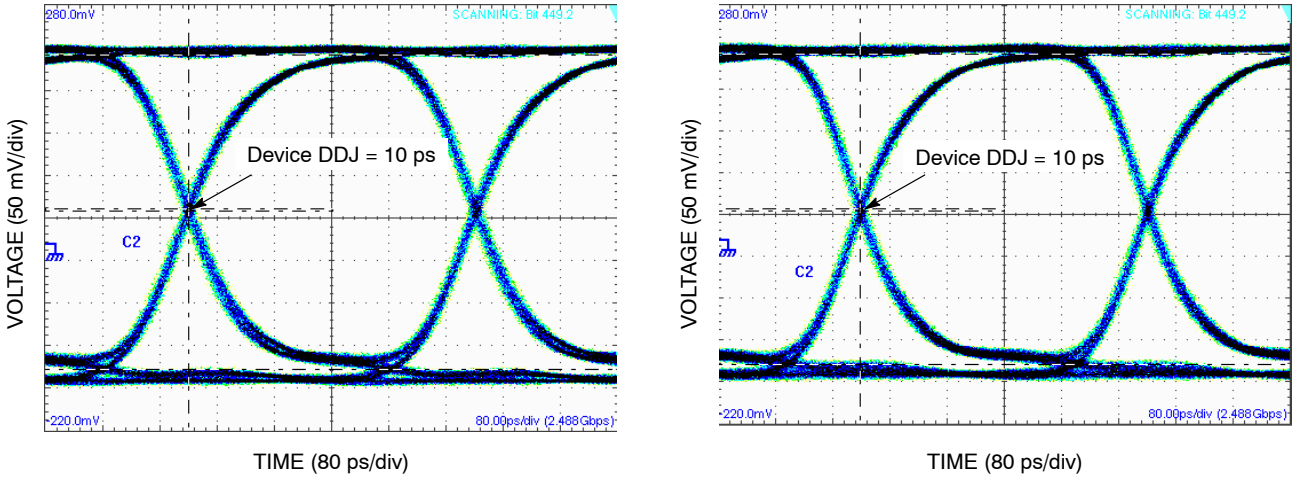


Figure 5. Typical Output Waveform at 2.488 Gb/s with 2^{23-1} (V_{INPP} = 100 mV (left) & V_{INPP} = 400 mV (right), Input Signal DDJ = 30 ps)

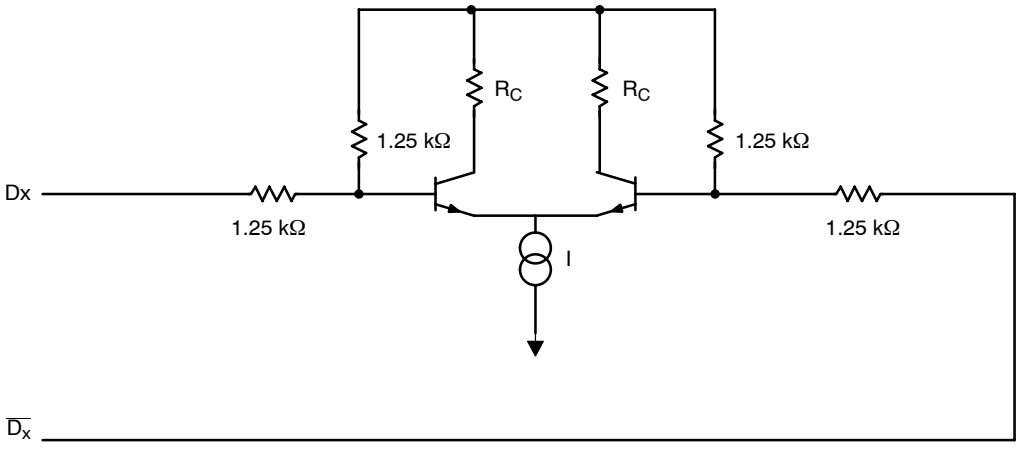


Figure 6. Input Structure

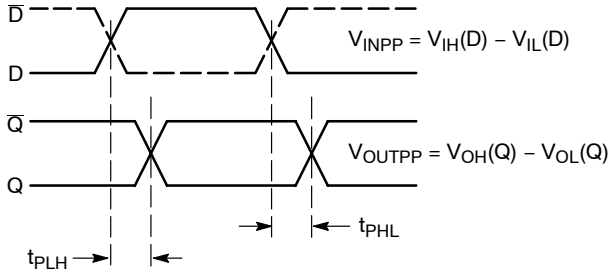


Figure 7. AC Reference Measurement

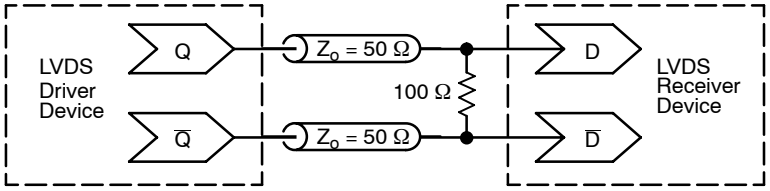


Figure 8. Typical LVDS Termination for Output Driver and Device Evaluation

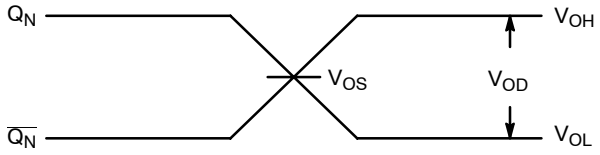


Figure 9. LVDS Output

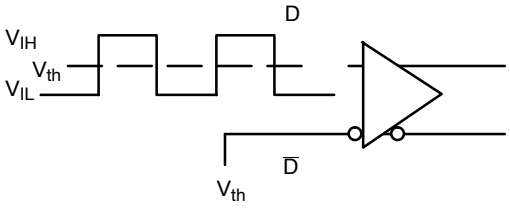


Figure 10. Differential Input Driven Single−Ended

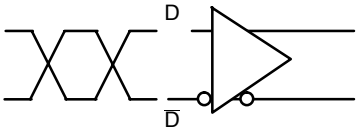


Figure 11. Differential Inputs Driven Differentially

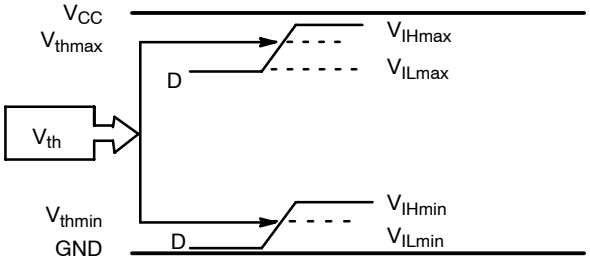


Figure 12. V_{th} Diagram

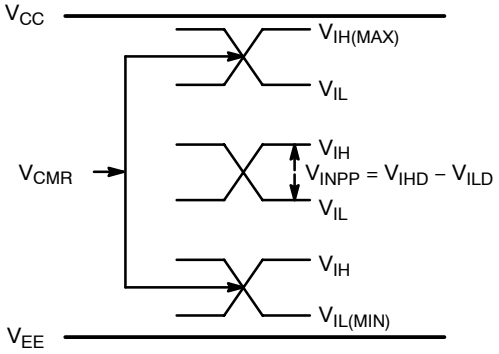


Figure 13. V_{CMR} Diagram

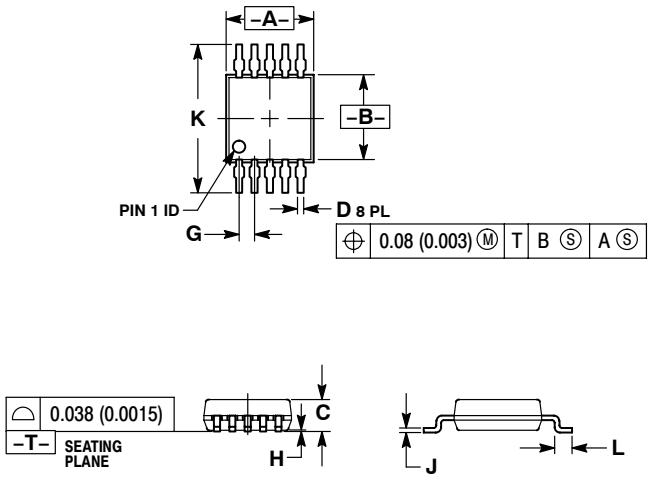
ORDERING INFORMATION

Device	Package	Shipping†
NB4N855SMR4	Micro−10	1000 / Tape & Reel
NB4N855SMR4G	Micro−10 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

PACKAGE DIMENSIONS

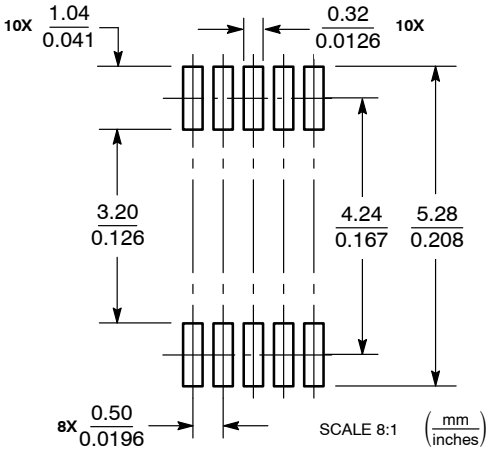
Micro−10
CASE 846B−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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