

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed primarily for CW large-signal output and driver applications at 2450 MHz. Devices are suitable for use in industrial, medical and scientific applications.

- Typical CW Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1} = 55$  mA,  $I_{DQ2} = 195$  mA,  $P_{out} = 25$  Watts CW,  $f = 2450$  MHz  
 Power Gain — 27.7 dB  
 Power Added Efficiency — 43.8%
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2450 MHz, 25 Watts CW Output Power

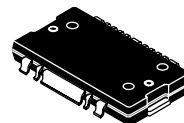
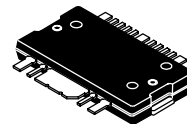
### Features

- Qualified Up to a Maximum of 28  $V_{DD}$  Operation
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- Excellent Thermal Stability
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

**MW7IC2425NR1**  
**MW7IC2425GNR1**  
**MW7IC2425NBR1**

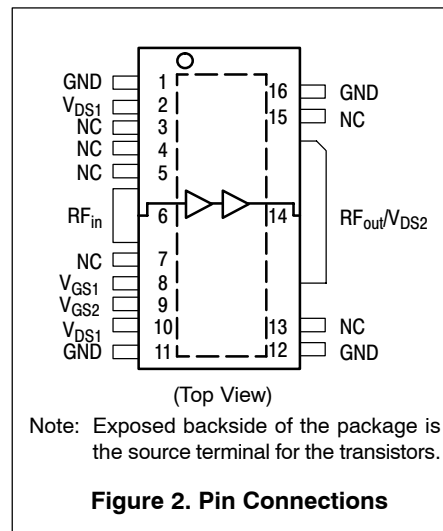
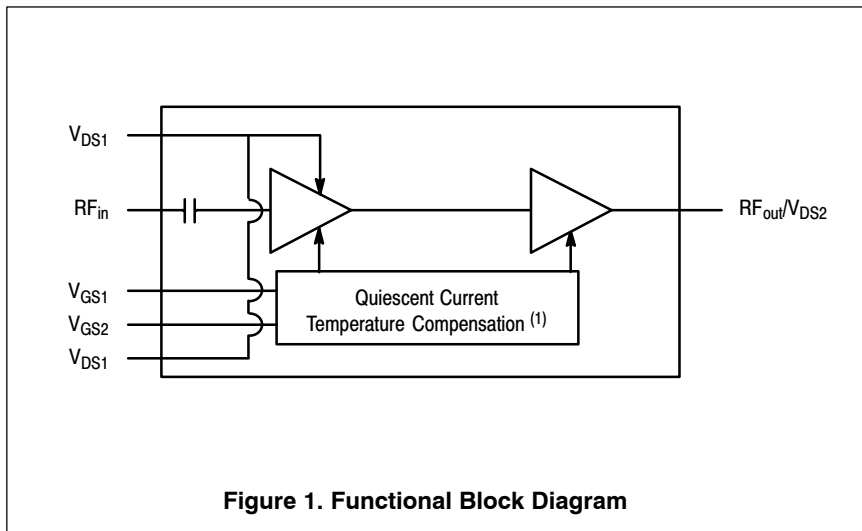
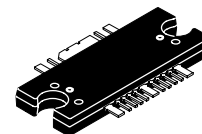
**2450 MHz, 25 W CW, 28 V**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**

**CASE 1886-01**  
**TO-270 WB-16**  
**PLASTIC**  
**MW7IC2425NR1**



**CASE 1887-01**  
**TO-270 WB-16 GULL**  
**PLASTIC**  
**MW7IC2425GNR1**

**CASE 1329-09**  
**TO-272 WB-16**  
**PLASTIC**  
**MW7IC2425NBR1**



1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	- 65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C
Input Power	$P_{in}$	20	dBm

**Table 2. Thermal Characteristics** (In Freescale Narrowband Test Fixture)

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case (Case Temperature 80°C, $P_{out} = 25$ W CW)	$R_{\theta JC}$	6.1 1.2	°C/W
		Stage 1, 28 Vdc, $I_{DQ1} = 55$ mA	
		Stage 2, 28 Vdc, $I_{DQ2} = 195$ mA	

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	II (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Stage 1 - Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 1 - On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 20$ $\mu\text{Adc}$ )	$V_{GS(th)}$	1.2	1.9	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28$ Vdc, $I_{DQ1} = 55$ mA) (4)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_{DQ1} = 55$ mA) (4,5)	$V_{GG(Q)}$	10.3	11.2	12.6	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Measured in Freescale Narrowband Test Fixture.
5. See Appendix A for functional test measurements and test fixture.

(continued)

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 2 - Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 2 - On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 80\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.2	1.9	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2} = 195\text{ mAdc}$ ) (1)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2} = 195\text{ mAdc}$ ) (1,2)	$V_{GG(Q)}$	9.5	10.5	11.5	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 800\text{ mAdc}$ )	$V_{DS(on)}$	0.15	0.47	0.8	Vdc

**Stage 2 - Dynamic Characteristics** (3)

Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	111	—	pF
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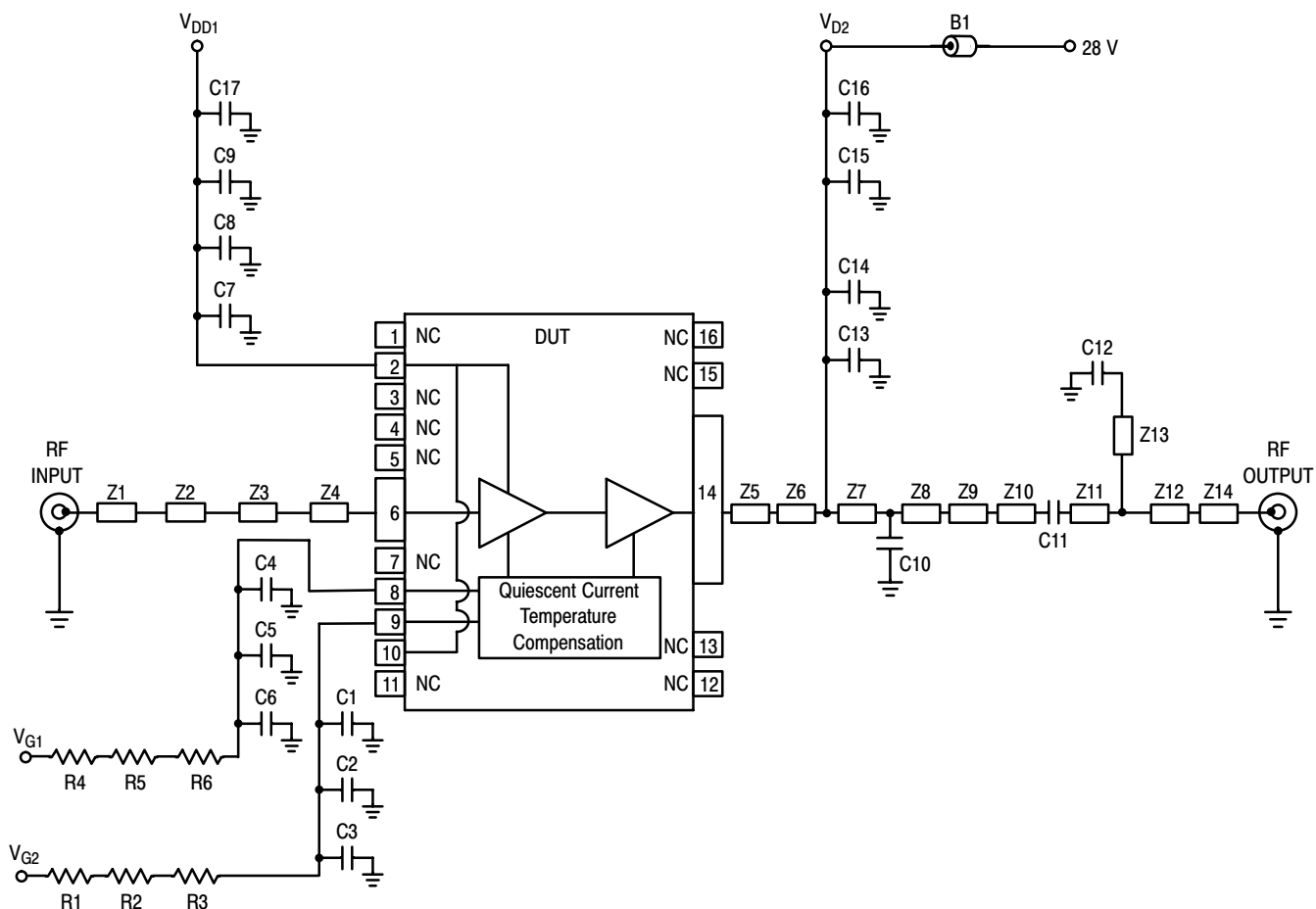
**Narrowband Performance Specifications** (4) (In Freescale Narrowband Test Fixture, (2) 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 55\text{ mA}$ ,  $I_{DQ2} = 195\text{ mA}$ ,  $P_{out} = 25\text{ W CW}$ ,  $f = 2450\text{ MHz}$

Power Gain	$G_{ps}$	25.5	27.7	30.5	dB
Power Added Efficiency	PAE	41.5	43.8	—	%
Input Return Loss	IRL	—	-18	-10	dB

**Functional Tests** (2) (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 77\text{ mA}$ ,  $I_{DQ2} = 275\text{ mA}$ ,  $P_{out} = 4\text{ W Avg.}$ ,  $f = 2700\text{ MHz}$ , WiMAX, OFDM 802.16d, 64 QAM  $3/4$ , 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF. ACPR measured in 1 MHz Channel Bandwidth @  $\pm 8.5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	25.5	28.5	30.5	dB
Power Added Efficiency	PAE	15	17	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	—	9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-50	-46	dBc
Input Return Loss	IRL	—	-15	-10	dB

1. Measured in Freescale Narrowband Test Fixture.
2. See Appendix A for functional test fixture documentation.
3. Part internally matched both on input and output.
4. Measurement made with device in straight lead configuration before any lead forming operation is applied.



- |    |                                |      |  |
|----|--------------------------------|------|--|
| Z1 | 0.500" x 0.027" Microstrip     | Z9   | 0.040" x 0.061" Microstrip                   |
| Z2 | 0.075" x 0.127" Microstrip     | Z10  | 0.020" x 0.050" Microstrip                   |
| Z3 | 1.640" x 0.027" Microstrip     | Z11  | 0.050" x 0.050" Microstrip                   |
| Z4 | 0.100" x 0.042" Microstrip     | Z12  | 0.050" x 0.027" Microstrip                   |
| Z5 | 0.151" x 0.268" Microstrip     | Z13* | 0.338" x 0.020" Microstrip                   |
| Z6 | 0.025" x 0.268" x 0.056" Taper | Z14  | 1.551" x 0.027" Microstrip                   |
| Z7 | 0.100" x 0.056" Microstrip     | PCB  | Rogers R04350B, 0.0133", $\epsilon_r = 3.48$ |
| Z8 | 0.306" x 0.056" Microstrip     |      |  |
- \* Line length includes microstrip bends

**Figure 3. MW7IC2425NR1 (GNR1)(NBR1) Narrowband Test Circuit Schematic**

**Table 6. MW7IC2425NR1 (GNR1)(NBR1) Narrowband Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
B1	47 $\Omega$ , 100 MHz Short Ferrite Bead	2743019447	Fair-Rite
C1, C4, C7, C12, C15	6.8 pF Chip Capacitors	ATC600S6R8CT250XT	ATC
C2, C5, C8, C13	10 nF Chip Capacitors	C0603C103J5RAC	Kemet
C3, C6, C9, C14	1 $\mu$ F, 50 V Chip Capacitors	GRM32RR71H105KA01B	Murata
C10	2.4 pF Chip Capacitor	ATC600S2R4BT250XT	ATC
C11	3.3 pF Chip Capacitor	ATC600S3R3BT250XT	ATC
C16, C17	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88B	Murata
R1, R4	12 K $\Omega$ , 1/4 W Chip Resistors	CRCW12061202FKEA	Vishay
R2, R3, R5, R6	1 K $\Omega$ , 1/4 W Chip Resistors	CRCW12061001FKEA	Vishay

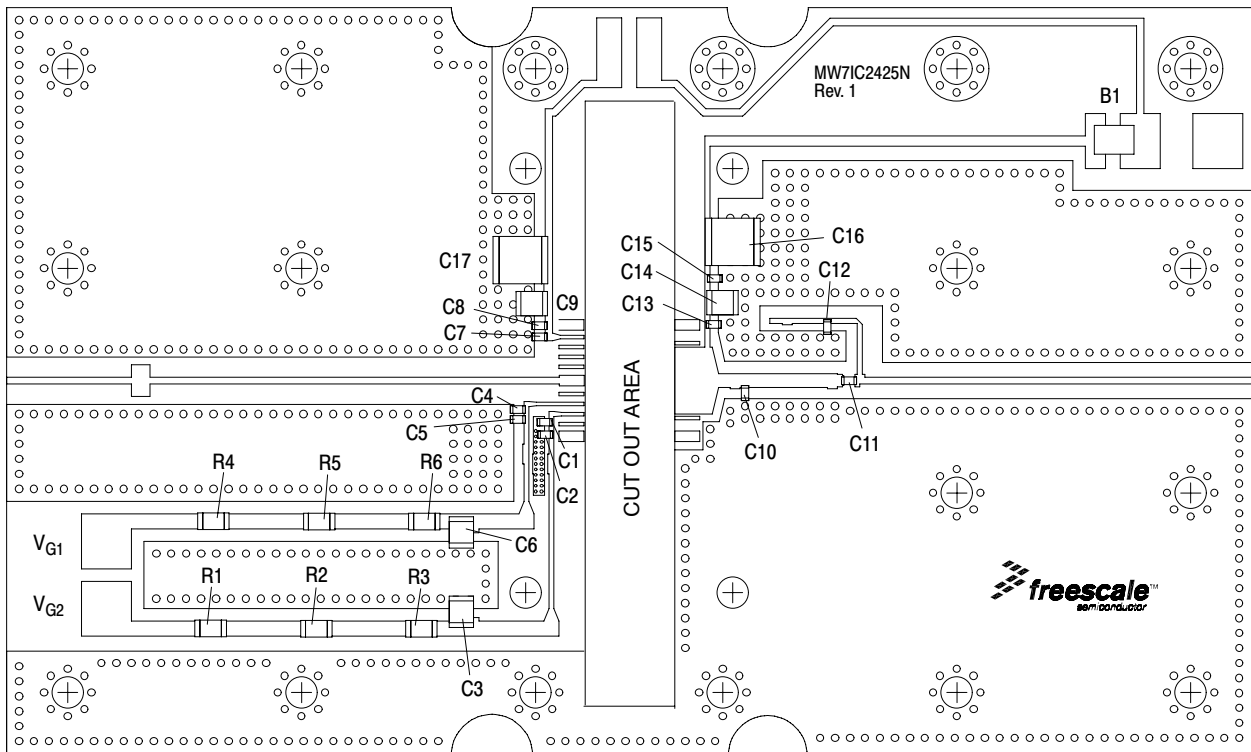
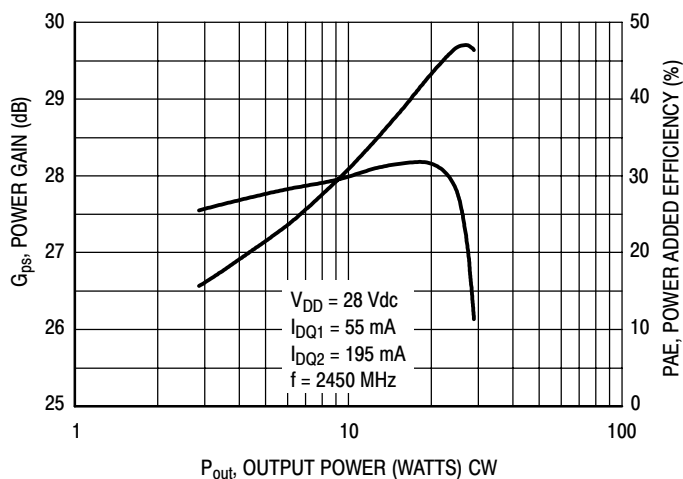
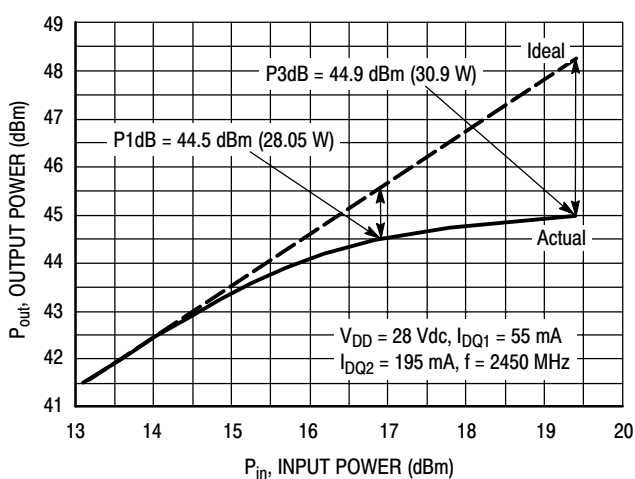


Figure 4. MW7IC2425NR1(GNR1)(NBR1) Narrowband Test Circuit Component Layout

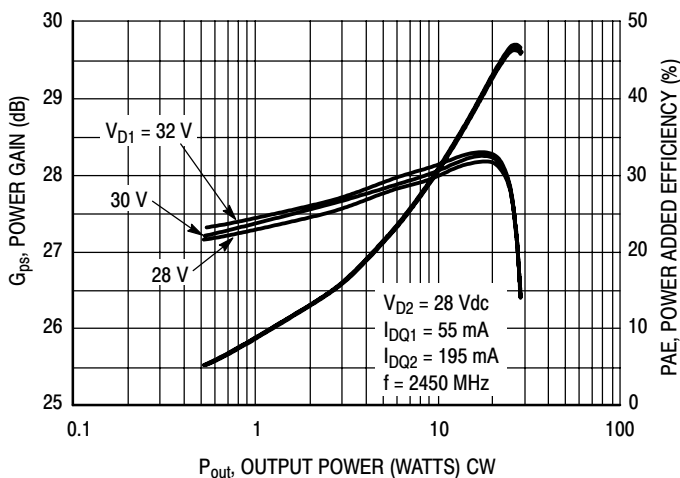
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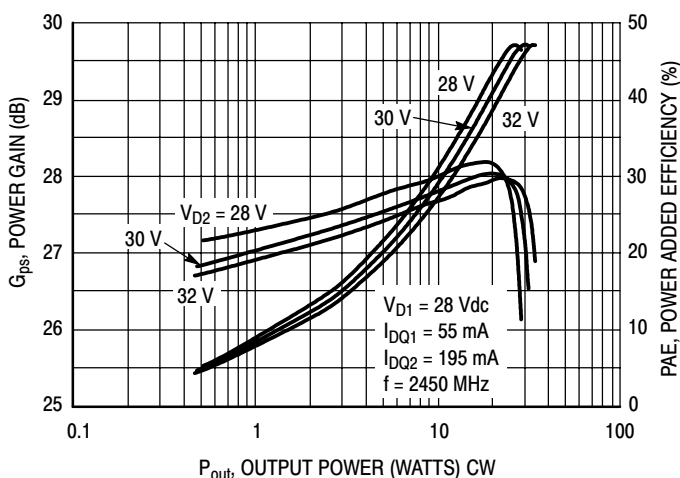
**Figure 5. Power Gain and Power Added Efficiency versus CW Output Power**



**Figure 6. CW Output Power versus Input Power**

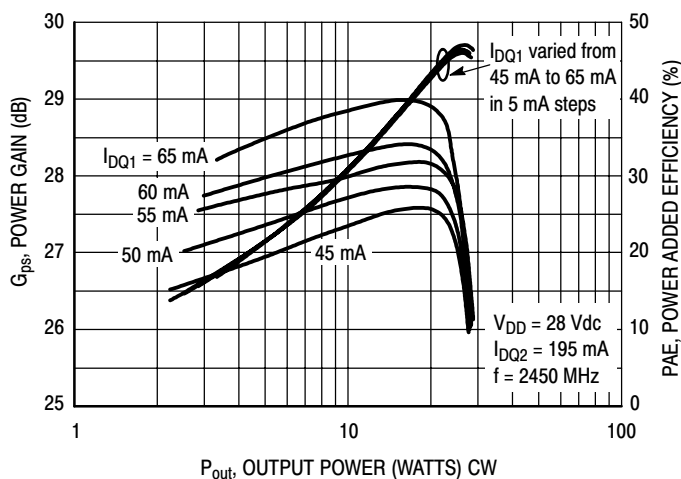


**Figure 7. Power Gain and Power Added Efficiency versus CW Output Power as a Function of  $V_{D1}$**

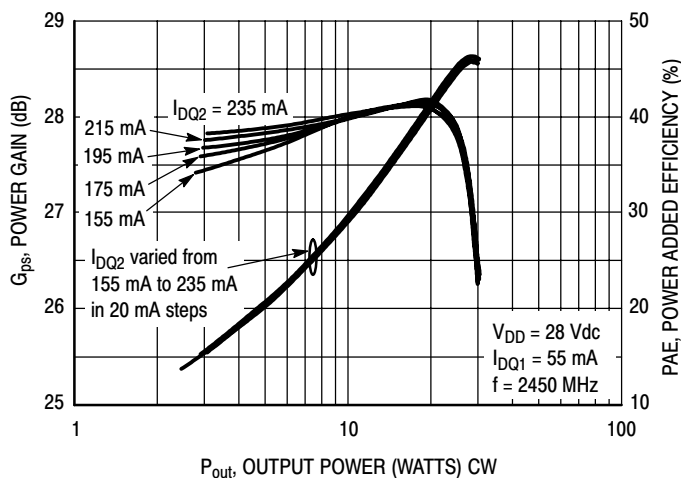


**Figure 8. Power Gain and Power Added Efficiency versus CW Output Power as a Function of  $V_{D2}$**

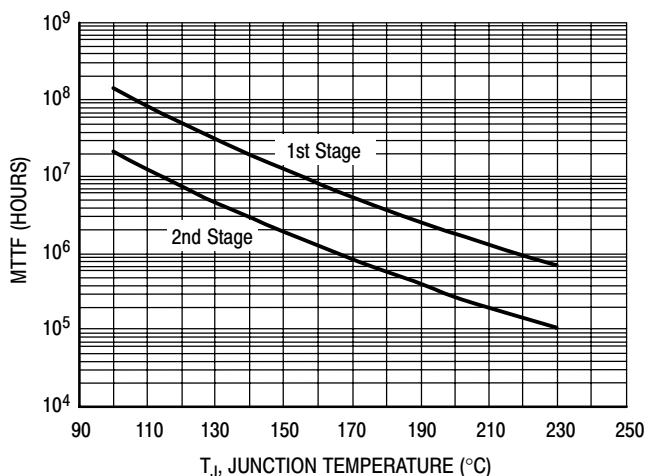
### TYPICAL CHARACTERISTICS — NARROWBAND



**Figure 9. Power Gain and Power Added Efficiency versus CW Output Power as a Function of  $I_{DQ1}$**



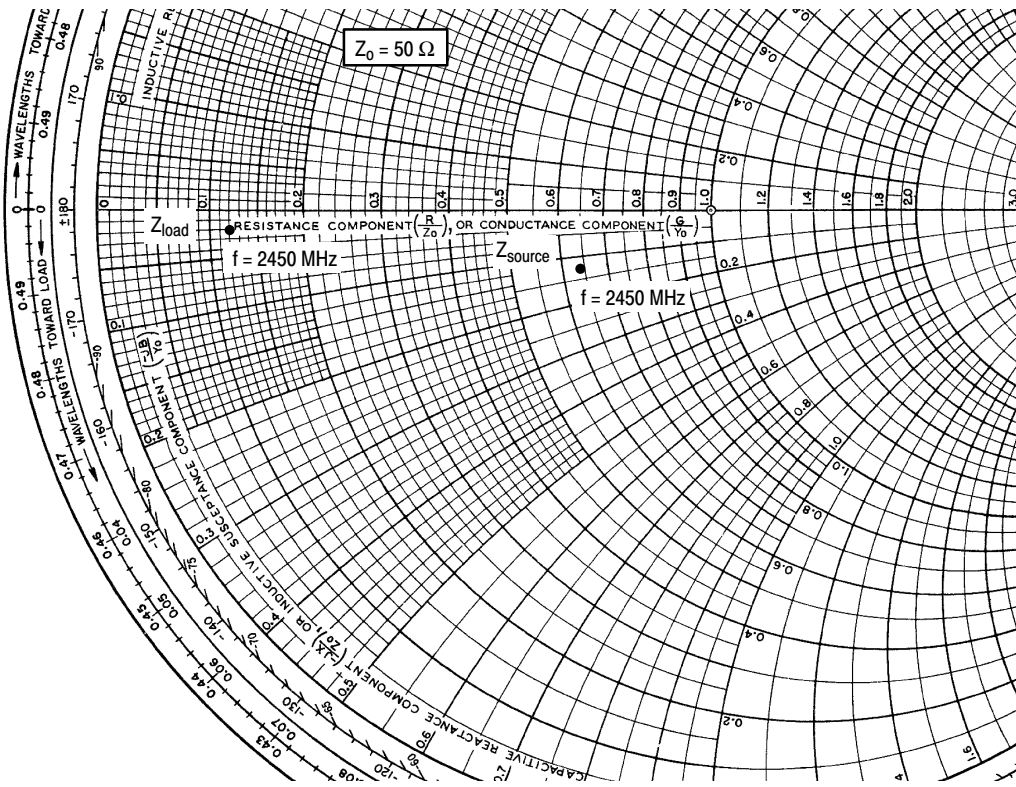
**Figure 10. Power Gain and Power Added Efficiency versus CW Output Power as a Function of  $I_{DQ2}$**



This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 28$  Vdc,  $P_{out} = 25$  W CW, and PAE = 43.8%.

MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 11. MTTF versus Junction Temperature**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 55 \text{ mA}$ ,  $I_{DQ2} = 195 \text{ mA}$ ,  $P_{out} = 25 \text{ W CW}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
2450	$32 - j6.256$	$6.2 - j1.17$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

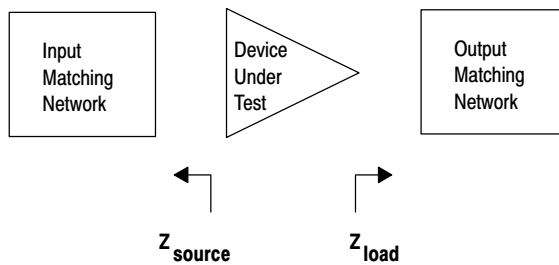
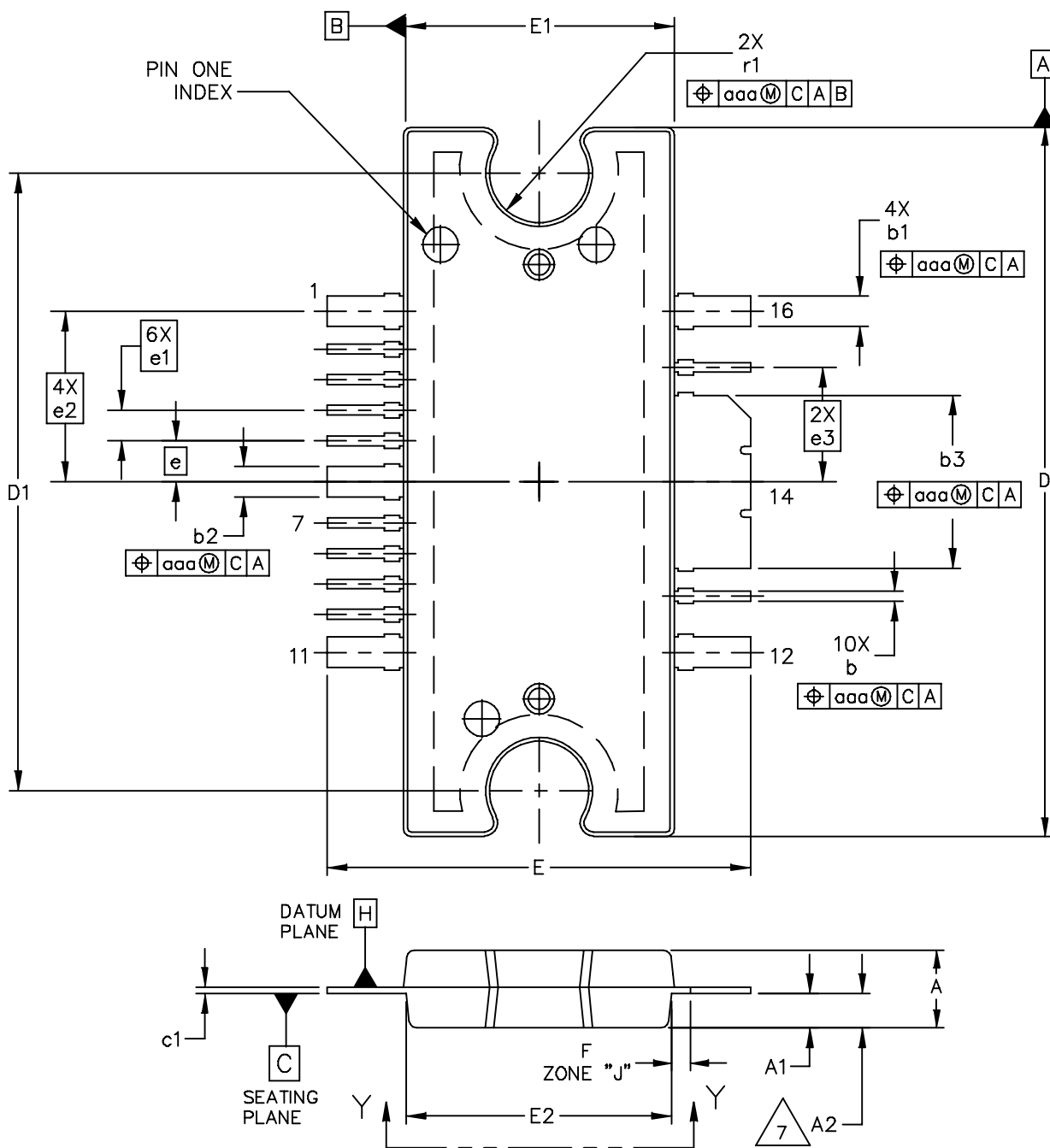


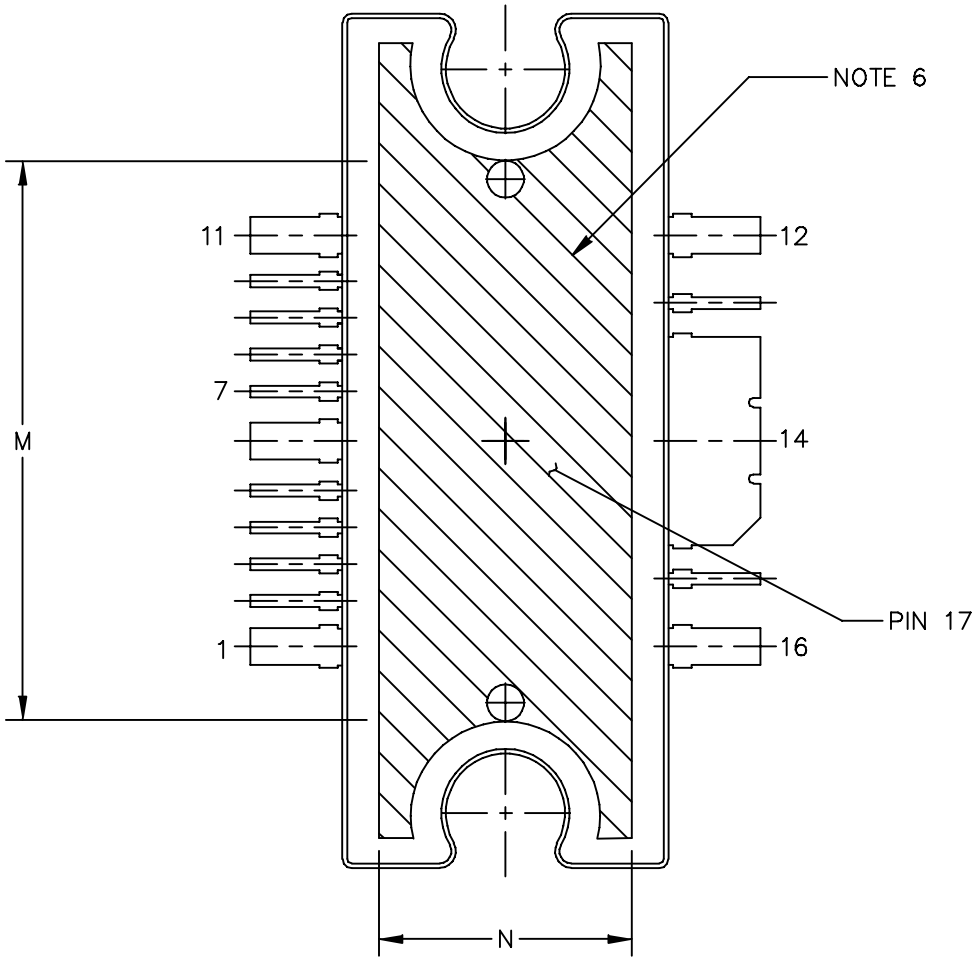
Figure 12. Series Equivalent Source and Load Impedance — Narrowband



### PACKAGE DIMENSIONS



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		CASE NUMBER: 1329-09		23 AUG 2007	
		STANDARD: NON-JEDEC			



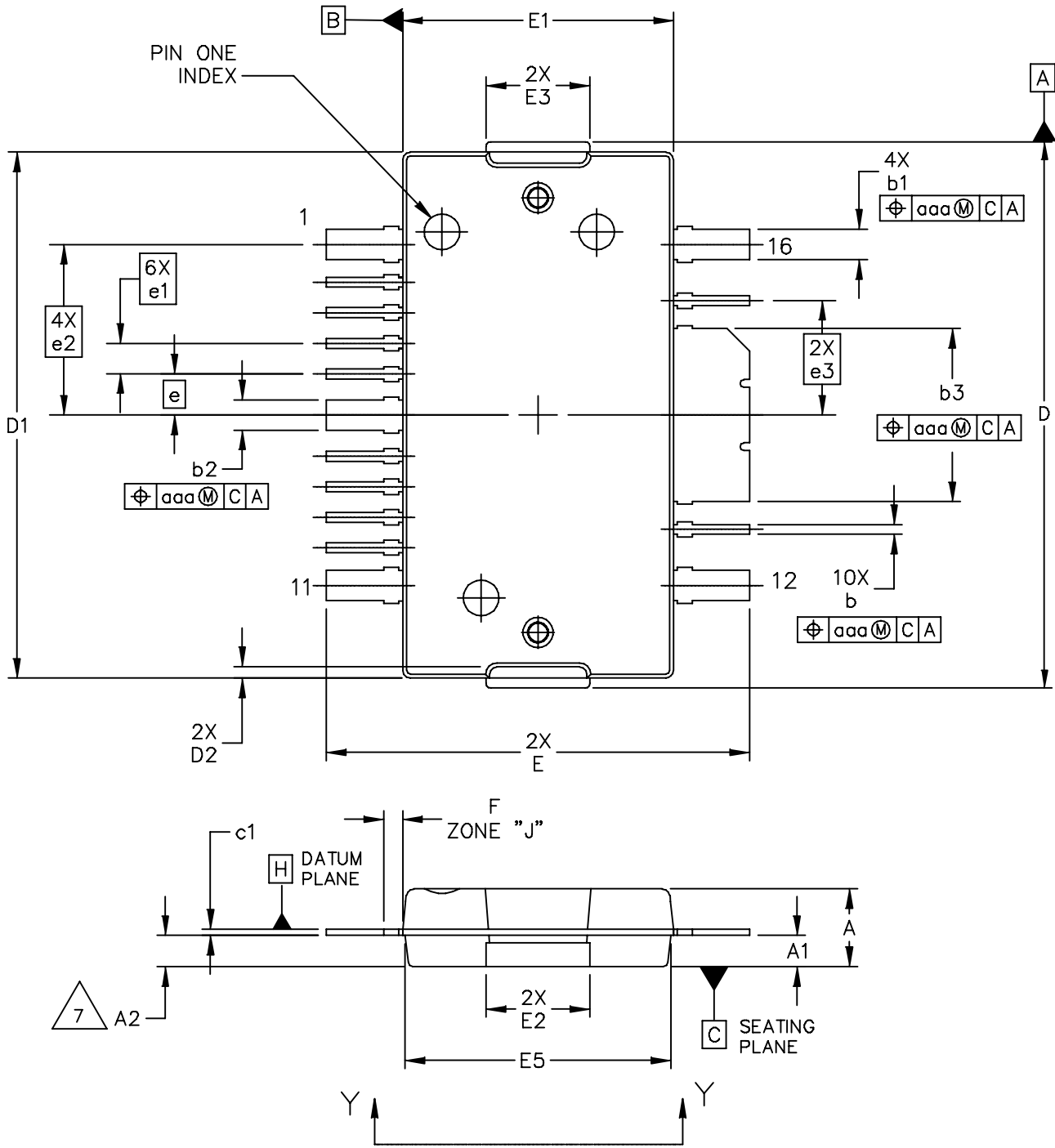
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	STANDARD: NON-JEDEC		

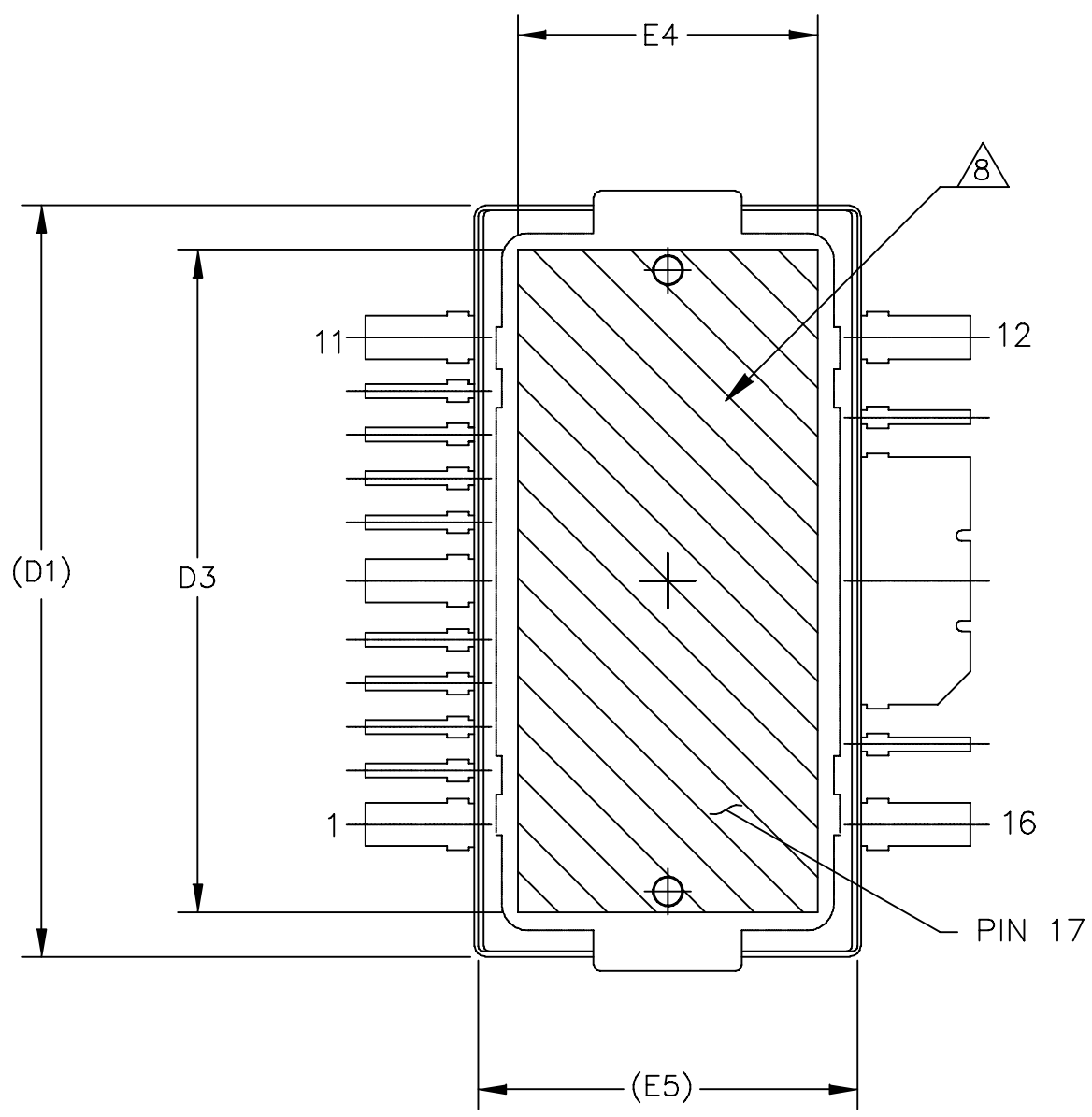
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----	aaa	.004		.10	
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VIEW Y-Y

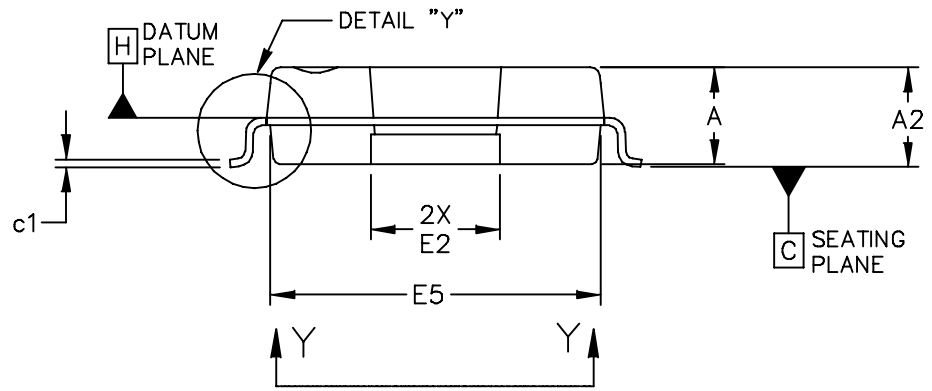
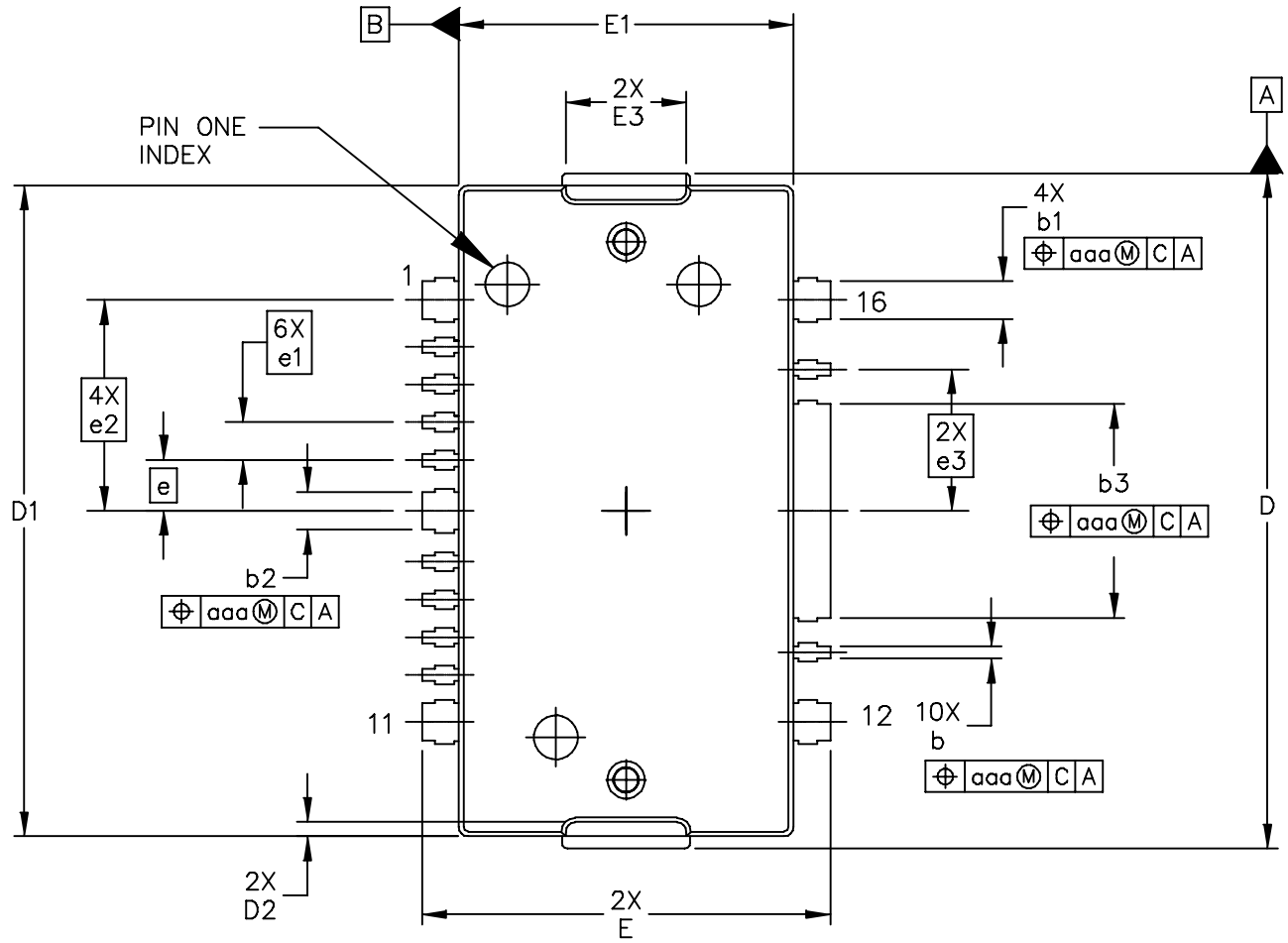
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MW7IC2425NR1 MW7IC2425GNR1 MW7IC2425NBR1

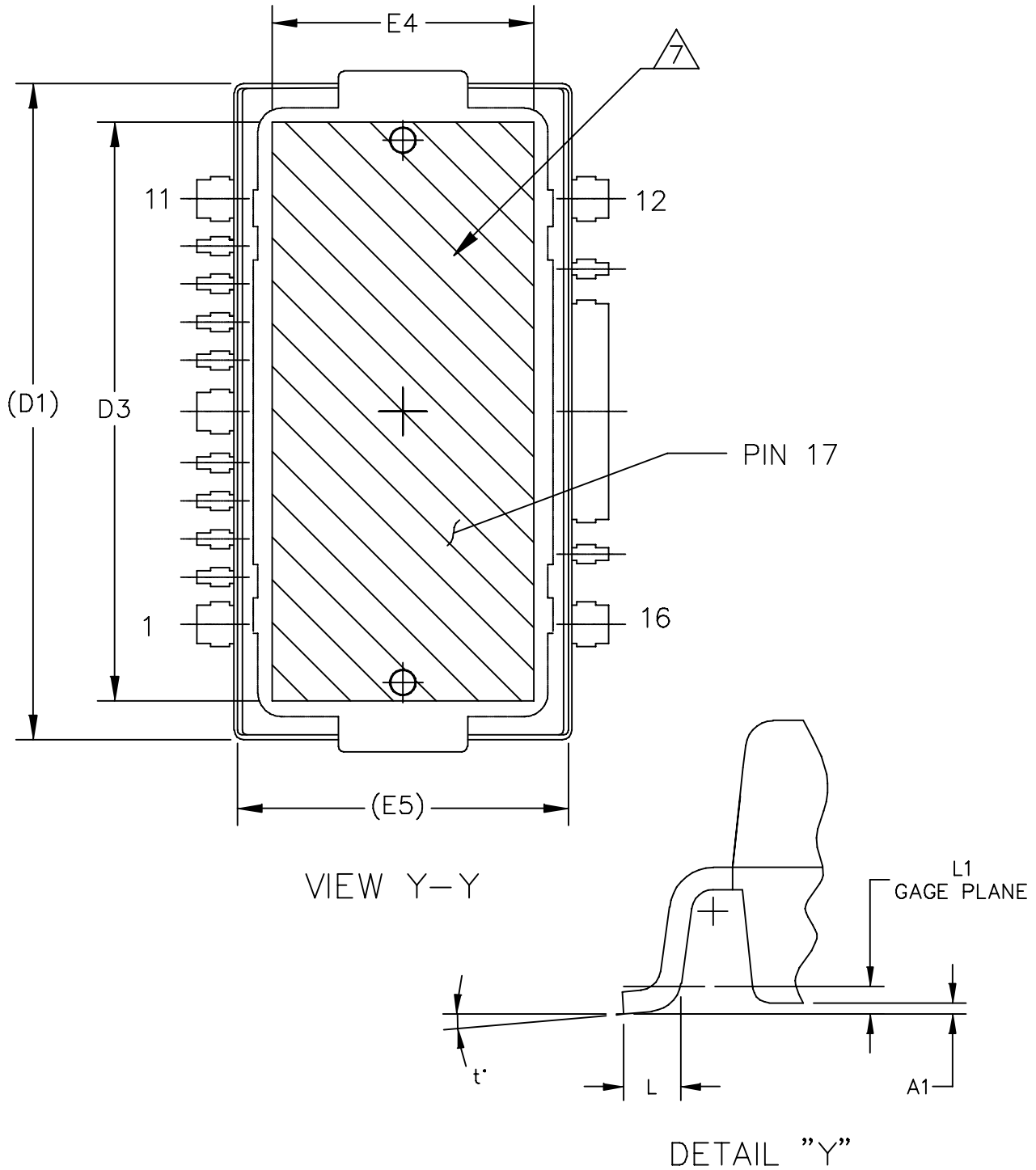
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUM -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.011	.017	0.28	0.43
A2	.040	.042	1.02	1.07	b1	.037	.043	0.94	1.09
D	.712	.720	18.08	18.29	b2	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b3	.225	.231	5.72	5.87
D2	.011	.019	0.28	0.48	c1	.007	.011	.18	.28
D3	.600	---	15.24	---	e	.054 BSC		1.37 BSC	
E	.551	.559	14	14.2	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.224 BSC		5.69 BSC	
E2	.132	.140	3.35	3.56	e3	.150 BSC		3.81 BSC	
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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			STANDARD: NON-JEDEC		



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TITLE: TO-270 WIDE BODY 16 LEAD, GULL WING	DOCUMENT NO: 98ASA10755D		REV: A
	CASE NUMBER: 1887-01		31 AUG 2007
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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUM -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.011	.017	0.28	0.43
D	.712	.720	18.08	18.29	b1	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b2	.037	.043	0.94	1.09
D2	.011	.019	0.28	0.48	b3	.225	.231	5.72	5.87
D3	.600	---	15.24	---	c1	.007	.011	0.18	0.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.132	.140	3.35	3.56	e2	.224 BSC		5.69 BSC	
E3	.124	.132	3.15	3.35	e3	.150 BSC		3.81 BSC	
E4	.270	---	6.86	---	t	2'	8'	2'	8'
E5	.346	.350	8.79	8.89	aaa	.004		0.10	
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## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

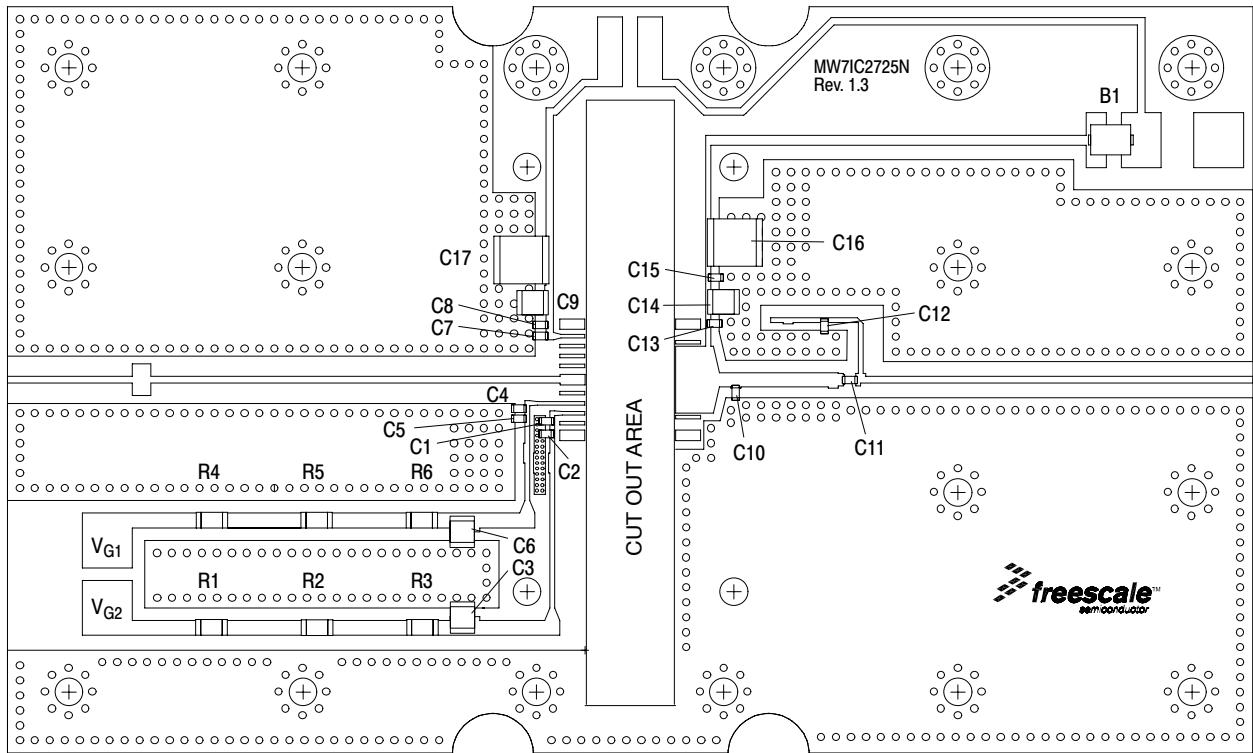
## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2009	<ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>

## APPENDIX A

### MW7IC2425NR1/GNR1/NBR1 FUNCTIONAL TEST DATA, FIXTURE AND THERMAL DATA



Z1	0.500" x 0.027" Microstrip	Z9	0.040" x 0.061" Microstrip
Z2	0.075" x 0.127" Microstrip	Z10	0.020" x 0.050" Microstrip
Z3	1.640" x 0.027" Microstrip	Z11	0.050" x 0.050" Microstrip
Z4	0.100" x 0.042" Microstrip	Z12	0.050" x 0.027" Microstrip
Z5	0.151" x 0.268" Microstrip	Z13*	0.338" x 0.020" Microstrip
Z6	0.025" x 0.268" x 0.056" Taper	Z14	1.551" x 0.027" Microstrip
Z7	0.050" x 0.056" Microstrip	PCB	Rogers R04350B, 0.0133", $\epsilon_r = 3.48$
Z8	0.356" x 0.056" Microstrip		

\* Line length includes microstrip bends

**Figure 1. MW7IC2425NR1(GNR1)(NBR1) Test Circuit Component Layout**

**Table 1. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQ1} = 77$ mA, $I_{DQ2} = 275$ mA, $P_{out} = 4$ W Avg., $f = 2700$ MHz, WiMAX, OFDM 802.16d, 64 QAM $3/4$ , 4 Bursts, 10 MHz Channel Bandwidth, Input Signal PAR = 9.5 dB @ 0.01% Probability on CCDF. ACPR measured in 1 MHz Channel Bandwidth @ $\pm 8.5$ MHz Offset.					
Power Gain	$G_{ps}$	25.5	28.5	30.5	dB
Power Added Efficiency	PAE	15	17	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	—	9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-50	-46	dBc
Input Return Loss	IRL	—	-15	-10	dB

(continued)



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