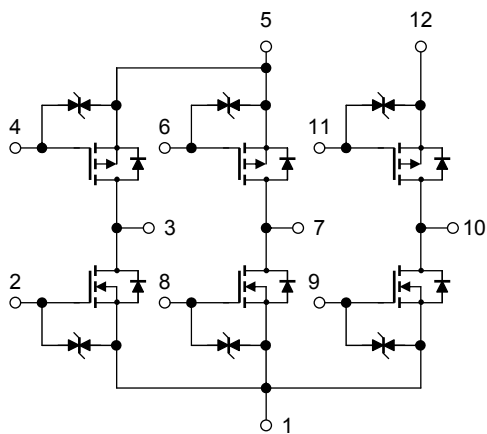


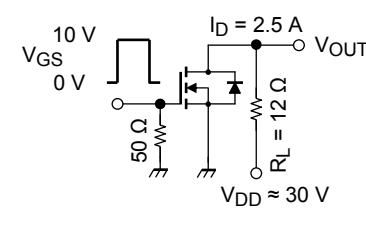
Array Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance of channel to ambient (6-device operation, $T_a = 25^\circ\text{C}$)	$\Sigma R_{\text{th}}(\text{ch-a})$	28.4	$^\circ\text{C/W}$
Thermal resistance of channel to case (6-device operation, $T_c = 25^\circ\text{C}$)	$\Sigma R_{\text{th}}(\text{ch-c})$	3.47	$^\circ\text{C/W}$
Maximum lead temperature for soldering purposes (3.2 mm from case for $t = 10$ s)	T_L	260	$^\circ\text{C}$

Electrical Characteristics (Ta = 25°C) (Nch MOS FET)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	μA
Drain source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	60	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 4\text{ V}, I_D = 2.5\text{ A}$	—	0.21	0.32	Ω
			$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$	—	0.12	0.16	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 2.5\text{ A}$	3.0	5.0	—	S
Input capacitance		C_{iss}	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	370	—	pF
Reverse transfer capacitance		C_{rss}		—	60	—	pF
Output capacitance		C_{oss}		—	180	—	pF
Switching time	Rise time	t_r	 <p>$V_{IN}: t_r, t_f < 5\text{ ns}, \text{duty} \leq 1\%, t_w = 10\text{ }\mu\text{s}$</p>	—	18	—	ns
	Turn-on time	t_{on}		—	25	—	
	Fall time	t_f		—	55	—	
	Turn-off time	t_{off}		—	170	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx 48\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$	—	12	—	nC
Gate-source charge		Q_{gs}		—	8	—	nC
Gate-drain ("miller") charge		Q_{gd}		—	4	—	nC

Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	5	A
Pulse drain reverse current	I_{DRP}	—	—	—	20	A
Diode forward voltage	V_{DSF}	$I_{DR} = 5\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = 5\text{ A}, V_{GS} = 0\text{ V}$	—	70	—	ns
Reverse recovery charge	Q_{rr}	$di_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	0.1	—	μC

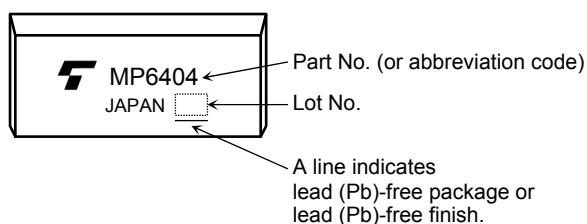
Electrical Characteristics (Ta = 25°C) (Pch MOS FET)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 10	μA
Drain cut-off current		I_{DSS}	$V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$	—	—	-100	μA
Drain source breakdown voltage		$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-60	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-0.8	—	-2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = -4\text{ V}, I_D = -2.5\text{ A}$	—	0.24	0.28	Ω
			$V_{GS} = -10\text{ V}, I_D = -2.5\text{ A}$	—	0.16	0.19	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -2.5\text{ A}$	2.0	4.0	—	S
Input capacitance		C_{iss}	$V_{DB} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	630	—	μF
Reverse transfer capacitance		C_{rss}		—	95	—	μF
Output capacitance		C_{oss}		—	290	—	μF
Switching time	Rise time	t_r		—	25	—	ns
	Turn-on time	t_{on}		—	45	—	
	Fall time	t_f		—	55	—	
	Turn-off time	t_{off}		—	200	—	
Total gate charge (gate-source plus gate-drain)		Q_g	$V_{DD} \approx -48\text{ V}, V_{GS} = -10\text{ V}, I_D = -5\text{ A}$	—	22	—	nC
Gate-source charge		Q_{gs}		—	16	—	nC
Gate-drain ("miller") charge		Q_{gd}		—	6	—	nC

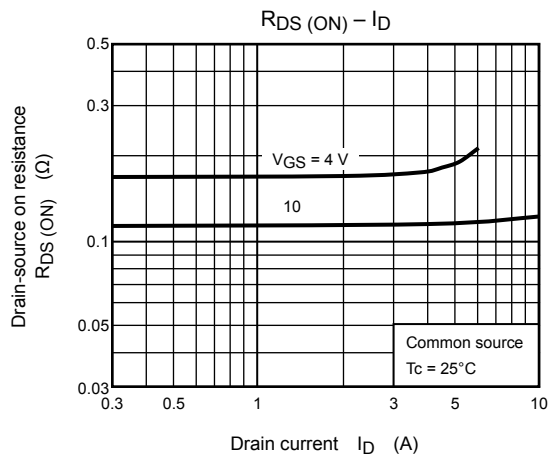
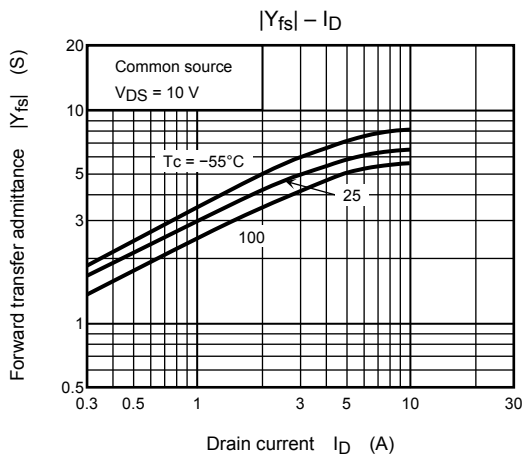
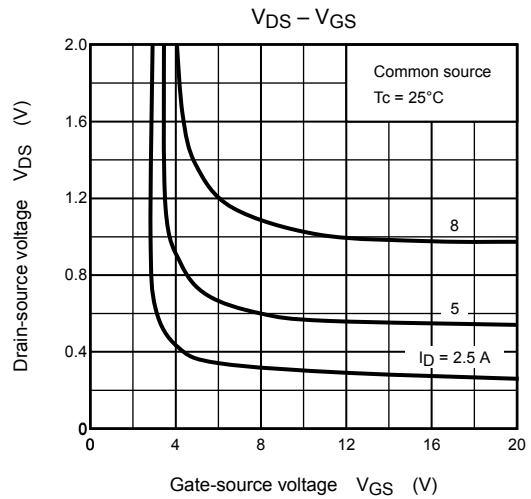
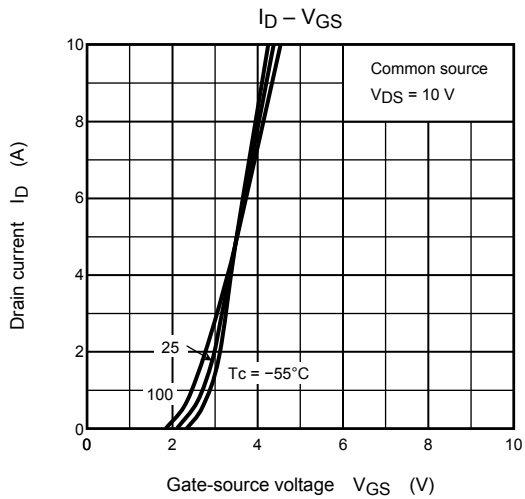
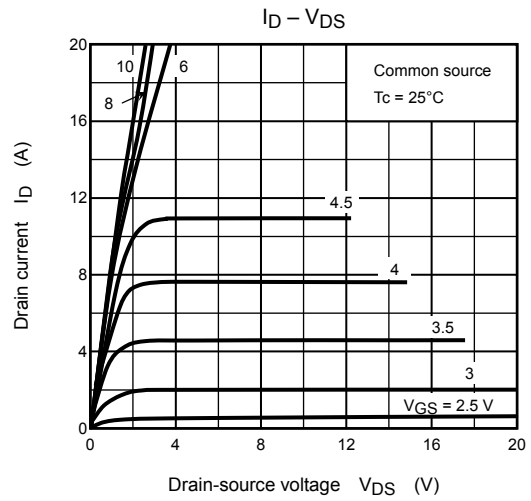
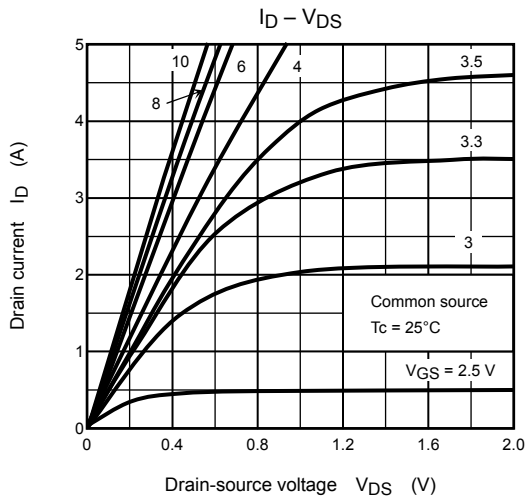
Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	-5	A
Pulse drain reverse current	I_{DRP}	—	—	—	-20	A
Diode forward voltage	V_{DSF}	$I_{DR} = -5\text{ A}, V_{GS} = 0\text{ V}$	—	—	1.7	V
Reverse recovery time	t_{rr}	$I_{DR} = -5\text{ A}, V_{GS} = 0\text{ V}$	—	80	—	ns
Reverse recovery charge	Q_{rr}	$di_{DR}/dt = 50\text{ A}/\mu\text{s}$	—	0.1	—	μC

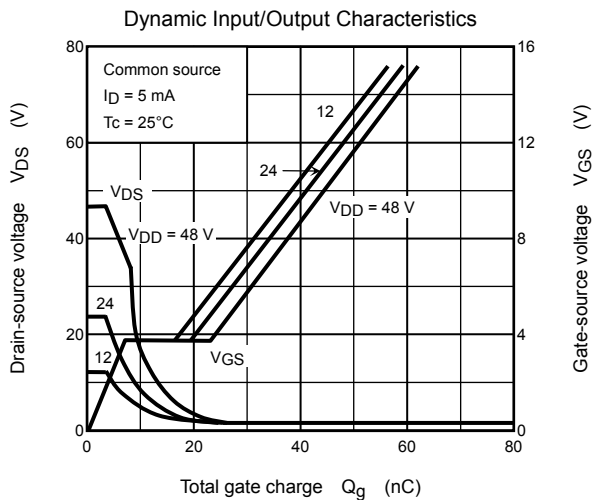
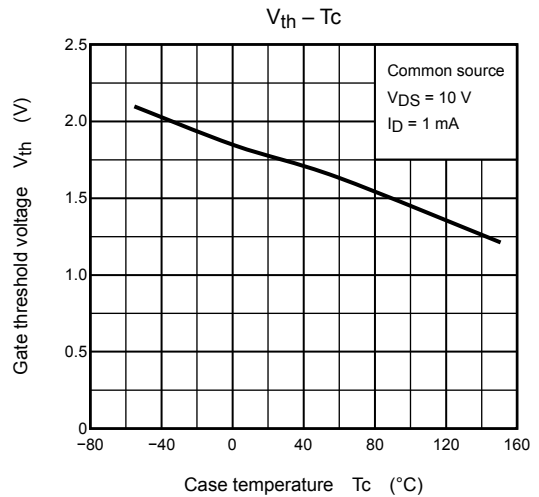
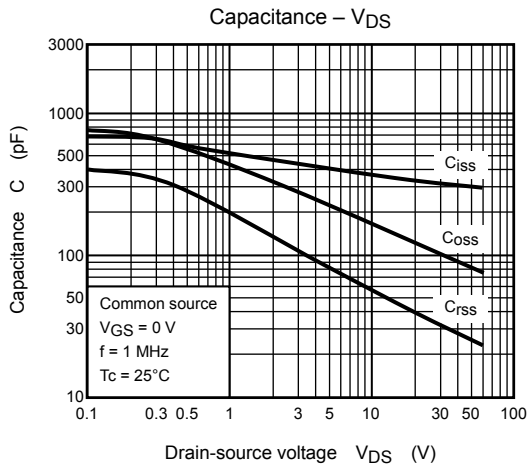
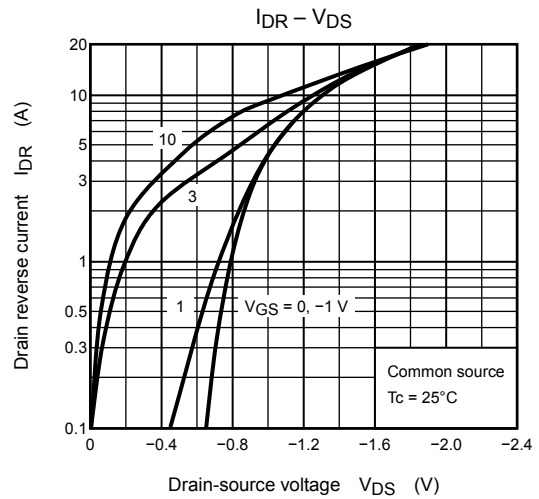
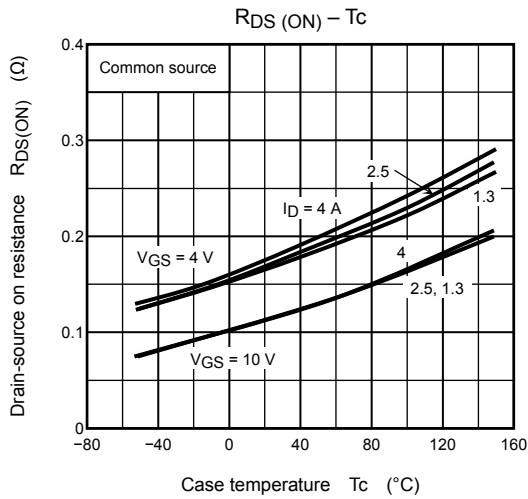
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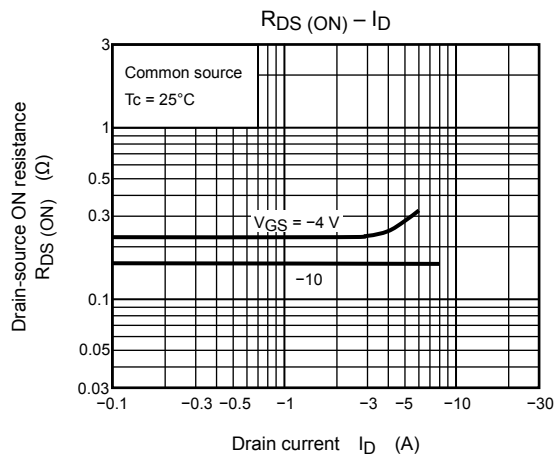
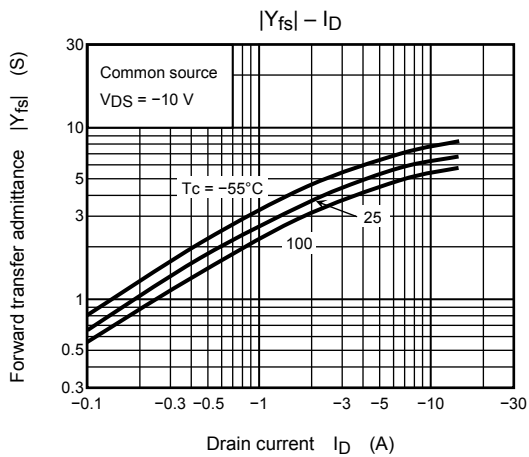
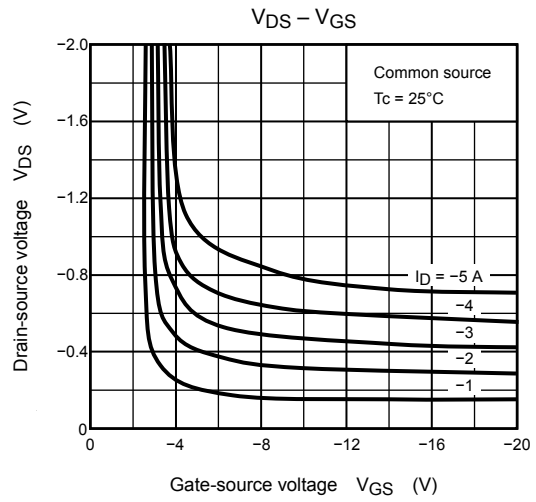
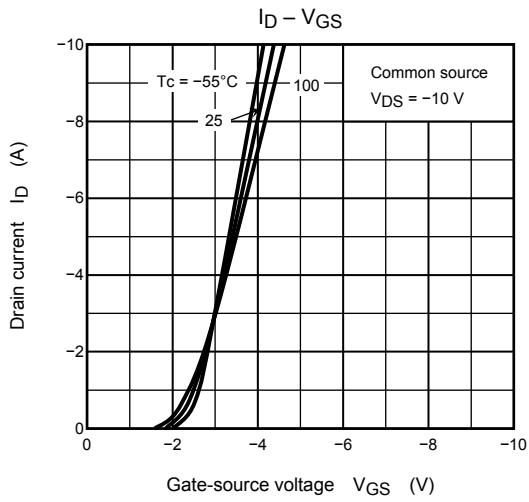
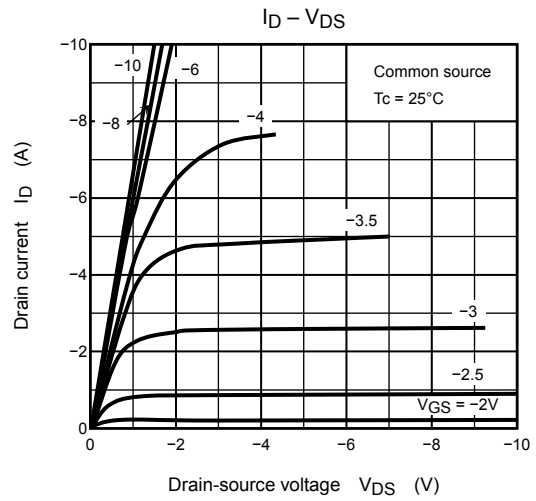
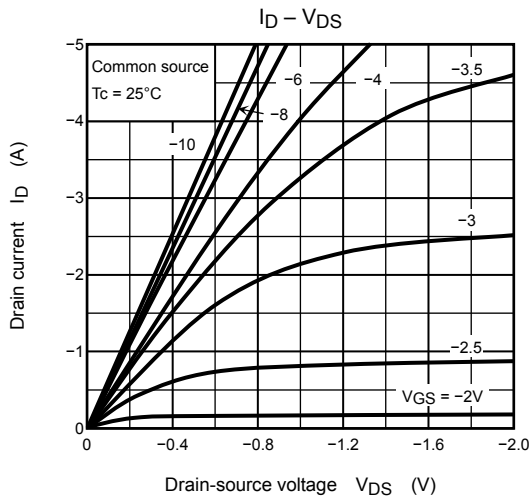
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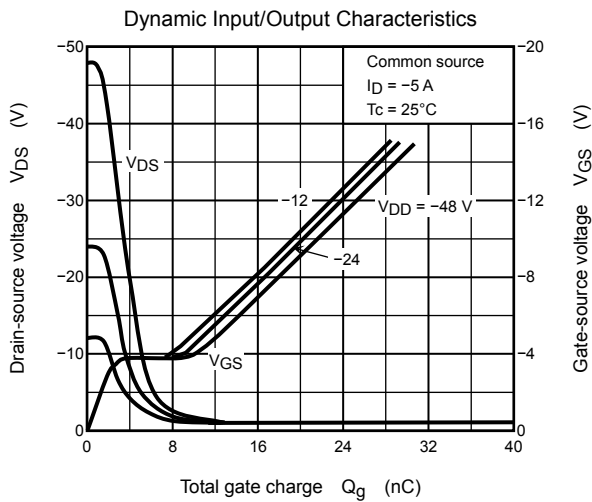
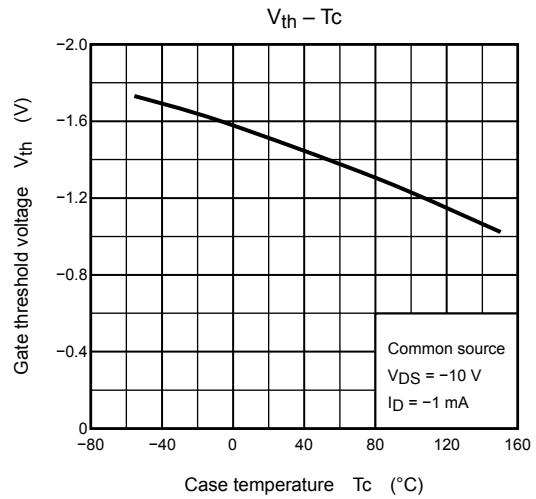
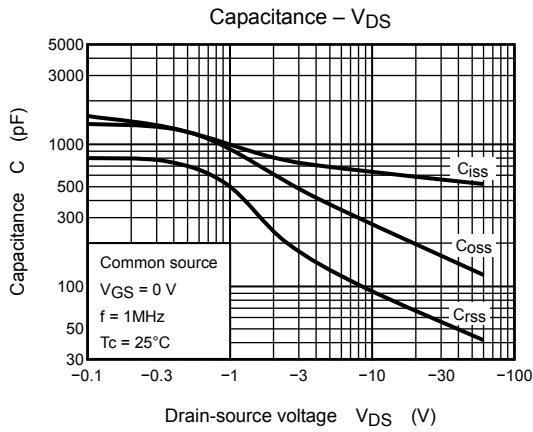
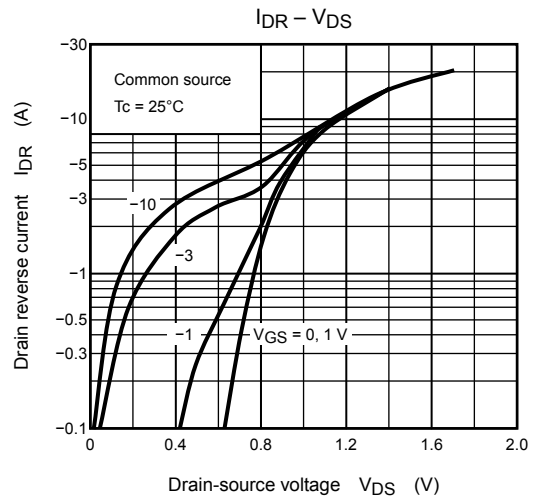
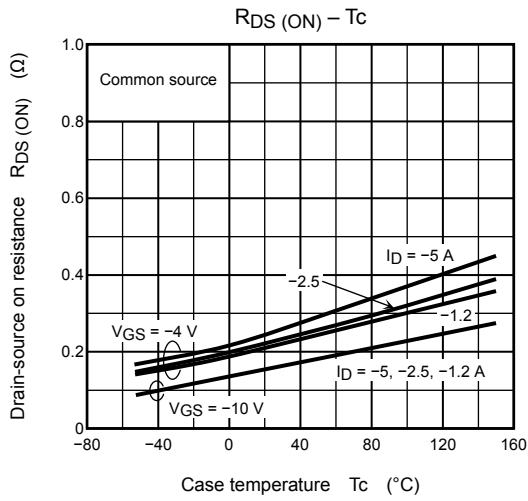
Nch MOS FET

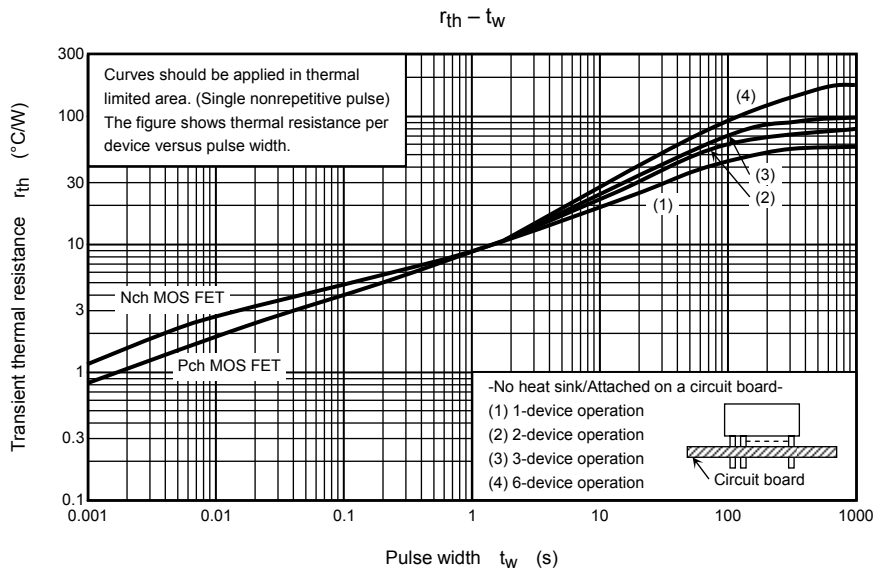
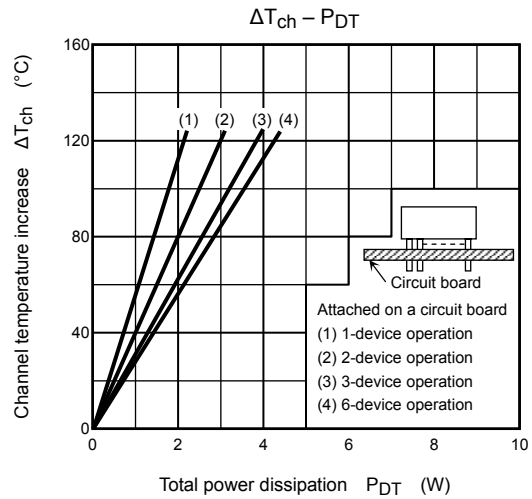
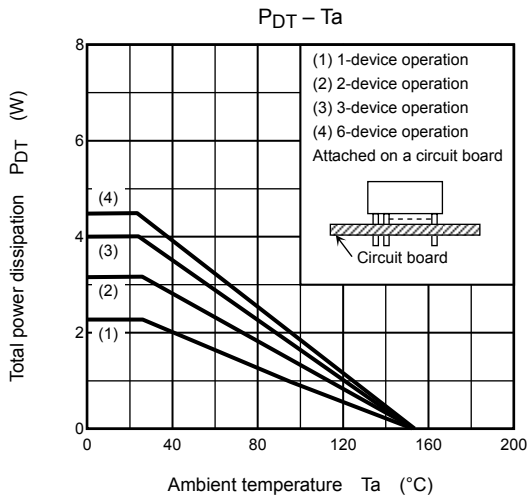


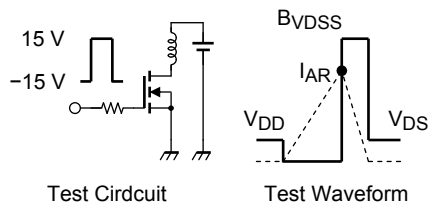
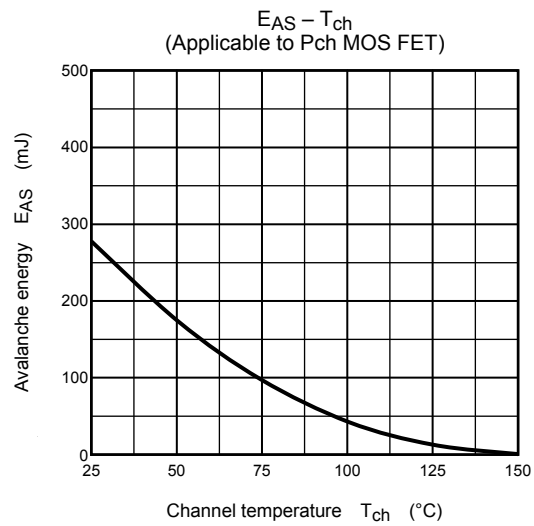
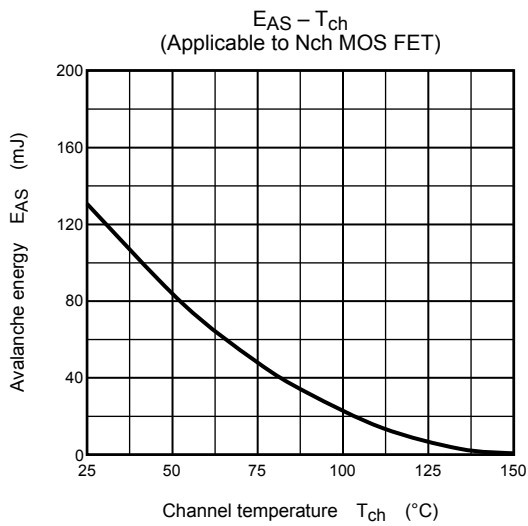
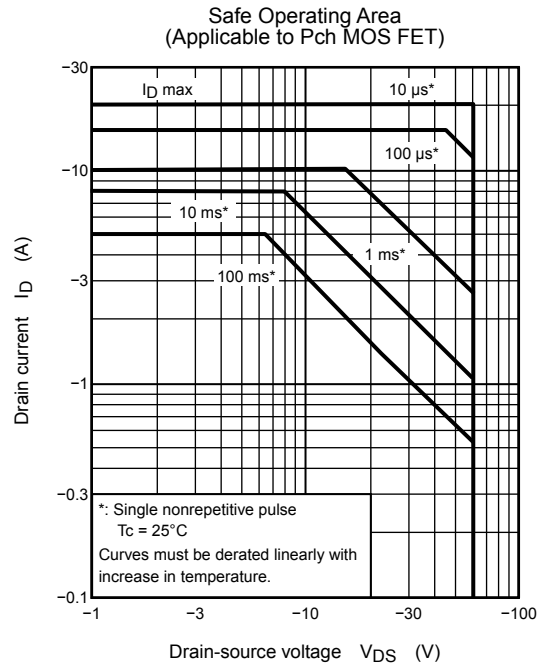
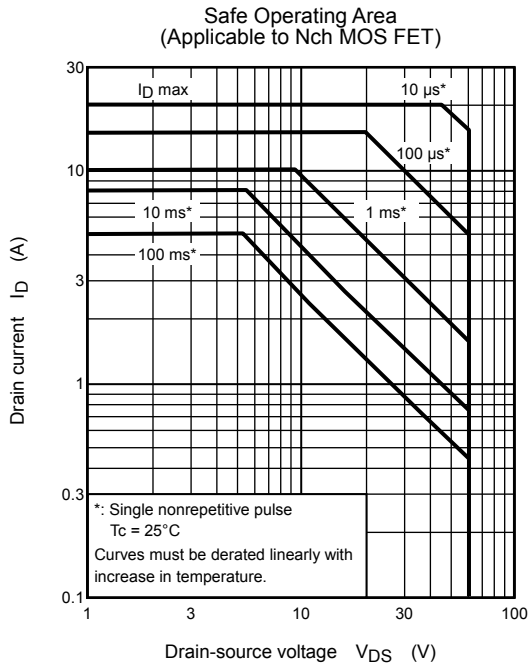
Pch MOS FET



Pch MOS FET

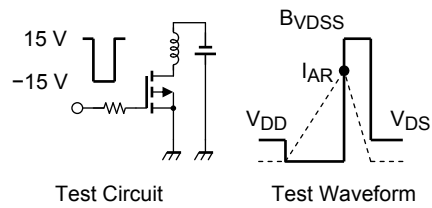






Peak $I_{AR} = 5 \text{ A}$, $R_G = 25 \Omega$
 $V_{DD} = 25 \text{ V}$, $L = 7 \text{ mH}$

$$E_{AS} = \frac{1}{2} L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$



Peak $I_{AR} = -5 \text{ A}$, $R_G = 25 \Omega$
 $V_{DD} = -25 \text{ V}$, $L = 14.84 \text{ mH}$

$$E_{AS} = \frac{1}{2} L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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