

12 channel configurable power management integrated circuit


The PF0200 Power Management Integrated Circuit (PMIC) provides a highly programmable/ configurable architecture, with fully integrated power devices and minimal external components. With up to four buck converters, one boost regulator, six linear regulators, RTC supply, and coin-cell charger, the PF0200 can provide power for a complete system, including applications processors, memory, and system peripherals, in a wide range of applications. With on-chip One Time Programmable (OTP) memory, the PF0200 is available in pre-programmed standard versions, or non-programmed to support custom programming. The PF0200 is especially suited to the i.MX 6SoloLite, i.MX 6Solo and i.MX 6DualLite versions of the i.MX 6 family of devices and is supported by full system level reference designs, and pre-programmed versions of the device. This device is powered by SMARTMOS technology.

Features:


- Three to four buck converters, depending on configuration
- Boost regulator to 5.0 V output
- Six general purpose linear regulators
- Programmable output voltage, sequence, and timing
- OTP (One Time Programmable) memory for device configuration
- Coin cell charger and RTC supply
- DDR termination reference voltage
- Power control logic with processor interface and event detection
- I²C control
- Individually programmable ON, OFF, and Standby modes

PF0200

POWER MANAGEMENT



EP SUFFIX (E-TYPE)
56 QFN 8X8
98ASA00405D



ES SUFFIX (WF-TYPE)
56 QFN 8X8
98ASA00589D

Applications

- Tablets
- IPTV
- Industrial Control
- Medical monitoring
- Home automation/ alarm/ energy management

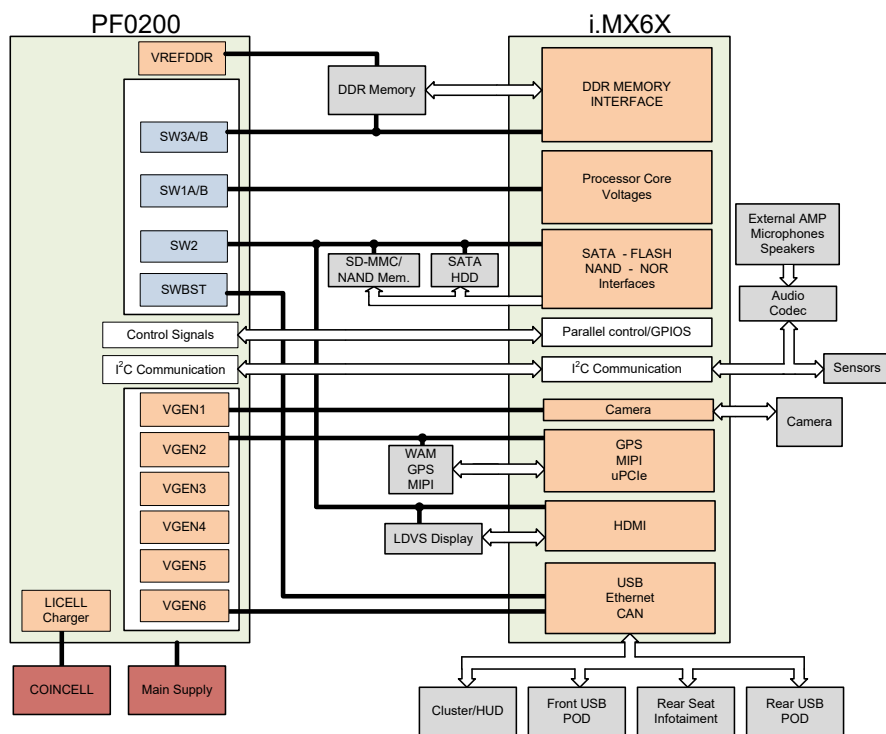


Figure 1. Simplified application diagram

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1 Orderable parts

The PF0200 is available with both pre-programmed and non-programmed OTP memory configurations. The non-programmed device uses “NP” as the programming code. The pre-programmed devices are identified using the program codes from [Table 1](#), which also list the associated NXP reference designs where applicable. Details of the OTP programming for each device can be found in [Table 8](#). Contact your NXP representative for more details.

Table 1. Orderable part variations

| Part number | Temperature (T _A) | Package | Programming | Reference designs | Qualification tier | Notes |
|----------------|-------------------------------|---|-------------|-------------------|---------------------|--------|
| MMPF0200NPAEP | -40 to 85 °C | 56 QFN 8x8 mm - 0.5 mm pitch E-Type QFN (full lead) | NP | N/A | Consumer | (2)(1) |
| MMPF0200F0AEP | | | F0 | N/A | | (2)(1) |
| MMPF0200F3AEP | | | F3 | N/A | | (2)(1) |
| MMPF0200F4AEP | | | F4 | N/A | | (2)(1) |
| MMPF0200F6AEP | | | F6 | i.MX6SX-SDB | | (2)(1) |
| MMPF0200F0ANES | -40 to 105 °C | 56 QFN 8x8 mm - 0.5 mm pitch WF-Type QFN (wetable flank) | F0 | N/A | Extended Industrial | (2)(1) |
| MMPF0200F3ANES | | | F3 | N/A | | (2)(1) |
| MMPF0200F4ANES | | | F4 | N/A | | (2)(1) |

Notes

1. For Tape and Reel add an R2 suffix to the part number.
2. For programming details see [Table 8](#).

2 Internal block diagram

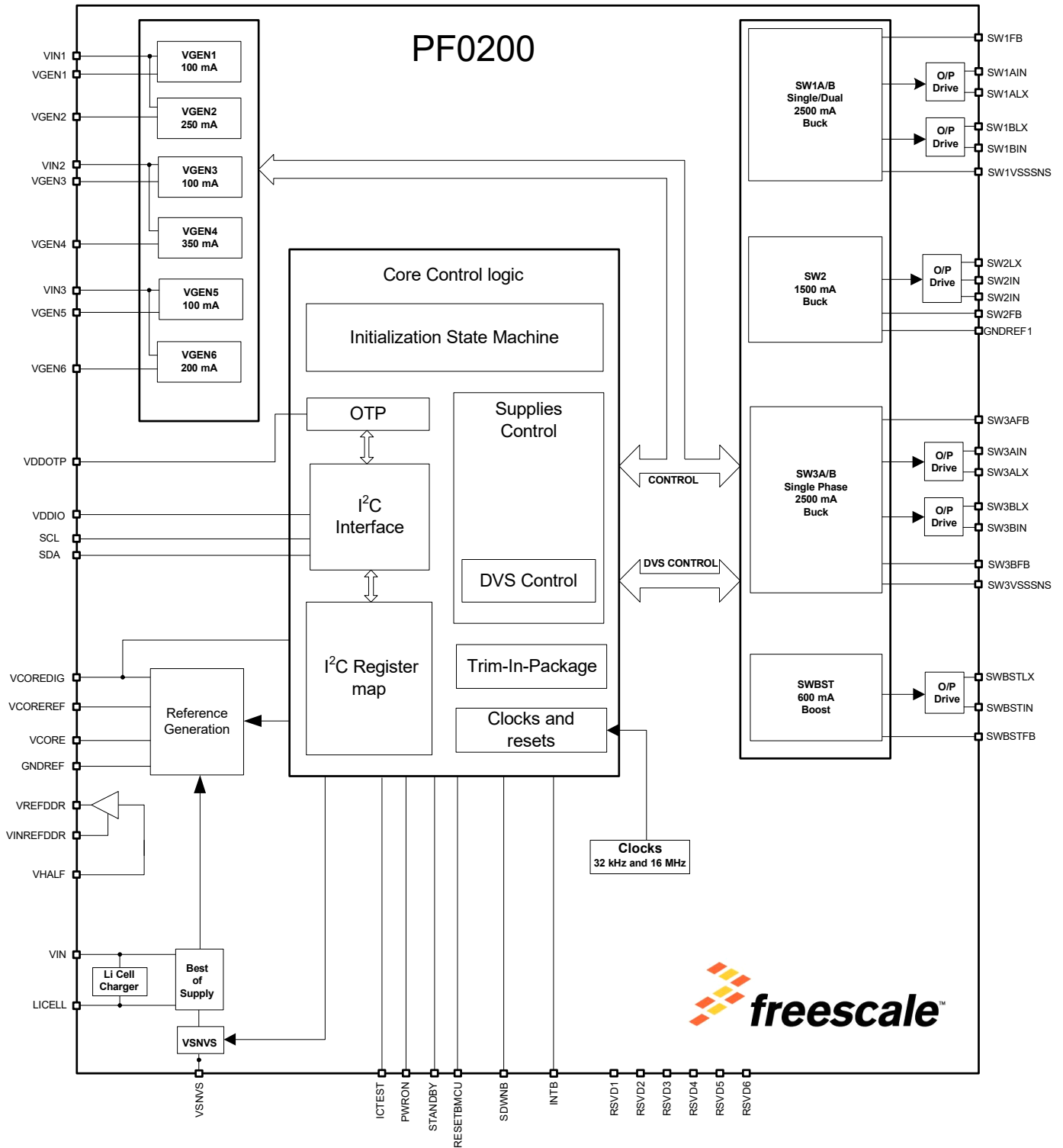


Figure 2. PF0200 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

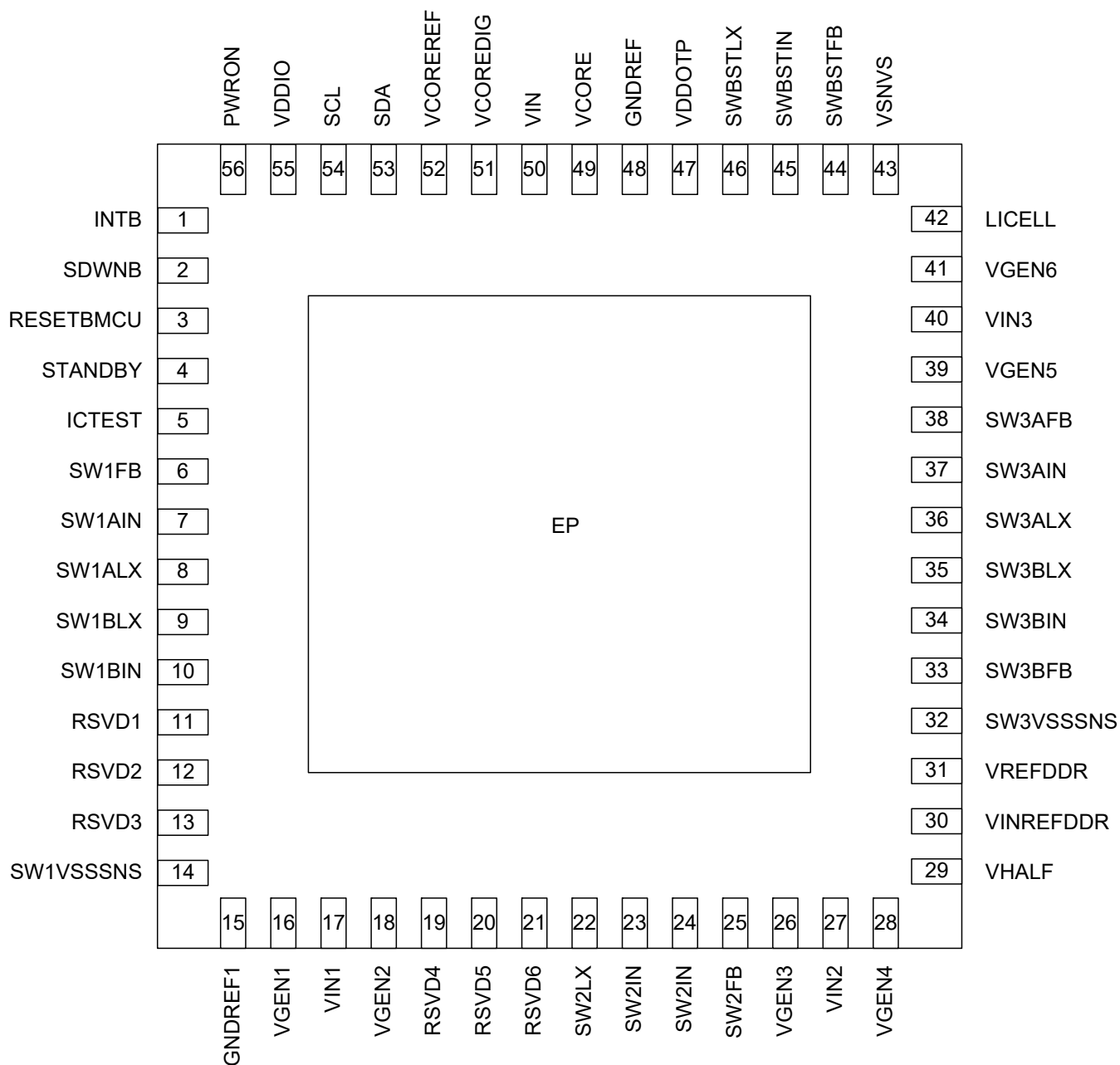


Figure 3. Pinout diagram

3.2 Pin definitions

Table 2. PF0200 pin definitions

| Pin number | Pin name | Pin function | Max rating | Type | Definition |
|------------|-----------------------|--------------|------------|--------------------|---|
| 1 | INTB | O | 3.6 V | Digital | Open drain interrupt signal to processor |
| 2 | SDWNB | O | 3.6 V | Digital | Open drain signal to indicate an imminent system shutdown |
| 3 | RESETBMCU | O | 3.6 V | Digital | Open drain reset output to processor. Alternatively can be used as a Power Good output. |
| 4 | STANDBY | I | 3.6 V | Digital | Standby input signal from processor |
| 5 | ICTEST | I | 7.5 V | Digital/ Analog | Reserved pin. Connect to GND in application. |
| 6 | SW1FB ⁽⁴⁾ | I | 3.6 V | Analog | Output voltage feedback for SW1A/B. Route this trace separately from the high-current path and terminate at the output capacitance. |
| 7 | SW1AIN ⁽⁴⁾ | I | 4.8 V | Analog | Input to SW1A regulator. Bypass with at least a 4.7 μ F ceramic capacitor and a 0.1 μ F decoupling capacitor as close to the pin as possible. |
| 8 | SW1ALX ⁽⁴⁾ | O | 4.8 V | Analog | Regulator 1A switch node connection |
| 9 | SW1BLX ⁽⁴⁾ | O | 4.8 V | Analog | Regulator 1B switch node connection |
| 10 | SW1BIN ⁽⁴⁾ | I | 4.8 V | Analog | Input to SW1B regulator. Bypass with at least a 4.7 μ F ceramic capacitor and a 0.1 μ F decoupling capacitor as close to the pin as possible. |
| 11 | RSVD1 | - | - | Reserved | Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected. |
| 12 | RSVD2 | - | - | Reserved | Reserved for pin to pin compatibility. Connect this pin to VIN. |
| 13 | RSVD3 | - | - | Reserved | Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected. |
| 14 | SW1VSSNS | GND | - | GND | Ground reference for regulator SW1AB. It is connected externally to GNDREF through a board ground plane. |
| 15 | GNDREF1 | GND | - | GND | Ground reference for regulator SW2. It is connected externally to GNDREF, via board ground plane. |
| 16 | VGEN1 | O | 2.5 V | Analog | VGEN1 regulator output, Bypass with a 2.2 μ F ceramic output capacitor. |
| 17 | VIN1 | I | 3.6 V | Analog | VGEN1, 2 input supply. Bypass with a 1.0 μ F decoupling capacitor as close to the pin as possible. |
| 18 | VGEN2 | O | 2.5 V | Analog | VGEN2 regulator output, Bypass with a 4.7 μ F ceramic output capacitor. |
| 19 | RSVD4 | - | - | Reserved | Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected. |
| 20 | RSVD5 | - | - | Reserved | Reserved for pin to pin compatibility. Connect this pin to VIN |
| 21 | RSVD6 | - | - | Reserved | Reserved for pin to pin compatibility. Internally connected. Leave this pin unconnected. |
| 22 | SW2LX ⁽⁴⁾ | O | 4.8 V | Analog | Regulator 2 switch node connection |
| 23 | SW2IN ⁽⁴⁾ | I | 4.8 V | Analog | Input to SW2 regulator. Connect pin 23 together with pin 24 and bypass with at least a 4.7 μ F ceramic capacitor and a 0.1 μ F decoupling capacitor as close to these pins as possible. |
| 24 | SW2IN ⁽⁴⁾ | I | 4.8 V | Analog | |
| 25 | SW2FB ⁽⁴⁾ | I | 3.6 V | Analog | Output voltage feedback for SW2. Route this trace separately from the high-current path and terminate at the output capacitance. |
| 26 | VGEN3 | O | 3.6 V | Analog | VGEN3 regulator output. Bypass with a 2.2 μ F ceramic output capacitor. |
| 27 | VIN2 | I | 3.6 V | Analog | VGEN3,4 input. Bypass with a 1.0 μ F decoupling capacitor as close to the pin as possible. |

Table 2. PF0200 pin definitions (continued)

| Pin number | Pin name | Pin function | Max rating | Type | Definition |
|------------|------------------------|--------------|---------------------|------------------|--|
| 28 | VGEN4 | O | 3.6 V | Analog | VGEN4 regulator output. Bypass with a 4.7 μ F ceramic output capacitor. |
| 29 | VHALF | I | 3.6 V | Analog | Half supply reference for VREFDDR |
| 30 | VINREFDDR | I | 3.6 V | Analog | VREFDDR regulator input. Bypass with at least 1.0 μ F decoupling capacitor as close to the pin as possible. |
| 31 | VREFDDR | O | 3.6 V | Analog | VREFDDR regulator output |
| 32 | SW3VSSNS | GND | - | GND | Ground reference for the SW3 regulator. Connect to GNDREF externally via the board ground plane. |
| 33 | SW3BFB ⁽⁴⁾ | I | 3.6 V | Analog | Output voltage feedback for SW3B. Route this trace separately from the high-current path and terminate at the output capacitance. |
| 34 | SW3BIN ⁽⁴⁾ | I | 4.8 V | Analog | Input to SW3B regulator. Bypass with at least a 4.7 μ F ceramic capacitor and a 0.1 μ F decoupling capacitor as close to the pin as possible. |
| 35 | SW3BLX ⁽⁴⁾ | O | 4.8 V | Analog | Regulator 3B switch node connection |
| 36 | SW3ALX ⁽⁴⁾ | O | 4.8 V | Analog | Regulator 3A switch node connection |
| 37 | SW3AIN ⁽⁴⁾ | I | 4.8 V | Analog | Input to SW3A regulator. Bypass with at least a 4.7 μ F ceramic capacitor and a 0.1 μ F decoupling capacitor as close to the pin as possible. |
| 38 | SW3AFB ⁽⁴⁾ | I | 3.6 V | Analog | Output voltage feedback for SW3A. Route this trace separately from the high-current path and terminate at the output capacitance. |
| 39 | VGEN5 | O | 3.6 V | Analog | VGEN5 regulator output. Bypass with a 2.2 μ F ceramic output capacitor. |
| 40 | VIN3 | I | 4.8 V | Analog | VGEN5, 6 input. Bypass with a 1.0 μ F decoupling capacitor as close to the pin as possible. |
| 41 | VGEN6 | O | 3.6 V | Analog | VGEN6 regulator output. Bypass with a 2.2 μ F ceramic output capacitor. |
| 42 | LICELL | I/O | 3.6 V | Analog | Coin cell supply input/output |
| 43 | VSNVS | O | 3.6 V | Analog | LDO or coin cell output to processor |
| 44 | SWBSTFB ⁽⁴⁾ | I | 5.5 V | Analog | Boost regulator feedback. Connect this pin to the output rail close to the load. Keep this trace away from other noisy traces and planes. |
| 45 | SWBSTIN ⁽⁴⁾ | I | 4.8 V | Analog | Input to SWBST regulator. Bypass with at least a 2.2 μ F ceramic capacitor and a 0.1 μ F decoupling capacitor as close to the pin as possible. |
| 46 | SWBSTLX ⁽⁴⁾ | O | 7.5 V | Analog | SWBST switch node connection |
| 47 | VDDOTP | I | 10 V ⁽³⁾ | Digital & Analog | Supply to program OTP fuses |
| 48 | GNDREF | GND | - | GND | Ground reference for the main band gap regulator. |
| 49 | VCORE | O | 3.6 V | Analog | Analog Core supply |
| 50 | VIN | I | 4.8 V | Analog | Main chip supply |
| 51 | VCOREDIG | O | 1.5 V | Analog | Digital Core supply |
| 52 | VCOREREF | O | 1.5 V | Analog | Main band gap reference |
| 53 | SDA | I/O | 3.6 V | Digital | I ² C data line (Open drain) |
| 54 | SCL | I | 3.6 V | Digital | I ² C clock |
| 55 | VDDIO | I | 3.6 V | Analog | Supply for I ² C bus. Bypass with 0.1 μ F decoupling capacitor as close to the pin as possible. |
| 56 | PWRON | I | 3.6 V | Digital | Power On/off from processor |

Table 2. PF0200 pin definitions (continued)

| Pin number | Pin name | Pin function | Max rating | Type | Definition |
|------------|----------|--------------|------------|------|---|
| - | EP | GND | - | GND | Expose pad. Functions as ground return for buck regulators. Tie this pad to the inner and external ground planes through vias to allow effective thermal dissipation. |

Notes

3. 10 V Maximum voltage rating during OTP fuse programming. 7.5 V Maximum DC voltage rated otherwise.
4. Unused switching regulators should be connected as follow: Pins SWxLX and SWxFB should be unconnected and Pin SWxIN should be connected to VIN with a 0.1 μ F bypass capacitor.

4 General product characteristics

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause malfunction or permanent damage to the device. The detailed maximum voltage rating per pin can be found in the pin list section.

| Symbol | Description | Value | Unit | Notes |
|---------------------------|--|-------------------------|------|-------|
| Electrical ratings | | | | |
| V_{IN} | Main input supply voltage | -0.3 to 4.8 | V | |
| V_{DDOTP} | OTP programming input supply voltage | -0.3 to 10 | V | |
| V_{LCELL} | Coin cell voltage | -0.3 to 3.6 | V | |
| V_{ESD} | ESD Ratings Human Body Model Charge Device Model | ± 2000 ± 500 | V | (5) |

Notes

- ESD testing is performed in accordance with the Human Body Model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the Charge Device Model (CDM), Robotic (CZAP = 4.0 pF).

4.2 Thermal characteristics

Table 4. Thermal ratings

| Symbol | Description (rating) | Min. | Max. | Unit | |
|------------------------|--|------------|-----------|------|--------|
| Thermal ratings | | | | | |
| T_A | Ambient Operating Temperature Range PF0200A PF0200AN | -40 -40 | 85 105 | °C | |
| T_J | Operating Junction Temperature Range | -40 | 125 | °C | (6) |
| T_{ST} | Storage Temperature Range | -65 | 150 | °C | |
| T_{PPRT} | Peak Package Reflow Temperature | – | Note 8 | °C | (7)(8) |

QFN56 Thermal resistance and package dissipation ratings

| | | | | | |
|-----------------------|--|--------|----------|------|-------------|
| $R_{\theta JA}$ | Junction to Ambient Natural Convection Four layer board (2s2p) Eight layer board (2s6p) | – – | 28 15 | °C/W | (9)(10)(11) |
| $R_{\theta JMA}$ | Junction to Ambient (@200 ft/min) Four layer board (2s2p) | – | 22 | °C/W | (9)(11) |
| $R_{\theta JB}$ | Junction to Board | – | 10 | °C/W | (12) |
| $R_{\theta JCBOTTOM}$ | Junction to Case Bottom | – | 1.2 | °C/W | (13) |
| Ψ_{JT} | Junction to Package Top Natural Convection | – | 2.0 | °C/W | (14) |

Notes

- Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See [Table 5](#) for thermal protection features.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
- NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes) and enter the core ID to view all orderable parts, and review parametrics.
- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
- Per JEDEC JESD51-6 with the board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.2.1 Power dissipation

During operation, the temperature of the die should not exceed the operating junction temperature noted in [Table 4](#). To optimize the thermal management and to avoid overheating, the PF0200 provides thermal protection. An internal comparator monitors the die temperature. Interrupts THERM110I, THERM120I, THERM125I, and THERM130I will be generated when the respective thresholds specified in [Table 5](#) are crossed in either direction. The temperature range can be determined by reading the THERMxxxS bits in register INTSENSE0.

In the event of excessive power dissipation, thermal protection circuitry will shut down the PF0200. This thermal protection will act above the thermal protection threshold listed in [Table 5](#). To avoid any unwanted power downs resulting from internal noise, the protection is debounced for 8.0 ms. This protection should be considered as a fail-safe mechanism and therefore the system should be configured such that this protection is not tripped under normal conditions.

Table 5. Thermal protection thresholds

| Parameter | Min. | Typ. | Max. | Units | Notes |
|-------------------------------------|------|------|------|-------|-------|
| Thermal 110 °C Threshold (THERM110) | 100 | 110 | 120 | °C | |
| Thermal 120 °C Threshold (THERM120) | 110 | 120 | 130 | °C | |
| Thermal 125 °C Threshold (THERM125) | 115 | 125 | 135 | °C | |
| Thermal 130 °C Threshold (THERM130) | 120 | 130 | 140 | °C | |
| Thermal Warning Hysteresis | 2.0 | – | 4.0 | °C | |
| Thermal Protection Threshold | 130 | 140 | 150 | °C | |

4.3 Electrical characteristics

4.3.1 General specifications

Table 6. General PMIC static characteristics

Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 2.8$ to 4.5 V, $V_{DDIO} = 1.7$ to 3.6 V, typical external component values and full load current range, unless otherwise noted.

| Pin name | Parameter | Load condition | Min. | Max. | Unit |
|-----------|-----------|----------------|------------------|------------------|------|
| PWRON | V_{IL} | – | 0.0 | $0.2 * V_{SNVS}$ | V |
| | V_{IH} | – | $0.8 * V_{SNVS}$ | 3.6 | V |
| RESETBMCU | V_{OL} | -2.0 mA | 0.0 | 0.4 | V |
| | V_{OH} | Open Drain | $0.7 * V_{IN}$ | V_{IN} | V |
| SCL | V_{IL} | – | 0.0 | $0.2 * V_{DDIO}$ | V |
| | V_{IH} | – | $0.8 * V_{DDIO}$ | 3.6 | V |
| SDA | V_{IL} | – | 0.0 | $0.2 * V_{DDIO}$ | V |
| | V_{IH} | – | $0.8 * V_{DDIO}$ | 3.6 | V |
| | V_{OL} | -2.0 mA | 0.0 | 0.4 | V |
| | V_{OH} | Open Drain | $0.7 * V_{DDIO}$ | V_{DDIO} | V |
| INTB | V_{OL} | -2.0 mA | 0.0 | 0.4 | V |
| | V_{OH} | Open Drain | $0.7 * V_{IN}$ | V_{IN} | V |
| SDWNB | V_{OL} | -2.0 mA | 0.0 | 0.4 | V |
| | V_{OH} | Open Drain | $0.7 * V_{IN}$ | V_{IN} | V |
| STANDBY | V_{IL} | – | 0.0 | $0.2 * V_{SNVS}$ | V |
| | V_{IH} | – | $0.8 * V_{SNVS}$ | 3.6 | V |
| VDDOTP | V_{IL} | – | 0.0 | 0.3 | V |
| | V_{IH} | – | 1.1 | 1.7 | V |

4.3.2 Current consumption

Table 7. Current consumption summary

Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{DDIO} = 1.7$ to 3.6 V, $LICELL = 1.8$ to 3.3 V, $V_{SNVS} = 3.0$ V, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{DDIO} = 3.3$ V, $LICELL = 3.0$ V, $V_{SNVS} = 3.0$ V and 25 °C, unless otherwise noted.

| Mode | PF0200 conditions | System Conditions | Typ. | Max. | Unit |
|-----------------------------|---|--|------|---------------------|---------|
| Coin Cell (15),(16),(19) | VSNVS from LICELL All other blocks off $V_{IN} = 0.0$ V $V_{SNVSVOLT}[2:0] = 110$ | No load on VSNVS | 4.0 | 7.0 | μ A |
| Off (15)(17) | VSNVS from VIN or LICELL Wake-up from PWRON active 32 k RC on All other blocks off $V_{IN} \geq UVDET$ | No load on VSNVS, PMIC able to wake-up | 17 | 25 | μ A |
| Sleep (18) | VSNVS from VIN Wake-up from PWRON active Trimmed reference active SW3A/B PFM Trimmed 16 MHz RC off 32 k RC on VREFDDR disabled | No load on VSNVS. DDR memories in self refresh | 122 | 220 ⁽²⁰⁾ | μ A |
| | | | 122 | 250 ⁽²¹⁾ | |
| Standby (18) | VSNVS from either VIN or LICELL SW1A/B combined in PFM SW2 in PFM SW3A/B combined in PFM SWBST off Trimmed 16 MHz RC enabled Trimmed reference active VGEN1-6 enabled VREFDDR enabled | No load on VSNVS. Processor enabled in low power mode. All rails powered on except boost (load = 0 mA) | 270 | 430 ⁽²⁰⁾ | μ A |
| | | | 270 | 525 ⁽²¹⁾ | |

Notes

15. At 25 °C only.
16. Refer to [Figure 4](#) for Coin Cell mode characteristics over temperature.
17. When V_{IN} is below the UVDET threshold, in the range of 1.8 V $\leq V_{IN} < 2.65$ V, the quiescent current increases by 50 μ A, typically.
18. For PFM operation, headroom should be 300 mV or greater.
19. Additional current may be drawn in the coin cell mode when RESETBMCU is pulled up to VSNVS due an internal path from RESETBMCU to VIN. The additional current is <30 μ A with a pull up resistor of 100 k Ω . The i.MX 6 processors have an internal pull-up from the POR_B pin to the VDD_SNVS_IN pin. If additional current in the coin cell mode is not desired for i.MX6 applications, use an external switch to disconnect the RESETBMCU path when VIN is removed. Pull-up RESETBMCU to a rail that is off in the coin cell mode, for non-i.MX 6 applications.
20. From -40 to 85 °C, Applicable to Consumer and Extended Industrial part numbers
21. From -40 to 105 °C, Applicable only to Extended Industrial parts

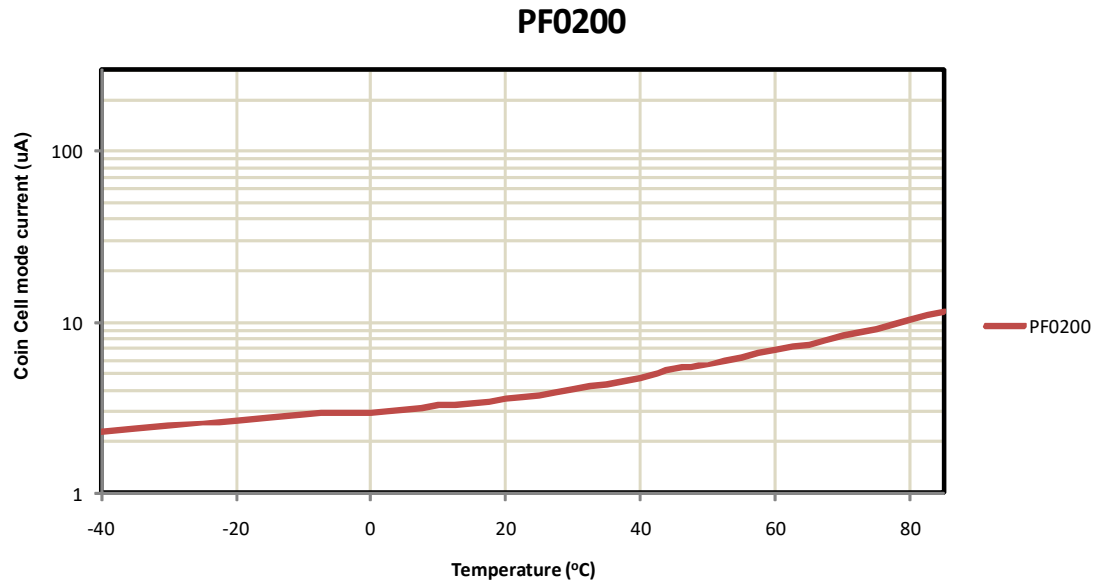


Figure 4. Coin cell mode current versus temperature

5 General description

The PF0200 is the Power Management Integrated Circuit (PMIC) designed primarily for use with NXP's i.MX 6 series of application processors.

5.1 Features

This section summarizes the PF0200 features.

- Input voltage range to PMIC: 2.8 - 4.5 V
- Buck regulators
 - Three to four channel configurable
 - SW1A/B, 2.5 A; 0.3 to 1.875 V
 - SW2, 1.5 A; 0.4 to 3.3 V
 - SW3A/B, 2.5 A (single phase); 0.4 to 3.3 V
 - SW3A, 1.25 A (independent); SW3B, 1.25 A (independent); 0.4 to 3.3 V
 - Dynamic voltage scaling
 - Modes: PWM, PFM, APS
 - Programmable output voltage
 - Programmable current limit
 - Programmable soft start
 - Programmable PWM switching frequency
 - Programmable OCP with fault interrupt
- Boost regulator
 - SWBST, 5.0 to 5.15 V, 0.6 A, OTG support
 - Modes: PFM and Auto
 - OCP fault interrupt
- LDOs
 - Six user programmable LDO
 - VGEN1, 0.80 to 1.55 V, 100 mA
 - VGEN2, 0.80 to 1.55 V, 250 mA
 - VGEN3, 1.8 to 3.3 V, 100 mA
 - VGEN4, 1.8 to 3.3 V, 350 mA
 - VGEN5, 1.8 to 3.3 V, 100 mA
 - VGEN6, 1.8 to 3.3 V, 200 mA
 - Soft start
 - LDO/Switch supply
 - VSNVS (1.0/1.1/1.2/1.3/1.5/1.8/3.0 V), 400 μ A
- DDR memory reference voltage
 - VREFDDR, 0.6 to 0.9 V, 10 mA
- 16 MHz internal master clock
- OTP(One time programmable) memory for device configuration
 - User programmable start-up sequence and timing
- Battery backed memory including coin cell charger
- I²C interface
- User programmable Standby, Sleep, and Off modes

5.2 Functional block diagram

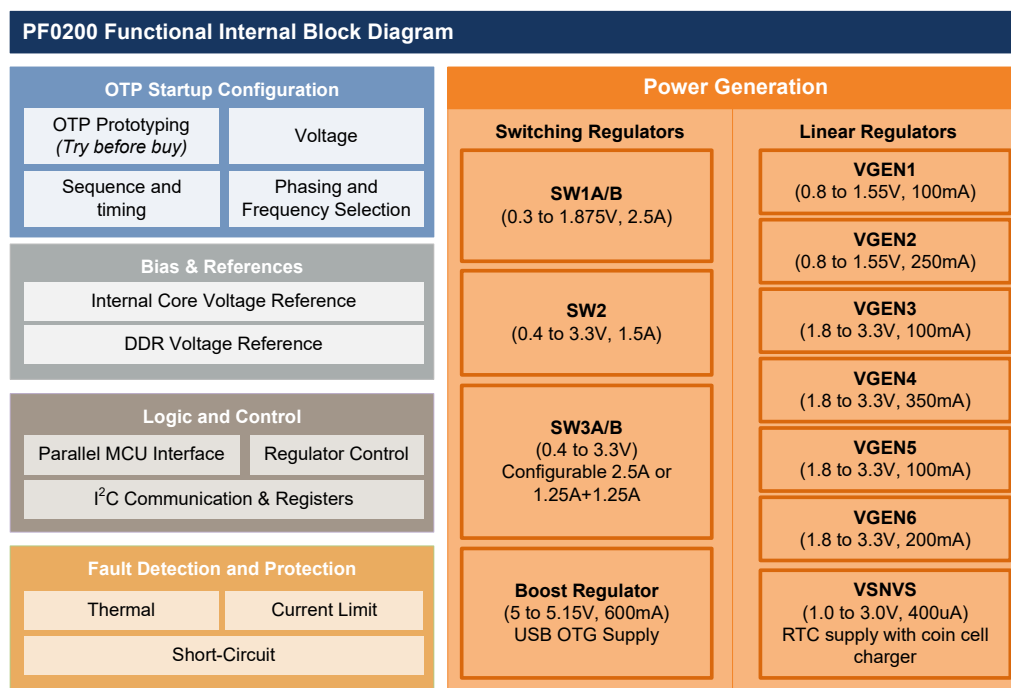


Figure 5. Functional block diagram

5.3 Functional description

5.3.1 Power generation

The PF0200 PMIC features three buck regulators (up to four independent outputs), one boost regulator, six general purpose LDOs, one switch/LDO combination and a DDR voltage reference to supply voltages for the application processor and peripheral devices.

The number of independent buck regulator outputs can be configured from three to four, thereby providing flexibility to operate with higher current capability, or to operate as independent outputs for applications requiring more voltage rails with lower current demands. The SW3 regulator can be configured as a single phase or with two independent outputs. The buck regulators provide the supply to processor cores and to other low-voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry.

Depending on the system power path configuration, the six general purpose LDO regulators can be directly supplied from the main input supply or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. A specific VREFDDR voltage reference is included to provide accurate reference voltage for DDR memories operating with or without VTT termination. The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS/SRTC circuitry on the i.MX processors; VSNVS may be powered from VIN, or from a coin cell.

5.3.2 Control logic

The PF0200 PMIC is fully programmable via the I²C interface. Additional communication is provided by direct logic interfacing including interrupt and reset. Start-up sequence of the device is selected upon the initial OTP configuration explained in the [Start-up](#) section, or by configuring the “Try Before Buy” feature to test different power up sequences before choosing the final OTP configuration.

The PF0200 PMIC has the interfaces for the power buttons and dedicated signaling interfacing with the processor. It also ensures supply of critical internal logic and other circuits from the coin cell in case of brief interruptions from the main battery. A charger for the coin cell is included as well.

5.3.2.1 Interface signals

PWRON

PWRON is an input signal to the IC that generates a turn-on event. It can be configured to detect a level, or an edge using the PWRON_CFG bit. Refer to section [Turn on events](#) for more details.

STANDBY

STANDBY is an input signal to the IC. When it is asserted the part enters standby mode and when de-asserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit. Refer to the section [Standby mode](#) for more details.

Note: When operating the PMIC at $V_{IN} \leq 2.85$ V and VSNVS is programmed for a 3.0 V output, a coin cell must be present to provide VSNVS, or the PMIC will not reliably enter and exit the STANDBY mode.

RESETBMCU

RESETBMCU is an open-drain, active low output configurable for two modes of operation. In its default mode, it is de-asserted 2.0 to 4.0 ms after the last regulator in the start-up sequence is enabled; refer to [Figure 6](#) as an example. In this mode, the signal can be used to bring the processor out of reset, or as an indicator that all supplies have been enabled; it is only asserted for a turn-off event.

When configured for its fault mode, RESETBMCU is de-asserted after the start-up sequence is completed only if no faults occurred during start-up. At anytime, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted, LOW. The PF0200 is turned off if the fault persists for more than 100 ms typically. The PWRON signal restarts the part, though if the fault persists, the sequence described above will be repeated. To enter the fault mode, set bit OTP_PG_EN of register OTP PWRGD EN to "1". This register, 0xE8, is located on [Extended page 1](#) of the register map. To test the fault mode, the bit may be set during TBB prototyping, or the mode may be permanently chosen by programming OTP fuses.

SDWNB

SDWNB is an open-drain, active low output that notifies the processor of an imminent PMIC shutdown. It is asserted low for one 32 kHz clock cycle before powering down and is then de-asserted in the OFF state.

INTB

INTB is an open-drain, active low output. It is asserted when any fault occurs, provided that the fault interrupt is unmasked. INTB is de-asserted after the fault interrupt is cleared by software, which requires writing a "1" to the fault interrupt bit.

6 Functional block requirements and behaviors

6.1 Start-up

The PF0200 can be configured to start-up from either the internal OTP configuration, or with a hard-coded configuration built into the device. The internal hard-coded configuration is enabled by connecting the VDDOTP pin to VCOREDIG through a 100 kohm resistor. The OTP configuration is enabled by connecting VDDOTP to GND.

For NP devices, selecting the OTP configuration causes the PF0200 to not start-up. However, the PF0200 can be controlled through the I²C port for prototyping and programming. Once programmed, the NP device will startup with the customer programmed configuration.

6.1.1 Device start-up configuration

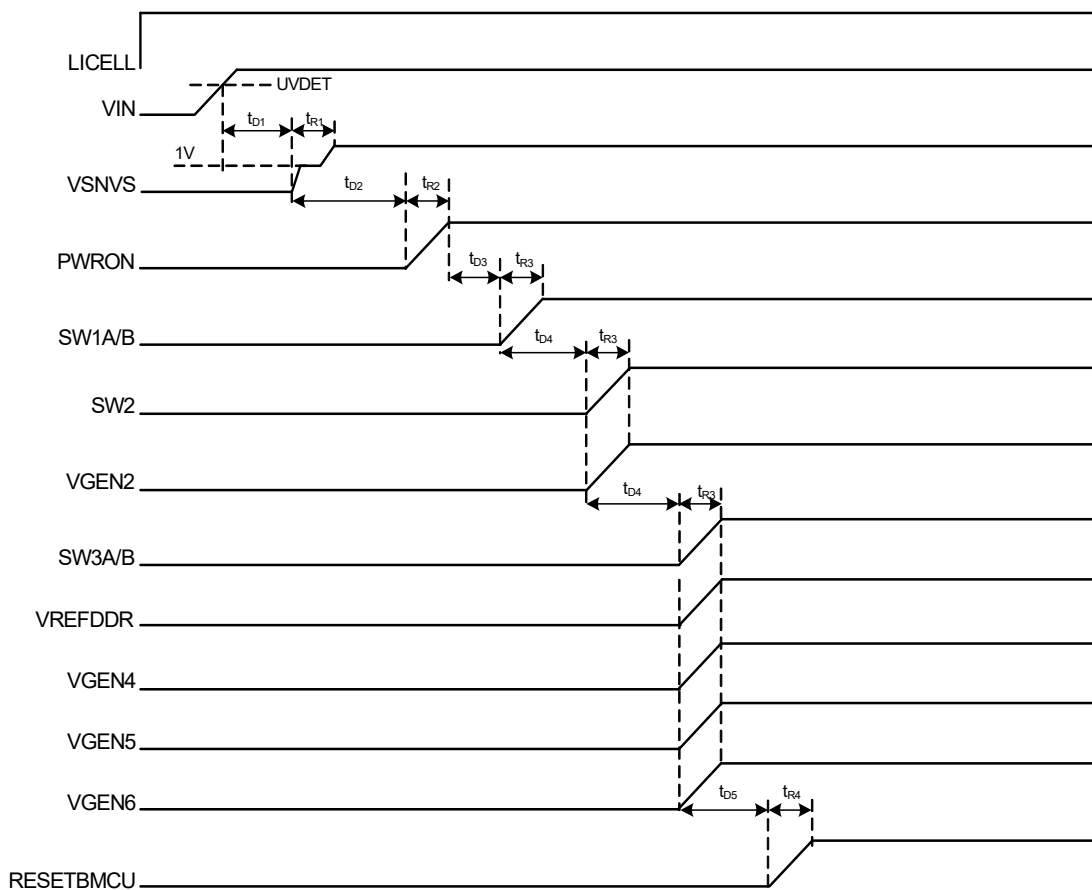
[Table 8](#) shows the Default Configuration which can be accessed on all devices as described above, as well as the pre-programmed OTP configurations.

Table 8. Start-up configuration

| Registers | Default configuration | Pre-programmed OTP configuration | | | |
|----------------------------------|-----------------------|----------------------------------|---------|---------|---------|
| | All devices | F0 | F3 | F4 | F6 |
| Default I ² C Address | 0x08 | 0x08 | 0x08 | 0x08 | 0x08 |
| VSNVS_VOLT | 3.0 V | 3.0 V | 3.0 V | 3.0 V | 3.0 V |
| SW1AB_VOLT | 1.375 V | 1.375 V | 1.375 V | 1.375 V | 1.375 V |
| SW1AB_SEQ | 1 | 1 | 2 | 2 | 2 |
| SW2_VOLT | 3.0 V | 3.3 V | 3.15 V | 3.15 V | 3.3 V |
| SW2_SEQ | 2 | 5 | 1 | 1 | 4 |
| SW3A_VOLT | 1.5 V | 1.5 V | 1.2 V | 1.5 V | 1.35 V |
| SW3A_SEQ | 3 | 3 | 4 | 4 | 3 |
| SW3B_VOLT | 1.5 V | 1.5 V | 1.2 V | 1.5 V | 1.35 V |
| SW3B_SEQ | 3 | 3 | 4 | 4 | 3 |
| SWBST_VOLT | - | 5.0 V | 5.0 V | 5.0 V | 5.0 V |
| SWBST_SEQ | - | 13 | 6 | 6 | - |
| VREFDDR_SEQ | 3 | 3 | 4 | 4 | 3 |
| VGEN1_VOLT | - | 1.5 V | 1.2 V | 1.2 V | 1.2 V |
| VGEN1_SEQ | - | 9 | 4 | 4 | 5 |
| VGEN2_VOLT | 1.5 V | 1.5 V | - | - | 1.5 V |
| VGEN2_SEQ | 2 | 10 | - | - | - |
| VGEN3_VOLT | - | 2.5 V | 1.8 V | 1.8 V | 2.8 V |
| VGEN3_SEQ | - | 11 | 3 | 3 | 5 |
| VGEN4_VOLT | 1.8 V | 1.8 V | 1.8 V | 1.8 V | 1.8 V |
| VGEN4_SEQ | 3 | 7 | 3 | 3 | 4 |
| VGEN5_VOLT | 2.5 V | 2.8 V | 2.5 V | 2.5 V | 3.3 V |
| VGEN5_SEQ | 3 | 12 | 5 | 5 | 5 |
| VGEN6_VOLT | 2.8 V | 3.3 V | - | - | 3.0 V |
| VGEN6_SEQ | 3 | 8 | - | - | 1 |

Table 8. Start-up configuration (continued)

| Registers | Default configuration | Pre-programmed OTP configuration | | | |
|--------------------------|-----------------------------|----------------------------------|------------------|------------------|------------------|
| | All devices | F0 | F3 | F4 | F6 |
| PU CONFIG, SEQ_CLK_SPEED | 1.0 ms | 2.0 ms | 1.0 ms | 1.0 ms | 0.5 ms |
| PU CONFIG, SWDVS_CLK | 6.25 mV/ μ s | 1.5625 mV/ μ s | 12.5 mV/ μ s | 12.5 mV/ μ s | 6.25 mV/ μ s |
| PU CONFIG, PWRON | Level sensitive | | | | |
| SW1AB CONFIG | SW1AB Single Phase, 2.0 MHz | | | | |
| SW2 CONFIG | 2.0 MHz | | | | |
| SW3A CONFIG | SW3AB Single Phase, 2.0 MHz | | | | |
| SW3B CONFIG | 2.0 MHz | | | | |
| PG EN | RESETBMCU in Default Mode | | | | |



*VSNVS will start from 1.0 V if LICELL is valid before VIN.

Figure 6. Default start-up sequence

Table 9. Default start-up sequence timing

| Parameter | Description | Min. | Typ. | Max. | Unit | Notes |
|-------------------------|----------------------------------|------|------|------|------|-------|
| t_{D1} | Turn-on delay of VSNVS | – | 5.0 | – | ms | (22) |
| t_{R1} | Rise time of VSNVS | – | 3.0 | – | ms | |
| t_{D2} | User determined delay | – | 1.0 | – | ms | |
| t_{R2} | Rise time of PWRON | – | (23) | – | ms | (23) |
| t_{D3} | Turn-on delay of first regulator | | | | | |
| | SEQ_CLK_SPEED[1:0] = 00 | – | 2.0 | – | ms | (24) |
| | SEQ_CLK_SPEED[1:0] = 01 | – | 2.5 | – | | |
| | SEQ_CLK_SPEED[1:0] = 10 | – | 4.0 | – | | |
| SEQ_CLK_SPEED[1:0] = 11 | – | 7.0 | – | | | |
| t_{R3} | Rise time of regulators | – | 0.2 | – | ms | (25) |
| t_{D4} | Delay between regulators | | | | | |
| | SEQ_CLK_SPEED[1:0] = 00 | – | 0.5 | – | ms | |
| | SEQ_CLK_SPEED[1:0] = 01 | – | 1.0 | – | | |
| | SEQ_CLK_SPEED[1:0] = 10 | – | 2.0 | – | | |
| SEQ_CLK_SPEED[1:0] = 11 | – | 4.0 | – | | | |
| t_{R4} | Rise time of RESETBMCU | – | 0.2 | – | ms | |
| t_{D5} | Turn-on delay of RESETBMCU | – | 2.0 | – | ms | |

Notes

22. Assumes LICELL voltage is valid before VIN is applied. If LICELL is not valid before VIN is applied then VSNVS turn-on delay may extend to a maximum of 24 ms.
23. Depends on the external signal driving PWRON.
24. Default configuration.
25. Rise time is a function of slew rate of regulators and nominal voltage selected.

6.1.2 One time programmability (OTP)

OTP allows the programming of start-up configurations for a variety of applications. Before permanently programming the IC by programming fuses, a configuration may be prototyped by using the “Try Before Buy” (TBB) feature. An error correction code(ECC) algorithm is available to correct a single bit error and to detect multiple bit errors when fuses are programmed.

The parameters that can be configured by OTP are listed below.

- General: I²C slave address, PWRON pin configuration, start-up sequence and timing
- Buck regulators: Output voltage, single phase or independent mode configuration, switching frequency, and soft start ramp rate
- Boost regulator and LDOs: Output voltage

NOTE: When prototyping or programming fuses, the user must ensure that register settings are consistent with the hardware configuration. This is most important for the buck regulators, where the quantity, size, and value of the inductors depend on the configuration (single phase or independent mode) and the switching frequency. Additionally, if an LDO is powered by a buck regulator, it will be gated by the buck regulator in the start-up sequence.

6.1.2.1 Start-up sequence and timing

Each regulator has 5-bits allocated to program its start-up time slot from a turn on event; therefore, each can be placed from position one to thirty-one in the start-up sequence. The all zeros code indicates that a regulator is not part of the start-up sequence and will remain off. See [Table 10](#). The delay between each position is equal; however, four delay options are available. See [Table 11](#). The start-up sequence will terminate at the last programmed regulator.

Table 10. Start-up sequence

| SWxx_SEQ[4:0]/ VGENx_SEQ[4:0]/ VREFDDR_SEQ[4:0] | Sequence |
|---|-------------------------|
| 00000 | Off |
| 00001 | SEQ_CLK_SPEED[1:0] * 1 |
| 00010 | SEQ_CLK_SPEED[1:0] * 2 |
| * | * |
| * | * |
| * | * |
| * | * |
| 11111 | SEQ_CLK_SPEED[1:0] * 31 |

Table 11. Start-up sequence clock speed

| SEQ_CLK_SPEED[1:0] | Time (μ s) |
|--------------------|-----------------|
| 00 | 500 |
| 01 | 1000 |
| 10 | 2000 |
| 11 | 4000 |

6.1.2.2 PWRON pin configuration

The PWRON pin can be configured as either a level sensitive input (PWRON_CFG = 0), or as an edge sensitive input (PWRON_CFG = 1). As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into Sleep mode. As an edge sensitive input, such as when connected to a mechanical switch, a falling edge will turn on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part will turn off or enter Sleep mode.

Table 12. PWRON configuration

| PWRON_CFG | Mode |
|-----------|--|
| 0 | PWRON pin HIGH = ON PWRON pin LOW = OFF or Sleep mode |
| 1 | PWRON pin pulled LOW momentarily = ON PWRON pin LOW for 4.0 seconds = OFF or Sleep mode |

6.1.2.3 I²C address configuration

The I²C device address can be programmed from 0x08 to 0x0F. This allows flexibility to change the I²C address to avoid bus conflicts. Address bit, I2C_SLV_ADDR[3] in OTP_I2C_ADDR register is hard coded to "1" while the lower three LSBs of the I²C address (I2C_SLV_ADDR[2:0]) are programmable as shown in [Table 13](#).

Table 13. I²C address configuration

| I2C_SLV_ADDR[3] hard coded | I2C_SLV_ADDR[2:0] | I ² C device address (Hex) |
|-------------------------------|-------------------|--|
| 1 | 000 | 0x08 |
| 1 | 001 | 0x09 |
| 1 | 010 | 0x0A |
| 1 | 011 | 0x0B |

Table 13. I²C address configuration (continued)

| I2C_SLV_ADDR[3] hard coded | I2C_SLV_ADDR[2:0] | I ² C device address (Hex) |
|-------------------------------|-------------------|--|
| 1 | 100 | 0x0C |
| 1 | 101 | 0x0D |
| 1 | 110 | 0x0E |
| 1 | 111 | 0x0F |

6.1.2.4 Soft start ramp rate

The start-up ramp rate or soft start ramp rate can be chosen from the same options as shown in [Dynamic voltage scaling](#).

6.1.3 OTP prototyping

It is possible to test the desired configuration by using the “Try Before Buy” feature, before permanently programming fuses. The configuration is loaded from the OTP registers with this feature. These registers merely serve as temporary storage for the values to be written to the fuses, for the values read from the fuses, or for the values read from the default configuration. To avoid confusion, these registers will be referred to as the TBBOTP registers. The portion of the register map that concerns OTP is shown in [Table 121](#) and [Table 122](#).

The contents of the TBBOTP registers are initialized to zero when a valid VIN is first applied. The values that are then loaded into the TBBOTP registers depend on the setting of the VDDOTP pin and on the value of the TBB_POR and FUSE_POR_XOR bits. Refer to [Table 14](#).

- If VDDOTP = VCOREDIG (1.5 V), the values are loaded from the default configuration.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 1, the values are loaded from the fuses. It is required to set all the FUSE_PORx bits to load the fuses.
- If VDDOTP = 0.0 V, TBB_POR = 0 and FUSE_POR_XOR = 0, the TBBOTP registers remain initialized at zero.

The initial value of TBB_POR is always “0”; only when VDDOTP = 0.0 V and TBB_POR is set to “1” are the values from the TBBOTP registers maintained and not loaded from a different source.

The contents of the TBBOTP registers are modified by I²C. To communicate with I²C, VIN must be valid and VDDIO, to which SDA and SCL are pulled up, must be powered by a 1.7 to 3.6 V supply. V_{IN}, or the coin cell voltage must be valid to maintain the contents of the registers. To power on with the contents of the TBBOTP registers, the following conditions must exist; VIN is valid, VDDOTP = 0.0 V, TBB_POR = 1 and there is a valid turn-on event.

6.1.4 Reading OTP fuses

As described in the previous section, the contents of the fuses are loaded to the TBBOTP registers. When the following conditions are met; VIN is valid, VDDOTP = 0.0 V, TBB_POR = 0, and FUSE_POR_XOR = 1. If ECC is enabled at the time the fuses were programmed, the error corrected values can be loaded into the TBBOTP registers if desired. Once the fuses are loaded and a turn-on event occurs, the PMIC will power on with the configuration programmed in the fuses. Contact your NXP representative for more details on reading the OTP fuses.

6.1.5 Programming OTP fuses

The parameters that can be programmed are shown in the TBBOTP registers in the [Extended page 1](#) of the register map. The PF0200 offers ECC, the control registers for which functions are located in [Extended page 2](#) of the register map. There are ten banks of twenty-six fuses, each that can be programmed.

Table 14. Source of start-up sequence

| VDDOTP(V) | TBB_POR | FUSE_POR_XOR | Start-up sequence |
|-----------|---------|--------------|-------------------|
| 0 | 0 | 0 | None |
| 0 | 0 | 1 | OTP fuses |
| 0 | 1 | x | TBBOTP registers |
| 1.5 | x | x | Factory defined |

6.2 16 MHz and 32 kHz clocks

There are two clocks: a trimmed 16 MHz, RC oscillator and an untrimmed 32 kHz, RC oscillator. The 16 MHz oscillator is specified within -8.0/+8.0%. The 32 kHz untrimmed clock is only used in the following conditions:

- $V_{IN} < UVDET$
- All regulators are in SLEEP mode
- All regulators are in PFM switching mode

A 32 kHz clock, derived from the 16 MHz trimmed clock, is used when accurate timing is needed under the following conditions:

- During start-up, $V_{IN} > UVDET$
- $PWRON_CFG = 1$, for power button debounce timing

In addition, when the 16 MHz is active in the ON mode, the debounce times in [Table 25](#) are referenced to the 32 kHz derived from the 16 MHz clock. The exceptions are the LOWVINI and PWRONI interrupts, which are referenced to the 32 kHz untrimmed clock.

Table 15. 16 MHz clock specifications

Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 2.8$ to 4.5 V, LICELL = 1.8 to 3.3 V and typical external component values. Typical values are characterized at $V_{IN} = 3.6$ V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

| Symbol | Parameters | Min. | Typ. | Max. | Units | Notes |
|---------------|----------------------------|------|------|------|-------|-------|
| $V_{IN16MHz}$ | Operating Voltage From VIN | 2.8 | – | 4.5 | V | |
| f_{16MHz} | 16 MHz Clock Frequency | 14.7 | 16 | 17.3 | MHz | |
| f_{2MHz} | 2.0 MHz Clock Frequency | 1.84 | – | 2.16 | MHz | (26) |

Notes

26. 2.0 MHz clock is derived from the 16 MHz clock.

6.2.1 Clock adjustment

The 16 MHz clock and hence the switching frequency of the regulators, can be adjusted to improve the noise integrity of the system. By changing the factory trim values of the 16MHz clock, the user may add an offset as small as $\pm 3.0\%$ of the nominal frequency.

6.3 Bias and references block description

6.3.1 Internal core voltage references

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREF. The bandgap and the rest of the core circuitry are supplied from VCORE. The performance of the regulators is directly dependent on the performance of the bandgap. No external DC loading is allowed on VCORE, VCOREDIG, or VCOREREF. VCOREDIG is kept powered as long as there is a valid supply and/or valid coin cell. [Table 16](#) shows the main characteristics of the core circuitry.

Table 16. Core voltages electrical specifications⁽²⁸⁾

Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 2.8$ to 4.5 V, LICELL = 1.8 to 3.3 V, and typical external component values. Typical values are characterized at $V_{IN} = 3.6$ V, LICELL = 3.0 V, and 25 °C, unless otherwise noted.

| Symbol | Parameters | Min. | Typ. | Max. | Units | Notes |
|---|--|------|-------|------|-------|-------|
| VCOREDIG (digital core supply) | | | | | | |
| $V_{COREDIG}$ | Output Voltage ON mode | – | 1.5 | – | V | (27) |
| | Coin cell mode and OFF | – | 1.3 | – | | |
| VCORE (Analog core supply) | | | | | | |
| V_{CORE} | Output Voltage ON mode and charging | – | 2.775 | – | V | (27) |
| | OFF and Coin cell mode | – | 0.0 | – | | |
| VCOREREF (bandgap / regulator reference) | | | | | | |
| $V_{COREREF}$ | Output Voltage | – | 1.2 | – | V | (27) |
| $V_{COREREFACC}$ | Absolute Accuracy | – | 0.5 | – | % | |
| $V_{COREREFTEMP}$ | Temperature Drift | – | 0.25 | – | % | |

Notes

27. 3.0 V $< V_{IN} < 4.5$ V, no external loading on VCOREDIG, VCORE, or VCOREREF. Extended operation down to UVDET, but no system malfunction.

28. For information only.

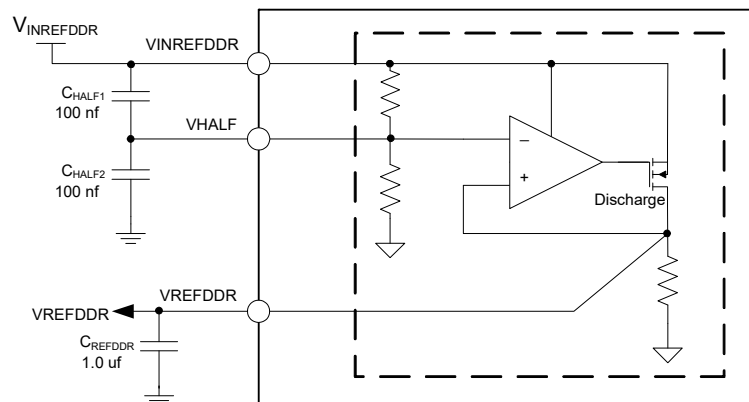
6.3.1.1 External components

Table 17. External components for core voltages

| Regulator | Capacitor value (μ F) |
|-----------|----------------------------|
| VCOREDIG | 1.0 |
| VCORE | 1.0 |
| VCOREREF | 0.22 |

6.3.2 VREFDDR voltage reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. Its typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low-frequency pole. This divider then utilizes a voltage follower to drive the load.

**Figure 7. VREFDDR block diagram**

6.3.2.1 VREFDDR control register

The VREFDDR voltage reference is controlled by a single bit in VREFDDCTRL register in [Table 18](#).

Table 18. Register VREFDDCTRL - ADDR 0x6A

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| UNUSED | 3:0 | – | 0x00 | UNUSED |
| VREFDDREN | 4 | R/W | 0x00 | Enable or disables VREFDDR output voltage 0 = VREFDDR Disabled 1 = VREFDDR Enabled |
| UNUSED | 7:5 | – | 0x00 | UNUSED |

External components

Table 19. VREFDDR external components⁽²⁹⁾

| Capacitor | Capacitance (μF) |
|------------------------------------|------------------|
| VINREFDDR ⁽³⁰⁾ to VHALF | 0.1 |
| VHALF to GND | 0.1 |
| VREFDDR | 1.0 |

Notes

29. Use X5R or X7R capacitors.

30. VINREFDDR to GND, 1.0 μF minimum capacitance is provided by buck regulator output.

VREFDDR specifications

Table 20. VREFDDR electrical characteristics

Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $I_{REFDDR} = 0.0$ mA, $V_{INREFDDR} = 1.5$ V and typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $I_{REFDDR} = 0.0$ mA, $V_{INREFDDR} = 1.5$ V, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|-----------------|---|------|------|------|------|-------|
| VREFDDR | | | | | | |
| $V_{INREFDDR}$ | Operating Input Voltage Range | 1.2 | – | 1.8 | V | |
| I_{REFDDR} | Operating Load Current Range | 0.0 | – | 10 | mA | |
| $I_{REFDDRLIM}$ | Current Limit I_{REFDDR} when V_{REFDDR} is forced to $V_{INREFDDR}/4$ | 10.5 | 15 | 25 | mA | |
| $I_{REFDDRQ}$ | Quiescent Current | – | 8.0 | – | μA | (31) |

Active mode – DC

| | | | | | | |
|-----------------|---|-------|------------------|-----|-------|--|
| V_{REFDDR} | Output Voltage 1.2 V < $V_{INREFDDR}$ < 1.8 V 0.0 mA < I_{REFDDR} < 10 mA | – | $V_{INREFDDR}/2$ | – | V | |
| $V_{REFDDRTOL}$ | Output Voltage Tolerance ($T_A = -40$ to 85 °C) 1.2 V < $V_{INREFDDR}$ < 1.8 V 0.6 mA ≤ I_{REFDDR} ≤ 10 mA | –1.0 | – | 1.0 | % | |
| $V_{REFDDRTOL}$ | Output Voltage Tolerance ($T_A = -40$ to 85 °C), applicable only to the extended Industrial version 1.2 V < $V_{INREFDDR}$ < 1.8 V 0.6 mA ≤ I_{REFDDR} ≤ 10 mA | –1.20 | – | 1.2 | % | |
| $V_{REFDDRLOR}$ | Load Regulation 1.0 mA < I_{REFDDR} < 10 mA 1.2 V < $V_{INREFDDR}$ < 1.8 V | – | 0.40 | – | mV/mA | |

Table 20. VREFDDR electrical characteristics (continued)

Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $I_{REFDDR} = 0.0$ mA, $V_{INREFDDR} = 1.5$ V and typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $I_{REFDDR} = 0.0$ mA, $V_{INREFDDR} = 1.5$ V, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|-------------------------|--|------|------|------|---------|-------|
| Active mode – AC | | | | | | |
| $t_{ONREFDDR}$ | Turn-on Time Enable to 90% of end value $V_{INREFDDR} = 1.2$ V, 1.8 V $I_{REFDDR} = 0.0$ mA | – | – | 100 | μ s | |
| $t_{OFFREFDDR}$ | Turn-off Time Disable to 10% of initial value $V_{INREFDDR} = 1.2$ V, 1.8 V $I_{REFDDR} = 0.0$ mA | – | – | 10 | ms | |
| $V_{REFDDROSH}$ | Start-up Overshoot $V_{INREFDDR} = 1.2$ V, 1.8 V $I_{REFDDR} = 0.0$ mA | – | 1.0 | 6.0 | % | |
| $V_{REFDRTLRL}$ | Transient Load Response $V_{INREFDDR} = 1.2$ V, 1.8 V | – | 5.0 | – | mV | |

Notes

31. When VREFDDR is off there is a quiescent current of 1.5 μ A typical.

6.4 Power generation

6.4.1 Modes of operation

The operation of the PF0200 can be reduced to five states, or modes: ON, OFF, Sleep, Standby, and Coin Cell. [Figure 8](#) shows the state diagram of the PF0200, along with the conditions to enter and exit from each state.

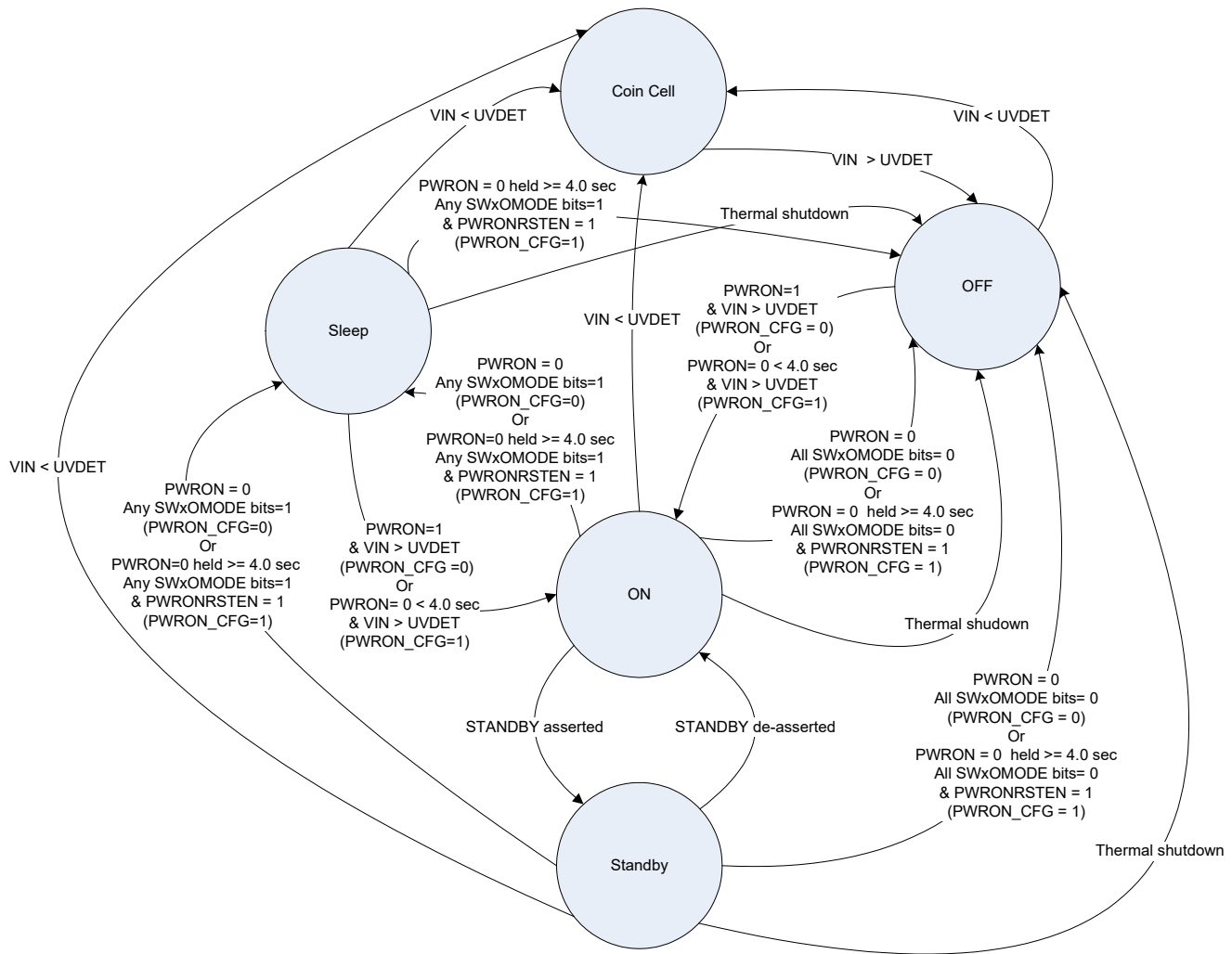


Figure 8. State diagram

To complement the state diagram in [Figure 8](#), a description of the states is provided in following sections. Note that V_{IN} must exceed the rising UVDET threshold to allow a power up. Refer to [Table 27](#) for the UVDET thresholds. Additionally, I²C control is not possible in the Coin Cell mode and the interrupt signal, INTB, is only active in Sleep, Standby, and ON states.

6.4.1.1 ON mode

The PF0200 enters the On mode after a turn-on event. RESETBMCU is de-asserted, high, in this mode of operation.

6.4.1.2 OFF mode

The PF0200 enters the Off mode after a turn-off event. A thermal shutdown event also forces the PF0200 into the Off mode. Only VCOREDIG and VSNVS are powered in the mode of operation. To exit the Off mode, a valid turn-on event is required. RESETBMCU is asserted, LOW, in this mode.

6.4.1.3 Standby mode

- Depending on STANDBY pin configuration, Standby is entered when the STANDBY pin is asserted. This is typically used for low-power mode of operation.
- When STANDBY is de-asserted, Standby mode is exited.

A product may be designed to go into a Low-power mode after periods of inactivity. The STANDBY pin is provided for board level control of going in and out of such deep sleep modes (DSM).

When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the regulators or disabling some regulators. The configuration of the regulators in Standby is pre-programmed through the I²C interface.

Note that the STANDBY pin is programmable for Active High or Active Low polarity, and that decoding of a Standby event will take into account the programmed input polarity as shown in [Table 21](#). When the PF0200 is powered up first, regulator settings for the Standby mode are mirrored from the regulator settings for the ON mode. To change the STANDBY pin polarity to Active Low, set the STANDBYINV bit via software first, and then change the regulator settings for Standby mode as required. For simplicity, STANDBY will generally be referred to as active high throughout this document.

Table 21. Standby Pin and polarity control

| STANDBY (Pin) ⁽³³⁾ | STANDBYINV (I ² C bit) ⁽³⁴⁾ | STANDBY Control ⁽³²⁾ |
|-------------------------------|---|---------------------------------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Notes

- 32. STANDBY = 0: System is not in Standby, STANDBY = 1: System is in Standby
- 33. The state of the STANDBY pin only has influence in On mode.
- 34. Bit 6 in Power Control Register (ADDR - 0x1B)

Since STANDBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a Standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into Standby mode.

When enabled (STBYDLY = 01, 10, or 11) per [Table 22](#), STBYDLY will delay the Standby initiated response for the entire IC, until the STBYDLY counter expires. An allowance should be made for three additional 32 k cycles required to synchronize the Standby event.

Table 22. STANDBY delay - initiated response

| STBYDLY[1:0] ⁽³⁵⁾ | Function |
|------------------------------|---------------------------|
| 00 | No Delay |
| 01 | One 32 k period (default) |
| 10 | Two 32 k periods |
| 11 | Three 32 k periods |

Notes

- 35. Bits [5:4] in Power Control Register (ADDR - 0x1B)

6.4.1.4 Sleep mode

- Depending on PWRON pin configuration, Sleep mode is entered when PWRON is de-asserted and SWxOMODE bit is set.
- To exit Sleep mode, assert the PWRON pin.

In the Sleep mode, the regulator will use the set point as programmed by SW1ABOFF[5:0] for SW1A/B and by SWxOFF[6:0] for SW2 and SW3A/B. The activated regulators will maintain settings for this mode and voltage until the next turn-on event. [Table 23](#) shows the control bits in Sleep mode. During Sleep mode, interrupts are active and the INTB pin will report any unmasked fault event.

Table 23. Regulator mode control

| SWxOMODE | Off operational mode (sleep) ⁽³⁶⁾ |
|----------|--|
| 0 | Off |
| 1 | PFM |

Notes

36. For sleep mode, an activated switching regulator, should use the off mode set point as programmed by SW1ABOFF[5:0] for SW1A/B and SWxOFF[6:0] for SW2 and SW3A/B.

6.4.1.5 Coin cell mode

In the Coin Cell state, the coin cell is the only valid power source ($V_{IN} = 0.0\text{ V}$) to the PMIC. No turn-on event is accepted in the Coin Cell state. Transition to the OFF state requires that V_{IN} surpasses UVDET threshold. RESETBMCU is held low in this mode.

If the coin cell is depleted, a complete system reset will occur. At the next application of power and the detection of a Turn-on event, the system will be re-initialized with all I²C bits including those that reset on COINPORB, are restored to their default states.

6.4.2 State machine flow summary

[Table 24](#) provides a summary matrix of the PF0200 flow diagram to show the conditions needed to transition from one state to another.

Table 24. State machine flow summary

| STATE | | Next state | | | | | |
|---------------|-----------|--|------------------|--|------------------|---|---|
| | | OFF | Coin cell | Sleep | Standby | ON | |
| Initial State | OFF | X | $V_{IN} < UVDET$ | X | X | PWRON_CFG = 0 PWRON = 1 & $V_{IN} > UVDET$ or PWRON_CFG = 1 PWRON = 0 < 4.0 s & $V_{IN} > UNDET$ | |
| | Coin cell | $V_{IN} > UVDET$ | X | X | X | X | |
| | Sleep | Thermal Shutdown | $V_{IN} < UVDET$ | X | X | X | PWRON_CFG = 0 PWRON = 1 & $V_{IN} > UVDET$ or PWRON_CFG = 1 PWRON = 0 < 4.0 s & $V_{IN} > UNDET$ |
| | | PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s Any SWxOMODE = 1 & PWRONRSTEN = 1 | | | | | |
| | Standby | Thermal Shutdown | $V_{IN} < UVDET$ | PWRON_CFG = 0 PWRON = 0 Any SWxOMODE = 1 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s Any SWxOMODE = 1 & PWRONRSTEN = 1 | X | Standby de-asserted | |
| | | PWRON_CFG = 0 PWRON = 0 All SWxOMODE = 0 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s All SWxOMODE = 0 & PWRONRSTEN = 1 | | | | | |
| | ON | Thermal Shutdown | $V_{IN} < UVDET$ | PWRON_CFG = 0 PWRON = 0 Any SWxOMODE = 1 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s Any SWxOMODE = 1 & PWRONRSTEN = 1 | Standby asserted | X | |
| | | PWRON_CFG = 0 PWRON = 0 All SWxOMODE = 0 or PWRON_CFG = 1 PWRON = 0 ≥ 4.0 s All SWxOMODE = 0 & PWRONRSTEN = 1 | | | | | |

6.4.2.1 Turn on events

From OFF and Sleep modes, the PMIC is powered on by a turn-on event. The type of Turn-on event depends on the configuration of PWRON. PWRON may be configured as an active high when PWRON_CFG = 0, or as the input of a mechanical switch when PWRON_CFG = 1. V_{IN} must be greater than UVDET for the PMIC to turn-on. When PWRON is configured as an active high and PWRON is high (pulled up to VSNVS) before V_{IN} is valid, a V_{IN} transition from 0.0 V to a voltage greater than UVDET is also a Turn-on event. See the State diagram, [Figure 8](#), and the [Table 24](#) for more details. Any regulator enabled in the Sleep mode will remain enabled when transitioning from Sleep to ON, i.e., the regulator will not be turned off and then on again to match the start-up sequence. The following is a more detailed description of the PWRON configurations:

- If PWRON_CFG = 0, the PWRON signal is high and $V_{IN} > UVDET$, the PMIC will turn on; the interrupt and sense bits, PWRONI and PWRONS respectively, will be set.
- If PWRON_CFG = 1, $V_{IN} > UVDET$ and PWRON transitions from high to low, the PMIC will turn on; the interrupt and sense bits, PWRONI and PWRONS respectively, will be set.

The sense bit will show the real time status of the PWRON pin. In this configuration, the PWRON input can be a mechanical switch debounced through a programmable debouncer, PWRONDBNC[1:0], to avoid a response to a very short (i.e., unintentional) key press. The interrupt is generated for both the falling and the rising edge of the PWRON pin. By default, a 30 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONDBNC[1:0] as defined in the table below. The interrupt is cleared by software, or when cycling through the OFF mode.

Table 25. PWRON hardware debounce bit settings

| Bits | State | Turn on debounce (ms) | Falling edge INT debounce (ms) | Rising edge INT debounce (ms) |
|----------------|-------|-----------------------|--------------------------------|-------------------------------|
| PWRONDBNC[1:0] | 00 | 0.0 | 31.25 | 31.25 |
| | 01 | 31.25 | 31.25 | 31.25 |
| | 10 | 125 | 125 | 31.25 |
| | 11 | 750 | 750 | 31.25 |

Notes

37. The sense bit, PWRONS, is not debounced and follows the state of the PWRON pin.

6.4.2.2 Turn off events

PWRON pin

The PWRON pin is used to power off the PF0200. The PWRON pin can be configured with OTP to power off the PMIC under the following two conditions:

1. PWRON_CFG bit = 0, SWxOMODE bit = 0 and PWRON pin is low.
2. PWRON_CFG bit = 1, SWxOMODE bit = 0, PWRONRSTEN = 1 and PWRON is held low for longer than 4.0 seconds. Alternatively, the system can be configured to restart automatically by setting the RESTARTEN bit.

Thermal protection

If the die temperature surpasses a given threshold, the thermal protection circuit will power off the PMIC to avoid damage. A turn-on event will not power on the PMIC while it is in thermal protection. The part will remain in Off mode until the die temperature decreases below a given threshold. There are no specific interrupts related to this other than the warning interrupt. See [Power dissipation](#) section for more detailed information.

Undervoltage detection

When the voltage at VIN drops below the undervoltage falling threshold, UVDET, the state machine will transition to the Coin Cell mode.

6.4.3 Power tree

The PF0200 PMIC features four buck regulators, one boost regulator, six general purpose LDOs, one switch/LDO combination, and a DDR voltage reference to supply voltages for the application processor and peripheral devices. The buck regulators as well as the boost regulator are supplied directly from the main input supply (V_{IN}). The inputs to all of the buck regulators must be tied to V_{IN} , whether they are powered on or off. The six general use LDO regulators are directly supplied from the main input supply or from the switching regulators depending on the application requirements. Since VREFDDR is intended to provide DDR memory reference voltage, it should be supplied by any rail supplying voltage to DDR memories; the typical application recommends the use of SW3 as the input supply for VREFDDR. VSNVS is supplied by either the main input supply or the coin cell. Refer to [Table 26](#) for a summary of all power supplies provided by the PF0200.

Table 26. Power tree summary

| Supply | Output voltage (V) | Step size (mV) | Maximum load current (mA) |
|---------|---------------------|----------------|---------------------------|
| SW1A/B | 0.3 - 1.875 | 25 | 2500 |
| SW2 | 0.4 - 3.3 | 25/50 | 1500 |
| SW3A/B | 0.4 - 3.3 | 25/50 | 1250 ⁽³⁸⁾ |
| SWBST | 5.00/5.05/5.10/5.15 | 50 | 600 |
| VGEN1 | 0.80 - 1.55 | 50 | 100 |
| VGEN2 | 0.80 - 1.55 | 50 | 250 |
| VGEN3 | 1.8 - 3.3 | 100 | 100 |
| VGEN4 | 1.8 - 3.3 | 100 | 350 |
| VGEN5 | 1.8 - 3.3 | 100 | 100 |
| VGEN6 | 1.8 - 3.3 | 100 | 200 |
| VSNVS | 1.0 - 3.0 | NA | 0.4 |
| VREFDDR | 0.5*SW3A_OUT | NA | 10 |

Notes

38. Current rating per independent phase, when SW3A/B is set in single phase, current capability is up to 2500 mA.

[Figure 9](#) shows a simplified power map with various recommended options to supply the different block within the PF0200, as well as the typical application voltage domain on the i.MX 6 application processors. Note that each application power tree is dependent upon the system's voltage and current requirements, therefore a proper input voltage should be selected for the regulators.

The minimum operating voltage for the main V_{IN} supply is 2.8 V, for lower voltages proper operation is not guaranteed. However at initial power up, the input voltage must surpass the rising UVDET threshold before proper operation is guaranteed. Refer to the representative tables and text specifying each supply for information on performance metrics and operating ranges. [Table 27](#) summarizes the UVDET thresholds.

Table 27. UVDET threshold

| UVDET Threshold | V_{IN} |
|-----------------|----------|
| Rising | 3.1 V |
| Falling | 2.65 V |

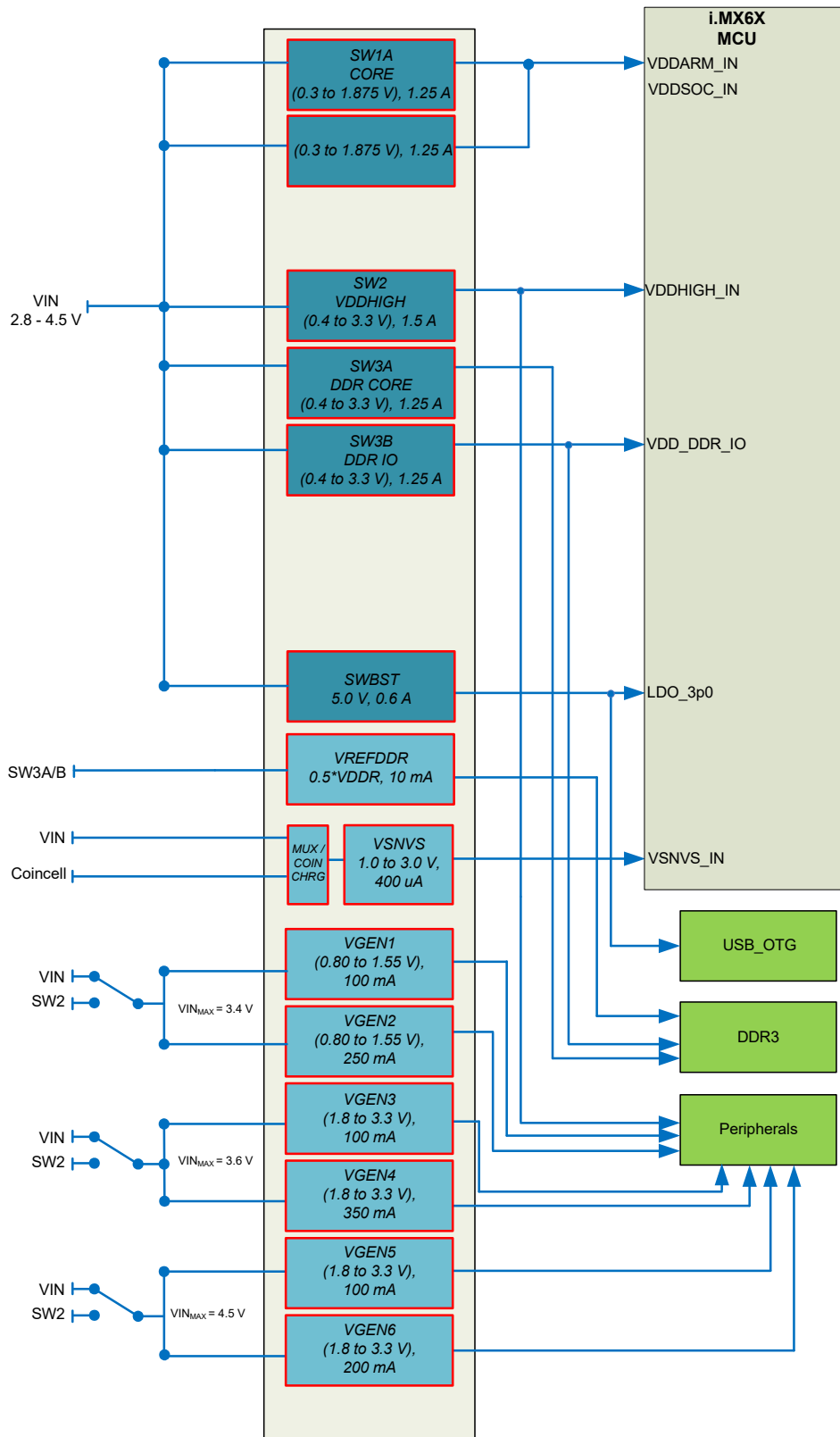


Figure 9. PF0200 typical power map

6.4.4 Buck regulators

Each buck regulator is capable of operating in PFM, APS, and PWM switching modes.

6.4.4.1 Current limit

Each buck regulator has a programmable current limit. In an overcurrent condition, the current is limited cycle-by-cycle. If the current limit condition persists for more than 8.0 ms, a fault interrupt is generated.

6.4.4.2 General control

To improve system efficiency the buck regulators can operate in different switching modes. Changing between switching modes can occur by any of the following means: I²C programming, exiting/entering the Standby mode, exiting/entering Sleep mode, and load current variation. Available switching modes for buck regulators are presented in [Table 28](#).

Table 28. Switching mode description

| Mode | Description |
|------|--|
| OFF | The regulator is switched off and the output voltage is discharged. |
| PFM | In this mode, the regulator is always in PFM mode, which is useful at light loads for optimized efficiency. |
| PWM | In this mode, the regulator is always in PWM mode operation regardless of load conditions. |
| APS | In this mode, the regulator moves automatically between pulse skipping mode and PWM mode depending on load conditions. |

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms (typical) after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes.

[Table 29](#) summarizes the Buck regulator programmability for Normal and Standby modes.

Table 29. Regulator mode control

| SWxMODE[3:0] | Normal mode | Standby mode |
|--------------|-------------|--------------|
| 0000 | Off | Off |
| 0001 | PWM | Off |
| 0010 | Reserved | Reserved |
| 0011 | PFM | Off |
| 0100 | APS | Off |
| 0101 | PWM | PWM |
| 0110 | PWM | APS |
| 0111 | Reserved | Reserved |
| 1000 | APS | APS |
| 1001 | Reserved | Reserved |
| 1010 | Reserved | Reserved |
| 1011 | Reserved | Reserved |
| 1100 | APS | PFM |
| 1101 | PWM | PFM |
| 1110 | Reserved | Reserved |
| 1111 | Reserved | Reserved |

Transitioning between Normal and Standby modes can affect a change in switching modes as well as output voltage. The rate of the output voltage change is controlled by the Dynamic Voltage Scaling (DVS), explained in [Dynamic voltage scaling](#). The output voltage options are the same for Normal and Standby modes for each regulator.

When in Standby mode, the regulator outputs the voltage programmed in its standby voltage register and will operate in the mode selected by the SWxMODE[3:0] bits. Upon exiting Standby mode, the regulator will return to its normal switching mode and its output voltage programmed in its voltage register.

Any regulators whose SWxOMODE bit is set to “1” will enter Sleep mode if a PWRON turn-off event occurs, and any regulator whose SWxOMODE bit is set to “0” will be turned off. In Sleep mode, the regulator outputs the voltage programmed in its off (Sleep) voltage register and operates in the PFM mode. The regulator will exit the Sleep mode when a turn-on event occurs. Any regulator whose SWxOMODE bit is set to “1” will remain on and change to its normal configuration settings when exiting the Sleep state to the ON state. Any regulator whose SWxOMODE bit is set to “0” will be powered up with the same delay in the start-up sequence as when powering On from Off. At this point, the regulator returns to its default ON state output voltage and switch mode settings.

[Table 23](#) shows the control bits in Sleep mode. When Sleep mode is activated by the SWxOMODE bit, the regulator will use the set point as programmed by SW1ABOFF[5:0] for SW1A/B and by SWxOFF[6:0] for SW2 and SW3A/B.

Dynamic voltage scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor.

1. Normal operation: The output voltage is selected by I²C bits SW1AB[5:0] for SW1A/B and SWx[6:0] for SW2 and SW3A/B. A voltage transition initiated by I²C is governed by the DVS stepping rates shown in [Table 32](#) and [Table 33](#).
2. Standby Mode: The output voltage can be higher, or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I²C bits SW1ABSTBY[5:0] for SW1A/B and by bits SWxSTBY[6:0] for SW2 and SW3A/B. Voltage transitions initiated by a Standby event are governed by the SW1ABDVSSPEED[1:0] and SWxDVSSPEED[1:0] I²C bits shown in [Table 32](#) and [Table 33](#), respectively.
3. Sleep Mode: The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I²C bits SW1ABOFF[5:0] for SW1A/B and by bits SWxOFF[6:0] for SW2, and SW3A/B. Voltage transitions initiated by a turn-off event are governed by the SW1ABDVSSPEED[1:0] and SWxDVSSPEED[1:0] I²C bits shown in [Table 32](#) and [Table 33](#), respectively.

[Table 30](#), [Table 31](#), [Table 32](#), and [Table 33](#) summarize the set point control and DVS time stepping applied to all regulators.

Table 30. DVS control logic for SW1A/B

| STANDBY | Set Point Selected by |
|---------|-----------------------|
| 0 | SW1AB[5:0] |
| 1 | SW1ABSTBY[5:0] |

Table 31. DVS control logic for SW2 and SW3A/B

| STANDBY | Set Point Selected by |
|---------|-----------------------|
| 0 | SWx[6:0] |
| 1 | SWxSTBY[6:0] |

Table 32. DVS speed selection for SW1A/B

| SW1ABDVSSPEED[1:0] | Function |
|--------------------|-----------------------------|
| 00 | 25 mV step each 2.0 μ s |
| 01 (default) | 25 mV step each 4.0 μ s |
| 10 | 25 mV step each 8.0 μ s |
| 11 | 25 mV step each 16 μ s |

Table 33. DVS speed selection for SW2 and SW3A/B

| SWxDVSSPEED[1:0] | Function SWx[6] = 0 or SWxSTBY[6] = 0 | Function SWx[6] = 1 or SWxSTBY[6] = 1 |
|------------------|--|--|
| 00 | 25 mV step each 2.0 μ s | 50 mV step each 4.0 μ s |
| 01 (default) | 25 mV step each 4.0 μ s | 50 mV step each 8.0 μ s |
| 10 | 25 mV step each 8.0 μ s | 50 mV step each 16 μ s |
| 11 | 25 mV step each 16 μ s | 50 mV step each 32 μ s |

The regulators have a strong sourcing capability and sinking capability in PWM mode, therefore the fastest rising and falling slopes are determined by the regulator in PWM mode. However, if the regulators are programmed in PFM or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

The following diagram shows the general behavior for the regulators when initiated with I²C programming, or standby control.

During the DVS period the overcurrent condition on the regulator should be masked.

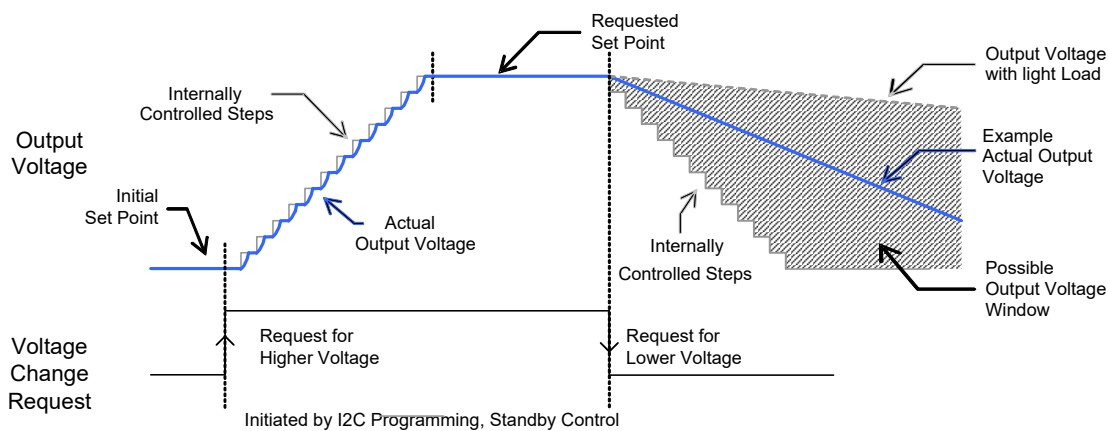


Figure 10. Voltage stepping with DVS

Regulator phase clock

The SWxPHASE[1:0] bits select the phase of the regulator clock as shown in [Table 34](#). By default, each regulator is initialized at 90 ° out of phase with respect to each other. For example, SW1A/B is set to 0 °, SW2 is set to 90 ° and SW3A/B is set to 180 ° by default at power up.

Table 34. Regulator phase clock selection

| SWxPHASE[1:0] | Phase of clock sent to regulator (degrees) |
|---------------|--|
| 00 | 0 |
| 01 | 90 |
| 10 | 180 |
| 11 | 270 |

The SWxFREQ[1:0] register is used to set the desired switching frequency for each one of the buck regulators. [Table 36](#) shows the selectable options for SWxFREQ[1:0]. For each frequency, all phases will be available, this allows regulators operating at different frequencies to have different relative switching phases. However, not all combinations are practical. For example, 2.0 MHz, 90 ° and 4.0 MHz, 180 ° are the same in terms of phasing. [Table 35](#) shows the optimum phasing when using more than one switching frequency.

Table 35. Optimum phasing

| Frequencies | Optimum phasing |
|-------------------------------|---------------------|
| 1.0 MHz 2.0 MHz | 0 ° 180 ° |
| 1.0 MHz 4.0 MHz | 0 ° 180 ° |
| 2.0 MHz 4.0 MHz | 0 ° 180 ° |
| 1.0 MHz 2.0 MHz 4.0 MHz | 0 ° 90 ° 90 ° |

Table 36. Regulator frequency configuration

| SWxFREQ[1:0] | Frequency |
|--------------|-----------|
| 00 | 1.0 MHz |
| 01 | 2.0 MHz |
| 10 | 4.0 MHz |
| 11 | Reserved |

Programmable maximum current

The maximum current, ISW_{xMAX} , of each buck regulator is programmable. This allows the use of smaller inductors where lower currents are required. Programmability is accomplished by choosing the number of paralleled power stages in each regulator. The SWx_PWRSTG[2:0] bits on the [Extended page 2](#) of the register map control the number of power stages. See [Table 37](#) for the programmable options. Bit[0] must always be enabled to ensure the stage with the current sensor is chosen. The default setting, SWx_PWRSTG[2:0] = 111, represents the highest maximum current. The current limit for each option is also scaled by the percentage of power stages that are enabled.

Table 37. Programmable current configuration

| Regulators | Control bits | | | % of power stages enabled | Rated current (A) |
|------------|-------------------|---|---|---------------------------|-------------------|
| SW1AB | SW1AB_PWRSTG[2:0] | | | | $ISW1AB_{MAX}$ |
| | 0 | 0 | 1 | 40% | 1.0 |
| | 0 | 1 | 1 | 80% | 2.0 |
| | 1 | 0 | 1 | 60% | 1.5 |
| | 1 | 1 | 1 | 100% | 2.5 |
| SW2 | SW2_PWRSTG[2:0] | | | | $ISW2_{MAX}$ |
| | 0 | 0 | 1 | 38% | 0.55 |
| | 0 | 1 | 1 | 75% | 1.125 |
| | 1 | 0 | 1 | 63% | 0.95 |
| | 1 | 1 | 1 | 100% | 1.5 |
| SW3A | SW3A_PWRSTG[2:0] | | | | $ISW3A_{MAX}$ |
| | 0 | 0 | 1 | 40% | 0.5 |
| | 0 | 1 | 1 | 80% | 1.0 |
| | 1 | 0 | 1 | 60% | 0.75 |
| | 1 | 1 | 1 | 100% | 1.25 |

Table 37. Programmable current configuration (continued)

| Regulators | Control bits | | | % of power stages enabled | Rated current (A) |
|------------|------------------|---|---|---------------------------|----------------------|
| SW3B | SW3B_PWRSTG[2:0] | | | | ISW3B _{MAX} |
| | 0 | 0 | 1 | 40% | 0.5 |
| | 0 | 1 | 1 | 80% | 1.0 |
| | 1 | 0 | 1 | 60% | 0.75 |
| | 1 | 1 | 1 | 100% | 1.25 |

6.4.4.3 SW1A/B

SW1A/B is a 2.5 A single phase regulator. The SW1ALX and SW1BLX pins should be connected together on the board. SW1_CONFIG[1:0] = 01 is the only configuration supported.

The single phase configuration is programmed by OTP by using SW1_CONFIG[1:0] bits in the register map [Extended page 1](#), as shown in [Table 38](#).

Table 38. SW1 configuration

| SW1_CONFIG[1:0] | Description |
|-----------------|------------------|
| 00 | Reserved |
| 01 | A/B Single Phase |
| 10 | Reserved |
| 11 | Reserved |

SW1A/B single phase

In this configuration, SW1A/B is connected as a single phase with a single inductor. This configuration allows reduced component count by using only one inductor for SW1A/B. [Figure 11](#) shows the physical connection for SW1A/B in single phase.

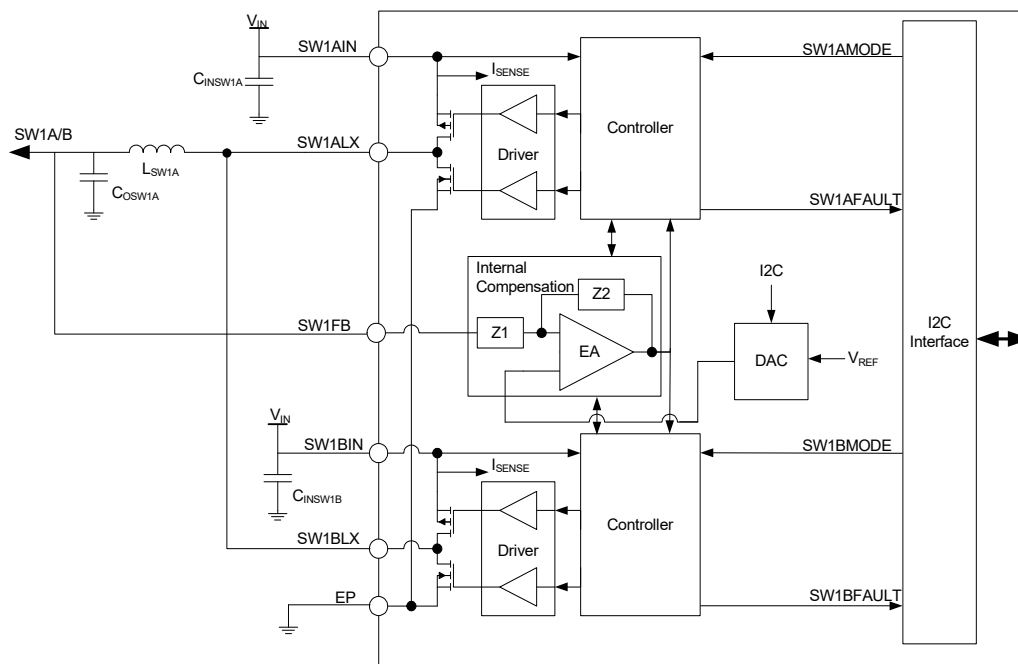


Figure 11. SW1A/B single phase block diagram

Both SW1ALX and SW1BLX nodes operate at the same DVS, frequency, and phase configured by the SW1ABCONF register.

SW1A/B setup and control registers

SW1A/B output voltage is programmable from 0.300 to 1.875 V in steps of 25 mV. The output voltage set point is independently programmed for Normal, Standby, and Sleep mode by setting the SW1AB[5:0], SW1ABSTBY[5:0], and SW1ABOFF[5:0] bits respectively. [Table 39](#) shows the output voltage coding for SW1A/B. Note: Output voltages of 0.6 V and below are not supported.

Table 39. SW1A/B output voltage configuration

| Set point | SW1AB[5:0] SW1ABSTBY[5:0] SW1ABOFF[5:0] | SW1AB output (V) | Set point | SW1AB[5:0] SW1ABSTBY[5:0] SW1ABOFF[5:0] | SW1AB output (V) |
|-----------|---|------------------|-----------|---|------------------|
| 0 | 000000 | 0.3000 | 32 | 100000 | 1.1000 |
| 1 | 000001 | 0.3250 | 33 | 100001 | 1.1250 |
| 2 | 000010 | 0.3500 | 34 | 100010 | 1.1500 |
| 3 | 000011 | 0.3750 | 35 | 100011 | 1.1750 |
| 4 | 000100 | 0.4000 | 36 | 100100 | 1.2000 |
| 5 | 000101 | 0.4250 | 37 | 100101 | 1.2250 |
| 6 | 000110 | 0.4500 | 38 | 100110 | 1.2500 |
| 7 | 000111 | 0.4750 | 39 | 100111 | 1.2750 |
| 8 | 001000 | 0.5000 | 40 | 101000 | 1.3000 |
| 9 | 001001 | 0.5250 | 41 | 101001 | 1.3250 |
| 10 | 001010 | 0.5500 | 42 | 101010 | 1.3500 |
| 11 | 001011 | 0.5750 | 43 | 101011 | 1.3750 |
| 12 | 001100 | 0.6000 | 44 | 101100 | 1.4000 |
| 13 | 001101 | 0.6250 | 45 | 101101 | 1.4250 |
| 14 | 001110 | 0.6500 | 46 | 101110 | 1.4500 |
| 15 | 001111 | 0.6750 | 47 | 101111 | 1.4750 |
| 16 | 010000 | 0.7000 | 48 | 110000 | 1.5000 |
| 17 | 010001 | 0.7250 | 49 | 110001 | 1.5250 |
| 18 | 010010 | 0.7500 | 50 | 110010 | 1.5500 |
| 19 | 010011 | 0.7750 | 51 | 110011 | 1.5750 |
| 20 | 010100 | 0.8000 | 52 | 110100 | 1.6000 |
| 21 | 010101 | 0.8250 | 53 | 110101 | 1.6250 |
| 22 | 010110 | 0.8500 | 54 | 110110 | 1.6500 |
| 23 | 010111 | 0.8750 | 55 | 110111 | 1.6750 |
| 24 | 011000 | 0.9000 | 56 | 111000 | 1.7000 |
| 25 | 011001 | 0.9250 | 57 | 111001 | 1.7250 |
| 26 | 011010 | 0.9500 | 58 | 111010 | 1.7500 |
| 27 | 011011 | 0.9750 | 59 | 111011 | 1.7750 |
| 28 | 011100 | 1.0000 | 60 | 111100 | 1.8000 |
| 29 | 011101 | 1.0250 | 61 | 111101 | 1.8250 |
| 30 | 011110 | 1.0500 | 62 | 111110 | 1.8500 |
| 31 | 011111 | 1.0750 | 63 | 111111 | 1.8750 |

[Table 40](#) provides a list of registers used to configure and operate SW1A/B and a detailed description on each one of these register is provided in [Table 41](#) through [Table 45](#).

Table 40. SW1A/B register summary

| Register | Address | Output |
|-----------|---------|--|
| SW1ABVOLT | 0x20 | SW1AB Output voltage set point in normal operation |
| SW1ABSTBY | 0x21 | SW1AB Output voltage set point on Standby |
| SW1ABOFF | 0x22 | SW1AB Output voltage set point on Sleep |
| SW1ABMODE | 0x23 | SW1AB Switching Mode selector register |
| SW1ABCONF | 0x24 | SW1AB DVS, Phase, Frequency and ILIM configuration |

Table 41. Register SW1ABVOLT - ADDR 0x20

| Name | Bit # | R/W | Default | Description |
|--------|-------|-----|---------|---|
| SW1AB | 5:0 | R/W | 0x00 | Sets the SW1AB output voltage during normal operation mode. See Table 39 for all possible configurations. |
| UNUSED | 7:6 | – | 0x00 | UNUSED |

Table 42. Register SW1ABSTBY - ADDR 0x21

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| SW1ABSTBY | 5:0 | R/W | 0x00 | Sets the SW1AB output voltage during Standby mode. See Table 39 for all possible configurations. |
| UNUSED | 7:6 | – | 0x00 | UNUSED |

Table 43. Register SW1ABOFF - ADDR 0x22

| Name | Bit # | R/W | Default | Description |
|----------|-------|-----|---------|--|
| SW1ABOFF | 5:0 | R/W | 0x00 | Sets the SW1AB output voltage during Sleep mode. See Table 39 for all possible configurations. |
| UNUSED | 7:6 | – | 0x00 | UNUSED |

Table 44. Register SW1ABMODE - ADDR 0x23

| Name | Bit # | R/W | Default | Description |
|------------|-------|-----|---------|--|
| SW1ABMODE | 3:0 | R/W | 0x80 | Sets the SW1AB switching operation mode. See Table 29 for all possible configurations. |
| UNUSED | 4 | – | 0x00 | UNUSED |
| SW1ABOMODE | 5 | R/W | 0x00 | Set status of SW1AB when in Sleep mode 0 = OFF 1 = PFM |
| UNUSED | 7:6 | – | 0x00 | UNUSED |

Table 45. Register SW1ABCONF - ADDR 0x24

| Name | Bit # | R/W | Default | Description |
|---------------|-------|-----|---------|--|
| SW1ABILIM | 0 | R/W | 0x00 | SW1AB current limit level selection 0 = High level current limit 1 = Low level current limit |
| UNUSED | 1 | R/W | 0x00 | Unused |
| SW1ABFREQ | 3:2 | R/W | 0x00 | SW1A/B switching frequency selector See Table 36 . |
| SW1ABPHASE | 5:4 | R/W | 0x00 | SW1A/B Phase clock selection See Table 34 . |
| SW1ABDVSSPEED | 7:6 | R/W | 0x00 | SW1A/B DVS speed selection See Table 32 . |

SW1A/B external components

Table 46. SW1A/B external component recommendations

| Components | Description | Mode |
|-------------------------------------|---------------------------------|--|
| | | A/B Single Phase |
| C _{INSW1A} ⁽³⁹⁾ | SW1A Input capacitor | 4.7 μ F |
| C _{IN1AHF} ⁽³⁹⁾ | SW1A Decoupling input capacitor | 0.1 μ F |
| C _{INSW1B} ⁽³⁹⁾ | SW1B Input capacitor | 4.7 μ F |
| C _{IN1BHF} ⁽³⁹⁾ | SW1B Decoupling input capacitor | 0.1 μ F |
| C _{OSW1AB} ⁽³⁹⁾ | SW1A/B Output capacitor | 4 x 22 μ F |
| L _{SW1A} | SW1A/B Inductor | 1.0 μ H DCR = 12 m Ω I _{SAT} = 4.5 A |

Notes

39. Use X5R or X7R capacitors.

SW1A/B specifications

Table 47. SW1A/B electrical characteristics

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SW1x}} = 3.6$ V, $V_{SW1AB} = 1.2$ V, $I_{SW1AB} = 100$ mA, SW1AB_PWRSTG[2:0] = [111], typical external component values, $f_{SW1AB} = 2.0$ MHz, unless otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SW1x}} = 3.6$ V, $V_{SW1AV} = 1.2$ V, $I_{SW1AB} = 100$ mA, SW1AB_PWRSTG[2:0] = [111], and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|------------------------------------|---|----------------------------|----------------------------------|----------------------------|---------|-------|
| SW1A/B (single phase) | | | | | | |
| $V_{IN_{SW1A}}$ $V_{IN_{SW1B}}$ | Operating Input Voltage | 2.8 | – | 4.5 | V | |
| V_{SW1AB} | Nominal Output Voltage | – | Table 39 | – | V | |
| $V_{SW1ABACC}$ | Output Voltage Accuracy <ul style="list-style-type: none"> PWM, APS, 2.8 V < V_{IN} < 4.5 V, $0 < I_{SW1AB} < 2.5$ A 0.625 V $\leq V_{SW1AB} \leq 1.450$ V 1.475 V $\leq V_{SW1AB} \leq 1.875$ V PFM, steady state, 2.8 V < V_{IN} < 4.5 V, $0 < I_{SW1AB} < 150$ mA 0.625 V < $V_{SW1AB} < 0.675$ V 0.7 V < $V_{SW1AB} < 0.85$ V 0.875 V < $V_{SW1AB} < 1.875$ V | -25 -3.0% | - - | 25 3.0% | mV % | (40) |
| I_{SW1AB} | Rated Output Load Current, 2.8 V < V_{IN} < 4.5 V, 0.625 V < $V_{SW1AB} < 1.875$ V | – | – | 2500 | mA | (41) |
| $I_{SW1ABLIM}$ | Current Limiter Peak Current Detection <ul style="list-style-type: none"> SW1A/B Single Phase (current through inductor) SW1ABILIM = 0 SW1ABILIM = 1 | 4.5 3.3 | 6.5 4.9 | 8.5 6.4 | A | (41) |
| $V_{SW1ABOSH}$ | Start-up Overshoot $I_{SW1AB} = 0.0$ mA DVS clk = 25 mV/4 μ s, $V_{IN} = V_{IN_{SW1x}} = 4.5$ V, $V_{SW1AB} = 1.875$ V | – | – | 66 | mV | |
| $t_{ON_{SW1AB}}$ | Turn-on Time Enable to 90% of end value $I_{SW1AB} = 0.0$ mA DVS clk = 25 mV/4 μ s, $V_{IN} = V_{IN_{SW1x}} = 4.5$ V, $V_{SW1AB} = 1.875$ V | – | – | 500 | μ s | |
| f_{SW1AB} | Switching Frequency SW1ABFREQ[1:0] = 00 SW1ABFREQ[1:0] = 01 SW1ABFREQ[1:0] = 10 | – – – | 1.0 2.0 4.0 | – – – | MHz | |
| η_{SW1AB} | Efficiency (Single Phase) <ul style="list-style-type: none"> $V_{IN} = 3.6$ V, $f_{SW1AB} = 2.0$ MHz, $L_{SW1AB} = 1.0$ μH PFM, 0.9 V, 1.0 mA PFM, 1.2 V, 50 mA APS, PWM, 1.2 V, 500 mA APS, PWM, 1.2 V, 750 mA APS, PWM, 1.2 V, 1250 mA APS, PWM, 1.2 V, 2500 mA | – – – – – – | 82 84 86 87 82 71 | – – – – – – | % | |
| ΔV_{SW1AB} | Output Ripple | – | 10 | – | mV | |
| $V_{SW1ABLIR}$ | Line Regulation (APS, PWM) | – | – | 20 | mV | |
| $V_{SW1ABLOR}$ | DC Load Regulation (APS, PWM) | – | – | 20 | mV | |
| $V_{SW1ABLOTR}$ | Transient Load Regulation <ul style="list-style-type: none"> Transient load = 0 to 1.25 A, $di/dt = 100$ mA/μs Overshoot Undershoot | – – | – – | 50 50 | mV | |

Table 47. SW1A/B electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SW1x}} = 3.6$ V, $V_{SW1AB} = 1.2$ V, $I_{SW1AB} = 100$ mA, $SW1AB_PWRSTG[2:0] = [111]$, typical external component values, $f_{SW1AB} = 2.0$ MHz, unless otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SW1x}} = 3.6$ V, $V_{SW1AV} = 1.2$ V, $I_{SW1AB} = 100$ mA, $SW1AB_PWRSTG[2:0] = [111]$, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--|--|--------|-----------|--------|------------|-------|
| SW1A/B (single phase) (continued) | | | | | | |
| I_{SW1ABQ} | Quiescent Current PFM Mode APS Mode | – – | 18 235 | – – | μ A | |
| $R_{ONSW1AP}$ | SW1A P-MOSFET R_{DSON} $V_{IN_{SW1A}} = 3.3$ V | – | 215 | 245 | m Ω | |
| $R_{ONSW1AN}$ | SW1A N-MOSFET R_{DSON} $V_{IN_{SW1A}} = 3.3$ V | – | 258 | 326 | m Ω | |
| I_{SW1APQ} | SW1A P-MOSFET Leakage Current $V_{IN_{SW1A}} = 4.5$ V | – | – | 7.5 | μ A | |
| I_{SW1ANQ} | SW1A N-MOSFET Leakage Current $V_{IN_{SW1A}} = 4.5$ V | – | – | 2.5 | μ A | |
| $R_{ONSW1BP}$ | SW1B P-MOSFET R_{DSON} $V_{IN_{SW1B}} = 3.3$ V | – | 215 | 245 | m Ω | |
| $R_{ONSW1BN}$ | SW1B N-MOSFET R_{DSON} $V_{IN_{SW1B}} = 3.3$ V | – | 258 | 326 | m Ω | |
| I_{SW1BPQ} | SW1B P-MOSFET Leakage Current $V_{IN_{SW1B}} = 4.5$ V | – | – | 7.5 | μ A | |
| I_{SW1BNQ} | SW1B N-MOSFET Leakage Current $V_{IN_{SW1B}} = 4.5$ V | – | – | 2.5 | μ A | |
| $R_{SW1ABDIS}$ | Discharge Resistance | – | 600 | – | Ω | |

Notes

- 40. Accuracy specification is inclusive of load and line regulation.
- 41. Current rating of SW1AB supports the Power Virus mode of operation of the i.MX6X processor.

SW1AB single phase

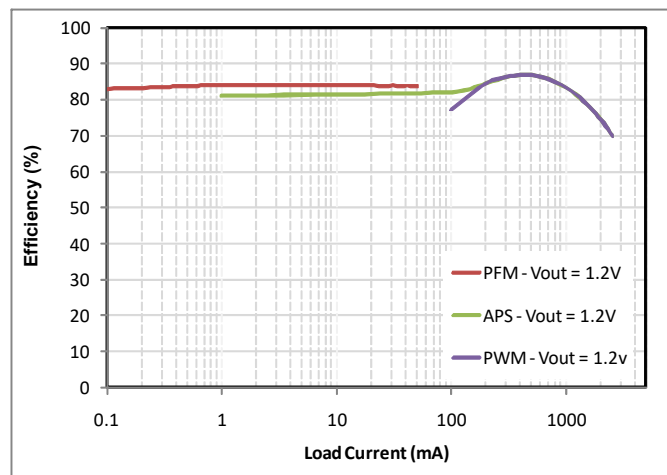


Figure 12. SW1AB efficiency waveforms

6.4.4.4 SW2

SW2 is a single phase, 1.5 A rated buck regulator. [Table 28](#) describes the modes, and [Table 29](#) show the options for the SWxMODE[3:0] bits. [Figure 13](#) shows the block diagram and the external component connections for SW2 regulator.

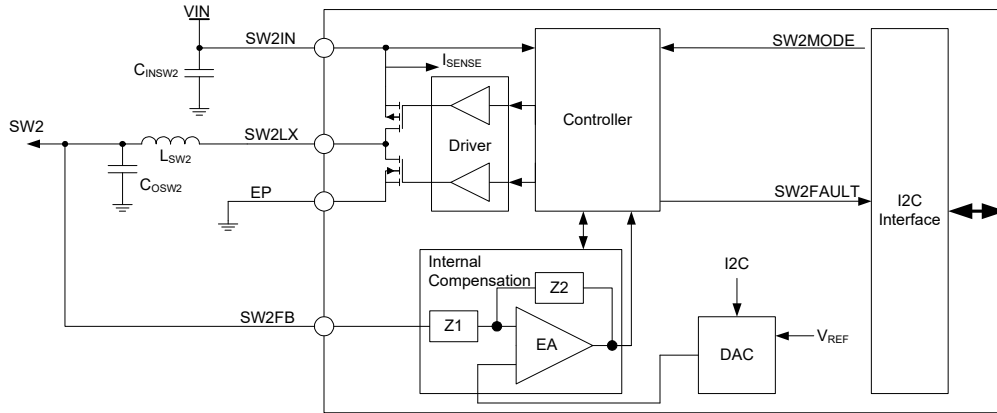


Figure 13. SW2 block diagram

SW2 setup and control registers

SW2 output voltage is programmable from 0.400 to 3.300 V; however, bit SW2[6] in register SW2VOLT is read-only during normal operation. Its value is determined by the default configuration, or may be changed by using the OTP registers. Therefore, once SW2[6] is set to “0”, the output will be limited to the lower output voltages from 0.400 to 1.975 V with 25 mV increments, as determined by bits SW2[5:0]. Likewise, once bit SW2[6] is set to “1”, the output voltage will be limited to the higher output voltage range from 0.800 to 3.300 V with 50 mV increments, as determined by bits SW2[5:0].

In order to optimize the performance of the regulator, it is recommended that only voltages from 2.000 to 3.300 V be used in the high range, and the lower range be used for voltages from 0.400 to 1.975 V.

The output voltage set point is independently programmed for Normal, Standby, and Sleep mode by setting the SW2[5:0], SW2STBY[5:0] and SW2OFF[5:0] bits, respectively. However, the initial state of bit SW2[6] will be copied into bits SW2STBY[6], and SW2OFF[6] bits. Therefore, the output voltage range will remain the same in all three operating modes. [Table 48](#) shows the output voltage coding valid for SW2. Note: Output voltages of 0.6 V and below are not supported.

Table 48. SW2 output voltage configuration

| Low output voltage range ⁽⁴²⁾ | | | High output voltage range | | |
|--|---|------------|---------------------------|---|------------|
| Set point | SW2[6:0] SW2STBY[6:0] SW2OFF[6:0] | SW2 output | Set point | SW2[6:0] SW2STBY[6:0] SW2OFF[6:0] | SW2 output |
| 0 | 0000000 | 0.4000 | 64 | 1000000 | 0.8000 |
| 1 | 0000001 | 0.4250 | 65 | 1000001 | 0.8500 |
| 2 | 0000010 | 0.4500 | 66 | 1000010 | 0.9000 |
| 3 | 0000011 | 0.4750 | 67 | 1000011 | 0.9500 |
| 4 | 0000100 | 0.5000 | 68 | 1000100 | 1.0000 |
| 5 | 0000101 | 0.5250 | 69 | 1000101 | 1.0500 |
| 6 | 0000110 | 0.5500 | 70 | 1000110 | 1.1000 |
| 7 | 0000111 | 0.5750 | 71 | 1000111 | 1.1500 |
| 8 | 0001000 | 0.6000 | 72 | 1001000 | 1.2000 |
| 9 | 0001001 | 0.6250 | 73 | 1001001 | 1.2500 |
| 10 | 0001010 | 0.6500 | 74 | 1001010 | 1.3000 |
| 11 | 0001011 | 0.6750 | 75 | 1001011 | 1.3500 |

Table 48. SW2 output voltage configuration (continued)

| Low output voltage range ⁽⁴²⁾ | | | High output voltage range | | |
|--|---|------------|---------------------------|---|------------|
| Set point | SW2[6:0] SW2STBY[6:0] SW2OFF[6:0] | SW2 output | Set point | SW2[6:0] SW2STBY[6:0] SW2OFF[6:0] | SW2 output |
| 12 | 0001100 | 0.7000 | 76 | 1001100 | 1.4000 |
| 13 | 0001101 | 0.7250 | 77 | 1001101 | 1.4500 |
| 14 | 0001110 | 0.7500 | 78 | 1001110 | 1.5000 |
| 15 | 0001111 | 0.7750 | 79 | 1001111 | 1.5500 |
| 16 | 0010000 | 0.8000 | 80 | 1010000 | 1.6000 |
| 17 | 0010001 | 0.8250 | 81 | 1010001 | 1.6500 |
| 18 | 0010010 | 0.8500 | 82 | 1010010 | 1.7000 |
| 19 | 0010011 | 0.8750 | 83 | 1010011 | 1.7500 |
| 20 | 0010100 | 0.9000 | 84 | 1010100 | 1.8000 |
| 21 | 0010101 | 0.9250 | 85 | 1010101 | 1.8500 |
| 22 | 0010110 | 0.9500 | 86 | 1010110 | 1.9000 |
| 23 | 0010111 | 0.9750 | 87 | 1010111 | 1.9500 |
| 24 | 0011000 | 1.0000 | 88 | 1011000 | 2.0000 |
| 25 | 0011001 | 1.0250 | 89 | 1011001 | 2.0500 |
| 26 | 0011010 | 1.0500 | 90 | 1011010 | 2.1000 |
| 27 | 0011011 | 1.0750 | 91 | 1011011 | 2.1500 |
| 28 | 0011100 | 1.1000 | 92 | 1011100 | 2.2000 |
| 29 | 0011101 | 1.1250 | 93 | 1011101 | 2.2500 |
| 30 | 0011110 | 1.1500 | 94 | 1011110 | 2.3000 |
| 31 | 0011111 | 1.1750 | 95 | 1011111 | 2.3500 |
| 32 | 0100000 | 1.2000 | 96 | 1100000 | 2.4000 |
| 33 | 0100001 | 1.2250 | 97 | 1100001 | 2.4500 |
| 34 | 0100010 | 1.2500 | 98 | 1100010 | 2.5000 |
| 35 | 0100011 | 1.2750 | 99 | 1100011 | 2.5500 |
| 36 | 0100100 | 1.3000 | 100 | 1100100 | 2.6000 |
| 37 | 0100101 | 1.3250 | 101 | 1100101 | 2.6500 |
| 38 | 0100110 | 1.3500 | 102 | 1100110 | 2.7000 |
| 39 | 0100111 | 1.3750 | 103 | 1100111 | 2.7500 |
| 40 | 0101000 | 1.4000 | 104 | 1101000 | 2.8000 |
| 41 | 0101001 | 1.4250 | 105 | 1101001 | 2.8500 |
| 42 | 0101010 | 1.4500 | 106 | 1101010 | 2.9000 |
| 43 | 0101011 | 1.4750 | 107 | 1101011 | 2.9500 |
| 44 | 0101100 | 1.5000 | 108 | 1101100 | 3.0000 |
| 45 | 0101101 | 1.5250 | 109 | 1101101 | 3.0500 |
| 46 | 0101110 | 1.5500 | 110 | 1101110 | 3.1000 |
| 47 | 0101111 | 1.5750 | 111 | 1101111 | 3.1500 |
| 48 | 0110000 | 1.6000 | 112 | 1110000 | 3.2000 |

Table 48. SW2 output voltage configuration (continued)

| Low output voltage range ⁽⁴²⁾ | | | High output voltage range | | |
|--|---|------------|---------------------------|---|------------|
| Set point | SW2[6:0] SW2STBY[6:0] SW2OFF[6:0] | SW2 output | Set point | SW2[6:0] SW2STBY[6:0] SW2OFF[6:0] | SW2 output |
| 49 | 0110001 | 1.6250 | 113 | 1110001 | 3.2500 |
| 50 | 0110010 | 1.6500 | 114 | 1110010 | 3.3000 |
| 51 | 0110011 | 1.6750 | 115 | 1110011 | Reserved |
| 52 | 0110100 | 1.7000 | 116 | 1110100 | Reserved |
| 53 | 0110101 | 1.7250 | 117 | 1110101 | Reserved |
| 54 | 0110110 | 1.7500 | 118 | 1110110 | Reserved |
| 55 | 0110111 | 1.7750 | 119 | 1110111 | Reserved |
| 56 | 0111000 | 1.8000 | 120 | 1111000 | Reserved |
| 57 | 0111001 | 1.8250 | 121 | 1111001 | Reserved |
| 58 | 0111010 | 1.8500 | 122 | 1111010 | Reserved |
| 59 | 0111011 | 1.8750 | 123 | 1111011 | Reserved |
| 60 | 0111100 | 1.9000 | 124 | 1111100 | Reserved |
| 61 | 0111101 | 1.9250 | 125 | 1111101 | Reserved |
| 62 | 0111110 | 1.9500 | 126 | 1111110 | Reserved |
| 63 | 0111111 | 1.9750 | 127 | 1111111 | Reserved |

Notes

42. For voltages less than 2.0 V, only use set points 0 to 63

Setup and control of SW2 is done through I²C registers listed in [Table 49](#), and a detailed description of each one of the registers is provided in [Tables 50](#) to [Table 54](#).

Table 49. SW2 register summary

| Register | Address | Description |
|----------|---------|---|
| SW2VOLT | 0x35 | Output voltage set point on normal operation |
| SW2STBY | 0x36 | Output voltage set point on Standby |
| SW2OFF | 0x37 | Output voltage set point on Sleep |
| SW2MODE | 0x38 | Switching Mode selector register |
| SW2CONF | 0x39 | DVS, Phase, Frequency, and ILIM configuration |

Table 50. Register SW2VOLT - ADDR 0x35

| Name | Bit # | R/W | Default | Description |
|--------|-------|-----|---------|--|
| SW2 | 5:0 | R/W | 0x00 | Sets the SW2 output voltage during normal operation mode. See Table 48 for all possible configurations. |
| SW2 | 6 | R | 0x00 | Sets the operating output voltage range for SW2. Set during OTP or TBB configuration only. See Table 48 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 51. Register SW2STBY - ADDR 0x36

| Name | Bit # | R/W | Default | Description |
|---------|-------|-----|---------|--|
| SW2STBY | 5:0 | R/W | 0x00 | Sets the SW2 output voltage during Standby mode. See Table 48 for all possible configurations. |
| SW2STBY | 6 | R | 0x00 | Sets the operating output voltage range for SW2 on Standby mode. This bit inherits the value configured on bit SW2[6] during OTP or TBB configuration. See Table 48 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 52. Register SW2OFF - ADDR 0x37

| Name | Bit # | R/W | Default | Description |
|--------|-------|-----|---------|--|
| SW2OFF | 5:0 | R/W | 0x00 | Sets the SW2 output voltage during Sleep mode. See Table 48 for all possible configurations. |
| SW2OFF | 6 | R | 0x00 | Sets the operating output voltage range for SW2 on Sleep mode. This bit inherits the value configured on bit SW2[6] during OTP or TBB configuration. See Table 48 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 53. Register SW2MODE - ADDR 0x38

| Name | Bit # | R/W | Default | Description |
|----------|-------|-----|---------|--|
| SW2MODE | 3:0 | R/W | 0x80 | Sets the SW2 switching operation mode. See Table 28 for all possible configurations. |
| UNUSED | 4 | – | 0x00 | UNUSED |
| SW2OMODE | 5 | R/W | 0x00 | Set status of SW2 when in Sleep mode 0 = OFF 1 = PFM |
| UNUSED | 7:6 | – | 0x00 | UNUSED |

Table 54. Register SW2CONF - ADDR 0x39

| Name | Bit # | R/W | Default | Description |
|-------------|-------|-----|---------|--|
| SW2ILIM | 0 | R/W | 0x00 | SW2 current limit level selection 0 = High level current limit 1 = Low level current limit |
| UNUSED | 1 | R/W | 0x00 | Unused |
| SW2FREQ | 3:2 | R/W | 0x00 | SW2 switching frequency selector. See Table 36 . |
| SW2PHASE | 5:4 | R/W | 0x00 | SW2 Phase clock selection. See Table 34 . |
| SW2DVSSPEED | 7:6 | R/W | 0x00 | SW2 DVS speed selection. See Table 33 . |

SW2 external components

Table 55. SW2 external component recommendations

| Components | Description | Values |
|--------------------------------|--------------------------------|--|
| $C_{IN_{SW2}}$ ⁽⁴³⁾ | SW2 Input capacitor | 4.7 μ F |
| C_{IN2HF} ⁽⁴³⁾ | SW2 Decoupling input capacitor | 0.1 μ F |
| C_{OSW2} ⁽⁴³⁾ | SW2 Output capacitor | 2 x 22 μ F |
| L_{SW2} | SW2 Inductor | 1.0 μ H DCR = 50 m Ω I_{SAT} = 2.65 A |

Notes

43. Use X5R or X7R capacitors.

SW2 specifications

Table 56. SW2 electrical characteristics

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SW2}} = 3.6$ V, $V_{SW2} = 3.15$ V, $I_{SW2} = 100$ mA, $SW2_PWRSTG[2:0] = [111]$, typical external component values, $f_{SW2} = 2.0$ MHz, unless otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SW2}} = 3.6$ V, $V_{SW2} = 3.15$ V, $I_{SW2} = 100$ mA, $SW2_PWRSTG[2:0] = [111]$, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|-------------------------------|---|-----------------------|--------------------------|--------------------|---------|-------|
| Switch mode supply SW2 | | | | | | |
| $V_{IN_{SW2}}$ | Operating Input Voltage | 2.8 | – | 4.5 | V | (44) |
| V_{SW2} | Nominal Output Voltage | – | Table 48 | – | V | |
| V_{SW2ACC} | Output Voltage Accuracy <ul style="list-style-type: none"> PWM, APS, 2.8 V < V_{IN} < 4.5 V, $0 < I_{SW2} < 1.5$ A <ul style="list-style-type: none"> 0.625 V < $V_{SW2} < 0.85$ V 0.875 V < $V_{SW2} < 1.975$ V 2.0 V < $V_{SW2} < 3.3$ V PFM, 2.8 V < V_{IN} < 4.5 V, $0 < I_{SW2} \leq 50$ mA <ul style="list-style-type: none"> 0.625 V < $V_{SW2} < 0.675$ V 0.7 V < $V_{SW2} < 0.85$ V 0.875 V < $V_{SW2} < 1.975$ V 2.0 V < $V_{SW2} < 3.3$ V | –25 –3.0% –6.0% | – – – | 25 3.0% 6.0% | mV % | (45) |
| I_{SW2} | Rated Output Load Current 2.8 V < V_{IN} < 4.5 V, 0.625 V < $V_{SW2} < 3.3$ V | – | – | 1500 | mA | (46) |
| I_{SW2LIM} | Current Limiter Peak Current Detection <ul style="list-style-type: none"> Current through Inductor $SW2ILIM = 0$ $SW2ILIM = 1$ | 2.1 1.57 | 3.0 2.25 | 3.9 2.93 | A | |
| V_{SW2OSH} | Start-up Overshoot $I_{SW2} = 0.0$ mA DVS clk = 25 mV/4 μ s, $V_{IN} = V_{IN_{SW2}} = 4.5$ V | – | – | 66 | mV | |
| $t_{ON_{SW2}}$ | Turn-on Time Enable to 90% of end value $I_{SW2} = 0.0$ mA DVS clk = 50 mV/8 μ s, $V_{IN} = V_{IN_{SW2}} = 4.5$ V | – | – | 550 | μ s | |
| f_{sw2} | Switching Frequency $SW2FREQ[1:0] = 00$ $SW2FREQ[1:0] = 01$ $SW2FREQ[1:0] = 10$ | – – – | 1.0 2.0 4.0 | – – – | MHz | |

Table 56. SW2 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SW2}} = 3.6$ V, $V_{SW2} = 3.15$ V, $I_{SW2} = 100$ mA, $SW2_PWRSTG[2:0] = [111]$, typical external component values, $f_{SW2} = 2.0$ MHz, unless otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SW2}} = 3.6$ V, $V_{SW2} = 3.15$ V, $I_{SW2} = 100$ mA, $SW2_PWRSTG[2:0] = [111]$, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---------------------------|--|------|------|------|------|-------|
| η_{SW2} | Efficiency | | | | | |
| | • $V_{IN} = 3.6$ V, $f_{SW2} = 2.0$ MHz, $L_{SW2} = 1.0$ μ H | | | | | |
| | PFM, 3.15 V, 1.0 mA | – | 94 | – | % | |
| | PFM, 3.15 V, 50 mA | – | 95 | – | | |
| | APS, PWM, 3.15 V, 400 mA | – | 96 | – | | |
| | APS, PWM, 3.15 V, 600 mA | – | 94 | – | | |
| | APS, PWM, 3.15 V, 1000 mA | – | 92 | – | | |
| APS, PWM, 3.15 V, 1500 mA | – | 89 | – | | | |

Switch mode supply SW2 (continued)

| | | | | | | |
|------------------|---|---|-----|-----|------------|--|
| ΔV_{SW2} | Output Ripple | – | 10 | – | mV | |
| V_{SW2LIR} | Line Regulation (APS, PWM) | – | – | 20 | mV | |
| V_{SW2LOR} | DC Load Regulation (APS, PWM) | – | – | 20 | mV | |
| $V_{SW2LOTR}$ | Transient Load Regulation | | | | mV | |
| | • Transient load = 0.0 mA to 1.0 A, di/dt = 100 mA/ μ s | | | | | |
| | Overshoot | – | – | 50 | | |
| | Undershoot | – | – | 50 | | |
| I_{SW2Q} | Quiescent Current | | | | μ A | |
| | PFM Mode | – | 23 | – | | |
| | APS Mode (Low output voltage settings) | – | 145 | – | | |
| | APS Mode (High output voltage settings) | – | 305 | – | | |
| $R_{ON_{SW2P}}$ | SW2 P-MOSFET $R_{DS(ON)}$ at $V_{IN} = V_{IN_{SW2}} = 3.3$ V | – | 190 | 209 | m Ω | |
| $R_{ON_{SW2N}}$ | SW2 N-MOSFET $R_{DS(ON)}$ at $V_{IN} = V_{IN_{SW2}} = 3.3$ V | – | 212 | 255 | m Ω | |
| I_{SW2PQ} | SW2 P-MOSFET Leakage Current $V_{IN} = V_{IN_{SW2}} = 4.5$ V | – | – | 12 | μ A | |
| I_{SW2NQ} | SW2 N-MOSFET Leakage Current $V_{IN} = V_{IN_{SW2}} = 4.5$ V | – | – | 4.0 | μ A | |
| R_{SW2DIS} | Discharge Resistance | – | 600 | – | Ω | |

Notes

44. When output is set to > 2.6 V the output will follow the input down when V_{IN} gets near 2.8 V.
45. Accuracy specification is inclusive of load and line regulation.
46. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation:
 $(V_{IN_{SW2}} - V_{SW2}) = I_{SW2} \cdot (\text{DCR of Inductor} + R_{ON_{SW2P}} + \text{PCB trace resistance})$.

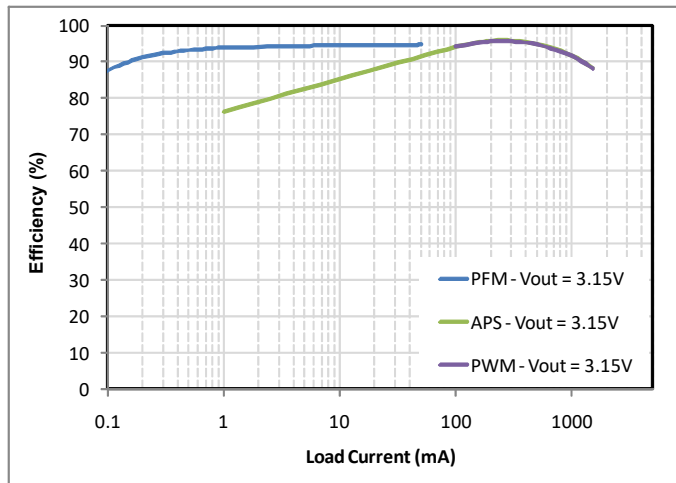


Figure 14. SW2 efficiency waveforms

6.4.4.5 SW3A/B

SW3A/B are 1.25 to 2.5 A rated buck regulators, depending on the configuration. [Table 28](#) describes the available switching modes and [Table 29](#) show the actual configuration options for the SW3xMODE[3:0] bits.

SW3A/B can be configured in various phasing schemes, depending on the desired cost/performance trade-offs. The following configurations are available:

- A single phase
- Independent regulators

The desired configuration is programmed in OTP by using the SW3_CONFIG[1:0] bits. [Table 57](#) shows the options for the SW3CFG[1:0] bits.

Table 57. SW3 Configuration

| SW3_CONFIG[1:0] | Description |
|-----------------|------------------|
| 00 | A/B Single Phase |
| 01 | A/B Single Phase |
| 10 | Reserved |
| 11 | A/B Independent |

SW3A/B single phase

In this configuration, SW3ALX and SW3BLX are connected in single phase with a single inductor as shown in [Figure 15](#). This configuration reduces cost and component count. Feedback is taken from the SW3AFB pin and the SW3BFB pin must be left open. Although control is from SW3A, registers of both regulators, SW3A and SW3B, must be identically set.

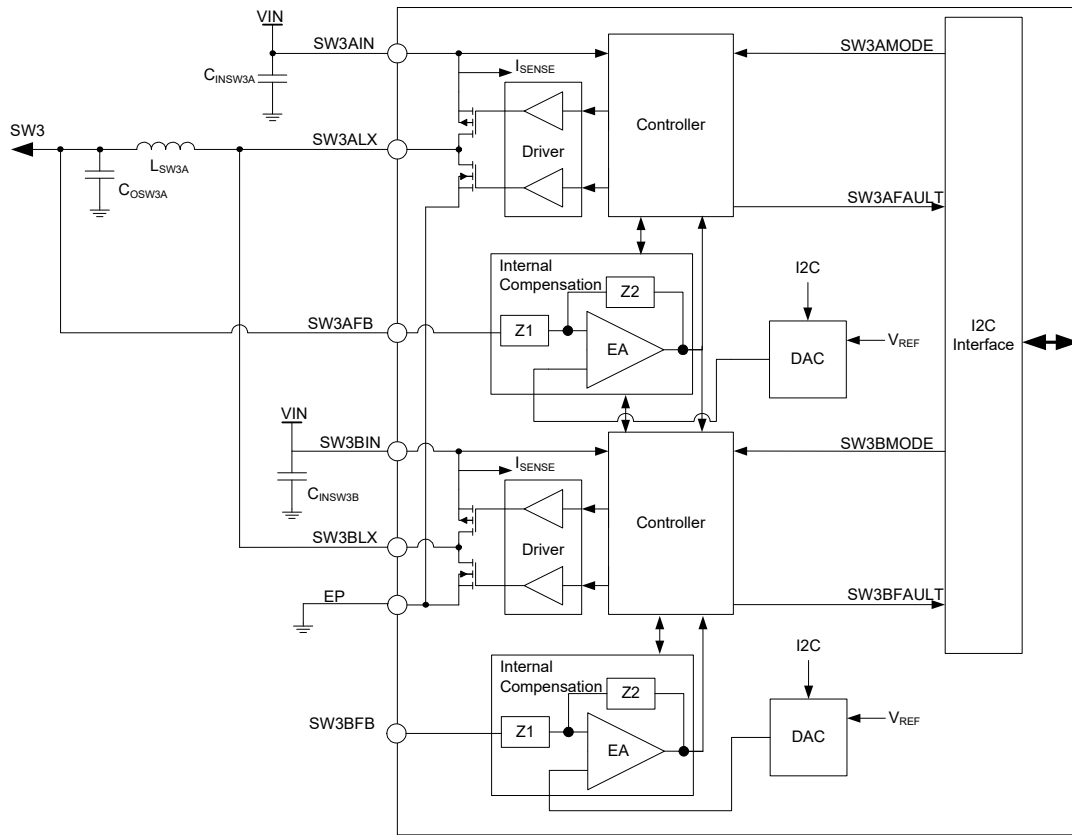


Figure 15. SW3A/B single phase block diagram

Table 58. SW3A/B output voltage configuration

| Low output voltage range ⁽⁴⁷⁾ | | | High output voltage range | | |
|--|--|-------------|---------------------------|--|------------|
| Set point | SW3x[6:0] SW3xSTBY[6:0] SW3xOFF[6:0] | SW3x output | Set Point | SW3x[6:0] SW3xSTBY[6:0] SW3xOFF[6:0] | sw3xoutput |
| 0 | 0000000 | 0.4000 | 64 | 1000000 | 0.8000 |
| 1 | 0000001 | 0.4250 | 65 | 1000001 | 0.8500 |
| 2 | 0000010 | 0.4500 | 66 | 1000010 | 0.9000 |
| 3 | 0000011 | 0.4750 | 67 | 1000011 | 0.9500 |
| 4 | 0000100 | 0.5000 | 68 | 1000100 | 1.0000 |
| 5 | 0000101 | 0.5250 | 69 | 1000101 | 1.0500 |
| 6 | 0000110 | 0.5500 | 70 | 1000110 | 1.1000 |
| 7 | 0000111 | 0.5750 | 71 | 1000111 | 1.1500 |
| 8 | 0001000 | 0.6000 | 72 | 1001000 | 1.2000 |
| 9 | 0001001 | 0.6250 | 73 | 1001001 | 1.2500 |
| 10 | 0001010 | 0.6500 | 74 | 1001010 | 1.3000 |
| 11 | 0001011 | 0.6750 | 75 | 1001011 | 1.3500 |
| 12 | 0001100 | 0.7000 | 76 | 1001100 | 1.4000 |
| 13 | 0001101 | 0.7250 | 77 | 1001101 | 1.4500 |
| 14 | 0001110 | 0.7500 | 78 | 1001110 | 1.5000 |
| 15 | 0001111 | 0.7750 | 79 | 1001111 | 1.5500 |
| 16 | 0010000 | 0.8000 | 80 | 1010000 | 1.6000 |
| 17 | 0010001 | 0.8250 | 81 | 1010001 | 1.6500 |
| 18 | 0010010 | 0.8500 | 82 | 1010010 | 1.7000 |
| 19 | 0010011 | 0.8750 | 83 | 1010011 | 1.7500 |
| 20 | 0010100 | 0.9000 | 84 | 1010100 | 1.8000 |
| 21 | 0010101 | 0.9250 | 85 | 1010101 | 1.8500 |
| 22 | 0010110 | 0.9500 | 86 | 1010110 | 1.9000 |
| 23 | 0010111 | 0.9750 | 87 | 1010111 | 1.9500 |
| 24 | 0011000 | 1.0000 | 88 | 1011000 | 2.0000 |
| 25 | 0011001 | 1.0250 | 89 | 1011001 | 2.0500 |
| 26 | 0011010 | 1.0500 | 90 | 1011010 | 2.1000 |
| 27 | 0011011 | 1.0750 | 91 | 1011011 | 2.1500 |
| 28 | 0011100 | 1.1000 | 92 | 1011100 | 2.2000 |
| 29 | 0011101 | 1.1250 | 93 | 1011101 | 2.2500 |
| 30 | 0011110 | 1.1500 | 94 | 1011110 | 2.3000 |
| 31 | 0011111 | 1.1750 | 95 | 1011111 | 2.3500 |
| 32 | 0100000 | 1.2000 | 96 | 1100000 | 2.4000 |
| 33 | 0100001 | 1.2250 | 97 | 1100001 | 2.4500 |
| 34 | 0100010 | 1.2500 | 98 | 1100010 | 2.5000 |
| 35 | 0100011 | 1.2750 | 99 | 1100011 | 2.5500 |

Table 58. SW3A/B output voltage configuration (continued)

| Low output voltage range ⁽⁴⁷⁾ | | | High output voltage range | | |
|--|--|-------------|---------------------------|--|------------|
| Set point | SW3x[6:0] SW3xSTBY[6:0] SW3xOFF[6:0] | SW3x output | Set Point | SW3x[6:0] SW3xSTBY[6:0] SW3xOFF[6:0] | sw3xoutput |
| 36 | 0100100 | 1.3000 | 100 | 1100100 | 2.6000 |
| 37 | 0100101 | 1.3250 | 101 | 1100101 | 2.6500 |
| 38 | 0100110 | 1.3500 | 102 | 1100110 | 2.7000 |
| 39 | 0100111 | 1.3750 | 103 | 1100111 | 2.7500 |
| 40 | 0101000 | 1.4000 | 104 | 1101000 | 2.8000 |
| 41 | 0101001 | 1.4250 | 105 | 1101001 | 2.8500 |
| 42 | 0101010 | 1.4500 | 106 | 1101010 | 2.9000 |
| 43 | 0101011 | 1.4750 | 107 | 1101011 | 2.9500 |
| 44 | 0101100 | 1.5000 | 108 | 1101100 | 3.0000 |
| 45 | 0101101 | 1.5250 | 109 | 1101101 | 3.0500 |
| 46 | 0101110 | 1.5500 | 110 | 1101110 | 3.1000 |
| 47 | 0101111 | 1.5750 | 111 | 1101111 | 3.1500 |
| 48 | 0110000 | 1.6000 | 112 | 1110000 | 3.2000 |
| 49 | 0110001 | 1.6250 | 113 | 1110001 | 3.2500 |
| 50 | 0110010 | 1.6500 | 114 | 1110010 | 3.3000 |
| 51 | 0110011 | 1.6750 | 115 | 1110011 | Reserved |
| 52 | 0110100 | 1.7000 | 116 | 1110100 | Reserved |
| 53 | 0110101 | 1.7250 | 117 | 1110101 | Reserved |
| 54 | 0110110 | 1.7500 | 118 | 1110110 | Reserved |
| 55 | 0110111 | 1.7750 | 119 | 1110111 | Reserved |
| 56 | 0111000 | 1.8000 | 120 | 1111000 | Reserved |
| 57 | 0111001 | 1.8250 | 121 | 1111001 | Reserved |
| 58 | 0111010 | 1.8500 | 122 | 1111010 | Reserved |
| 59 | 0111011 | 1.8750 | 123 | 1111011 | Reserved |
| 60 | 0111100 | 1.9000 | 124 | 1111100 | Reserved |
| 61 | 0111101 | 1.9250 | 125 | 1111101 | Reserved |
| 62 | 0111110 | 1.9500 | 126 | 1111110 | Reserved |
| 63 | 0111111 | 1.9750 | 127 | 1111111 | Reserved |

Notes

47. For voltages less than 2.0 V, only use set points 0 to 63.

[Table 59](#) provides a list of registers used to configure and operate SW3A/B. A detailed description on each of these register is provided on [Tables 60](#) through [Table 69](#).

Table 59. SW3AB register summary

| Register | Address | Output |
|----------|---------|---|
| SW3AVOLT | 0x3C | SW3A Output voltage set point on normal operation |
| SW3ASTBY | 0x3D | SW3A Output voltage set point on Standby |
| SW3AOFF | 0x3E | SW3A Output voltage set point on Sleep |
| SW3AMODE | 0x3F | SW3A Switching mode selector register |
| SW3ACONF | 0x40 | SW3A DVS, phase, frequency and ILIM configuration |
| SW3BVOLT | 0x43 | SW3B Output voltage set point on normal operation |
| SW3BSTBY | 0x44 | SW3B Output voltage set point on Standby |
| SW3BOFF | 0x45 | SW3B Output voltage set point on Sleep |
| SW3BMODE | 0x46 | SW3B Switching mode selector register |
| SW3BCONF | 0x47 | SW3B DVS, phase, frequency and ILIM configuration |

Table 60. Register SW3AVOLT - ADDR 0x3C

| Name | Bit # | R/W | Default | Description |
|--------|-------|-----|---------|--|
| SW3A | 5:0 | R/W | 0x00 | Sets the SW3A output voltage (Independent) or SW3A/B output voltage (Single phase), during normal operation mode. See Table 58 for all possible configurations. |
| SW3A | 6 | R | 0x00 | Sets the operating output voltage range for SW3A (Independent) or SW3A/B (Single phase). Set during OTP or TBB configuration only. See Table 58 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 61. Register SW3ASTBY - ADDR 0x3D

| Name | Bit # | R/W | Default | Description |
|----------|-------|-----|---------|---|
| SW3ASTBY | 5:0 | R/W | 0x00 | Sets the SW3A output voltage (Independent) or SW3A/B output voltage (Single phase), during Standby mode. See Table 58 for all possible configurations. |
| SW3ASTBY | 6 | R | 0x00 | Sets the operating output voltage range for SW3A (Independent) or SW3A/B (Single phase) on Standby mode. This bit inherits the value configured on bit SW3A[6] during OTP or TBB configuration. See Table 58 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 62. Register SW3AOFF - ADDR 0x3E

| Name | Bit # | R/W | Default | Description |
|---------|-------|-----|---------|---|
| SW3AOFF | 5:0 | R/W | 0x00 | Sets the SW3A output voltage (Independent) or SW3A/B output voltage (Single phase), during Sleep mode. See Table 58 for all possible configurations. |
| SW3AOFF | 6 | R | 0x00 | Sets the operating output voltage range for SW3A (Independent) or SW3A/B (Single phase) on Sleep mode. This bit inherits the value configured on bit SW3A[6] during OTP or TBB configuration. See Table 58 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 63. Register SW3AMODE - ADDR 0x3F

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| SW3AMODE | 3:0 | R/W | 0x80 | Sets the SW3A (Independent) or SW3A/B (Single phase) switching operation mode. See Table 28 for all possible configurations. |
| UNUSED | 4 | – | 0x00 | UNUSED |
| SW3AOMODE | 5 | R/W | 0x00 | Set status of SW3A (Independent) or SW3A/B (Single phase) when in Sleep mode. 0 = OFF 1 = PFM |
| UNUSED | 7:6 | – | 0x00 | UNUSED |

Table 64. Register SW3ACONF - ADDR 0x40

| Name | Bit # | R/W | Default | Description |
|--------------|-------|-----|---------|---|
| SW3AILIM | 0 | R/W | 0x00 | SW3A current limit level selection 0 = High level current limit 1 = Low level current limit |
| UNUSED | 1 | R/W | 0x00 | Unused |
| SW3AFREQ | 3:2 | R/W | 0x00 | SW3A switching frequency selector. See Table 36 . |
| SW3APHASE | 5:4 | R/W | 0x00 | SW3A Phase clock selection. See Table 34 . |
| SW3ADVSSPEED | 7:6 | R/W | 0x00 | SW3A DVS speed selection. See Table 33 . |

Table 65. Register SW3BVOLT - ADDR 0x43

| Name | Bit # | R/W | Default | Description |
|--------|-------|-----|---------|---|
| SW3B | 5:0 | R/W | 0x00 | Sets the SW3B output voltage (Independent) during normal operation mode. See Table 58 for all possible configurations. |
| SW3B | 6 | R | 0x00 | Sets the operating output voltage range for SW3B (Independent). Set during OTP or TBB configuration only. See Table 58 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 66. Register SW3BSTBY - ADDR 0x44

| Name | Bit # | R/W | Default | Description |
|----------|-------|-----|---------|--|
| SW3BSTBY | 5:0 | R/W | 0x00 | Sets the SW3B output voltage (Independent) during Standby mode. See Table 58 for all possible configurations. |
| SW3BSTBY | 6 | R | 0x00 | Sets the operating output voltage range for SW3B (Independent) on Standby mode. This bit inherits the value configured on bit SW3B[6] during OTP or TBB configuration. See Table 58 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 67. Register SW3BOFF - ADDR 0x45

| Name | Bit # | R/W | Default | Description |
|---------|-------|-----|---------|--|
| SW3BOFF | 5:0 | R/W | 0x00 | Sets the SW3B output voltage (Independent) during Sleep mode. See Table 58 for all possible configurations. |
| SW3BOFF | 6 | R | 0x00 | Sets the operating output voltage range for SW3B (Independent) on Sleep mode. This bit inherits the value configured on bit SW3B[6] during OTP or TBB configuration. See Table 58 for all possible configurations. |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 68. Register SW3BMODE - ADDR 0x46

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|---|
| SW3BMODE | 3:0 | R/W | 0x80 | Sets the SW3B (Independent) switching operation mode. See Table 28 for all possible configurations. |
| UNUSED | 4 | – | 0x00 | UNUSED |
| SW3BOMODE | 5 | R/W | 0x00 | Set status of SW3B (Independent) when in Sleep mode. 0 = OFF 1 = PFM |
| UNUSED | 7:6 | – | 0x00 | UNUSED |

Table 69. Register SW3BCONF - ADDR 0x47

| Name | Bit # | R/W | Default | Description |
|--------------|-------|-----|---------|---|
| SW3BILIM | 0 | R/W | 0x00 | SW3B current limit level selection 0 = High level Current limit 1 = Low level Current limit |
| UNUSED | 1 | R/W | 0x00 | Unused |
| SW3BFREQ | 3:2 | R/W | 0x00 | SW3B switching frequency selector. See Table 36 . |
| SW3BPHASE | 5:4 | R/W | 0x00 | SW3B Phase clock selection. See Table 34 . |
| SW3BDVSSPEED | 7:6 | R/W | 0x00 | SW3B DVS speed selection. See Table 33 . |

SW3A/B external components

Table 70. SW3A/B external component requirements

| Components | Description | Mode | |
|--------------------------------|---------------------------------|---|---|
| | | SW3A/B single phase | SW3A independent SW3B independent |
| C_{IN3A} ⁽⁴⁸⁾ | SW3A Input capacitor | 4.7 μ F | 4.7 μ F |
| C_{IN3AHF} ⁽⁴⁸⁾ | SW3A Decoupling input capacitor | 0.1 μ F | 0.1 μ F |
| C_{IN3B} ⁽⁴⁸⁾ | SW3B Input capacitor | 4.7 μ F | 4.7 μ F |
| C_{IN3BHF} ⁽⁴⁸⁾ | SW3B Decoupling input capacitor | 0.1 μ F | 0.1 μ F |
| C_{OS3A} ⁽⁴⁸⁾ | SW3A Output capacitor | 4 x 22 μ F | 2 x 22 μ F |
| C_{OS3B} ⁽⁴⁸⁾ | SW3B Output capacitor | – | 2 x 22 μ F |
| L_{SW3A} | SW3A Inductor | 1.0 μ H DCR = 50 m Ω I_{SAT} = 3.9 A | 1.0 μ H DCR = 60 m Ω I_{SAT} = 3.0 A |
| L_{SW3B} | SW3B Inductor | – | 1.0 μ H DCR = 60 m Ω I_{SAT} = 3.0 A |
| Notes | | | |
| 48. Use X5R or X7R capacitors. | | | |

SW3A/B specifications

Table 71. SW3A/B electrical characteristics

All parameters are specified at Consumer T_A = -40 to 85 °C and Extended Industrial T_A = -40 to 105 °C, $V_{IN} = V_{IN3A} = 3.6$ V, $V_{SW3x} = 1.5$ V, $I_{SW3x} = 100$ mA, SW3x_PWRSTG[2:0] = [111], typical external component values, $f_{SW3x} = 2.0$ MHz, single phase and independent mode unless, otherwise noted. Typical values are characterized at $V_{IN} = V_{IN3A} = 3.6$ V, $V_{SW3x} = 1.5$ V, $I_{SW3x} = 100$ mA, SW3x_PWRSTG[2:0] = [111], and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|----------------------------------|--|-----------------------|--------------------------|--------------------|---------|-------|
| Switch mode supply SW3a/B | | | | | | |
| V_{IN3A} | Operating Input Voltage ⁽⁴⁹⁾ | 2.8 | – | 4.5 | V | |
| V_{SW3x} | Nominal Output Voltage | - | Table 58 | - | V | |
| $V_{SW3xACC}$ | Output Voltage Accuracy <ul style="list-style-type: none"> PWM, APS 2.8 V < V_{IN} < 4.5 V, 0 < I_{SW3x} < $I_{SW3xMAX}$ 0.625 V < V_{SW3x} < 0.85 V 0.875 V < V_{SW3x} < 1.975 V 2.0 V < V_{SW3x} < 3.3 V PFM, steady state (2.8 V < V_{IN} < 4.5 V, 0 < I_{SW3x} < 50 mA) 0.625 V < V_{SW3x} < 0.675 V 0.7 V < V_{SW3x} < 0.85 V 0.875 V < V_{SW3x} < 1.975 V 2.0 V < V_{SW3x} < 3.3 V | -25 -3.0% -6.0% | – – – | 25 3.0% 6.0% | mV % | (50) |
| I_{SW3x} | Rated Output Load Current ⁽⁵¹⁾ <ul style="list-style-type: none"> 2.8 V < V_{IN} < 4.5 V, 0.625 V < V_{SW3x} < 3.3 V PWM, APS mode single phase PWM, APS mode independent (per phase) | – – | – – | 2500 1250 | mA | |

Table 71. SW3A/B electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SW3x}} = 3.6$ V, $V_{SW3x} = 1.5$ V, $I_{SW3x} = 100$ mA, $SW3x_PWRSTG[2:0] = [111]$, typical external component values, $f_{SW3x} = 2.0$ MHz, single phase and independent mode unless, otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SW3x}} = 3.6$ V, $V_{SW3x} = 1.5$ V, $I_{SW3x} = 100$ mA, $SW3x_PWRSTG[2:0] = [111]$, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--|--|----------------------------|----------------------------------|----------------------------|------------|-------|
| Switch mode supply SW3a/B (continued) | | | | | | |
| $I_{SW3xLIM}$ | Current Limiter Peak Current Detection <ul style="list-style-type: none"> Single phase (Current through inductor) SW3xILIM = 0 SW3xILIM = 1 Independent mode (Current through inductor per phase) SW3xILIM = 0 SW3xILIM = 1 | 3.5 2.7 | 5.0 3.8 | 6.5 4.9 | A | |
| $V_{SW3xOSH}$ | Start-up Overshoot $I_{SW3x} = 0.0$ mA DVS clk = 25 mV/4 μ s, $V_{IN} = V_{IN_{SW3x}} = 4.5$ V | – | – | 66 | mV | |
| $t_{ON_{SW3x}}$ | Turn-on Time Enable to 90% of end value $I_{SW3x} = 0$ mA DVS clk = 25 mV/4 μ s, $V_{IN} = V_{IN_{SW3x}} = 4.5$ V | – | – | 500 | μ s | |
| f_{SW3x} | Switching Frequency SW3xFREQ[1:0] = 00 SW3xFREQ[1:0] = 01 SW3xFREQ[1:0] = 10 | – – – | 1.0 2.0 4.0 | – – – | MHz | |
| η_{SW3AB} | Efficiency (Single Phase) <ul style="list-style-type: none"> $f_{SW3} = 2.0$ MHz, $L_{SW3x} 1.0$ μH PFM, 1.5 V, 1.0 mA PFM, 1.5 V, 50 mA APS, PWM 1.5 V, 500 mA APS, PWM 1.5 V, 750 mA APS, PWM 1.5 V, 1250 mA APS, PWM 1.5 V, 2500 mA | – – – – – – | 84 85 85 84 80 74 | – – – – – – | % | |
| ΔV_{SW3x} | Output Ripple | – | 10 | – | mV | |
| $V_{SW3xLIR}$ | Line Regulation (APS, PWM) | – | – | 20 | mV | |
| $V_{SW3xLOR}$ | DC Load Regulation (APS, PWM) | – | – | 20 | mV | |
| $V_{SW3xLOTR}$ | Transient Load Regulation <ul style="list-style-type: none"> Transient Load = 0.0 mA to $I_{SW3x}/2$, $di/dt = 100$ mA/μs Overshoot Undershoot | – – | – – | 50 50 | mV | |
| I_{SW3xQ} | Quiescent Current <ul style="list-style-type: none"> PFM Mode (Single Phase) APS Mode (Single Phase) PFM Mode (Independent mode) APS Mode (SW3A Independent mode) APS Mode (SW3B Independent mode) | – – – – – | 22 300 50 250 150 | – – – – – | μ A | |
| $R_{ON_{SW3AP}}$ | SW3A P-MOSFET $R_{DS(on)}$ at $V_{IN} = V_{IN_{SW3A}} = 3.3$ V | – | 215 | 245 | m Ω | |
| $R_{ON_{SW3AN}}$ | SW3A N-MOSFET $R_{DS(on)}$ at $V_{IN} = V_{IN_{SW3A}} = 3.3$ V | – | 258 | 326 | m Ω | |
| I_{SW3APQ} | SW3A P-MOSFET Leakage Current $V_{IN} = V_{IN_{SW3A}} = 4.5$ V | – | – | 7.5 | μ A | |

Table 71. SW3A/B electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SW3x}} = 3.6$ V, $V_{SW3x} = 1.5$ V, $I_{SW3x} = 100$ mA, $SW3x_PWRSTG[2:0] = [111]$, typical external component values, $f_{SW3x} = 2.0$ MHz, single phase and independent mode unless, otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SW3x}} = 3.6$ V, $V_{SW3x} = 1.5$ V, $I_{SW3x} = 100$ mA, $SW3x_PWRSTG[2:0] = [111]$, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--|---|------|------|------|------------|-------|
| Switch mode supply SW3a/B (continued) | | | | | | |
| I_{SW3ANQ} | SW3A N-MOSFET Leakage Current $V_{IN} = V_{IN_{SW3A}} = 4.5$ V | – | – | 2.5 | μ A | |
| $R_{ONSW3BP}$ | SW3B P-MOSFET $R_{DS(on)}$ at $V_{IN} = V_{IN_{SW3B}} = 3.3$ V | – | 215 | 245 | m Ω | |
| $R_{ONSW3BN}$ | SW3B N-MOSFET $R_{DS(on)}$ at $V_{IN} = V_{IN_{SW3B}} = 3.3$ V | – | 258 | 326 | m Ω | |
| I_{SW3BPQ} | SW3B P-MOSFET Leakage Current $V_{IN} = V_{IN_{SW3B}} = 4.5$ V | – | – | 7.5 | μ A | |
| I_{SW3BPQ} | SW3B N-MOSFET Leakage Current $V_{IN} = V_{IN_{SW3B}} = 4.5$ V | – | – | 2.5 | μ A | |
| $R_{SW3xDIS}$ | Discharge Resistance | – | 600 | – | Ω | |

Notes

- 49. When output is set to > 2.6 V the output will follow the input down when V_{IN} gets near 2.8 V.
- 50. Accuracy specification is inclusive of load and line regulation.
- 51. The higher output voltages available depend on the voltage drop in the conduction path as given by the following equation:
 $(V_{IN_{SW3x}} - V_{SW3x}) = I_{SW3x} * (DCR \text{ of Inductor} + R_{ON_{SW3xP}} + \text{PCB trace resistance})$.

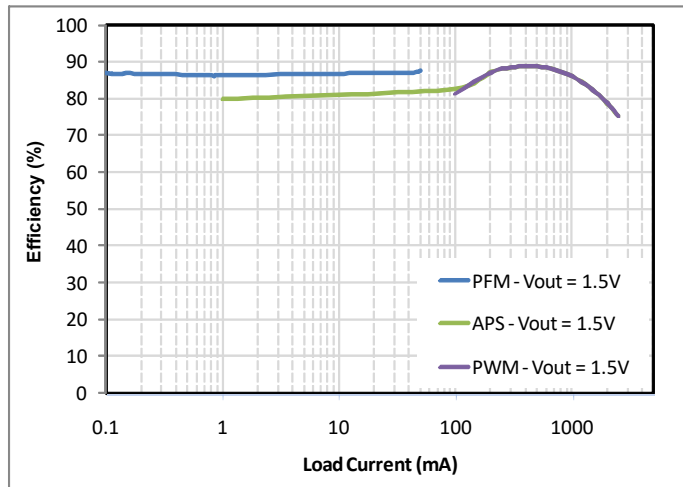


Figure 17. SW3AB single phase efficiency waveforms

6.4.5 Boost regulator

SWBST is a boost regulator with a programmable output from 5.0 to 5.15 V. SWBST can supply the VUSB regulator for the USB PHY in OTG mode, as well as the VBUS voltage. Note that the parasitic leakage path for a boost regulator will cause the SWBSTOUT and SWBSTFB voltage to be a Schottky drop below the input voltage whenever SWBST is disabled. The switching NMOS transistor is integrated on-chip. [Figure 18](#) shows the block diagram and component connection for the boost regulator.

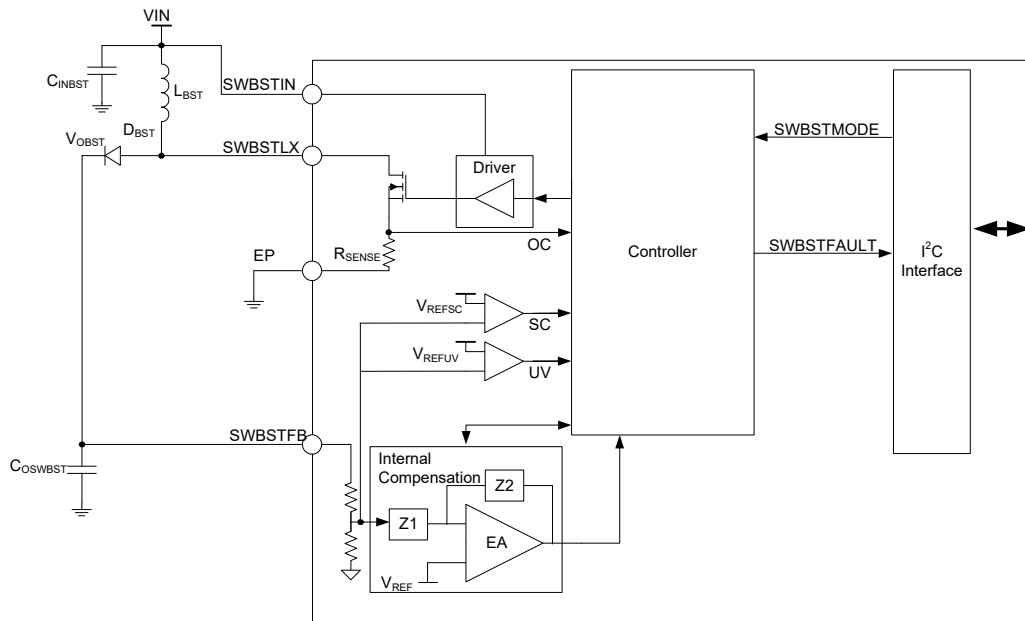


Figure 18. Boost regulator architecture

6.4.5.1 SWBST setup and control

Boost regulator control is done through a single register SWBSTCTL described in [Table 72](#). SWBST is included in the power-up sequence if its OTP power-up timing bits, SWBST_SEQ[4:0], are not all zeros.

Table 72. Register SWBSTCTL - ADDR 0x66

| Name | Bit # | R/W | Default | Description |
|----------------|-------|-----|---------|---|
| SWBST1VOLT | 1:0 | R/W | 0x00 | Set the output voltage for SWBST 00 = 5.000 V 01 = 5.050 V 10 = 5.100 V 11 = 5.150 V |
| SWBST1MODE | 3:2 | R | 0x02 | Set the Switching mode on Normal operation 00 = OFF 01 = PFM 10 = Auto (Default) ⁽⁵²⁾ 11 = APS |
| UNUSED | 4 | – | 0x00 | UNUSED |
| SWBST1STBYMODE | 6:5 | R/W | 0x02 | Set the Switching mode on Standby 00 = OFF 01 = PFM 10 = Auto (Default) ⁽⁵²⁾ 11 = APS |
| UNUSED | 7 | – | 0x00 | UNUSED |

Notes

52. In Auto mode, the controller automatically switches between PFM and APS modes depending on the load current. The SWBST regulator starts up by default in the Auto mode, if SWBST is part of the startup sequence.

6.4.5.2 SWBST external components

Table 73. SWBST external component requirements

| Components | Description | Values |
|--------------------------------|----------------------------------|----------------------|
| C_{INBST} ⁽⁵³⁾ | SWBST input capacitor | 10 μ F |
| $C_{INBSTHF}$ ⁽⁵³⁾ | SWBST decoupling input capacitor | 0.1 μ F |
| C_{OBST} ⁽⁵³⁾ | SWBST output capacitor | 2 x 22 μ F |
| L_{SBST} | SWBST inductor | 2.2 μ H |
| D_{BST} | SWBST boost diode | 1.0 A, 20 V Schottky |
| Notes | | |
| 53. Use X5R or X7R capacitors. | | |

6.4.5.3 SWBST specifications

Table 74. SWBST electrical specifications

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SWBST}} = 3.6$ V, $V_{SWBST} = 5.0$ V, $I_{SWBST} = 100$ mA, typical external component values, $f_{SWBST} = 2.0$ MHz, otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SWBST}} = 3.6$ V, $V_{SWBST} = 5.0$ V, $I_{SWBST} = 100$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameters | Min. | Typ. | Max. | Units | Notes |
|---------------------------------|---|--------|--------------------------|------------|------------|-----------------|
| Switch mode supply SWBST | | | | | | |
| $V_{IN_{SWBST}}$ | Input Voltage Range | 2.8 | – | 4.5 | V | |
| V_{SWBST} | Nominal Output Voltage | – | Table 72 | – | V | |
| $V_{SWBSTACC}$ | Output Voltage Accuracy $2.8 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ $0 < I_{SWBST} < I_{SWBST_{MAX}}$ | -4.0 | – | 3.0 | % | |
| ΔV_{SWBST} | Output Ripple $2.8 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ $0 < I_{SWBST} < I_{SWBST_{MAX}}$, excluding reverse recovery of Schottky diode | – | – | 120 | mV Vp-p | |
| $V_{SWBSTLOR}$ | DC Load Regulation $0 < I_{SWBST} < I_{SWBST_{MAX}}$ | – | 0.5 | – | mV/mA | |
| $V_{SWBSTLIR}$ | DC Line Regulation $2.8 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$, $I_{SWBST} = I_{SWBST_{MAX}}$ | – | 50 | – | mV | |
| I_{SWBST} | Continuous Load Current $2.8 \text{ V} \leq V_{IN} \leq 3.0 \text{ V}$ $3.0 \text{ V} \leq V_{IN} \leq 4.5 \text{ V}$ | – – | – – | 500 600 | mA | |
| I_{SWBSTQ} | Quiescent Current AUTO | – | 222 | 289 | μ A | |
| $R_{DSONBST}$ | MOSFET on Resistance | – | 206 | 306 | m Ω | |
| $I_{SWBSTLIM}$ | Peak Current Limit | 1400 | 2200 | 3200 | mA | ⁽⁵⁴⁾ |
| $V_{SWBSTOSH}$ | Start-up Overshoot $I_{SWBST} = 0.0$ mA | – | – | 500 | mV | |
| $V_{SWBSTTR}$ | Transient Load Response I_{SWBST} from 1.0 to 100 mA in 1.0 μ s Maximum transient Amplitude | – | – | 300 | mV | |
| $V_{SWBSTTR}$ | Transient Load Response I_{SWBST} from 100 to 1.0 mA in 1.0 μ s Maximum transient Amplitude | – | – | 300 | mV | |

Table 74. SWBST electrical specifications (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = V_{IN_{SWBST}} = 3.6$ V, $V_{SWBST} = 5.0$ V, $I_{SWBST} = 100$ mA, typical external component values, $f_{SWBST} = 2.0$ MHz, otherwise noted. Typical values are characterized at $V_{IN} = V_{IN_{SWBST}} = 3.6$ V, $V_{SWBST} = 5.0$ V, $I_{SWBST} = 100$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameters | Min. | Typ. | Max. | Units | Notes |
|---|---|------|------|------|---------|-------|
| Switch mode supply SWBST (continued) | | | | | | |
| $t_{SWBSTTR}$ | Transient Load Response I_{SWBST} from 1.0 to 100 mA in 1.0 μ s Time to settle 80% of transient | – | – | 500 | μ s | |
| $t_{SWBSTTR}$ | Transient Load Response I_{SWBST} from 100 to 1.0 mA in 1.0 μ s Time to settle 80% of transient | – | – | 20 | ms | |
| $I_{SWBSTHSQ}$ | NMOS Off Leakage $SWBSTIN = 4.5$ V, $SWBSTMODE [1:0] = 00$ | – | 1.0 | 5.0 | μ A | |
| $t_{ON_{SWBST}}$ | Turn-on Time Enable to 90% of V_{SWBST} , $I_{SWBST} = 0.0$ mA | – | – | 2.0 | ms | |
| f_{SWBST} | Switching Frequency | – | 2.0 | – | MHz | |
| η_{SWBST} | Efficiency $I_{SWBST} = I_{SWBST_{MAX}}$ | – | 86 | – | % | |

Notes

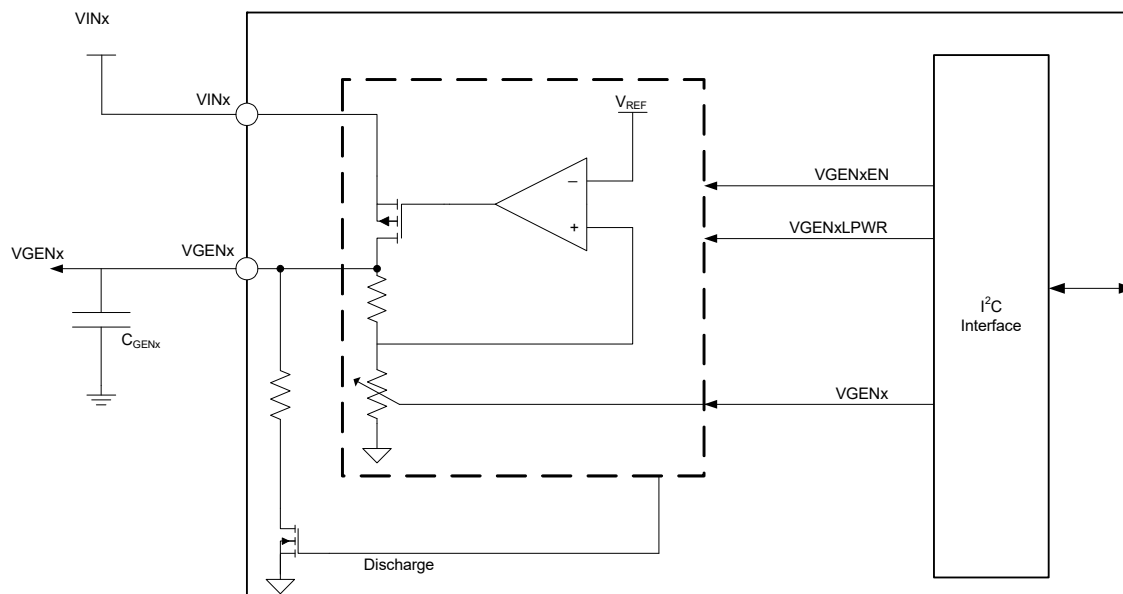
54. Only in Auto mode.

6.4.6 LDO regulators description

This section describes the LDO regulators provided by the PF0200. All regulators use the main bandgap as reference. Refer to [Bias and references block description](#) section for further information on the internal reference voltages.

A Low Power mode is automatically activated by reducing bias currents when the load current is less than $I_{Lmax}/5$. However, the lowest bias currents may be attained by forcing the part into its Low Power mode by setting the $VGENxLPWR$ bit. The use of this bit is only recommended when the load is expected to be less than $I_{Lmax}/50$, otherwise performance may be degraded.

When a regulator is disabled, the output will be discharged by an internal pull-down. The pull-down is also activated when $RESETBMCU$ is low.


Figure 19. General LDO block diagram

6.4.6.1 Transient response waveforms

Idealized stimulus and response waveforms for transient line and transient load tests are depicted in [Figure 20](#). Note that the transient line and load response refers to the overshoot, or undershoot only, excluding the DC shift.

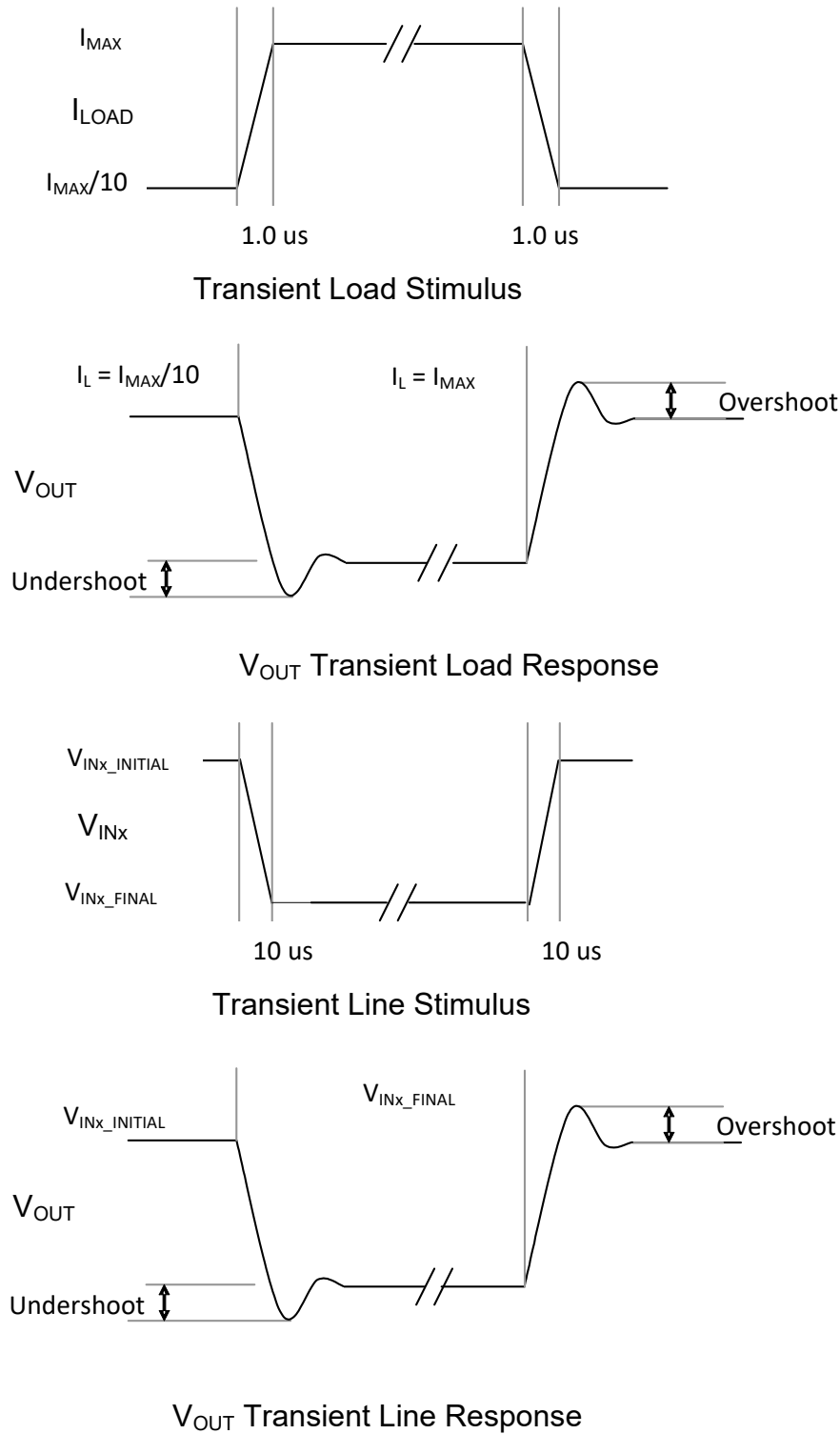


Figure 20. Transient waveforms

6.4.6.2 Short-circuit protection

All general purpose LDOs have short-circuit protection capability. The Short-circuit Protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize the chance of product damage. If a short-circuit condition is detected, the LDO will be disabled by resetting its VGENxEN bit, while at the same time, an interrupt VGENxFAULTI will be generated to flag the fault to the system processor. The VGENxFAULTI interrupt is maskable through the VGENxFAULTM mask bit.

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, the regulators will not automatically be disabled upon a short-circuit detection. However, the current limiter will continue to limit the output current of the regulator. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators will be disabled if an overloaded condition occurs. A fault interrupt, VGENxFAULTI, will be generated in an overload condition regardless of the state of the REGSCPEN bit. See [Table 75](#) for SCP behavior configuration.

Table 75. Short-circuit behavior

| REGSCPEN[0] | Short-circuit behavior |
|-------------|------------------------|
| 0 | Current limit |
| 1 | Shutdown |

6.4.6.3 LDO regulator control

Each LDO is fully controlled through its respective VGENxCTL register. This register enables the user to set the LDO output voltage according to [Table 76](#) for VGEN1 and VGEN2; and uses the voltage set point on [Table 77](#) for VGEN3 through VGEN6.

Table 76. VGEN1, VGEN2 output voltage configuration

| Set point | VGENx[3:0] | VGENx output (V) |
|-----------|------------|------------------|
| 0 | 0000 | 0.800 |
| 1 | 0001 | 0.850 |
| 2 | 0010 | 0.900 |
| 3 | 0011 | 0.950 |
| 4 | 0100 | 1.000 |
| 5 | 0101 | 1.050 |
| 6 | 0110 | 1.100 |
| 7 | 0111 | 1.150 |
| 8 | 1000 | 1.200 |
| 9 | 1001 | 1.250 |
| 10 | 1010 | 1.300 |
| 11 | 1011 | 1.350 |
| 12 | 1100 | 1.400 |
| 13 | 1101 | 1.450 |
| 14 | 1110 | 1.500 |
| 15 | 1111 | 1.550 |

Table 77. VGEN3/ 4/ 5/ 6 output voltage configuration

| Set point | VGENx[3:0] | VGENx output (V) |
|-----------|------------|------------------|
| 0 | 0000 | 1.80 |
| 1 | 0001 | 1.90 |
| 2 | 0010 | 2.00 |
| 3 | 0011 | 2.10 |
| 4 | 0100 | 2.20 |
| 5 | 0101 | 2.30 |
| 6 | 0110 | 2.40 |
| 7 | 0111 | 2.50 |
| 8 | 1000 | 2.60 |
| 9 | 1001 | 2.70 |
| 10 | 1010 | 2.80 |
| 11 | 1011 | 2.90 |
| 12 | 1100 | 3.00 |
| 13 | 1101 | 3.10 |
| 14 | 1110 | 3.20 |
| 15 | 1111 | 3.30 |

Besides the output voltage configuration, the LDOs can be enabled or disabled at anytime during normal mode operation, as well as programmed to stay “ON” or be disabled when the PMIC enters Standby mode. Each regulator has associated I²C bits for this. [Table 78](#) presents a summary of all valid combinations of the control bits on VGENxCTL register and the expected behavior of the LDO output.

Table 78. LDO control

| VGENxEN | VGENxLPWR | VGENxSTBY | STANDBY ⁽⁵⁵⁾ | VGENxOUT |
|---------|-----------|-----------|-------------------------|-----------|
| 0 | X | X | X | Off |
| 1 | 0 | 0 | X | On |
| 1 | 1 | 0 | X | Low Power |
| 1 | X | 1 | 0 | On |
| 1 | 0 | 1 | 1 | Off |
| 1 | 1 | 1 | 1 | Low Power |

Notes

55. STANDBY refers to a Standby event as described earlier.

For more detail information, [Table 79](#) through [Table 84](#) provide a description of all registers necessary to operate all six general purpose LDO regulators.

Table 79. Register VGEN1CTL - ADDR 0x6C

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| VGEN1 | 3:0 | R/W | 0x80 | Sets VGEN1 output voltage. See Table 76 for all possible configurations. |
| VGEN1EN | 4 | – | 0x00 | Enables or Disables VGEN1 output 0 = OFF 1 = ON |
| VGEN1STBY | 5 | R/W | 0x00 | Set VGEN1 output state when in Standby. Refer to Table 78 . |
| VGEN1LPWR | 6 | R/W | 0x00 | Enable Low Power mode for VGEN1. Refer to Table 78 . |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 80. Register VGEN2CTL - ADDR 0x6D

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| VGEN2 | 3:0 | R/W | 0x80 | Sets VGEN2 output voltage. See Table 76 for all possible configurations. |
| VGEN2EN | 4 | – | 0x00 | Enables or Disables VGEN2 output 0 = OFF 1 = ON |
| VGEN2STBY | 5 | R/W | 0x00 | Set VGEN2 output state when in Standby. Refer to Table 78 . |
| VGEN2LPWR | 6 | R/W | 0x00 | Enable Low Power Mode for VGEN2. Refer to Table 78 . |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 81. Register VGEN3CTL - ADDR 0x6E

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| VGEN3 | 3:0 | R/W | 0x80 | Sets VGEN3 output voltage. See Table 77 for all possible configurations. |
| VGEN3EN | 4 | – | 0x00 | Enables or Disables VGEN3 output 0 = OFF 1 = ON |
| VGEN3STBY | 5 | R/W | 0x00 | Set VGEN3 output state when in Standby. Refer to Table 78 . |
| VGEN3LPWR | 6 | R/W | 0x00 | Enable Low Power mode for VGEN3. Refer to Table 78 . |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 82. Register VGEN4CTL - ADDR 0x6F

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| VGEN4 | 3:0 | R/W | 0x80 | Sets VGEN4 output voltage. See Table 77 for all possible configurations. |
| VGEN4EN | 4 | – | 0x00 | Enables or Disables VGEN4 output 0 = OFF 1 = ON |
| VGEN4STBY | 5 | R/W | 0x00 | Set VGEN4 output state when in Standby. Refer to Table 78 . |
| VGEN4LPWR | 6 | R/W | 0x00 | Enable Low Power mode for VGEN4. Refer to Table 78 . |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 83. Register VGEN5CTL - ADDR 0x70

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| VGEN5 | 3:0 | R/W | 0x80 | Sets VGEN5 output voltage. See Table 77 for all possible configurations. |
| VGEN5EN | 4 | – | 0x00 | Enables or Disables VGEN5 output 0 = OFF 1 = ON |
| VGEN5STBY | 5 | R/W | 0x00 | Set VGEN5 output state when in Standby. Refer to Table 78 . |
| VGEN5LPWR | 6 | R/W | 0x00 | Enable Low Power mode for VGEN5. Refer to Table 78 . |
| UNUSED | 7 | – | 0x00 | UNUSED |

Table 84. Register VGEN6CTL - ADDR 0x71

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|--|
| VGEN6 | 3:0 | R/W | 0x80 | Sets VGEN6 output voltage. See Table 77 for all possible configurations. |
| VGEN6EN | 4 | – | 0x00 | Enables or Disables VGEN6 output 0 = OFF 1 = ON |
| VGEN6STBY | 5 | R/W | 0x00 | Set VGEN6 output state when in Standby. Refer to Table 78 . |
| VGEN6LPWR | 6 | R/W | 0x00 | Enable Low Power mode for VGEN6. Refer to Table 78 . |
| UNUSED | 7 | – | 0x00 | UNUSED |

6.4.6.4 External components

[Table 85](#) lists the typical component values for the general purpose LDO regulators.

Table 85. LDO external components

| Regulator | Output capacitor (μF) ⁽⁵⁶⁾ |
|-----------|--|
| VGEN1 | 2.2 |
| VGEN2 | 4.7 |
| VGEN3 | 2.2 |
| VGEN4 | 4.7 |
| VGEN5 | 2.2 |
| VGEN6 | 2.2 |

Notes

56. Use X5R/X7R ceramic capacitors.

6.4.6.5 LDO specifications

VGEN1

Table 86. VGEN1 electrical characteristics

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN1}[3:0] = 1111$, $I_{GEN1} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN1}[3:0] = 1111$, $I_{GEN1} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|-----------------|--|------|--------------------------|------|---------------|-------|
| VGEN1 | | | | | | |
| V_{IN1} | Operating Input Voltage | 1.75 | – | 3.40 | V | |
| $V_{GEN1NOM}$ | Nominal Output Voltage | – | Table 76 | – | V | |
| I_{GEN1} | Operating Load Current | 0.0 | – | 100 | mA | |
| VGEN1 DC | | | | | | |
| $V_{GEN1TOL}$ | Output Voltage Tolerance 1.75 V < V_{IN1} < 3.4 V 0.0 mA < I_{GEN1} < 100 mA $V_{GEN1}[3:0] = 0000$ to 1111 | -3.0 | – | 3.0 | % | |
| $V_{GEN1LOR}$ | Load Regulation (V_{GEN1} at $I_{GEN1} = 100$ mA) - (V_{GEN1} at $I_{GEN1} = 0.0$ mA) For any 1.75 V < V_{IN1} < 3.4 V | – | 0.15 | – | mV/mA | |
| $V_{GEN1LIR}$ | Line Regulation (V_{GEN1} at $V_{IN1} = 3.4$ V) - (V_{GEN1} at $V_{IN1} = 1.75$ V) For any 0.0 mA < I_{GEN1} < 100 mA | – | 0.30 | – | mV/mA | |
| $I_{GEN1LIM}$ | Current Limit I_{GEN1} when VGEN1 is forced to $V_{GEN1NOM}/2$ | 122 | 167 | 200 | mA | |
| $I_{GEN1OCP}$ | Overcurrent Protection Threshold I_{GEN1} required to cause the SCP function to disable LDO when REGSCPEN = 1 | 115 | – | 200 | mA | |
| I_{GEN1Q} | Quiescent Current No load, Change in I_{VIN} and I_{VIN1} When VGEN1 enabled | – | 14 | – | μA | |

Table 86. VGEN1 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN1}[3:0] = 1111$, $I_{GEN1} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN1}[3:0] = 1111$, $I_{GEN1} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--|--|-------------|----------------------|----------------------|---------|-------|
| VGEN1 AC and transient | | | | | | |
| $PSRR_{VGEN1}$ | PSRR <ul style="list-style-type: none"> $I_{GEN1} = 75$ mA, 20 Hz to 20 kHz $V_{GEN1}[3:0] = 0000 - 1101$ $V_{GEN1}[3:0] = 1110, 1111$ | 50 37 | 60 45 | – – | dB | (57) |
| $NOISE_{VGEN1}$ | Output Noise Density <ul style="list-style-type: none"> $V_{IN1} = 1.75$ V, $I_{GEN1} = 75$ mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz | – – – | –108 –118 –124 | –100 –108 –112 | dBV/√Hz | |
| $SLWR_{VGEN1}$ | Turn-on Slew Rate <ul style="list-style-type: none"> 10% to 90% of end value 1.75 V $\leq V_{IN1} \leq 3.4$ V, $I_{GEN1} = 0.0$ mA $V_{GEN1}[3:0] = 0000$ to 0111 $V_{GEN1}[3:0] = 1000$ to 1111 | – – | – – | 12.5 16.5 | mV/μs | |
| $GEN1_{tON}$ | Turn-On Time <ul style="list-style-type: none"> Enable to 90% of end value, $V_{IN1} = 1.75$ V, 3.4 V $I_{GEN1} = 0.0$ mA | 60 | – | 500 | μs | |
| $GEN1_{tOFF}$ | Turn-Off Time <ul style="list-style-type: none"> Disable to 10% of initial value, $V_{IN1} = 1.75$ V $I_{GEN1} = 0.0$ mA | – | – | 10 | ms | |
| $GEN1_{OSHT}$ | Start-Up Overshoot <ul style="list-style-type: none"> $V_{IN1} = 1.75$ V, 3.4 V, $I_{GEN1} = 0.0$ mA | – | 1.0 | 2.0 | % | |
| $V_{GEN1LOTR}$ | Transient Load Response <ul style="list-style-type: none"> $V_{IN1} = 1.75$ V, 3.4 V $I_{GEN1} = 10$ to 100 mA in 1.0 μs. Peak of overshoot or undershoot of V_{GEN1} with respect to final value Refer to Figure 20 | – | – | 3.0 | % | |
| $V_{GEN1LITR}$ | Transient Line Response <ul style="list-style-type: none"> $I_{GEN1} = 75$ mA $V_{IN1_{INITIAL}} = 1.75$ V to $V_{IN1_{FINAL}} = 2.25$ V for $V_{GEN1}[3:0] = 0000$ to 1101 $V_{IN1_{INITIAL}} = V_{GEN1} + 0.3$ V to $V_{IN1_{FINAL}} = V_{GEN1} + 0.8$ V for $V_{GEN1}[3:0] = 1110, 1111$ Refer to Figure 20 | – | 5.0 | 8.0 | mV | |
| Notes | | | | | | |
| 57. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. | | | | | | |

VGEN2

Table 87. VGEN2 electrical characteristics

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN2}[3:0] = 1111$, $I_{GEN2} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN2}[3:0] = 1111$, $I_{GEN2} = 10$ mA and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--------|-----------|------|------|------|------|-------|
|--------|-----------|------|------|------|------|-------|

VGEN2

| | | | | | | |
|------------------|-------------------------|------|--------------------------|------|----|--|
| V_{IN1} | Operating Input Voltage | 1.75 | – | 3.40 | V | |
| $V_{GEN2_{NOM}}$ | Nominal Output Voltage | – | Table 76 | – | V | |
| I_{GEN2} | Operating Load Current | 0.0 | – | 250 | mA | |

VGEN2 active mode - DC

| | | | | | | |
|------------------|--|------|------|-----|-------|--|
| $V_{GEN2_{TOL}}$ | Output Voltage Tolerance 1.75 V < V_{IN1} < 3.4 V 0.0 mA < I_{GEN2} < 250 mA $V_{GEN2}[3:0] = 0000$ to 1111 | -3.0 | – | 3.0 | % | |
| $V_{GEN2_{LOR}}$ | Load Regulation (V_{GEN2} at $I_{GEN2} = 250$ mA) - (V_{GEN2} at $I_{GEN2} = 0.0$ mA) For any 1.75 V < V_{IN1} < 3.4 V | – | 0.05 | – | mV/mA | |
| $V_{GEN2_{LIR}}$ | Line Regulation (V_{GEN2} at $V_{IN1} = 3.4$ V) - (V_{GEN2} at $V_{IN1} = 1.75$ V) For any 0.0 mA < I_{GEN2} < 250 mA | – | 0.50 | – | mV/mA | |
| $I_{GEN2_{LIM}}$ | Current Limit I_{GEN2} when VGEN2 is forced to $V_{GEN2_{NOM}}/2$ | 305 | 417 | 510 | mA | |
| $I_{GEN2_{OCP}}$ | Over-current Protection Threshold I_{GEN2} required to cause the SCP function to disable LDO when REGSCPEN = 1 | 290 | – | 500 | mA | |
| $I_{GEN2_{Q}}$ | Quiescent Current No load, Change in I_{VIN} and I_{VIN1} When VGEN2 enabled | – | 16 | – | μA | |

VGEN2 AC and transient

| | | | | | | |
|--------------------|---|-------------|----------------------|----------------------|---------|------|
| $PSRR_{V_{GEN2}}$ | PSRR • $I_{GEN2} = 187.5$ mA, 20 Hz to 20 kHz $V_{GEN2}[3:0] = 0000 - 1101$ $V_{GEN2}[3:0] = 1110, 1111$ | 50 37 | 60 45 | – – | dB | (58) |
| $NOISE_{V_{GEN2}}$ | Output Noise Density • $V_{IN1} = 1.75$ V, $I_{GEN2} = 187.5$ mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz | – – – | -108 -118 -124 | -100 -108 -112 | dBV/√Hz | |
| $SLWR_{V_{GEN2}}$ | Turn-On Slew Rate • 10% to 90% of end value • 1.75 V ≤ V_{IN1} ≤ 3.4 V, $I_{GEN2} = 0.0$ mA $V_{GEN2}[3:0] = 0000$ to 0111 $V_{GEN2}[3:0] = 1000$ to 1111 | – – | – – | 12.5 16.5 | mV/μs | |
| $GEN2_{ION}$ | Turn-On Time Enable to 90% of end value, $V_{IN1} = 1.75$ V, 3.4 V $I_{GEN2} = 0.0$ mA | 60 | – | 500 | μs | |
| $GEN2_{IOFF}$ | Turn-Off Time Disable to 10% of initial value, $V_{IN1} = 1.75$ V $I_{GEN2} = 0.0$ mA | – | – | 10 | ms | |

Table 87. VGEN2 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN2[3:0]} = 1111$, $I_{GEN2} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN1} = 3.0$ V, $V_{GEN2[3:0]} = 1111$, $I_{GEN2} = 10$ mA and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|--|------|------|------|------|-------|
| VGEN2 AC and transient (continued) | | | | | | |
| $GEN2_{OSHT}$ | Start-up Overshoot $V_{IN1} = 1.75$ V, 3.4 V, $I_{GEN2} = 0.0$ mA | – | 1.0 | 2.0 | % | |
| $V_{GEN2LOTR}$ | Transient Load Response $V_{IN1} = 1.75$ V, 3.4 V $I_{GEN2} = 25$ to 250 mA in 1.0 μ s Peak of overshoot or undershoot of VGEN2 with respect to final value Refer to Figure 20 | – | – | 3.0 | % | |
| $V_{GEN2LITR}$ | Transient Line Response $I_{GEN2} = 187.5$ mA $V_{IN1_{INITIAL}} = 1.75$ V to $V_{IN1_{FINAL}} = 2.25$ V for $V_{GEN2[3:0]} = 0000$ to 1101 $V_{IN1_{INITIAL}} = V_{GEN2} + 0.3$ V to $V_{IN1_{FINAL}} = V_{GEN2} + 0.8$ V for $V_{GEN2[3:0]} = 1110, 1111$ Refer to Figure 20 | – | 5.0 | 8.0 | mV | |

Notes

58. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test.

VGEN3

Table 88. VGEN3 electrical characteristics

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN3}[3:0] = 1111$, $I_{GEN3} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN3}[3:0] = 1111$, $I_{GEN3} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | |
|-------------------------------|--|------------------------------------|--------------------------|------------------------------|-------------------------|------|
| VGEN3 | | | | | | |
| V_{IN2} | Operating Input Voltage $1.8\text{ V} \leq V_{GEN3NOM} \leq 2.5\text{ V}$ $2.6\text{ V} \leq V_{GEN3NOM} \leq 3.3\text{ V}$ | 2.8 V_{GEN3NO} $M^+ 0.250$ | – – | 3.6 3.6 | V | (59) |
| $V_{GEN3NOM}$ | Nominal Output Voltage | – | Table 77 | – | V | |
| I_{GEN3} | Operating Load Current | 0.0 | – | 100 | mA | |
| VGEN3 DC | | | | | | |
| $V_{GEN3TOL}$ | Output Voltage Tolerance $V_{IN2MIN} < V_{IN2} < 3.6\text{ V}$ $0.0\text{ mA} < I_{GEN3} < 100\text{ mA}$ $V_{GEN3}[3:0] = 0000$ to 1111 | -3.0 | – | 3.0 | % | |
| $V_{GEN3LOR}$ | Load Regulation $(V_{GEN3} \text{ at } I_{GEN3} = 100\text{ mA}) - (V_{GEN3} \text{ at } I_{GEN3} = 0.0\text{ mA})$ For any $V_{IN2MIN} < V_{IN2} < 3.6\text{ V}$ | – | 0.07 | – | mV/mA | |
| $V_{GEN3LIR}$ | Line Regulation $(V_{GEN3} \text{ at } V_{IN2} = 3.6\text{ V}) - (V_{GEN3} \text{ at } V_{IN2MIN})$ For any $0.0\text{ mA} < I_{GEN3} < 100\text{ mA}$ | – | 0.8 | – | mV/mA | |
| $I_{GEN3LIM}$ | Current Limit I_{GEN3} when VGEN3 is forced to $V_{GEN3NOM}/2$ | 127 | 167 | 200 | mA | |
| $I_{GEN3OCP}$ | Overcurrent Protection Threshold I_{GEN3} required to cause the SCP function to disable LDO when $REGSCPEN = 1$ | 120 | – | 200 | mA | |
| I_{GEN3Q} | Quiescent Current No load, Change in I_{VIN} and I_{VIN2} When VGEN3 enabled | – | 13 | – | μ A | |
| VGEN3 AC and transient | | | | | | |
| $PSRR_{VGEN3}$ | PSRR • $I_{GEN3} = 75\text{ mA}$, 20 Hz to 20 kHz $V_{GEN3}[3:0] = 0000 - 1110$, $V_{IN2} = V_{IN2MIN} + 100\text{ mV}$ $V_{GEN3}[3:0] = 0000 - 1000$, $V_{IN2} = V_{GEN3NOM} + 1.0\text{ V}$ | 35 55 | 40 60 | – – | dB | (60) |
| $NOISE_{VGEN3}$ | Output Noise Density • $V_{IN2} = V_{IN2MIN}$, $I_{GEN3} = 75\text{ mA}$ 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz | – – – | -114 -129 -135 | -102 -123 -130 | dBV/ $\sqrt{\text{Hz}}$ | |
| $SLWR_{VGEN3}$ | Turn-on Slew Rate • 10% to 90% of end value • $V_{IN2MIN} \leq V_{IN2} \leq 3.6\text{ V}$, $I_{GEN3} = 0.0\text{ mA}$ $V_{GEN3}[3:0] = 0000$ to 0011 $V_{GEN3}[3:0] = 0100$ to 0111 $V_{GEN3}[3:0] = 1000$ to 1011 $V_{GEN3}[3:0] = 1100$ to 1111 | – – – – | – – – – | 22.0 26.5 30.5 34.5 | mV/ μ s | |
| $GEN3_{ION}$ | Turn-on Time Enable to 90% of end value, $V_{IN2} = V_{IN2MIN}$, 3.6 V $I_{GEN3} = 0.0\text{ mA}$ | 60 | – | 500 | μ s | |

Table 88. VGEN3 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN3}[3:0] = 1111$, $I_{GEN3} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN3}[3:0] = 1111$, $I_{GEN3} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | |
|---|---|------|------|------|------|--|
| VGEN3 AC and transient (continued) | | | | | | |
| $GEN3_{TOFF}$ | Turn-off Time Disable to 10% of initial value, $V_{IN2} = VIN2_{MIN}$ $I_{GEN3} = 0.0$ mA | – | – | 10 | ms | |
| $GEN3_{OSHT}$ | Start-up Overshoot $V_{IN2} = VIN2_{MIN}$, 3.6 V, $I_{GEN3} = 0.0$ mA | – | 1.0 | 2.0 | % | |
| $V_{GEN3LOTR}$ | Transient Load Response $V_{IN2} = VIN2_{MIN}$, 3.6 V $I_{GEN3} = 10$ to 100 mA in $1.0\mu s$ Peak of overshoot or undershoot of VGEN3 with respect to final value. Refer to Figure 20 | – | – | 3.0 | % | |
| $V_{GEN3LITR}$ | Transient Line Response $I_{GEN3} = 75$ mA $VIN2_{INITIAL} = 2.8$ V to $VIN2_{FINAL} = 3.3$ V for $GEN3[3:0] = 0000$ to 0111 $VIN2_{INITIAL} = V_{GEN3} + 0.3$ V to $VIN2_{FINAL} = V_{GEN3} + 0.8$ V for $GEN3[3:0] = 1000$ to 1010 $VIN2_{INITIAL} = V_{GEN3} + 0.25$ V to $VIN2_{FINAL} = 3.6$ V for $GEN3[3:0] = 1011$ to 1111 Refer to Figure 20 | – | 5.0 | 8.0 | mV | |

Notes

59. When the LDO Output voltage is set above 2.6 V, the minimum allowed input voltage needs to be at least the output voltage plus 0.25 V, for proper regulation due to the dropout voltage generated through the internal LDO transistor.
60. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. $VIN2_{MIN}$ refers to the minimum allowed input voltage for a particular output voltage.

VGEN4**Table 89. VGEN4 electrical characteristics**

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN4}[3:0] = 1111$, $I_{GEN4} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN4}[3:0] = 1111$, $I_{GEN4} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|------------------|---|--------------------------------|--------------------------|------------|------|-------|
| VGEN4 | | | | | | |
| V_{IN2} | Operating Input Voltage 1.8 V $\leq V_{GEN4_{NOM}} \leq 2.5$ V 2.6 V $\leq V_{GEN4_{NOM}} \leq 3.3$ V | 2.8 $V_{GEN4_{NO}} + 0.250$ | – – | 3.6 3.6 | V | (61) |
| $V_{GEN4_{NOM}}$ | Nominal Output Voltage | – | Table 77 | – | V | |
| I_{GEN4} | Operating Load Current | 0.0 | – | 350 | mA | |

VGEN4 DC

| | | | | | | |
|---------------|--|------|------|-----|-------|--|
| $V_{GEN4TOL}$ | Output Voltage Tolerance $VIN2_{MIN} < V_{IN2} < 3.6$ V 0.0 mA $< I_{GEN4} < 350$ mA $V_{GEN4}[3:0] = 0000$ to 1111 | -3.0 | – | 3.0 | % | |
| $V_{GEN4LOR}$ | Load Regulation (V_{GEN4} at $I_{GEN4} = 350$ mA) - (V_{GEN4} at $I_{GEN4} = 0.0$ mA) For any $VIN2_{MIN} < V_{IN2} < 3.6$ V | – | 0.07 | – | mV/mA | |

Table 89. VGEN4 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN4}[3:0] = 1111$, $I_{GEN4} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN4}[3:0] = 1111$, $I_{GEN4} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|-------------------------------|---|------------------|----------------------|------------------------------|---------|-------|
| VGEN4 DC (continued) | | | | | | |
| $V_{GEN4LIR}$ | Line Regulation (V_{GEN4} at 3.6 V) - (V_{GEN4} at V_{IN2MIN}) For any 0.0 mA < I_{GEN4} < 350 mA | – | 0.80 | – | mV/mA | |
| $I_{GEN4LIM}$ | Current Limit I_{GEN4} when VGEN4 is forced to $V_{GEN4NOM}/2$ | 435 | 584.5 | 700 | mA | |
| $I_{GEN4OCP}$ | Overcurrent Protection Threshold I_{GEN4} required to cause the SCP function to disable LDO when $REGSCPEN = 1$ | 420 | – | 700 | mA | |
| I_{GEN4Q} | Quiescent Current No load, Change in I_{VIN} and I_{VIN2} When VGEN4 enabled | – | 13 | – | μA | |
| VGEN4 AC and transient | | | | | | |
| $PSRR_{VGEN4}$ | PSRR • $I_{GEN4} = 262.5$ mA, 20 Hz to 20 kHz $V_{GEN4}[3:0] = 0000 - 1110$, $V_{IN2} = V_{IN2MIN} + 100$ mV $V_{GEN4}[3:0] = 0000 - 1000$, $V_{IN2} = V_{GEN4NOM} + 1.0$ V | 35 55 | 40 60 | – – | dB | (62) |
| $NOISE_{VGEN4}$ | Output Noise Density • $V_{IN2} = V_{IN2MIN}$, $I_{GEN4} = 262.5$ mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz | – – – | –114 –129 –135 | –102 –123 –130 | dBV/√Hz | |
| $SLWR_{VGEN4}$ | Turn-on Slew Rate • 10% to 90% of end value • $V_{IN2MIN} \leq V_{IN2} \leq 3.6$ V, $I_{GEN4} = 0.0$ mA $V_{GEN4}[3:0] = 0000$ to 0011 $V_{GEN4}[3:0] = 0100$ to 0111 $V_{GEN4}[3:0] = 1000$ to 1011 $V_{GEN4}[3:0] = 1100$ to 1111 | – – – – | – – – – | 22.0 26.5 30.5 34.5 | mV/μs | |
| $GEN4_{tON}$ | Turn-on Time Enable to 90% of end value, $V_{IN2} = V_{IN2MIN}$, 3.6 V $I_{GEN4} = 0.0$ mA | 60 | – | 500 | μs | |
| $GEN4_{tOFF}$ | Turn-off Time Disable to 10% of initial value, $V_{IN2} = V_{IN2MIN}$ $I_{GEN4} = 0.0$ mA | – | – | 10 | ms | |
| $GEN4_{OSHT}$ | Start-up Overshoot $V_{IN2} = V_{IN2MIN}$, 3.6 V, $I_{GEN4} = 0.0$ mA | – | 1.0 | 2.0 | % | |
| $V_{GEN4LOTR}$ | Transient Load Response $V_{IN2} = V_{IN2MIN}$, 3.6 V $I_{GEN4} = 35$ to 350 mA in 1.0 μs Peak of overshoot or undershoot of VGEN4 with respect to final value. Refer to Figure 20 | – | – | 3.0 | % | |

Table 89. VGEN4 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN4}[3:0] = 1111$, $I_{GEN4} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN2} = 3.6$ V, $V_{GEN4}[3:0] = 1111$, $I_{GEN4} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|--|------|------|------|------|-------|
| VGEN4 AC and transient (continued) | | | | | | |
| $V_{GEN4LITR}$ | Transient Line Response $I_{GEN4} = 262.5$ mA $V_{IN2_INITIAL} = 2.8$ V to $V_{IN2_FINAL} = 3.3$ V for $V_{GEN4}[3:0] = 0000$ to 0111 $V_{IN2_INITIAL} = V_{GEN4} + 0.3$ V to $V_{IN2_FINAL} = V_{GEN4} + 0.8$ V for $V_{GEN4}[3:0] = 1000$ to 1010 $V_{IN2_INITIAL} = V_{GEN4} + 0.25$ V to $V_{IN2_FINAL} = 3.6$ V for $V_{GEN4}[3:0] = 1011$ to 1111 Refer to Figure 20 | – | 5.0 | 8.0 | mV | |

Notes

- When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
- The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. V_{IN2_MIN} refers to the minimum allowed input voltage for a particular output voltage.

VGEN5**Table 90. VGEN5 electrical characteristics**

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN5}[3:0] = 1111$, $I_{GEN5} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN5}[3:0] = 1111$, $I_{GEN5} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|-----------------|---|--------------------------------------|--------------------------|------------|------|-------|
| VGEN5 | | | | | | |
| V_{IN3} | Operating Input Voltage 1.8 V \leq $V_{GEN5_NOM} \leq 2.5$ V 2.6 V \leq $V_{GEN5_NOM} \leq 3.3$ V | 2.8 V_{GEN5_NO} $M + 0.250$ | – – | 4.5 4.5 | V | (63) |
| V_{GEN5_NOM} | Nominal Output Voltage | – | Table 77 | – | V | |
| I_{GEN5} | Operating Load Current | 0.0 | – | 100 | mA | |

VGEN5 active mode – DC

| | | | | | | |
|---------------|---|------|------|-----|-------|--|
| $V_{GEN5TOL}$ | Output Voltage Tolerance $V_{IN3_MIN} < V_{IN3} < 4.5$ V 0.0 mA $< I_{GEN5} < 100$ mA $V_{GEN5}[3:0] = 0000$ to 1111 | -3.0 | – | 3.0 | % | |
| $V_{GEN5LOR}$ | Load Regulation $(V_{GEN5} \text{ at } I_{GEN5} = 100 \text{ mA}) - (V_{GEN5} \text{ at } I_{GEN5} = 0.0 \text{ mA})$ For any $V_{IN3_MIN} < V_{IN3} < 4.5$ mV | – | 0.10 | – | mV/mA | |
| $V_{GEN5LIR}$ | Line Regulation $(V_{GEN5} \text{ at } V_{IN3} = 4.5 \text{ V}) - (V_{GEN5} \text{ at } V_{IN3_MIN})$ For any $0.0 \text{ mA} < I_{GEN5} < 100 \text{ mA}$ | – | 0.50 | – | mV/mA | |
| $I_{GEN5LIM}$ | Current Limit I_{GEN5} when V_{GEN5} is forced to $V_{GEN5_NOM}/2$ | 122 | 167 | 200 | mA | |
| $I_{GEN5OCP}$ | Overcurrent Protection threshold I_{GEN5} required to cause the SCP function to disable LDO when $REGSCPEN = 1$ | 120 | – | 200 | mA | |

Table 90. VGEN5 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN5}[3:0] = 1111$, $I_{GEN5} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN5}[3:0] = 1111$, $I_{GEN5} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|------------------|----------------------|------------------------------|-----------------|-------|
| VGEN5 active mode – DC (continued) | | | | | | |
| I_{GEN5Q} | Quiescent Current No load, Change in V_{IN} and V_{IN3} When VGEN5 enabled | – | 13 | – | μ A | |
| VGEN5 AC and transient | | | | | | |
| $PSRR_{VGEN5}$ | PSRR • $I_{GEN5} = 75$ mA, 20 Hz to 20 kHz VGEN5[3:0] = 0000 - 1111, $V_{IN3} = V_{IN3_{MIN}} + 100$ mV VGEN5[3:0] = 0000 - 1111, $V_{IN3} = V_{GEN5_{NOM}} + 1.0$ V | 35 52 | 40 60 | – – | dB | (64) |
| $NOISE_{VGEN5}$ | Output Noise Density • $V_{IN3} = V_{IN3_{MIN}}$, $I_{GEN5} = 75$ mA 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz | – – – | –114 –129 –135 | –102 –123 –130 | dBV/ \sqrt Hz | |
| $SLWR_{VGEN5}$ | Turn-on Slew Rate • 10% to 90% of end value • $V_{IN3_{MIN}} \leq V_{IN3} \leq 4.5$ mV, $I_{GEN5} = 0.0$ mA VGEN5[3:0] = 0000 to 0011 VGEN5[3:0] = 0100 to 0111 VGEN5[3:0] = 1000 to 1011 VGEN5[3:0] = 1100 to 1111 | – – – – | – – – – | 22.0 26.5 30.5 34.5 | mV/ μ s | |
| $GEN5_{ION}$ | Turn-on Time Enable to 90% of end value, $V_{IN3} = V_{IN3_{MIN}}$, 4.5 V $I_{GEN5} = 0.0$ mA | 60 | – | 500 | μ s | |
| $GEN5_{IOFF}$ | Turn-off Time Disable to 10% of initial value, $V_{IN3} = V_{IN3_{MIN}}$ $I_{GEN5} = 0.0$ mA | – | – | 10 | ms | |
| $GEN5_{OSHT}$ | Start-up Overshoot $V_{IN3} = V_{IN3_{MIN}}$, 4.5 V, $I_{GEN5} = 0.0$ mA | – | 1.0 | 2.0 | % | |
| $V_{GEN5LOTR}$ | Transient Load Response $V_{IN3} = V_{IN3_{MIN}}$, 4.5 V $I_{GEN5} = 10$ to 100 mA in 1.0 μ s Peak of overshoot or undershoot of VGEN5 with respect to final value. Refer to Figure 20 | – | – | 3.0 | % | |
| $V_{GEN5LITR}$ | Transient Line Response $I_{GEN5} = 75$ mA $V_{IN3_{INITIAL}} = 2.8$ V to $V_{IN3_{FINAL}} = 3.3$ V for VGEN5[3:0] = 0000 to 0111 $V_{IN3_{INITIAL}} = V_{GEN5} + 0.3$ V to $V_{IN3_{FINAL}} = V_{GEN5} + 0.8$ V for VGEN5[3:0] = 1000 to 1111 Refer to Figure 20 | – | 5.0 | 8.0 | mV | |

Notes

63. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
64. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. $V_{IN3_{MIN}}$ refers to the minimum allowed input voltage for a particular output voltage.

VGEN6

Table 91. VGEN6 electrical characteristics

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN6}[3:0] = 1111$, $I_{GEN6} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN6}[3:0] = 1111$, $I_{GEN6} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---------------|---|------------------------------------|--------------------------|------------|------|-------|
| V_{IN3} | Operating Input Voltage $1.8 \text{ V} \leq V_{GEN6NOM} \leq 2.5 \text{ V}$ $2.6 \text{ V} \leq V_{GEN6NOM} \leq 3.3 \text{ V}$ | 2.8 V_{GEN6NO} $M + 0.250$ | – – | 4.5 4.5 | V | (65) |
| $V_{GEN6NOM}$ | Nominal Output Voltage | – | Table 77 | – | V | |
| I_{GEN6} | Operating Load Current | 0.0 | – | 200 | mA | |

VGEN6 DC

| | | | | | | |
|---------------|--|------|------|-----|---------------|--|
| $V_{GEN6TOL}$ | Output Voltage Tolerance $V_{IN3MIN} < V_{IN3} < 4.5 \text{ V}$ $0.0 \text{ mA} < I_{GEN6} < 200 \text{ mA}$ $V_{GEN6}[3:0] = 0000$ to 1111 | -3.0 | – | 3.0 | % | |
| $V_{GEN6LOR}$ | Load Regulation $(V_{GEN6} \text{ at } I_{GEN6} = 200 \text{ mA}) - (V_{GEN6} \text{ at } I_{GEN6} = 0.0 \text{ mA})$ For any $V_{IN3MIN} < V_{IN3} < 4.5 \text{ V}$ | – | 0.10 | – | mV/mA | |
| $V_{GEN6LIR}$ | Line Regulation $(V_{GEN6} \text{ at } V_{IN3} = 4.5 \text{ V}) - (V_{GEN6} \text{ at } V_{IN3MIN})$ For any $0.0 \text{ mA} < I_{GEN6} < 200 \text{ mA}$ | – | 0.50 | – | mV/mA | |
| $I_{GEN6LIM}$ | Current Limit I_{GEN6} when VGEN6 is forced to $V_{GEN6NOM}/2$ | 232 | 333 | 475 | mA | |
| $I_{GEN6OCP}$ | Overcurrent Protection Threshold I_{GEN6} required to cause the SCP function to disable LDO when $REGSCPEN = 1$ | 220 | – | 475 | mA | |
| I_{GEN6Q} | Quiescent Current No load, Change in I_{VIN} and I_{VIN3} When VGEN6 enabled | – | 13 | – | μA | |

VGEN6 AC and transient

| | | | | | | |
|-----------------|--|------------------|----------------------|------------------------------|-------------------------|------|
| $PSRR_{VGEN6}$ | PSRR • $I_{GEN6} = 150 \text{ mA}$, 20 Hz to 20 kHz $V_{GEN6}[3:0] = 0000 - 1111$, $V_{IN3} = V_{IN3MIN} + 100 \text{ mV}$ $V_{GEN6}[3:0] = 0000 - 1111$, $V_{IN3} = V_{GEN6NOM} + 1.0 \text{ V}$ | 35 52 | 40 60 | – – | dB | (66) |
| $NOISE_{VGEN6}$ | Output Noise Density • $V_{IN3} = V_{IN3MIN}$, $I_{GEN6} = 150 \text{ mA}$ 100 Hz – <1.0 kHz 1.0 kHz – <10 kHz 10 kHz – 1.0 MHz | – – – | -114 -129 -135 | -102 -123 -130 | dBV/ $\sqrt{\text{Hz}}$ | |
| $SLWR_{VGEN6}$ | Turn-On Slew Rate • 10% to 90% of end value • $V_{IN3MIN} \leq V_{IN3} \leq 4.5 \text{ V}$, $I_{GEN6} = 0.0 \text{ mA}$ $V_{GEN6}[3:0] = 0000$ to 0011 $V_{GEN6}[3:0] = 0100$ to 0111 $V_{GEN6}[3:0] = 1000$ to 1011 $V_{GEN6}[3:0] = 1100$ to 1111 | – – – – | – – – – | 22.0 26.5 30.5 34.5 | mV/ μs | |
| $GEN6_{TON}$ | Turn-on Time Enable to 90% of end value, $V_{IN3} = V_{IN3MIN}$, 4.5 V $I_{GEN6} = 0.0 \text{ mA}$ | 60 | – | 500 | μs | |

Table 91. VGEN6 electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN6}[3:0] = 1111$, $I_{GEN6} = 10$ mA, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{IN3} = 3.6$ V, $V_{GEN6}[3:0] = 1111$, $I_{GEN6} = 10$ mA, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|--|------|------|------|------|-------|
| VGEN6 AC and transient (continued) | | | | | | |
| $GEN6_{TOFF}$ | Turn-off Time Disable to 10% of initial value, $V_{IN3} = VIN3_{MIN}$ $I_{GEN6} = 0.0$ mA | – | – | 10 | ms | |
| $GEN6_{OSHT}$ | Start-up Overshoot $V_{IN3} = VIN3_{MIN}$, 4.5 V, $I_{GEN6} = 0$ mA | – | 1.0 | 2.0 | % | |
| $V_{GEN6LOTR}$ | Transient Load Response $V_{IN3} = VIN3_{MIN}$, 4.5 V $I_{GEN6} = 20$ to 200 mA in 1.0 μ s Peak of overshoot or undershoot of VGEN6 with respect to final value. Refer to Figure 20 | – | – | 3.0 | % | |
| $V_{GEN6LITR}$ | Transient Line Response $I_{GEN6} = 150$ mA $VIN3_{INITIAL} = 2.8$ V to $VIN3_{FINAL} = 3.3$ V for $V_{GEN6}[3:0] = 0000$ to 0111 $VIN3_{INITIAL} = V_{GEN6} + 0.3$ V to $VIN3_{FINAL} = V_{GEN6} + 0.8$ V for $V_{GEN6}[3:0] = 1000$ to 1111 Refer to Figure 20 | – | 5.0 | 8.0 | mV | |

Notes

65. When the LDO Output voltage is set above 2.6 V the minimum allowed input voltage need to be at least the output voltage plus 0.25 V for proper regulation due to the dropout voltage generated through the internal LDO transistor.
66. The PSRR of the regulators is measured with the perturbing signal at the input of the regulator. The power management IC is supplied separately from the input of the regulator and does not contain the perturbed signal. During measurements, care must be taken not to operate in the dropout region of the regulator under test. $VIN3_{MIN}$ refers to the minimum allowed input voltage for a particular output voltage.

6.4.7 VSNVS LDO/switch

VSNVS powers the low power, SNVS/RTC domain on the processor. It derives its power from either VIN, or coin cell, and cannot be disabled. When powered by both, VIN takes precedence when above the appropriate comparator threshold. When powered by VIN, VSNVS is an LDO capable of supplying seven voltages: 3.0, 1.8, 1.5, 1.3, 1.2, 1.1, and 1.0 V. The bits VSNVSVOLT[2:0] in register VSNVS_CONTROL determine the output voltage. When powered by coin cell, VSNVS is an LDO capable of supplying 1.8, 1.5, 1.3, 1.2, 1.1, or 1.0 V as shown in [Table 92](#). If the 3.0 V option is chosen with the coin cell, VSNVS tracks the coin cell voltage by means of a switch, whose maximum resistance is 100 Ω . In this case, the VSNVS voltage is simply the coin cell voltage minus the voltage drop across the switch, which is 40 mV at a rated maximum load current of 400 μ A.

The default setting of the VSNVSVOLT[2:0] is 110, or 3.0 V, unless programmed otherwise in OTP. However, when the coin cell is applied for the very first time, VSNVS will output 1.0 V. Only when VIN is applied thereafter will VSNVS transition to its default, or programmed value if different. Upon subsequent removal of VIN, with the coin cell attached, VSNVS will change configuration from an LDO to a switch for the “110” setting, and will remain as an LDO for the other settings, continuing to output the same voltages as when VIN is applied, providing certain conditions are met as described in [Table 92](#).

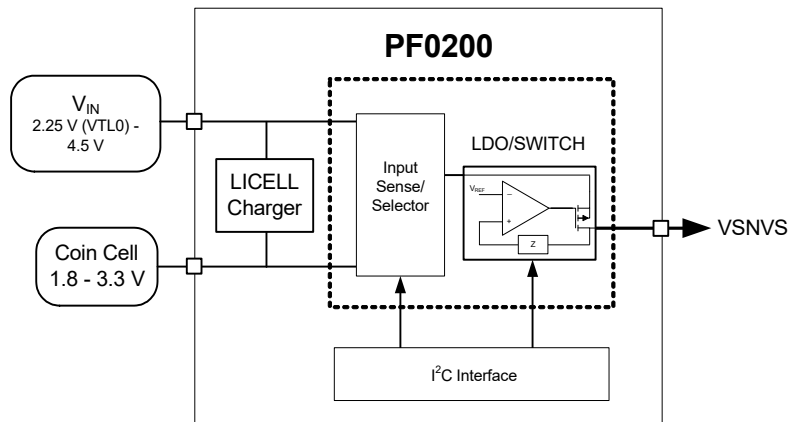


Figure 21. VSNVS supply switch architecture

Table 92 provides a summary of the VSNVS operation at different input voltage V_{IN} and with or without coin cell connected to the system.

Table 92. VSNVS modes of operation

| VSNVSVOLT[2:0] | V_{IN} | MODE |
|----------------|-------------|------------------|
| 110 | $> V_{TH1}$ | VIN LDO 3.0 V |
| 110 | $< V_{TL1}$ | Coin cell switch |
| 000 – 101 | $> V_{TH0}$ | VIN LDO |
| 000 – 101 | $< V_{TL0}$ | Coin cell LDO |

VSNVS control

The VSNVS output level is configured through the VSNVSVOLT[2:0]bits on VSNVSVCTL register as shown in table Table 93.

Table 93. Register VSNVSVCTL - ADDR 0x6B

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|---|
| VSNVSVOLT | 2:0 | R/W | 0x80 | Configures VSNVS output voltage. ⁽⁶⁷⁾ 000 = 1.0 V 001 = 1.1 V 010 = 1.2 V 011 = 1.3 V 100 = 1.5 V 101 = 1.8 V 110 = 3.0 V 111 = RSVD |
| UNUSED | 7:3 | – | 0x00 | UNUSED |

Notes

67. Only valid when a valid input voltage is present.

VSNVS external components

Table 94. VSNVS External Components

| Capacitor | Value (μ F) |
|-----------|------------------|
| VSNVS | 0.47 |

VSNVS specifications

Table 95. VSNVS electrical characteristics

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{SNVS} = 3.0$ V, $I_{SNVS} = 5.0$ μ A, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{SNVS} = 3.0$ V, $I_{SNVS} = 5.0$ μ A, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|----------------------|---|--------------------|------------------|----------------------|---------|-------|
| VSNVS | | | | | | |
| V_{INSNVS} | Operating Input Voltage Valid Coin Cell range Valid V_{IN} | 1.8 2.25 | – – | 3.3 4.5 | V | |
| I_{SNVS} | Operating Load Current $V_{INMIN} < V_{IN} < V_{INMAX}$ | 5.0 | – | 400 | μ A | |
| VSNVS DC, LDO | | | | | | |
| V_{SNVS} | Output Voltage <ul style="list-style-type: none"> $5.0 \mu\text{A} < I_{SNVS} < 400 \mu\text{A}$ (OFF) $3.20 \text{ V} < V_{IN} < 4.5 \text{ V}$, VSNVSVOLT[2:0] = 110 $V_{TL0}/V_{TH} < V_{IN} < 4.5 \text{ V}$, VSNVSVOLT[2:0] = [000] - [101] $5.0 \mu\text{A} < I_{SNVS} < 400 \mu\text{A}$ (ON) $3.20 \text{ V} < V_{IN} < 4.5 \text{ V}$, VSNVSVOLT[2:0] = 110 $UVDET < V_{IN} < 4.5 \text{ V}$, VSNVSVOLT[2:0] = [000] - [101] $5.0 \mu\text{A} < I_{SNVS} < 400 \mu\text{A}$ (Coin Cell mode) $2.84 \text{ V} < V_{COIN} < 3.3 \text{ V}$, VSNVSVOLT[2:0] = 110 $1.8 \text{ V} < V_{COIN} < 3.3 \text{ V}$, VSNVSVOLT[2:0] = [000] - [101] | -5.0% -8.0% | 3.0 1.0 - 1.8 | 7.0% 7.0% | V | |
| $V_{SNVSDROP}$ | Dropout Voltage $V_{IN} = V_{COIN} = 2.85 \text{ V}$, VSNVSVOLT[2:0] = 110, $I_{SNVS} = 400 \mu\text{A}$ | – | – | 50 | mV | |
| $I_{SNVSLIM}$ | Current Limit $V_{IN} > V_{TH1}$, VSNVSVOLT[2:0] = 110 $V_{IN} > V_{TH0}$, VSNVSVOLT[2:0] = 000 to 101 $V_{IN} < V_{TL0}$, VSNVSVOLT[2:0] = 000 to 101 | 1100 500 480 | – – – | 6750 6750 4500 | μ A | |
| V_{TH0} | V_{IN} Threshold (Coin Cell Powered to V_{IN} Powered) V_{IN} going high with valid coin cell VSNVSVOLT[2:0] = 000, 001, 010, 011, 100, 101 | 2.25 | 2.40 | 2.55 | V | |
| V_{TL0} | V_{IN} Threshold (V_{IN} Powered to Coin Cell Powered) V_{IN} going low with valid coin cell VSNVSVOLT[2:0] = 000, 001, 010, 011, 100, 101 | 2.20 | 2.35 | 2.50 | V | |
| V_{HYST1} | V_{IN} Threshold Hysteresis for V_{TH1} - V_{TL1} | 5.0 | – | – | mV | |
| V_{HYST0} | V_{IN} Threshold Hysteresis for V_{TH0} - V_{TL0} | 5.0 | – | – | mV | |
| $V_{SNVSCROSS}$ | Output Voltage During Crossover VSNVSVOLT[2:0] = 110 $V_{COIN} > 2.9 \text{ V}$ Switch to LDO: $V_{IN} > 2.825 \text{ V}$, $I_{SNVS} = 100 \mu\text{A}$ LDO to Switch: $V_{IN} < 3.05 \text{ V}$, $I_{SNVS} = 100 \mu\text{A}$ | 2.70 | – | – | V | (68) |

Notes

68. During crossover from V_{IN} to LICELL, the VSNVS output voltage may drop to 2.7 V before going to the LICELL voltage. Though this is outside the specified DC voltage level for the VDD_SNVS_IN pin of the i.MX 6, this momentary drop does not cause any malfunction. The i.MX 6's RTC continues to operate through the transition, and as a worst case it may switch to the internal RC oscillator for a few clock cycles before switching back to the external crystal oscillator.

Table 95. VSNVS electrical characteristics (continued)

All parameters are specified at Consumer $T_A = -40$ to 85 °C and Extended Industrial $T_A = -40$ to 105 °C, $V_{IN} = 3.6$ V, $V_{SNVS} = 3.0$ V, $I_{SNVS} = 5.0$ μ A, typical external component values, unless otherwise noted. Typical values are characterized at $V_{IN} = 3.6$ V, $V_{SNVS} = 3.0$ V, $I_{SNVS} = 5.0$ μ A, and 25 °C, unless otherwise noted.

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|-------------------------------|---|------|----------|------|------|-----------|
| VSNVS AC and transient | | | | | | |
| t_{ONSNVS} | Turn-on Time (Load capacitor, 0.47 μ F) $V_{IN} > UVDET$ to 90% of V_{SNVS} $V_{COIN} = 0.0$ V, $I_{SNVS} = 5.0$ μ A $VSNVSVOLT[2:0] = 000$ to 110 | – | – | 24 | ms | (70),(71) |
| $V_{SNVSOSH}$ | Start-up Overshoot $VSNVSVOLT[2:0] = 000$ to 110 $I_{SNVS} = 5.0$ μ A $dV_{IN}/dt = 50$ mV/ μ s | – | 40 | 70 | mV | |
| $V_{SNVSLITR}$ | Transient Line Response $I_{SNVS} = 75\%$ of $ISNVS_{MAX}$ 3.2 V $< V_{IN} < 4.5$ V, $VSNVSVOLT[2:0] = 110$ 2.45 V $< V_{IN} < 4.5$ V, $VSNVSVOLT[2:0] = [000] - [101]$ | – | 32 22 | – | mV | |
| $V_{SNVSLOTR}$ | Transient Load Response $VSNVSVOLT[2:0] = 110$ 3.1 V ($UVDETL$) $< V_{IN} \leq 4.5$ V $I_{SNVS} = 75$ to 750 μ A $VSNVSVOLT[2:0] = 000$ to 101 2.45 V $< V_{IN} \leq 4.5$ V $V_{TL0} > V_{IN}$, 1.8 V $\leq V_{COIN} \leq 3.3$ V $I_{SNVS} = 40$ to 400 μ A Refer to Figure 20 | 2.8 | – | – | V | |
| | | – | 1.0 | 2.0 | % | |

VSNVS DC, switch

| | | | | | | |
|----------------|---|-------|------|------|----------|------|
| V_{INSNVS} | Operating Input voltage Valid Coin Cell range | 1.8 | – | 3.3 | V | |
| I_{SNVS} | Operating Load Current | 5.0 | – | 400 | μ A | |
| $R_{DSONSNVS}$ | Internal Switch $R_{DS(on)}$ $V_{COIN} = 2.6$ V | – | – | 100 | Ω | |
| V_{TL1} | V_{IN} Threshold (V_{IN} Powered to Coin Cell Powered) $VSNVSVOLT[2:0] = 110$ | 2.725 | 2.90 | 3.00 | V | (72) |
| V_{TH1} | V_{IN} Threshold (Coin Cell Powered to V_{IN} Powered) $VSNVSVOLT[2:0] = 110$ | 2.775 | 2.95 | 3.1 | V | |

Notes

69. For 1.8 V I_{SNVS} limited to 100 μ A for $V_{COIN} < 2.1$ V
70. The start-up of VSNVS is not monotonic. It first rises to 1.0 V and then settles to its programmed value within the specified t_{R1} time.
71. From coin cell insertion to $V_{SNVS} = 1.0$ V, the delay time is typically 400 ms.
72. During crossover from V_{IN} to LICELL, the VSNVS output voltage may drop to 2.7 V before going to the LICELL voltage. Though this is outside the specified DC voltage level for the VDD_SNVS_IN pin of the i.MX 6, this momentary drop does not cause any malfunction. The i.MX 6's RTC continues to operate through the transition, and as a worst case it may switch to the internal RC oscillator for a few clock cycles before switching back to the external crystal oscillator.

6.4.7.1 Coin cell battery backup

The LICELL pin provides for a connection of a coin cell backup battery or a “super” capacitor. If the voltage at V_{IN} goes below the V_{IN} threshold (V_{TL1} and V_{TL0}), contact-bounced, or removed, the coin cell maintained logic will be powered by the voltage applied to LICELL. The supply for internal logic and the VSNVS rail will switch over to the LICELL pin when V_{IN} goes below V_{TL1} or V_{TL0} , even in the absence of a voltage at the LICELL pin, resulting in clearing of memory and turning off of VSNVS. When system operation below V_{TL1} is required, for systems not utilizing a coin cell, connect the LICELL pin to any system voltage between 1.8 and 3.0 V. A small capacitor should be placed from LICELL to ground under all circumstances.

Coin cell charger control

The coin cell charger circuit will function as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit while the coin cell voltage is programmable through the VCOIN[2:0] bits on register COINCTL on [Table 97](#). The coin cell charger voltage is programmable. In the ON state, the charger current is fixed at ICOINH1. In Sleep and Standby modes, the charger current is reduced to a typical 10 μ A. In the OFF state, coin cell charging is not available as the main battery could be depleted unnecessarily. The coin cell charging will be stopped when V_{IN} is below UVDET.

Table 96. Coin cell charger voltage

| VCOIN[2:0] | V_{COIN} (V) ⁽⁷³⁾ |
|------------|--------------------------------|
| 000 | 2.50 |
| 001 | 2.70 |
| 010 | 2.80 |
| 011 | 2.90 |
| 100 | 3.00 |
| 101 | 3.10 |
| 110 | 3.20 |
| 111 | 3.30 |

Notes

73. Coin cell voltages selected based on the type of LICELL used on the system.

Table 97. Register COINCTL - ADDR 0x1A

| Name | Bit # | R/W | Default | Description |
|----------|-------|-----|---------|---|
| VCOIN | 2:0 | R/W | 0x00 | Coin cell charger output voltage selection. See Table 96 for all options selectable through these bits. |
| COINCHEN | 3 | R/W | 0x00 | Enable or disable the Coin cell charger |
| UNUSED | 7:4 | – | 0x00 | UNUSED |

External components

Table 98. Coin cell charger external components

| Component | Value | Units |
|-------------------------|-------|-------|
| LICELL Bypass Capacitor | 100 | nF |

Coin cell specifications

Table 99. Coin cell charger specifications

| Parameter | Typ | Unit |
|---|-----|---------|
| Voltage Accuracy | 100 | mV |
| Coin Cell Charge Current in On mode ICOINH1 | 60 | μ A |
| Current Accuracy | 30 | % |

6.5 Control interface I²C block description

The PF0200 contains an I²C interface port which allows access by a processor, or any I²C master, to the register set. Via these registers the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

The SCL and SDA lines should be routed away from noisy signals and planes to minimize noise pick up. To prevent reflections in the SCL and SDA traces from creating false pulses, the rise and fall times of the SCL and SDA signals must be greater than 20 ns. This can be accomplished by reducing the drive strength of the I²C master via software. The i.MX6 I2C driver defaults to a 40 ohm drive strength. It is recommended to use a drive strength of 80 ohm or higher to increase the edge times. Alternatively, this can be accomplished by using small capacitors from SCL and SDA to ground. For example, use 5.1 pF capacitors from SCL and SDA to ground for bus pull-up resistors of 4.8 kohm. PWRON must be logic high for I²C communication to work robustly.

6.5.1 I²C device ID

I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. To allow flexibility in addressing for bus conflict avoidance, fuse programmability is provided to allow configuration for the lower 3 address LSB(s). Refer to [One time programmability \(OTP\)](#) for more details. This product supports 7-bit addressing only; support is not provided for 10-bit or general call addressing. Note, when the TBB bits for the I²C slave address are written, the next access to the chip, must then use the new slave address; these bits take affect right away.

6.5.2 I²C operation

The I²C mode of the interface is implemented generally following the Fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for General Call addressing.) Timing diagrams, electrical specifications, and further details can be found in the I²C specification, which is available for download at:

http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte will be sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to and from the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device will respond to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

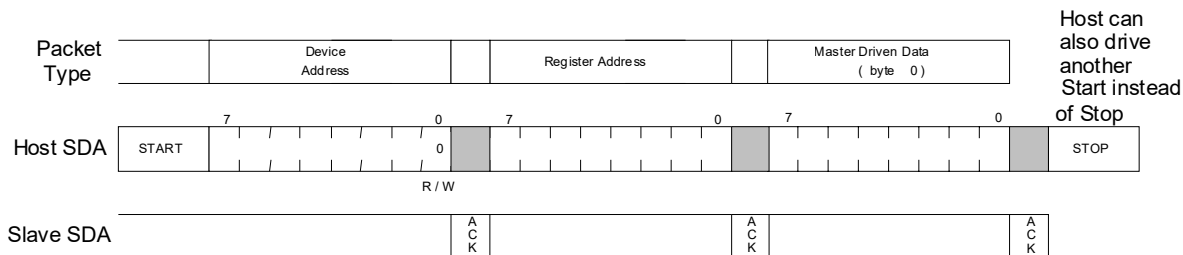


Figure 22. I²C write example

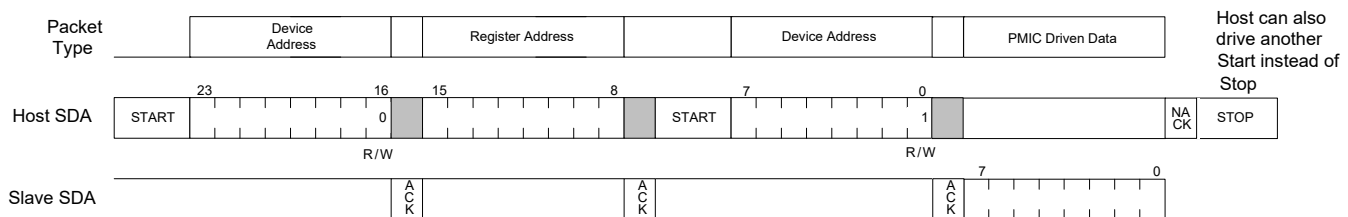


Figure 23. I²C read example

6.5.3 Interrupt handling

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INTB pin low.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing a “1” to the appropriate bit in the Interrupt Status register; this will also cause the INTB pin to go high. If there are multiple interrupt bits set the INTB pin will remain low until all are either masked or cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin will remain low.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin will not go low. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin will go low after unmasking.

The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable.

Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the INT summary [Table 100](#). Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

6.5.4 Interrupt bit summary

[Table 100](#) summarizes all interrupt, mask, and sense bits associated with INTB control. For more detailed behavioral descriptions, refer to the related chapters.

Table 100. Interrupt, mask and sense bits

| Interrupt | Mask | Sense | Purpose | Trigger | Debounce time (ms) |
|-------------|-------------|-------------|---|---------|-----------------------|
| LOWVINI | LOWVINM | LOWVINS | Low Input Voltage Detect Sense is 1 if below 2.80 V threshold | H to L | 3.9 ⁽⁷⁴⁾ |
| PWRONI | PWRONM | PWRONS | Power on button event | H to L | 31.25 ⁽⁷⁴⁾ |
| | | | Sense is 1 if PWRON is high. | L to H | 31.25 |
| THERM110 | THERM110M | THERM110S | Thermal 110 °C threshold Sense is 1 if above threshold | Dual | 3.9 |
| THERM120 | THERM120M | THERM120S | Thermal 120 °C threshold Sense is 1 if above threshold | Dual | 3.9 |
| THERM125 | THERM125M | THERM125S | Thermal 125 °C threshold Sense is 1 if above threshold | Dual | 3.9 |
| THERM130 | THERM130M | THERM130S | Thermal 130 °C threshold Sense is 1 if above threshold | Dual | 3.9 |
| SW1AFAULTI | SW1AFAULTM | SW1AFAULTS | Regulator 1A overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| SW1BFAULTI | SW1BFAULTM | SW1BFAULTS | Regulator 1B overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| SW2FAULTI | SW2FAULTM | SW2FAULTS | Regulator 2 overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| SW3AFAULTI | SW3AFAULTM | SW3AFAULTS | Regulator 3A overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| SW3BFAULTI | SW3BFAULTM | SW3BFAULTS | Regulator 3B overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| SWBSTFAULTI | SWBSTFAULTM | SWBSTFAULTS | SWBST overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| VGEN1FAULTI | VGEN1FAULTM | VGEN1FAULTS | VGEN1 overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |

Table 100. Interrupt, mask and sense bits (continued)

| Interrupt | Mask | Sense | Purpose | Trigger | Debounce time (ms) |
|-------------|-------------|-------------|--|---------|--------------------|
| VGEN2FAULTI | VGEN2FAULTM | VGEN2FAULTS | VGEN2 overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| VGEN3FAULTI | VGEN3FAULTM | VGEN3FAULTS | VGEN3 overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| VGEN4FAULTI | VGEN4FAULTM | VGEN4FAULTS | VGEN4 overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| VGEN5FAULTI | VGEN5FAULTM | VGEN1FAULTS | VGEN5 overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| VGEN6FAULTI | VGEN6FAULTM | VGEN6FAULTS | VGEN6 overcurrent limit Sense is 1 if above current limit | L to H | 8.0 |
| OTP_ECCI | OTP_ECCM | OTP_ECCS | 1 or 2 bit error detected in OTP registers Sense is 1 if error detected | L to H | 8.0 |

Notes

74. Debounce timing for the falling edge can be extended with PWRONDBNC[1:0].

A full description of all interrupt, mask, and sense registers is provided in [Tables 101](#) to [112](#).

Table 101. Register INTSTAT0 - ADDR 0x05

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-------|---------|------------------------------|
| PWRONI | 0 | R/W1C | 0 | Power on interrupt bit |
| LOWVINI | 1 | R/W1C | 0 | Low-voltage interrupt bit |
| THERM110I | 2 | R/W1C | 0 | 110 °C Thermal interrupt bit |
| THERM120I | 3 | R/W1C | 0 | 120 °C Thermal interrupt bit |
| THERM125I | 4 | R/W1C | 0 | 125 °C Thermal interrupt bit |
| THERM130I | 5 | R/W1C | 0 | 130 °C Thermal interrupt bit |
| UNUSED | 7:6 | – | 00 | Unused |

Table 102. Register INTMASK0 - ADDR 0x06

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-------|---------|-----------------------------------|
| PWRONM | 0 | R/W1C | 1 | Power on interrupt mask bit |
| LOWVINM | 1 | R/W1C | 1 | Low-voltage interrupt mask bit |
| THERM110M | 2 | R/W1C | 1 | 110 °C Thermal interrupt mask bit |
| THERM120M | 3 | R/W1C | 1 | 120 °C Thermal interrupt mask bit |
| THERM125M | 4 | R/W1C | 1 | 125 °C Thermal interrupt mask bit |
| THERM130M | 5 | R/W1C | 1 | 130 °C Thermal interrupt mask bit |
| UNUSED | 7:6 | – | 00 | Unused |

Table 103. Register INTSENSE0 - ADDR 0x07

| Name | Bit # | R/W | Default | Description |
|-----------|-------|-----|---------|---|
| PWRONS | 0 | R | 0 | Power on sense bit 0 = PWRON low 1 = PWRON high |
| LOWVINS | 1 | R | 0 | Low-voltage sense bit 0 = VIN > 2.8 V 1 = VIN ≤ 2.8 V |
| THERM110S | 2 | R | 0 | 110 °C Thermal sense bit 0 = Below threshold 1 = Above threshold |
| THERM120S | 3 | R | 0 | 120 °C Thermal sense bit 0 = Below threshold 1 = Above threshold |
| THERM125S | 4 | R | 0 | 125 °C Thermal sense bit 0 = Below threshold 1 = Above threshold |
| THERM130S | 5 | R | 0 | 130 °C Thermal sense bit 0 = Below threshold 1 = Above threshold |
| UNUSED | 6 | – | 0 | Unused |
| VDDOTPS | 7 | R | 00 | Additional VDDOTP voltage sense pin 0 = VDDOTP grounded 1 = VDDOTP to VCOREDIG or greater |

Table 104. Register INTSTAT1 - ADDR 0x08

| Name | Bit # | R/W | Default | Description |
|------------|-------|-------|---------|--------------------------------|
| SW1AFAULTI | 0 | R/W1C | 0 | SW1A Overcurrent interrupt bit |
| SW1BFAULTI | 1 | R/W1C | 0 | SW1B Overcurrent interrupt bit |
| RSVD | 2 | R/W1C | 0 | Reserved |
| SW2FAULTI | 3 | R/W1C | 0 | SW2 Overcurrent interrupt bit |
| SW3AFAULTI | 4 | R/W1C | 0 | SW3A Overcurrent interrupt bit |
| SW3BFAULTI | 5 | R/W1C | 0 | SW3B Overcurrent interrupt bit |
| RSVD | 6 | R/W1C | 0 | Reserved |
| UNUSED | 7 | – | 0 | Unused |

Table 105. Register INTMASK1 - ADDR 0x09

| Name | Bit # | R/W | Default | Description |
|------------|-------|-----|---------|-------------------------------------|
| SW1AFAULTM | 0 | R/W | 1 | SW1A Overcurrent interrupt mask bit |
| SW1BFAULTM | 1 | R/W | 1 | SW1B Overcurrent interrupt mask bit |
| RSVD | 2 | R/W | 1 | Reserved |
| SW2FAULTM | 3 | R/W | 1 | SW2 Overcurrent interrupt mask bit |
| SW3AFAULTM | 4 | R/W | 1 | SW3A Overcurrent interrupt mask bit |
| SW3BFAULTM | 5 | R/W | 1 | SW3B Overcurrent interrupt mask bit |
| RSVD | 6 | R/W | 1 | Reserved |
| UNUSED | 7 | – | 0 | Unused |

Table 106. Register INTSENSE1 - ADDR 0x0A

| Name | Bit # | R/W | Default | Description |
|------------|-------|-----|---------|---|
| SW1AFAULTS | 0 | R | 0 | SW1A Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| SW1BFAULTS | 1 | R | 0 | SW1B Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| RSVD | 2 | R | 0 | Reserved |
| SW2FAULTS | 3 | R | 0 | SW2 Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| SW3AFAULTS | 4 | R | 0 | SW3A Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| SW3BFAULTS | 5 | R | 0 | SW3B Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| RSVD | 6 | R | 0 | Reserved |
| UNUSED | 7 | – | 0 | Unused |

Table 107. Register INTSTAT3 - ADDR 0x0E

| Name | Bit # | R/W | Default | Description |
|-------------|-------|-------|---------|---------------------------------------|
| SWBSTFAULTI | 0 | R/W1C | 0 | SWBST overcurrent limit interrupt bit |
| UNUSED | 6:1 | – | 0x00 | Unused |
| OTP_ECCI | 7 | R/W1C | 0 | OTP error interrupt bit |

Table 108. Register INTMASK3 - ADDR 0x0F

| Name | Bit # | R/W | Default | Description |
|-------------|-------|-----|---------|--|
| SWBSTFAULTM | 0 | R/W | 1 | SWBST overcurrent limit interrupt mask bit |
| UNUSED | 6:1 | – | 0x00 | Unused |
| OTP_ECCM | 7 | R/W | 1 | OTP error interrupt mask bit |

Table 109. Register INTSENSE3 - ADDR 0x10

| Name | Bit # | R/W | Default | Description |
|-------------|-------|-----|---------|--|
| SWBSTFAULTS | 0 | R | 0 | SWBST overcurrent limit sense bit 0 = Normal operation 1 = Above current limit |
| UNUSED | 6:1 | – | 0x00 | Unused |
| OTP_ECCS | 7 | R | 0 | OTP error sense bit 0 = No error detected 1 = OTP error detected |

Table 110. Register INTSTAT4 - ADDR 0x11

| Name | Bit # | R/W | Default | Description |
|-------------|-------|-------|---------|---------------------------------|
| VGEN1FAULTI | 0 | R/W1C | 0 | VGEN1 Overcurrent interrupt bit |
| VGEN2FAULTI | 1 | R/W1C | 0 | VGEN2 Overcurrent interrupt bit |
| VGEN3FAULTI | 2 | R/W1C | 0 | VGEN3 Overcurrent interrupt bit |
| VGEN4FAULTI | 3 | R/W1C | 0 | VGEN4 Overcurrent interrupt bit |
| VGEN5FAULTI | 4 | R/W1C | 0 | VGEN5 Overcurrent interrupt bit |
| VGEN6FAULTI | 5 | R/W1C | 0 | VGEN6 Overcurrent interrupt bit |
| UNUSED | 7:6 | – | 00 | Unused |

Table 111. Register INTMASK4 - ADDR 0x12

| Name | Bit # | R/W | Default | Description |
|-------------|-------|-----|---------|--------------------------------------|
| VGEN1FAULTM | 0 | R/W | 1 | VGEN1 Overcurrent interrupt mask bit |
| VGEN2FAULTM | 1 | R/W | 1 | VGEN2 Overcurrent interrupt mask bit |
| VGEN3FAULTM | 2 | R/W | 1 | VGEN3 Overcurrent interrupt mask bit |
| VGEN4FAULTM | 3 | R/W | 1 | VGEN4 Overcurrent interrupt mask bit |
| VGEN5FAULTM | 4 | R/W | 1 | VGEN5 Overcurrent interrupt mask bit |
| VGEN6FAULTM | 5 | R/W | 1 | VGEN6 Overcurrent interrupt mask bit |
| UNUSED | 7:6 | – | 00 | Unused |

Table 112. Register INTSENSE4 - ADDR 0x13

| Name | Bit # | R/W | Default | Description |
|-------------|-------|-----|---------|--|
| VGEN1FAULTS | 0 | R | 0 | VGEN1 Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| VGEN2FAULTS | 1 | R | 0 | VGEN2 Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| VGEN3FAULTS | 2 | R | 0 | VGEN3 Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| VGEN4FAULTS | 3 | R | 0 | VGEN4 Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| VGEN5FAULTS | 4 | R | 0 | VGEN5 Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| VGEN6FAULTS | 5 | R | 0 | VGEN6 Overcurrent sense bit 0 = Normal operation 1 = Above current limit |
| UNUSED | 7:6 | – | 00 | Unused |

6.5.5 Specific registers

6.5.5.1 IC and Version Identification

The IC and other version details can be read via identification bits. These are hard-wired on chip and described in [Tables 113](#) to [115](#).

Table 113. Register DEVICEID - ADDR 0x00

| Name | Bit # | R/W | Default | Description |
|----------|-------|-----|---------|-------------------------------|
| DEVICEID | 3:0 | R | 0x01 | Die version. 0001 = PF0200 |
| UNUSED | 7:4 | – | 0x01 | Unused |

Table 114. Register SILICON REV- ADDR 0x03

| Name | Bit # | R/W | Default | Description |
|---|-------|-----|---------|--|
| METAL_LAYER_REV | 3:0 | R | XX | Represents the metal mask revision Pass 0.0 = 0000 . . Pass 0.15 = 1111 |
| FULL_LAYER_REV | 7:4 | R | XX | Represents the full mask revision Pass 1.0 = 0001 . . Pass 15.0 = 1111 |
| Notes 75. Default value depends on the silicon revision. | | | | |

Table 115. Register FABID - ADDR 0x04

| Name | Bit # | R/W | Default | Description |
|--------|-------|-----|---------|--|
| FIN | 1:0 | R | 0x00 | Allows for characterizing different options within the same reticule |
| FAB | 3:2 | R | 0x00 | Represents the wafer manufacturing facility |
| Unused | 7:0 | R | 0x00 | Unused |

6.5.5.2 Embedded memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[7:0], MEMB[7:0], MEMC[7:0], and MEMD[7:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced. The contents of the embedded memory are reset by COINPORB. The banks can be used for any system need for bit retention with coin cell backup.

Table 116. Register MEMA ADDR 0x1C

| Name | Bit # | R/W | Default | Description |
|------|-------|-----|---------|---------------|
| MEMA | 7:0 | R/W | 0 | Memory bank A |

Table 117. Register MEMB ADDR 0x1D

| Name | Bit # | R/W | Default | Description |
|------|-------|-----|---------|---------------|
| MEMB | 7:0 | R/W | 0 | Memory bank B |

Table 118. Register MEMC ADDR 0x1E

| Name | Bit # | R/W | Default | Description |
|------|-------|-----|---------|---------------|
| MEMC | 7:0 | R/W | 0 | Memory bank C |

Table 119. Register MEMD ADDR 0x1F

| Name | Bit # | R/W | Default | Description |
|------|-------|-----|---------|---------------|
| MEMD | 7:0 | R/W | 0 | Memory bank D |

6.5.6 Register bitmap

The register map is comprised of thirty-two pages, and its address and data fields are each eight bits wide. Only the first two pages can be accessed. On each page, registers 0 to 0x7F are referred to as *'functional'*, and registers 0x80 to 0xFF as *'extended'*. On each page, the functional registers are the same, but the extended registers are different. To access registers on [Extended page 1](#), one must first write 0x01 to the page register at address 0x7F, and to access registers [Extended page 2](#), one must first write 0x02 to the page register at address 0x7F. To access the [Functional page](#) from one of the extended pages, no write to the page register is necessary.

Registers that are missing in the sequence are reserved; reading from them will return a value 0x00, and writing to them will have no effect.

The contents of all registers are given in the tables defined in this chapter; each table is structure as follows:

Name: Name of the bit.

Bit #: The bit location in the register (7-0)

R/W: Read / Write access and control

- R is read-only access
- R/W is read and write access
- RW1C is read and write access with write 1 to clear

Reset: Reset signals are color coded based on the following legend.

| |
|--|
| Bits reset by SC and VCOREDIG_PORB |
| Bits reset by PWRON or loaded default or OTP configuration |
| Bits reset by DIGRESETB |
| Bits reset by PORB or RESETBMCU |
| Bits reset by VCOREDIG_PORB |
| Bits reset by POR or OFFB |

Default: The value after reset, as noted in the Default column of the memory map.

- Fixed defaults are explicitly declared as 0 or 1.
- "X" corresponds to Read / Write bits that are initialized at start-up, based on the OTP fuse settings or default if VDDOTP = 1.5 V. Bits are subsequently I²C modifiable, when their reset has been released. "X" may also refer to bits that may have other dependencies. For example, some bits may depend on the version of the IC, or a value from an analog block, for instance the sense bits for the interrupts.

6.5.6.1 Register map

Table 120. Functional page

| Add | Register name | R/W | Default | BITS[7:0] | | | | | | | |
|-----|---------------|------|--------------|---------------------|------|--------------|--------------|----------------------|--------------|--------------|--------------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00 | DeviceID | R | 8'b0001_0001 | - | - | - | - | DEVICE ID [3:0] | | | |
| | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 03 | SILICONREVID | R | 8'b0001_0000 | FULL_LAYER_REV[3:0] | | | | METAL_LAYER_REV[3:0] | | | |
| | | | | X | X | X | X | X | X | X | X |
| 04 | FABID | R | 8'b0000_0000 | - | - | - | - | FAB[1:0] | | FIN[1:0] | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05 | INTSTAT0 | RW1C | 8'b0000_0000 | - | - | THERM130I | THERM125I | THERM120I | THERM110I | LOWVINI | PWRONI |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06 | INTMASK0 | R/W | 8'b0011_1111 | - | - | THERM130M | THERM125M | THERM120M | THERM110M | LOWVINM | PWRONM |
| | | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 07 | INTSENSE0 | R | 8'b00xx_xxxx | VDDOTPS | RSVD | THERM130S | THERM125S | THERM120S | THERM110S | LOWVINS | PWRONS |
| | | | | 0 | 0 | x | x | x | x | x | x |
| 08 | INTSTAT1 | RW1C | 8'b0000_0000 | - | RSVD | SW3BFAULTI | SW3AFAULTI | SW2FAULTI | RSVD | SW1BFAULTI | SW1AFAULTI |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09 | INTMASK1 | R/W | 8'b0111_1111 | - | RSVD | SW3BFAULTM | SW3AFAULTM | SW2FAULTM | RSVD | SW1BFAULTM | SW1AFAULTM |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0A | INTSENSE1 | R | 8'b0xxx_xxxx | - | RSVD | SW3BFAULTS | SW3AFAULTS | SW2FAULTS | RSVD | SW1BFAULTS | SW1AFAULTS |
| | | | | 0 | x | x | x | x | x | x | x |
| 0E | INTSTAT3 | RW1C | 8'b0000_0000 | OTP_ECCI | - | - | - | - | - | - | SWBSTFAULTI |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0F | INTMASK3 | R/W | 8'b1000_0001 | OTP_ECCM | - | - | - | - | - | - | SWBSTFAULTM |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 10 | INTSENSE3 | R | 8'b0000_000x | OTP_ECCS | - | - | - | - | - | - | SWBSTFAULTS |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x |
| 11 | INTSTAT4 | RW1C | 8'b0000_0000 | - | - | VGEN6FAULTI | VGEN5FAULTI | VGEN4FAULTI | VGEN3FAULTI | VGEN2FAULTI | VGEN1FAULTI |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | INTMASK4 | R/W | 8'b0011_1111 | - | - | VGEN6 FAULTM | VGEN5 FAULTM | VGEN4 FAULTM | VGEN3 FAULTM | VGEN2 FAULTM | VGEN1 FAULTM |
| | | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 13 | INTSENSE4 | R | 8'b00xx_xxxx | - | - | VGEN6 FAULTS | VGEN5 FAULTS | VGEN4 FAULTS | VGEN3 FAULTS | VGEN2 FAULTS | VGEN1 FAULTS |
| | | | | 0 | 0 | x | x | x | x | x | x |
| 1A | COINCTL | R/W | 8'b0000_0000 | - | - | - | - | COINCHEN | VCOIN[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 120. Functional page (continued)

| Add | Register name | R/W | Default | BITS[7:0] | | | | | | | |
|-----|---------------|-------|--------------|--------------------|---------------|-----------------|---|-----------------|---|------------|-----------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1B | PWRCTL | R/W | 8'b0001_0000 | REGSCPEN | STANDBYINV | STBYDLY[1:0] | | PWRONBDBNC[1:0] | | PWRONRSTEN | RESTARTEN |
| | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1C | MEMA | R/W | 8'b0000_0000 | MEMA[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1D | MEMB | R/W | 8'b0000_0000 | MEMB[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1E | MEMC | R/W | 8'b0000_0000 | MEMC[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1F | MEMD | R/W | 8'b0000_0000 | MEMD[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 20 | SW1ABVOLT | R/W/M | 8'b00xx_xxxx | – | – | SW1AB[5:0] | | | | | |
| | | | | 0 | 0 | x | x | x | x | x | x |
| 21 | SW1ABSTBY | R/W | 8'b00xx_xxxx | – | – | SW1ABSTBY[5:0] | | | | | |
| | | | | 0 | 0 | x | x | x | x | x | x |
| 22 | SW1ABOFF | R/W | 8'b00xx_xxxx | – | – | SW1ABOFF[5:0] | | | | | |
| | | | | 0 | 0 | x | x | x | x | x | x |
| 23 | SW1ABMODE | R/W | 8'b0000_1000 | – | – | SW1ABOMODE | – | SW1ABMODE[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 24 | SW1ABCONF | R/W | 8'bx00_xx00 | SW1ABDVSSPEED[1:0] | | SW1BAPHASE[1:0] | | SW1ABFREQ[1:0] | | – | SW1ABILIM |
| | | | | x | x | 0 | 0 | x | x | 0 | 0 |
| 35 | SW2VOLT | R/W | 8'b0xxx_xxxx | – | SW2[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 36 | SW2STBY | R/W | 8'b0xxx_xxxx | – | SW2STBY[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 37 | SW2OFF | R/W | 8'b0xxx_xxxx | – | SW2OFF[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 38 | SW2MODE | R/W | 8'b0000_1000 | – | – | SW2OMODE | – | SW2MODE[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 39 | SW2CONF | R/W | 8'bx01_xx00 | SW2DVSSPEED[1:0] | | SW2PHASE[1:0] | | SW2FREQ[1:0] | | – | SW2ILIM |
| | | | | x | x | 0 | 1 | x | x | 0 | 0 |
| 3C | SW3AVOLT | R/W | 8'b0xxx_xxxx | – | SW3A[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 3D | SW3ASTBY | R/W | 8'b0xxx_xxxx | – | SW3ASTBY[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 3E | SW3AOFF | R/W | 8'b0xxx_xxxx | – | SW3AOFF[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |

Table 120. Functional page (continued)

| Add | Register name | R/W | Default | BITS[7:0] | | | | | | | |
|-----|---------------|-----|--------------|-------------------|---------------------|----------------|-----------|-----------------|----------------|-----------------|----------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 3F | SW3AMODE | R/W | 8'b0000_1000 | | | SW3AOMODE | – | SW3AMODE[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 40 | SW3ACONF | R/W | 8'bxx10_xxx0 | SW3ADVSSPEED[1:0] | | SW3APHASE[1:0] | | SW3AFREQ[1:0] | | – | SW3AILIM |
| | | | | x | x | 1 | 0 | x | x | 0 | 0 |
| 43 | SW3BVOLT | R/W | 8'b0xxx_xxxx | – | SW3B[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 44 | SW3BSTBY | R/W | 8'b0xxx_xxxx | – | SW3BSTBY[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 45 | SW3BOFF | R/W | 8'b0xxx_xxxx | – | SW3BOFF[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| 46 | SW3BMODE | R/W | 8'b0000_1000 | – | – | SW3BOMODE | – | SW3BMODE[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 47 | SW3BCONF | R/W | 8'bxx10_xxx0 | SW3BDVSSPEED[1:0] | | SW3BPHASE[1:0] | | SW3BFREQ[1:0] | | – | SW3BILIM |
| | | | | x | x | 1 | 0 | x | x | 0 | 0 |
| 66 | SWBSTCTL | R/W | 8'b0xx0_10xx | – | SWBST1STBYMODE[1:0] | | – | SWBST1MODE[1:0] | | SWBST1VOLT[1:0] | |
| | | | | 0 | x | x | 0 | 1 | 0 | x | x |
| 6A | VREFDDRCTL | R/W | 8'b000x_0000 | – | – | – | VREFDDREN | – | – | – | – |
| | | | | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 |
| 6B | VSNVSVCTL | R/W | 8'b0000_0xxx | – | – | – | – | – | VSNVSVOLT[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | x |
| 6C | VGEN1CTL | R/W | 8'b000x_xxxx | – | VGEN1LPWR | VGEN1STBY | VGEN1EN | VGEN1[3:0] | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| 6D | VGEN2CTL | R/W | 8'b000x_xxxx | – | VGEN2LPWR | VGEN2STBY | VGEN2EN | VGEN2[3:0] | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| 6E | VGEN3CTL | R/W | 8'b000x_xxxx | – | VGEN3LPWR | VGEN3STBY | VGEN3EN | VGEN3[3:0] | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| 6F | VGEN4CTL | R/W | 8'b000x_xxxx | – | VGEN4LPWR | VGEN4STBY | VGEN4EN | VGEN4[3:0] | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| 70 | VGEN5CTL | R/W | 8'b000x_xxxx | – | VGEN5LPWR | VGEN5STBY | VGEN5EN | VGEN5[3:0] | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| 71 | VGEN6CTL | R/W | 8'b000x_xxxx | – | VGEN6LPWR | VGEN6STBY | VGEN6EN | VGEN6[3:0] | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| 7F | Page Register | R/W | 8'b0000_0000 | – | – | – | PAGE[4:0] | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 121. Extended page 1

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---------|------------------|------|---------------|-----------|----------------|-----------------|----------------|-----------------|------------|-----------------|------------------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 80 | OTP FUSE READ EN | R/W | 8'b000x_xxxx0 | - | - | - | - | - | - | - | OTP FUSE READ EN |
| | | | | 0 | 0 | 0 | x | x | x | x | 0 |
| 84 | OTP LOAD MASK | R/W | 8'b0000_0000 | START | RL PWBRTN | FORCE PWRCTL | RL PWRCTL | RL OTP | RL OTP ECC | RL OTP FUSE | RL TRIM FUSE |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8A | OTP ECC SE1 | R | 8'bxxx0_0000 | - | - | - | ECC5_SE | ECC4_SE | ECC3_SE | ECC2_SE | ECC1_SE |
| | | | | x | x | x | 0 | 0 | 0 | 0 | 0 |
| 8B | OTP ECC SE2 | R | 8'bxxx0_0000 | - | - | - | ECC10_SE | ECC9_SE | ECC8_SE | ECC7_SE | ECC6_SE |
| | | | | x | x | x | 0 | 0 | 0 | 0 | 0 |
| 8C | OTP ECC DE1 | R | 8'bxxx0_0000 | - | - | - | ECC5_DE | ECC4_DE | ECC3_DE | ECC2_DE | ECC1_DE |
| | | | | x | x | x | 0 | 0 | 0 | 0 | 0 |
| 8D | OTP ECC DE2 | R | 8'bxxx0_0000 | - | - | - | ECC10_DE | ECC9_DE | ECC8_DE | ECC7_DE | ECC6_DE |
| | | | | x | x | x | 0 | 0 | 0 | 0 | 0 |
| A0 | OTP SW1AB VOLT | R/W | 8'b00xx_xxxx | - | - | SW1AB_VOLT[5:0] | | | | | |
| | | | | 0 | 0 | x | x | x | x | x | x |
| A1 | OTP SW1AB SEQ | R/W | 8'b000x_xxXx | - | - | - | SW1AB_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | X | x |
| A2 | OTP SW1AB CONFIG | R/W | 8'b0000_xxxx | - | - | - | - | SW1_CONFIG[1:0] | | SW1AB_FREQ[1:0] | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| AC | OTP SW2 VOLT | R/W | 8'b0xxx_xxxx | - | SW2_VOLT[5:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| AD | OTP SW2 SEQ | R/W | 8'b000x_xxxx | - | - | - | SW2_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| AE | OTP SW2 CONFIG | R/W | 8'b0000_00xx | - | - | - | - | - | - | SW2_FREQ[1:0] | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | x |
| B0 | OTP SW3A VOLT | R/W | 8'b0xxx_xxxx | - | SW3A_VOLT[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| B1 | OTP SW3A SEQ | R/W | 8'b000x_xxxx | - | - | - | SW3A_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| B2 | OTP SW3A CONFIG | R/W | 8'b0000_xxxx | - | - | - | - | SW3_CONFIG[1:0] | | SW3A_FREQ[1:0] | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |

Table 121. Extended page 1 (continued)

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---------|-----------------|------|--------------|-----------|----------------|---|------------------|-----------------|-----------------|------------------|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| B4 | OTP SW3B VOLT | R/W | 8'b0xxx_xxxx | – | SW3B_VOLT[6:0] | | | | | | |
| | | | | 0 | x | x | x | x | x | x | x |
| B5 | OTP SW3B SEQ | R/W | 8'b000x_xxxx | – | – | – | SW3B_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| B6 | OTP SW3B CONFIG | R/W | 8'b0000_00xx | – | – | – | – | – | – | SW3B_CONFIG[1:0] | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | x |
| BC | OTP SWBST VOLT | R/W | 8'b0000_00xx | – | – | – | – | – | – | SWBST_VOLT[1:0] | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | x |
| BD | OTP SWBST SEQ | R/W | 8'b0000_xxxx | – | – | – | SWBST_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| C0 | OTP VSNVS VOLT | R/W | 8'b0000_0xxx | – | – | – | – | – | VSNVS_VOLT[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | x |
| C4 | OTP VREFDDR SEQ | R/W | 8'b000x_x0xx | – | – | – | VREFDDR_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | 0 | x | x |
| C8 | OTP VGEN1 VOLT | R/W | 8'b0000_xxxx | – | – | – | – | VGEN1_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| C9 | OTP VGEN1 SEQ | R/W | 8'b000x_xxxx | – | – | – | VGEN1_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| CC | OTP VGEN2 VOLT | R/W | 8'b0000_xxxx | – | – | – | – | VGEN2_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| CD | OTP VGEN2 SEQ | R/W | 8'b000x_xxxx | – | – | – | VGEN2_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| D0 | OTP VGEN3 VOLT | R/W | 8'b0000_xxxx | – | – | – | – | VGEN3_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D1 | OTP VGEN3 SEQ | R/W | 8'b000x_xxxx | – | – | – | VGEN3_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| D4 | OTP VGEN4 VOLT | R/W | 8'b0000_xxxx | – | – | – | – | VGEN4_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D5 | OTP VGEN4 SEQ | R/W | 8'b000x_xxxx | – | – | – | VGEN4_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |

Table 121. Extended page 1 (continued)

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|--------------------|-------------------|-------|--------------|-----------|---------------|---|----------------|-----------------|--------------|---------------------|--------------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| D8 | OTP VGEN5 VOLT | R/W | 8'b0000_xxxx | - | - | - | - | VGEN5_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| D9 | OTP VGEN5 SEQ | R/W | 8'b000x_xxxx | - | - | - | VGEN5_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| DC | OTP VGEN6 VOLT | R/W | 8'b0000_xxxx | - | - | - | - | VGEN6_VOLT[3:0] | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| DD | OTP VGEN6 SEQ | R/W | 8'b000x_xxxx | - | - | - | VGEN6_SEQ[4:0] | | | | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| E0 | OTP PU CONFIG1 | R/W | 8'b000x_xxxx | - | - | - | PWRON_CFG1 | SWDVS_CLK1[1:0] | | SEQ_CLK_SPEED1[1:0] | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| E1 | OTP PU CONFIG2 | R/W | 8'b000x_xxxx | - | - | - | PWRON_CFG2 | SWDVS_CLK2[1:0] | | SEQ_CLK_SPEED2[1:0] | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| E2 | OTP PU CONFIG3 | R/W | 8'b000x_xxxx | - | - | - | PWRON_CFG3 | SWDVS_CLK3[1:0] | | SEQ_CLK_SPEED3[1:0] | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| E3 | OTP PU CONFIG XOR | R | 8'b000x_xxxx | - | - | - | PWRON_CFG_XOR | SWDVS_CLK3_XOR | | SEQ_CLK_SPEED_XOR | |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| E4 ⁽⁷⁶⁾ | OTP FUSE POR1 | R/W | 8'b0000_00x0 | TBB_POR | SOFT_FUSE_POR | - | - | - | - | FUSE_POR1 | - |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 |
| E5 ⁽⁷⁶⁾ | OTP FUSE POR1 | R/W | 8'b0000_00x0 | RSVD | RSVD | - | - | - | - | FUSE_POR2 | - |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 |
| E6 ⁽⁷⁶⁾ | OTP FUSE POR1 | R/W | 8'b0000_00x0 | RSVD | RSVD | - | - | - | - | FUSE_POR3 | - |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 |
| E7 | OTP FUSE POR XOR | R | 8'b0000_00x0 | RSVD | RSVD | - | - | - | - | FUSE_POR_XOR | - |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 |
| E8 | OTP PWRGD EN | R/W/M | 8'b0000_000x | - | - | - | - | - | - | - | OTP_PG_EN |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | 0 |
| F0 | OTP EN ECC0 | R/W | 8'b000x_xxxx | - | - | - | EN_ECC_BANK5 | EN_ECC_BANK4 | EN_ECC_BANK3 | EN_ECC_BANK2 | EN_ECC_BANK1 |
| | | | | 0 | 0 | 0 | x | x | x | x | x |
| F1 | OTP EN ECC1 | R/W | 8'b000x_xxxx | - | - | - | EN_ECC_BANK10 | EN_ECC_BANK9 | EN_ECC_BANK8 | EN_ECC_BANK7 | EN_ECC_BANK6 |
| | | | | 0 | 0 | 0 | x | x | x | x | x |

Table 121. Extended page 1 (continued)

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---------|---------------|------|--------------|-----------|---|---|---|-----------------|-------------------|------|----------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| F4 | OTP SPARE2_4 | R/W | 8'b0000_xxxx | - | - | - | - | RSVD | | | |
| | | | | 0 | 0 | 0 | 0 | x | x | x | x |
| F5 | OTP SPARE4_3 | R/W | 8'b0000_0xxx | - | - | - | - | - | RSVD | | |
| | | | | 0 | 0 | 0 | 0 | 0 | x | x | x |
| F6 | OTP SPARE6_2 | R/W | 8'b0000_00xx | - | - | - | - | - | RSVD | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | x | x |
| F7 | OTP SPARE7_1 | R/W | 8'b0000_0xxx | - | - | - | - | - | - | RSVD | |
| | | | | 0 | 0 | 0 | 0 | 0 | x | x | x |
| FE | OTP DONE | R/W | 8'b0000_000x | - | - | - | - | - | - | - | OTP_DONE |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x |
| FF | OTP I2C ADDR | R/W | 8'b0000_0xxx | - | - | - | - | I2C_SLV_ADDR[3] | I2C_SLV_ADDR[2:0] | | |
| | | | | 0 | 0 | 0 | 0 | 1 | x | x | x |

Notes

76. In PF0200 It is required to set all of the FUSE_PORx bits to be able to load the fuses.

Table 122. Extended page 2

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---------|------------------------|------|--------------|-----------------------------|---------------------|------|------|------|-------------------|--------------|---|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 81 | SW1AB_PWRSTG | R/W | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW1AB_PWRSTG[2:0] | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 84 | SW2_PWRSTG | R | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW2_PWRSTG[2:0] | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 85 | SW3A_PWRSTG | R | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW3A_PWRSTG[2:0] | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 86 | SW3B_PWRSTG | R | 8'b1111_1111 | RSVD | RSVD | RSVD | RSVD | RSVD | SW3B_PWRSTG[2:0] | | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 87 | PWRCTRL | R | 8'b0111_1111 | FSLEX_THERM_DISABLE | PWRGD_SHDWN_DISABLE | RSVD | RSVD | RSVD | RSVD | | |
| | | | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 88 | PWRCTRL_OTP_CTRL | R | 8'b0000_0001 | - | - | - | - | - | PWRGD_EN | OTP_SHDWN_EN | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 8D | I2C_WRITE_ADDRESS_TRAP | R/W | 8'b0000_0000 | I2C_WRITE_ADDRESS_TRAP[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 122. Extended page 2 (continued)

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|--------------------|---------------|------|--------------|--------------------------------|---------------|-------------------|--------------------|----------------|----------------|-------------------|----------------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 8E | I2C TRAP PAGE | R/W | 8'b0000_0000 | LET_IT_ROLL | RSVD | RSVD | I2C_TRAP_PAGE[4:0] | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8F | I2C TRAP CNTR | R/W | 8'b0000_0000 | I2C_WRITE_ADDRESS_COUNTER[7:0] | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 90 | IO DRV | R/W | 8'b00xx_xxxx | SDA_DRV[1:0] | | SDWNB_DRV[1:0] | | INTB_DRV[1:0] | | RESETMCU_DRV[1:0] | |
| | | | | 0 | 0 | x | x | x | x | x | x |
| D0 | OTP AUTO ECC0 | R/W | 8'b0000_0000 | - | - | - | AUTO_ECC_BANK5 | AUTO_ECC_BANK4 | AUTO_ECC_BANK3 | AUTO_ECC_BANK2 | AUTO_ECC_BANK1 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D1 | OTP AUTO ECC1 | R/W | 8'b0000_0000 | - | - | - | AUTO_ECC_BANK10 | AUTO_ECC_BANK9 | AUTO_ECC_BANK8 | AUTO_ECC_BANK7 | AUTO_ECC_BANK6 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D8 ⁽⁷⁷⁾ | Reserved | - | 8'b0000_0000 | RSVD | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D9 ⁽⁷⁷⁾ | Reserved | - | 8'b0000_0000 | RSVD | | | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E1 | OTP ECC CTRL1 | R/W | 8'b0000_0000 | ECC1_EN_TBB | ECC1_CALC_CIN | ECC1_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E2 | OTP ECC CTRL2 | R/W | 8'b0000_0000 | ECC2_EN_TBB | ECC2_CALC_CIN | ECC2_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E3 | OTP ECC CTRL3 | R/W | 8'b0000_0000 | ECC3_EN_TBB | ECC3_CALC_CIN | ECC3_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E4 | OTP ECC CTRL4 | R/W | 8'b0000_0000 | ECC4_EN_TBB | ECC4_CALC_CIN | ECC4_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E5 | OTP ECC CTRL5 | R/W | 8'b0000_0000 | ECC5_EN_TBB | ECC5_CALC_CIN | ECC5_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E6 | OTP ECC CTRL6 | R/W | 8'b0000_0000 | ECC6_EN_TBB | ECC6_CALC_CIN | ECC6_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E7 | OTP ECC CTRL7 | R/W | 8'b0000_0000 | ECC7_EN_TBB | ECC7_CALC_CIN | ECC7_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| E8 | OTP ECC CTRL8 | R/W | 8'b0000_0000 | ECC8_EN_TBB | ECC8_CALC_CIN | ECC8_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 122. Extended page 2 (continued)

| Address | Register Name | TYPE | Default | BITS[7:0] | | | | | | | |
|---------|-----------------|------|--------------|--------------|----------------|--------------------|---|---------------|-----------------|---------------|----------|
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| E9 | OTP ECC CTRL9 | R/W | 8'b0000_0000 | ECC9_EN_TBB | ECC9_CALC_CIN | ECC9_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| EA | OTP ECC CTRL10 | R/W | 8'b0000_0000 | ECC10_EN_TBB | ECC10_CALC_CIN | ECC10_CIN_TBB[5:0] | | | | | |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F1 | OTP FUSE CTRL1 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE1_EN | ANTIFUSE1_LOAD | ANTIFUSE1_RW | BYPASS1 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F2 | OTP FUSE CTRL2 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE2_EN | ANTIFUSE2_LOAD | ANTIFUSE2_RW | BYPASS2 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F3 | OTP FUSE CTRL3 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE3_EN | ANTIFUSE3_LOAD | ANTIFUSE3_RW | BYPASS3 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F4 | OTP FUSE CTRL4 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE4_EN | ANTIFUSE4_LOAD | ANTIFUSE4_RW | BYPASS4 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F5 | OTP FUSE CTRL5 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE5_EN | ANTIFUSE5_LOAD | ANTIFUSE5_RW | BYPASS5 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F6 | OTP FUSE CTRL6 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE6_EN | ANTIFUSE6_LOAD | ANTIFUSE6_RW | BYPASS6 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F7 | OTP FUSE CTRL7 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE7_EN | ANTIFUSE7_LOAD | ANTIFUSE7_RW | BYPASS7 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F8 | OTP FUSE CTRL8 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE8_EN | ANTIFUSE8_LOAD | ANTIFUSE8_RW | BYPASS8 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| F9 | OTP FUSE CTRL9 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE9_EN | ANTIFUSE9_LOAD | ANTIFUSE9_RW | BYPASS9 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| FA | OTP FUSE CTRL10 | R/W | 8'b0000_0000 | - | - | - | - | ANTIFUSE10_EN | ANTIFUSE10_LOAD | ANTIFUSE10_RW | BYPASS10 |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Notes

77. Do not write in reserved registers.

7 Typical applications

7.1 Introduction

Figure 24 provides a typical application diagram of the PF0200 PMIC together with its functional components. For details on component references and additional components such as filters, refer to the individual sections.

7.1.1 Application diagram

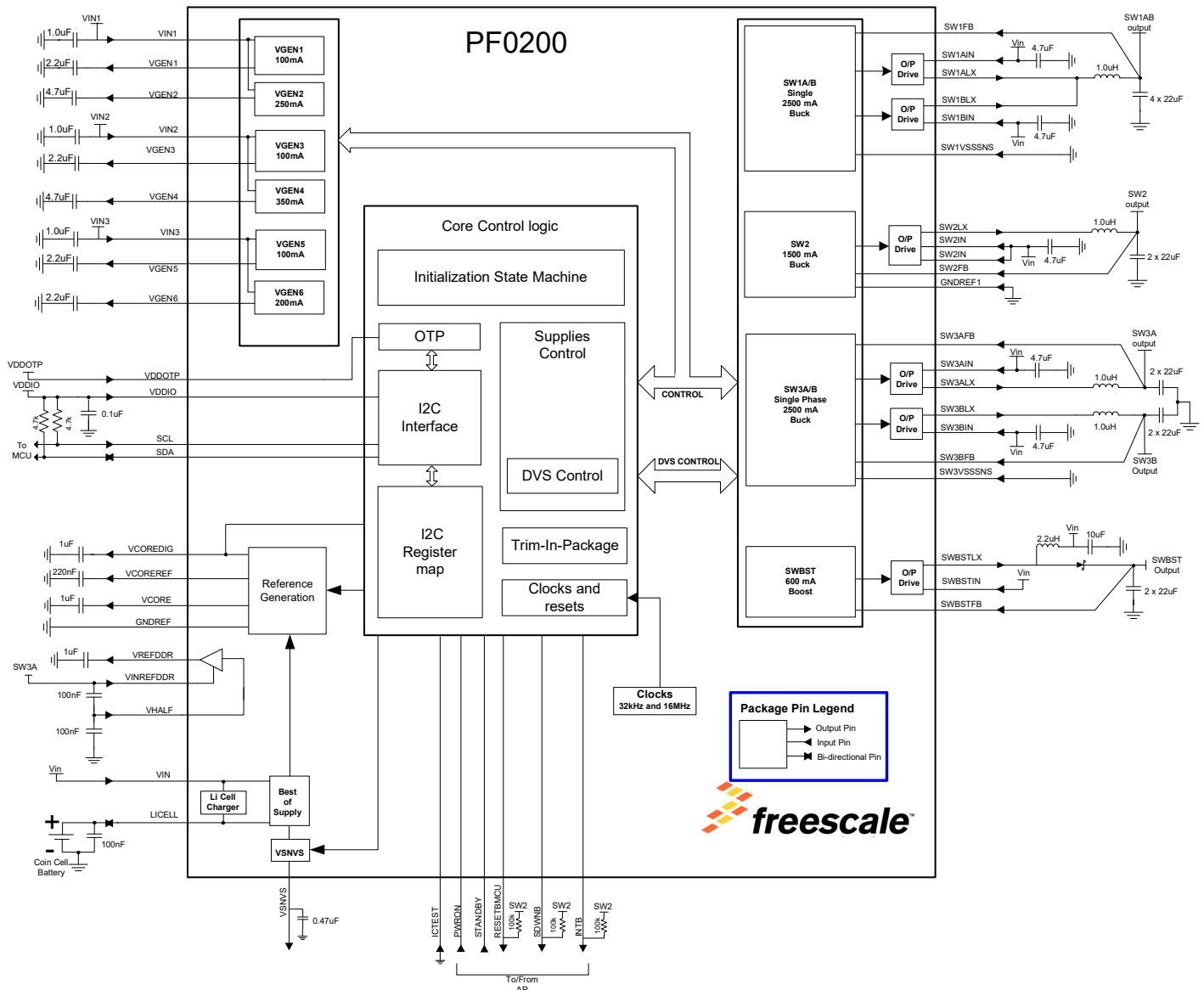


Figure 24. PF0200 typical application schematic

7.1.2 Bill of materials

The following table provides a complete list of the recommended components on a full featured system using the PF0200 Device. Critical components such as inductors, transistors, and diodes are provided with a recommended part number, but equivalent components may be used.

Table 123. Bill of materials (78)

| Value | Qty | Description | Part# | Manufacturer | Component/pin |
|---|-----|--|--------------------|------------------|--------------------------------|
| PMIC | | | | | |
| | 1 | Power management IC | PF0200 | NXP | |
| Buck, SW1AB - (0.300-1.875 V), 2.5 A | | | | | |
| 1.0 μ H | 1 | 4 x 4 x 2.1 $I_{SAT} = 4.5$ A for 10% drop, $DCR_{MAX} = 11.9$ m Ω | XFL4020-102MEB | Coilcraft | Output Inductor |
| 1.0 μ H | – | 5 x 5 x 1.5 $I_{SAT} = 3.6$ A for 10% drop, $DCR_{MAX} = 50$ m Ω | LPS5015_102ML | Coilcraft | Output Inductor (Alternate) |
| 1.0 μ H | – | 4 x 4 x 1.2 $I_{SAT} = 6.2$ A, $DCR = 37$ m Ω | FDSD0412-H-1R0M | Toko | Output inductor (Alternate) |
| 0.1 μ F | – | 3 x 3 x 1.5, $I_{SAT} = 4.5$ A, $DCR = 39$ m Ω | 74438335010 | Würth Elektronik | Output Inductor (Alternate) |
| 22 μ F | 4 | 10 V X5R 0805 | LMK212BJ226MG-T | Taiyo Yuden | Output capacitance |
| 22 μ F | 2 | 10V, X5R 0805 | GRM21BR61A226ME44L | Murata | Output capacitance (alternate) |
| 4.7 μ F | 2 | 10 V X5R 0603 | LMK107BJ475KA-T | Taiyo Yuden | Input capacitance |
| 4.7 μ F | 1 | 10V X5R 0603 | GRM155R61A104KA01D | Murata | Input capacitance (alternate) |
| 0.1 μ F | 1 | 10 V X5R 0402 | C0402C104K8PAC | Kemet | Input capacitance |
| Buck, SW2- (0.400-3.300 V), 1.5 A | | | | | |
| 1.0 μ H | 1 | 4 x 4 x 1.2 $I_{SAT} = 2.8$ A for 10% drop, $DCR_{MAX} = 60$ m Ω | LPS4012-102NL | Coilcraft | Output Inductor |
| 1.0 μ H | – | 3x 3 1.2 $I_{SAT} = 2.5$ A for 10% drop, $DCR_{MAX} = 42$ m Ω | XFL3012-102ML | Coilcraft | Output Inductor (Alternate) |
| 1.0 μ H | – | 4 x 4 x 1.2 $I_{SAT} = 6.2$ A, $DCR = 37$ m Ω | FDSD0412-H-1R0M | Toko | Output inductor (Alternate) |
| 0.1 μ F | – | 3 x 3 x 1.5, $I_{SAT} = 4.5$ A, $DCR = 39$ m Ω | 74438335010 | Würth Elektronik | Output Inductor (Alternate) |
| 22 μ F | 2 | 10 V X5R 0805 | LMK212BJ226MG-T | Taiyo Yuden | Output capacitance |
| 4.7 μ F | 1 | 10 V X5R 0603 | LMK107BJ475KA-T | Taiyo Yuden | Input capacitance |
| 0.1 μ F | 1 | 10 V X5R 0402 | C0402C104K8PAC | Kemet | Input capacitance |
| Buck, SW3AB - (0.400-3.300 V), 2.5 A | | | | | |
| 1.0 μ H | 1 | 4 x 4 x 2.1 $I_{SAT} = 4.5$ A for 10% drop, $DCR_{MAX} = 11.9$ m Ω | XFL4020-102MEB | Coilcraft | Output Inductor |
| 1.0 μ H | – | 5 x 5 x 1.5 $I_{SAT} = 3.6$ A for 10% drop, $DCR_{MAX} = 50$ m Ω | LPS5015_102ML | Coilcraft | Output Inductor (Alternate) |

Table 123. Bill of materials (78) (continued)

| Value | Qty | Description | Part# | Manufacturer | Component/pin |
|-------------|-----|---|-----------------|------------------|--------------------------------|
| 1.0 μ H | – | 4 x 4 x 1.2 $I_{SAT} = 6.2$ A, DCR = 37 m Ω | FDSD0412-H-1R0M | Toko | Output inductor (Alternate) |
| 0.1 μ F | – | 3 x 3 x 1.5, $I_{SAT} = 4.5$ A, DCR = 39 m Ω | 74438335010 | Würth Elektronik | Output Inductor (Alternate) |
| 22 μ F | 4 | 10 V X5R 0805 | LMK212BJ226MG-T | Taiyo Yuden | Output capacitance |
| 4.7 μ F | 2 | 10 V X5R 0603 | LMK107BJ475KA-T | Taiyo Yuden | Input capacitance |
| 0.1 μ F | 1 | 10 V X5R 0402 | C0402C104K8PAC | Kemet | Input capacitance |

BOOST, SWBST - 5.0 V, 600 mA

| | | | | | |
|-------------|---|--|------------------|------------------|--------------------------------|
| 2.2 μ H | 1 | 3 x 3 x 1.5 $I_{SAT} = 2.0$ A for 10% drop, DCR _{MAX} = 110 m Ω | LPS3015-222ML | Coilcraft | Output Inductor |
| 2.2 μ H | – | 3 x 3 x 1.2 $I_{SAT} = 3.1$ A, DCR = 105 m Ω | FDSD0312-H-2R2M | Toko | Output inductor (Alternate) |
| 2.2 μ H | – | 3 x 3 x 1.5, $I_{SAT} = 3.5$ A, DCR = 94 m Ω | 74438335022 | Würth Elektronik | Output Inductor (Alternate) |
| 22 μ F | 2 | 10 V X5R 0805 | LMK212BJ226MG-T | Taiyo Yuden | Output capacitance |
| 10 μ F | 1 | 10 V X5R 0805 | C2012X5R1A106MT | TDK | Input capacitance |
| 2.2 μ F | 1 | 6.3 V X5R 0402 | C0402C225M9PACTU | Kemet | Input capacitance |
| 0.1 μ F | 1 | 10 V X5R 0402 | C0402C104K8PAC | Kemet | Input capacitance |
| 1.0 A | 1 | 20 V SOD-123FL | MBR120VLSFT1G | ON Semiconductor | Schottky Diode |

LDO, VGEN1 - (0.80-1.55), 100 mA

| | | | | | |
|-------------|---|----------------|-------------------|---------------|--------------------|
| 2.2 μ F | 1 | 6.3 V X5R 0402 | C0402C225M9PACTU | Kemet | Output capacitance |
| 1.0 μ F | 1 | 10 V X5R 0402 | CC0402KRX5R6BB105 | Yageo America | Input capacitance |

LDO, VGEN2 - (0.80-1.55), 250 mA

| | | | | | |
|-------------|---|----------------|--------------------|--------|--------------------|
| 4.7 μ F | 1 | 6.3 V X5R 0402 | C0402X5R6R3-475MNP | Venkel | Output capacitance |
|-------------|---|----------------|--------------------|--------|--------------------|

LDO, VGEN3 - (1.80-3.30), 100 mA

| | | | | | |
|-------------|---|----------------|-------------------|---------------|--------------------|
| 2.2 μ F | 1 | 6.3 V X5R 0402 | C0402C225M9PACTU | Kemet | Output capacitance |
| 1.0 μ F | 1 | 10 V X5R 0402 | CC0402KRX5R6BB105 | Yageo America | Input capacitance |

LDO, VGEN4 - (1.80-3.30), 350 mA

| | | | | | |
|-------------|---|----------------|--------------------|--------|--------------------|
| 4.7 μ F | 1 | 6.3 V X5R 0402 | C0402X5R6R3-475MNP | Venkel | Output capacitance |
|-------------|---|----------------|--------------------|--------|--------------------|

LDO, VGEN5 - (1.80-3.30), 150 mA

| | | | | | |
|-------------|---|----------------|-------------------|---------------|--------------------|
| 2.2 μ F | 1 | 6.3 V X5R 0402 | C0402C225M9PACTU | Kemet | Output capacitance |
| 1.0 μ F | 1 | 10 V X5R 0402 | CC0402KRX5R6BB105 | Yageo America | Input capacitance |

LDO, VGEN6 - (1.80-3.30), 200 mA

| | | | | | |
|-------------|---|----------------|------------------|-------|--------------------|
| 2.2 μ F | 1 | 6.3 V X5R 0402 | C0402C225M9PACTU | Kemet | Output capacitance |
|-------------|---|----------------|------------------|-------|--------------------|

LDO/Switch VSNVS - (1.1-3.3), 200 mA

| | | | | | |
|--------------|---|----------------|----------------|-----|--------------------|
| 0.47 μ F | 1 | 6.3 V X5R 0402 | C1005X5R0J474K | TDK | Output capacitance |
|--------------|---|----------------|----------------|-----|--------------------|

Reference, VREFDDR - (0.20-1.65V), 10 mA

| | | | | | |
|-------------|---|---------------|-------------------|---------------|---------------------|
| 1.0 μ F | 1 | 10 V X5R 0402 | CC0402KRX5R6BB105 | Yageo America | Output capacitance |
| 0.1 μ F | 2 | 10 V X5R 0402 | C0402C104K8PAC | Kemet | VHALF, VINREFDDR |

Table 123. Bill of materials (78) (continued)

| Value | Qty | Description | Part# | Manufacturer | Component/pin |
|---|-----|---------------|--------------------|---------------|---------------|
| Internal references, VCOREDIG, VCOREREF, VCORE | | | | | |
| 1.0 μ F | 1 | 10 V X5R 0402 | CC0402KRX5R6BB105 | Yageo America | VCOREDIG |
| 1.0 μ F | 1 | 10 V X5R 0402 | CC0402KRX5R6BB105 | Yageo America | VCORE |
| 0.22 μ F | 1 | 10 V X5R 0402 | GRM155R61A224KE19D | Murata | VCOREREF |
| Coin cell | | | | | |
| 0.1 μ F | 1 | 10 V X5R 0402 | C0402C104K8PAC | Kemet | LICELL |
| Miscellaneous | | | | | |
| 0.1 μ F | 1 | 10 V X5R 0402 | C0402C104K8PAC | Kemet | VDDIO |
| 1.0 μ F | 1 | 10 V X5R 0402 | CC0402KRX5R6BB105 | Yageo America | VIN |
| 100 k Ω | 1 | 1/16 W 0402 | RK73H1ETTP1003F | KOA SPEER | PWRON |
| 100 k Ω | 1 | 1/16 W 0402 | RK73H1ETTP1003F | KOA SPEER | RESETMCU |
| 100 k Ω | 1 | 1/16 W 0402 | RK73H1ETTP1003F | KOA SPEER | SDWN |
| 100 k Ω | 1 | 1/16 W 0402 | RK73H1ETTP1003F | KOA SPEER | INTB |

Notes

78. NXP does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While NXP offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

7.2 PF0200 layout guidelines

7.2.1 General board recommendations

- It is recommended to use an eight layer board stack-up arranged as follows:
 - High current signal
 - GND
 - Signal
 - Power
 - Power
 - Signal
 - GND
 - High current signal
- Allocate TOP and BOTTOM PCB Layers for POWER ROUTING (high-current signals), copper-pour the unused area.
- Use internal layers sandwiched between two GND planes for the SIGNAL routing.

7.2.2 Component placement

It is desirable to keep all component related to the power stage as close to the PMIC as possible, specially decoupling input and output capacitors.

7.2.3 General routing requirements

- Some recommended things to keep in mind for manufacturability:
 - Via in pads require a 4.5 mil minimum annular ring. Pad must be 9.0 mils larger than the hole
 - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
 - Minimum allowed spacing between line and hole pad is 3.5 mils
 - Minimum allowed spacing between line and line is 3.0 mils

- Care must be taken with SWx_{FB} pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high power signals, like the ones on the SWx_{IN}, SWx, SWx_{LX}, SWBST_{IN}, SWBST, and SWBST_{LX} pins. They could be also shielded.
- Shield feedback traces of the regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
- Avoid coupling traces between important signal/low noise supplies (like REFCORE, VCORE, VCORED_{IG}) from any switching node (i.e. SW1_{ALX}, SW1_{BLX}, SW2_{LX}, SW3_{ALX}, SW3_{BLX}, and SWBST_{LX}).
- Make sure that all components related to a specific block are referenced to the corresponding ground.

7.2.4 Parallel routing requirements

- I²C signal routing
 - CLK is the fastest signal of the system, so it must be given special care.
 - To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.

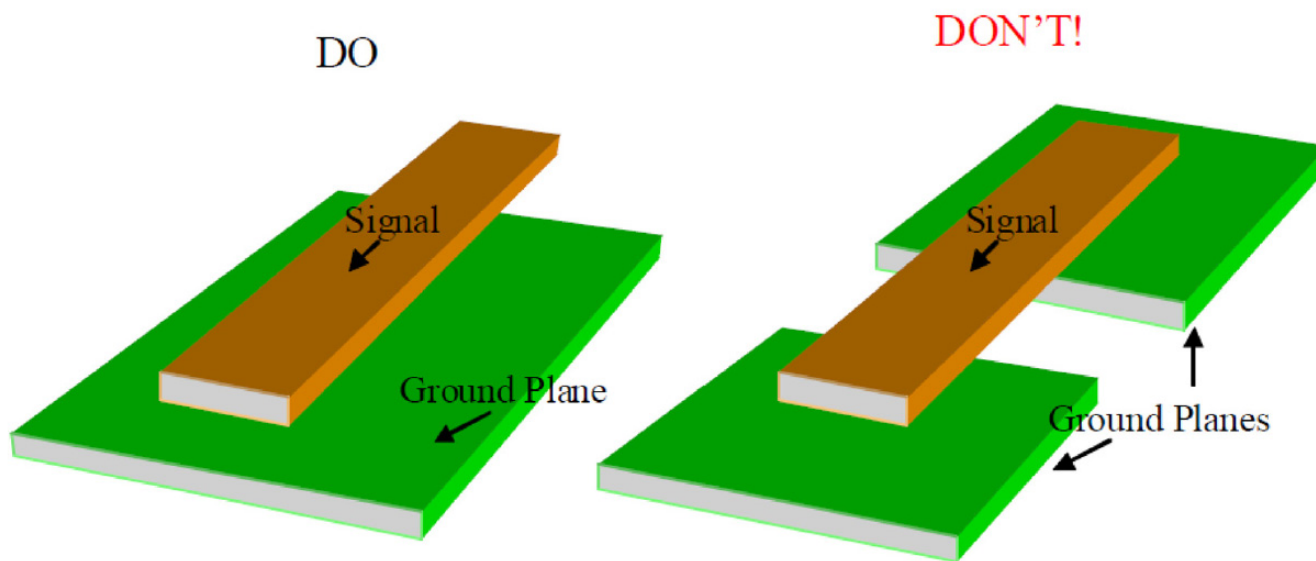


Figure 25. Recommended shielding for critical signals

- These signals can be placed on an outer layer of the board to reduce their capacitance with respect to the ground plane.
- Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

7.2.5 Switching regulator layout recommendations

- Per design, the switching regulators in PF0200 are designed to operate with only one input bulk capacitor. However, it is recommended to add a high-frequency filter input capacitor (C_{IN_hf}), to filter out any noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, closest to the IC pins.
- Make high-current ripple traces low-inductance (short, high W/L ratio).
- Make high-current traces wide or copper islands.

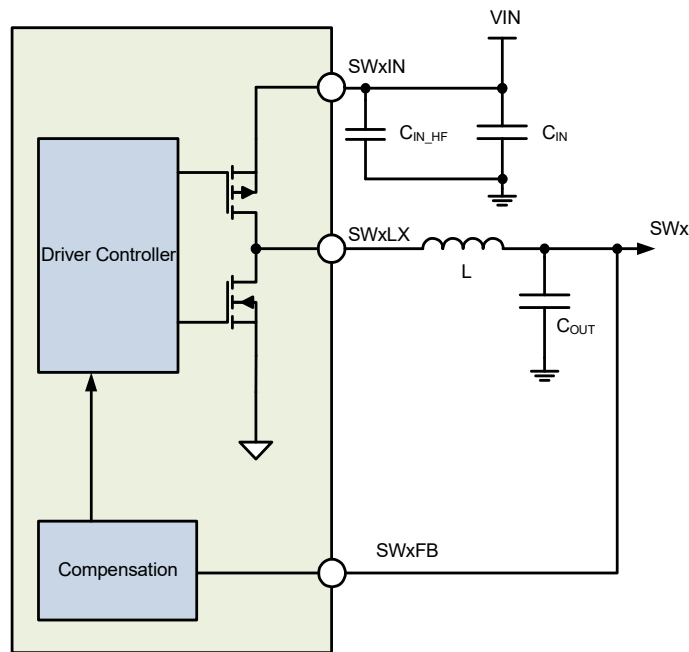


Figure 26. Generic buck regulator architecture

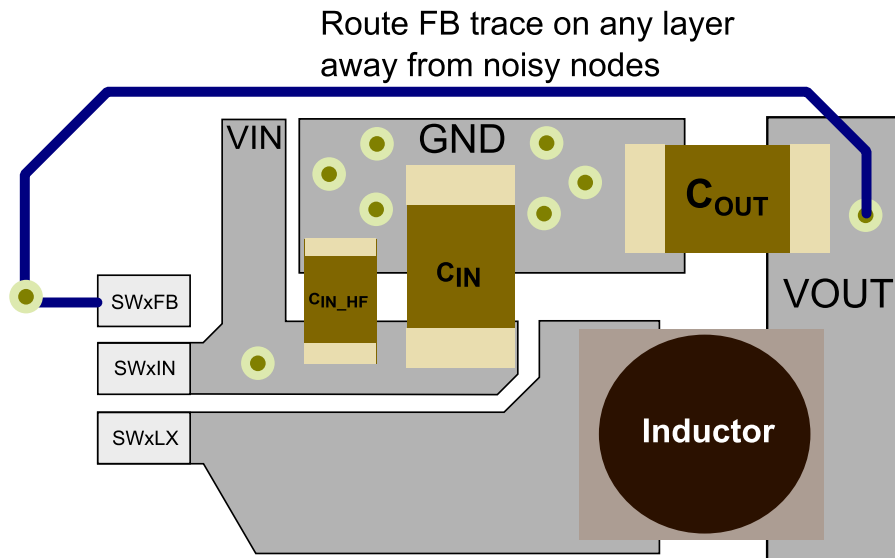


Figure 27. Recommended layout for buck regulators

7.3 Thermal information

7.3.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in [Table 4](#).

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θ_{JA} (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θ_{JMA} (Theta-JMA) will be used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, will continue to be commonly used.

The JEDEC standards can be consulted at <http://www.jedec.org>.

7.3.2 Estimation of junction temperature

An estimation of the chip junction temperature T_J can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

with:

T_A = Ambient temperature for the package in °C

$R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W

P_D = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature T_J is estimated using the following equation

$$T_J = T_B + (R_{\theta JB} \times P_D) \text{ with}$$

T_B = Board temperature at the package perimeter in °C

$R_{\theta JB}$ = Junction to board thermal resistance in °C/W

P_D = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

See [Functional block requirements and behaviors](#) for more details on thermal management.

8 Packaging

8.1 Packaging dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number. See the [Thermal characteristics](#) section for specific thermal characteristics for each package.

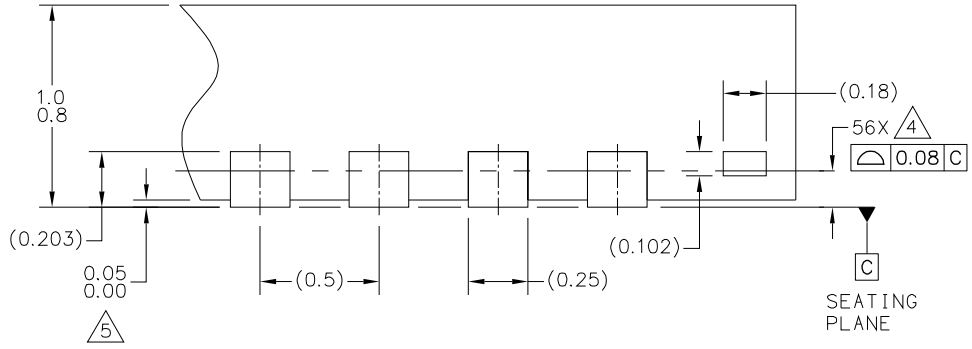
Table 124. Package drawing information

| Package | Suffix | Package outline drawing number |
|---|--------|--------------------------------|
| 56 QFN 8x8 mm - 0.5 mm pitch. E-Type (full lead) | EP | 98ASA00405D |
| 56 QFN 8x8 mm - 0.5 mm pitch. WF-Type (wetable flank) | ES | 98ASA00589D |



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DETAIL E
 VIEW ROTATED 90° CW

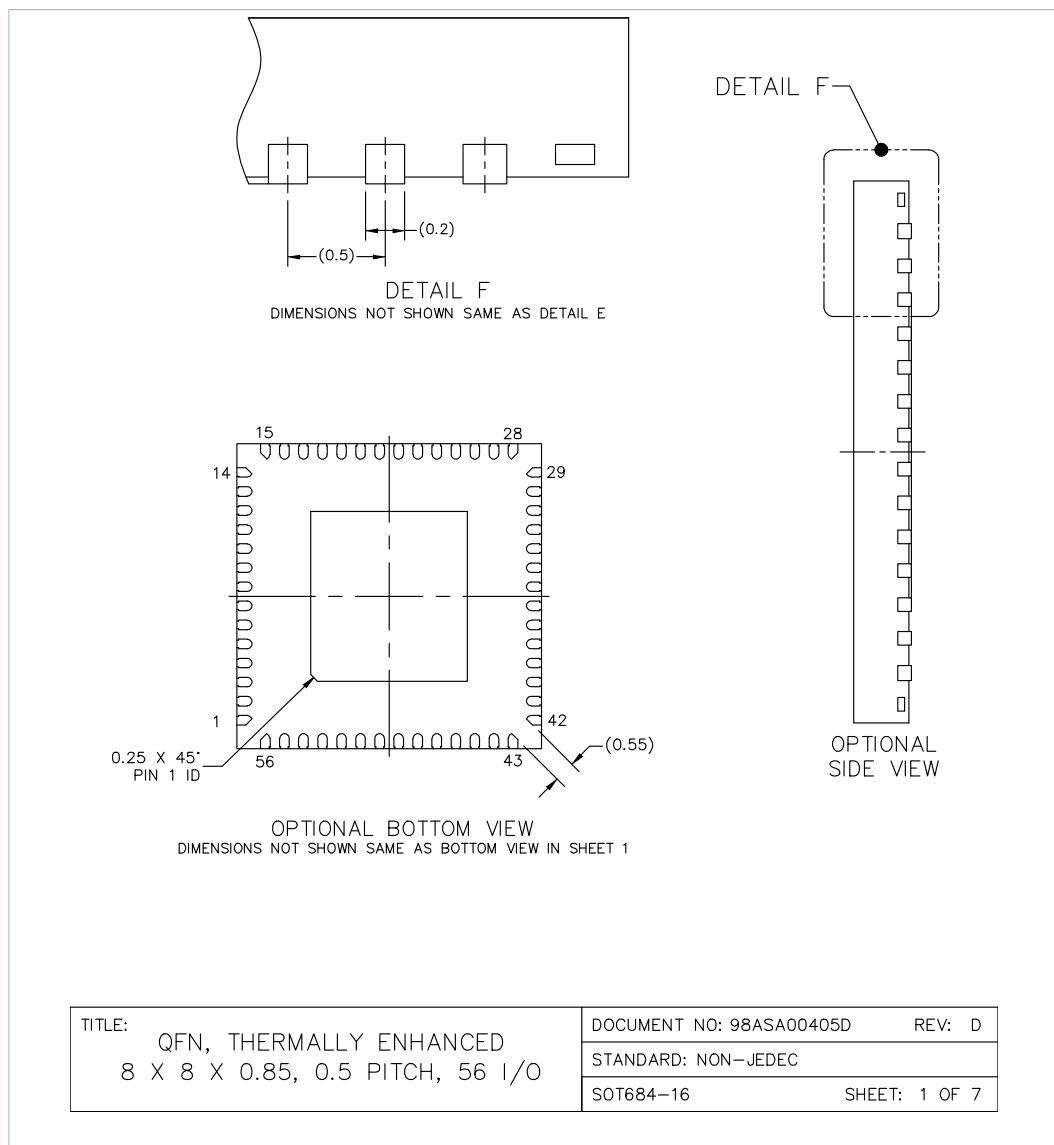
TITLE: QFN, THERMALLY ENHANCED
 8 X 8 X 0.85, 0.5 PITCH, 56 I/O


DOCUMENT NO: 98ASA00405D REV: D

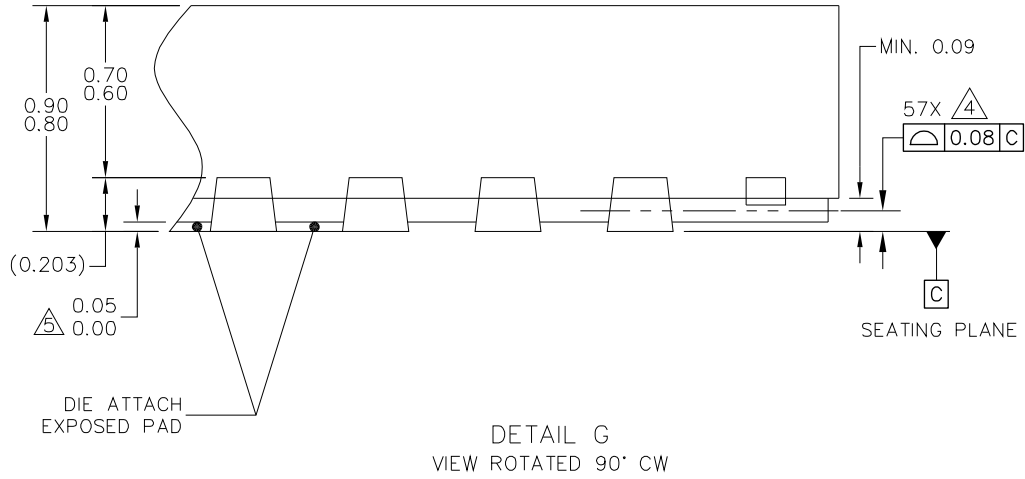
STANDARD: NON-JEDEC

SOT684-16

SHEET: 2



| | | | | | | | |
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| <p>NOTE:</p> <ol style="list-style-type: none"> 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. DIMENSIONING & TOLERANCING PER ASME Y14.5 – 1994. 3. THIS DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL TIP. 4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. 5. THIS DIMENSION APPLIES ONLY FOR TERMINALS. | | | | | | | |
| <p>TITLE: QFN, THERMALLY ENHANCED 8 X 8 X 0.85, 0.5 PITCH, 56 I/O</p> | <table border="1"> <tr> <td>DOCUMENT NO: 98ASA00405D</td> <td>REV: D</td> </tr> <tr> <td colspan="2">STANDARD: NON-JEDEC</td> </tr> <tr> <td>SOT684-16</td> <td>SHEET: 7</td> </tr> </table> | DOCUMENT NO: 98ASA00405D | REV: D | STANDARD: NON-JEDEC | | SOT684-16 | SHEET: 7 |
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| | STANDARD: NON-JEDEC | |
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| | STANDARD: NON-JEDEC | | |
| | SOT684-18 | 19 APR 2016 | |

9 Revision History

| Revision | Date | Description of changes |
|----------|--------|--|
| 3.0 | 2/2014 | <ul style="list-style-type: none"> Initial release |
| 4.0 | 5/2014 | <ul style="list-style-type: none"> Corrected VDDOTP maximum rating Corrected SWBSTFB maximum rating Added note to clarify SWBST default operation in Auto mode Changed VSNVS current limit Noted that voltage settings 0.6 V and below are not supported VSNVS Turn On Delay (t_{D1}) spec corrected from 15 ms to 5.0 ms |
| 5.0 | 7/2014 | <ul style="list-style-type: none"> Updated VTL1, VTH1 and VSNVSCROSS threshold specifications Updated per GPCN 16369 |
| 6.0 | 3/2015 | <ul style="list-style-type: none"> Added new part number MMPF0200F6AEP to the Orderable Parts table Added alternative capacitors in Bill of Materials |
| | 8/2016 | <ul style="list-style-type: none"> Updated to NXP document form and style |
| 7.0 | 7/2019 | <ul style="list-style-type: none"> Updated 98ASA00405D drawing as per PCN 201906034F01 Changed document status from Advance Information to Technical Data |
| 8.0 | 4/2022 | <ul style="list-style-type: none"> Added 98ASA00405D optional bottom view page for E-type package as per CIN 202204010I |

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