

# Kinetis K24F Sub-Family 256 KB Flash Data Sheet

## 120 MHz ARM® Cortex®-M4-based Microcontroller with FPU

The K24F product family features high memory densities, low power capabilities, and optimized integration. It shares the comprehensive enablement and scalability of the Kinetis family.

This product offers:

- 1-1 flash to RAM ratio, with 256 KB of embedded flash and 256 KB of embedded RAM to support application with high RAM density requirements.
- USB LS/FS OTG 2.0 with embedded 3.3 V, 120 mA LDO voltage regulator and USB device crystal-less operation.
- Run power consumption down to 220  $\mu$ A/MHz. Static power consumption down to 3.68  $\mu$ A with full state retention and 5  $\mu$ s wakeup. Lowest Static mode down to 173 nA

**MK24FN256VDC12**



121 XFBGA  
8 x 8 x 0.5 mm Pitch 0.65 mm

### Performance

- Up to 120 MHz ARM® Cortex®-M4 core with DSP instructions and floating point unit

### Memories and memory interfaces

- Up to 256 KB program flash memory and 256 KB RAM
- Serial programming interface (EzPort)
- Pre-programmed Kinetis flashloader for one-time, in-system factory programming

### System peripherals

- Multiple low-power modes, low-leakage wakeup unit
- 16-channel DMA controller
- External watchdog monitor
- Software watchdog

### Clocks

- 3 to 32 MHz and 32 kHz crystal oscillator
- Multipurpose clock generator with FLL and PLL
- 32 kHz, and 4 MHz internal reference clock
- 48 MHz internal reference

### Analog modules

- Two 16-bit SAR ADCs
- 12-bit DAC
- Two analog comparators (CMP)
- Voltage reference

### Communication interfaces

- USB full-/low-speed On-the-Go controller
- USB Device Charger detect (USBDCD)
- Three SPI modules
- Three I2C modules
- Six UART modules
- I2S module

### Timers

- Two 8-channel motor control/general purpose/PWM timers
- Two 2-channel quadrature decoder/general purpose timers
- Periodic interrupt timers and 16-bit low power timer
- Carrier modulator transmitter
- Real-time clock
- Programmable delay block

### Security and integrity modules

- Hardware CRC module
- 128-bit unique identification (ID) number per chip

### Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105 °C

### Ordering Information <sup>1</sup>

Part Number	Memory		Maximum number of I/O's
	Flash	SRAM (KB)	
MK24FN256VDC12	256 KB	256	83

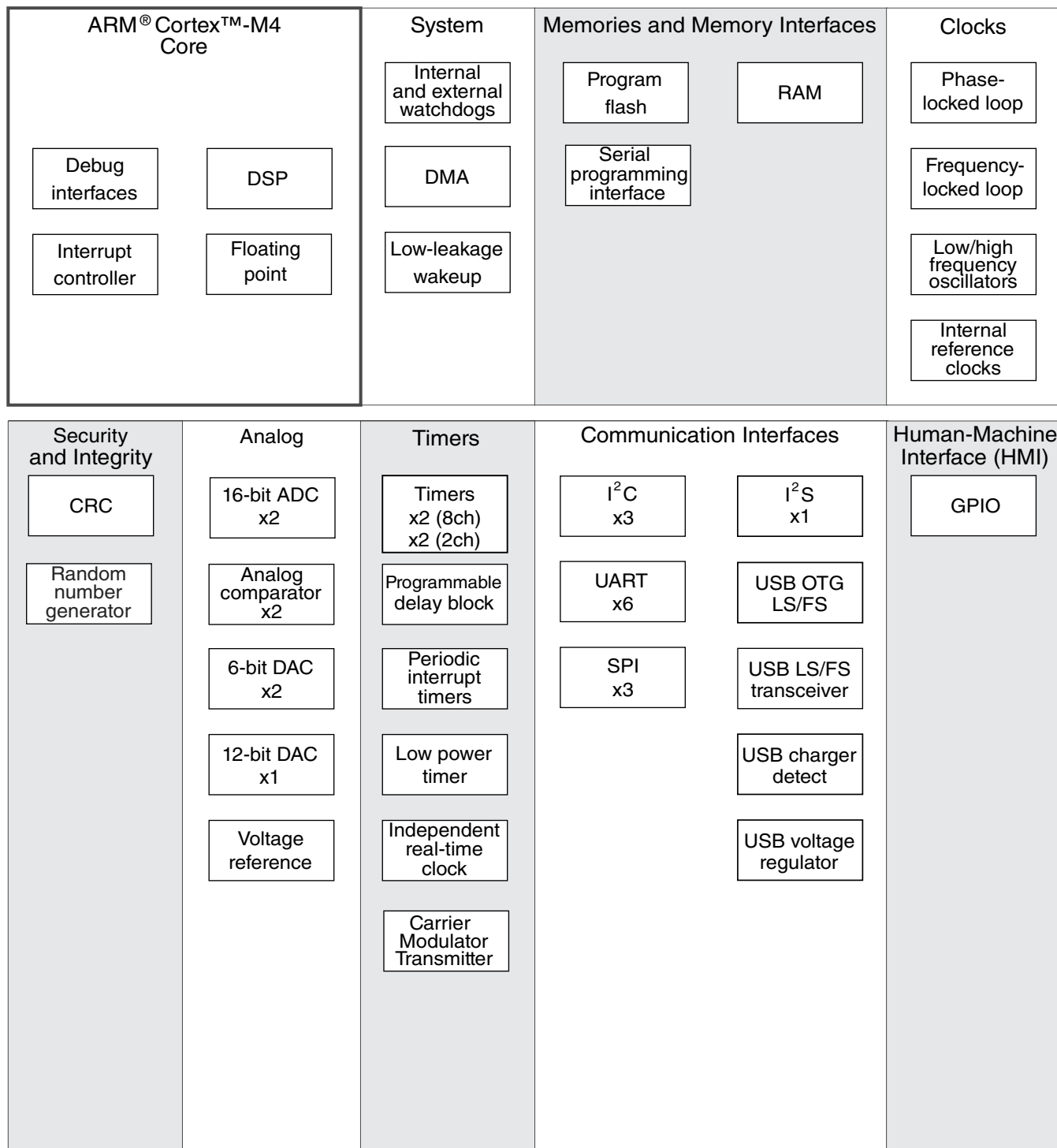
1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

### Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	<a href="#">Solution Advisor</a>
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K60PB <sup>1</sup>
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K24P121M120SF5RM <sup>1</sup>
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Package drawing	Package dimensions are provided in package drawings.	XFBGA 121-pin: 98ASA00595D <sup>1</sup>

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

## Kinetic K24 Family



**Figure 1. K24 block diagram**

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# 1 Ratings

## 1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 70 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

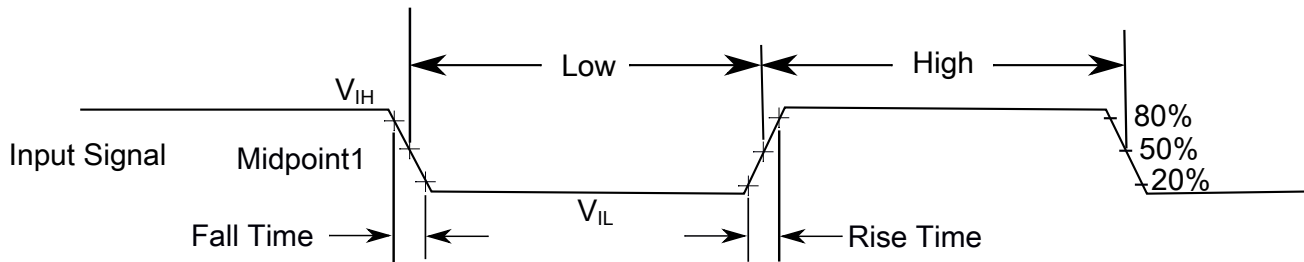
Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	185	mA
$V_{DIO}$	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
$V_{AIO}$	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Maximum current single pin limit (applies to all digital pins)	-25.0	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{USB0\_DP}$	USB0_DP input voltage	-0.3	3.63	V
$V_{USB0\_DM}$	USB0_DM input voltage	-0.3	3.63	V
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 2. Input signal measurement reference**

### 2.2 Nonswitching electrical specifications

## 2.2.1 Voltage and current operating requirements

**Table 1. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	3.6	V	
V <sub>DDA</sub>	Analog supply voltage	1.71	3.6	V	
V <sub>DD</sub> – V <sub>DDA</sub>	V <sub>DD</sub> -to-V <sub>DDA</sub> differential voltage	-0.1	0.1	V	
V <sub>SS</sub> – V <sub>SSA</sub>	V <sub>SS</sub> -to-V <sub>SSA</sub> differential voltage	-0.1	0.1	V	
V <sub>BAT</sub>	RTC battery supply voltage	1.71	3.6	V	
V <sub>IH</sub>	Input high voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	0.7 × V <sub>DD</sub> 0.75 × V <sub>DD</sub>	— —	V V	
V <sub>IL</sub>	Input low voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	— —	0.35 × V <sub>DD</sub> 0.3 × V <sub>DD</sub>	V V	
V <sub>HYS</sub>	Input hysteresis	0.06 × V <sub>DD</sub>	—	V	
I <sub>ICIO</sub>	Analog <sup>1</sup> , pin DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V (Negative current injection)</li> <li>• V<sub>IN</sub> &gt; V<sub>DD</sub>+0.3V (Positive current injection)</li> </ul>	-3 —	— +3	mA	2
I <sub>ICcont</sub>	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>• Negative current injection</li> <li>• Positive current injection</li> </ul>	-25 —	— +25	mA	
V <sub>ODPU</sub>	Open drain pullup voltage level	V <sub>DD</sub>	V <sub>DD</sub>	V	3
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	
V <sub>RFVBAT</sub>	V <sub>BAT</sub> voltage required to retain the VBAT register file	V <sub>POR_VBAT</sub>	—	V	4

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
2. All analog and I/O pins are internally clamped to V<sub>SS</sub> and V<sub>DD</sub> through ESD protection diodes. If V<sub>IN</sub> is less than V<sub>IO\_MIN</sub> or greater than V<sub>IO\_MAX</sub>, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{IO\_MIN}-V_{IN})/|I_{ICIO}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{IO\_MAX})/|I_{ICIO}|$ . Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
3. Open drain outputs must be pulled to V<sub>DD</sub>.
4. If V<sub>BAT</sub> is not used, the pin must be left floating.

## 2.2.2 LVD and POR operating requirements

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V <sub>LVW1H</sub>	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	2.62	2.70	2.78	V	1
V <sub>LVW2H</sub>		2.72	2.80	2.88	V	
V <sub>LVW3H</sub>		2.82	2.90	2.98	V	
V <sub>LVW4H</sub>		2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	1.74	1.80	1.86	V	1, 2
V <sub>LVW2L</sub>		1.84	1.90	1.96	V	
V <sub>LVW3L</sub>		1.94	2.00	2.06	V	
V <sub>LVW4L</sub>		2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage
2. , The reset state of the LVD is low range threshold. To utilize the LVD for the specified VDD range, change the LVD range to 'high range'.

**Table 3. VBAT power operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR_VBAT</sub>	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

## 2.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — High drive pad	V <sub>DD</sub> - 0.5	—	V	1

*Table continues on the next page...*



**Table 4. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -20\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -10\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$	—	V	
	Output high voltage — Normal drive pad				1
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -2.5\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$	—	V	
		$V_{DD} - 0.5$	—	V	
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$V_{OH\_RTC\_WAKEUP}$	Output high voltage — normal drive pad				
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}</math>, <math>I_{OH} = -5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}</math>, <math>I_{OH} = -1.5\text{ mA}</math></li> </ul>	$V_{BAT} - 0.5$	—	V	
		$V_{BAT} - 0.5$	—	V	
$I_{OH\_RTC\_WAKEUP}$	Output high current total for RTC_WAKEUP pins	—	100	mA	
$V_{OL}$	Output low voltage — high drive pad				1
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 20\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 10\text{ mA}</math></li> </ul>	—	0.5	V	
		—	0.5	V	
	Output low voltage — normal drive pad				1
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 2.5\text{ mA}</math></li> </ul>	—	0.5	V	
		—	0.5	V	
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$V_{OL\_RTC\_WAKEUP}$	Output low voltage — normal drive pad				
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{BAT} \leq 3.6\text{ V}</math>, <math>I_{OL} = 5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{BAT} \leq 2.7\text{ V}</math>, <math>I_{OL} = 1.5\text{ mA}</math></li> </ul>	—	0.5	V	
		—	0.5	V	
$I_{OL\_RTC\_WAKEUP}$	Output low current total for RTC_WAKEUP pins	—	100	mA	
$I_{IN}$	Input leakage current (per pin) for full temperature range	—	1	$\mu\text{A}$	2
$I_{IN}$	Input leakage current (per pin) at 25°C	—	0.025	$\mu\text{A}$	2
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) for full temperature range	—	1	$\mu\text{A}$	
$I_{IN\_RTC\_WAKEUP}$	Input leakage current (per RTC_WAKEUP pin) at 25°C	—	0.025	$\mu\text{A}$	
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	0.25	$\mu\text{A}$	
$I_{OZ\_RTC\_WAKEUP}$	Hi-Z (off-state) leakage current (per RTC_WAKEUP pin)	—	0.25	$\mu\text{A}$	
$R_{PU}$	Internal pullup resistors (except RTC_WAKEUP pins)	20	50	k $\Omega$	3
$R_{PD}$	Internal pulldown resistors (except RTC_WAKEUP pins)	20	50	k $\Omega$	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at  $V_{DD}=3.6\text{V}$
3. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{SS}$
4. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{DD}$

## 2.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$ , and  $VLLSx \rightarrow RUN$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz

**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	$\mu s$	
	• $VLLS0 \rightarrow RUN$	—	130	$\mu s$	
	• $VLLS1 \rightarrow RUN$	—	130	$\mu s$	
	• $VLLS2 \rightarrow RUN$	—	65	$\mu s$	
	• $VLLS3 \rightarrow RUN$	—	65	$\mu s$	
	• $LLS \rightarrow RUN$	—	4.9	$\mu s$	
	• $VLPS \rightarrow RUN$	—	4.8	$\mu s$	
	• $STOP \rightarrow RUN$	—	4.8	$\mu s$	

## 2.2.5 Power consumption operating behaviors

### Important

Please note that these specifications are preliminary and as per design targets. These are subject to change.

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA}$	Analog supply current	—	—	See note	mA	1
$I_{DD\_RUN}$	Run mode current — all peripheral clocks disabled, code executing from flash					2

*Table continues on the next page...*

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>@ 3.0 V</li> </ul>	—	27.3	38.8	mA	
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks enabled, code executing from flash <ul style="list-style-type: none"> <li>@ 3.0 V               <ul style="list-style-type: none"> <li>@ 25 °C</li> <li>@ 70 °C</li> <li>@ 105 °C</li> </ul> </li> </ul>	—	35.6	39	mA	3, 4
		—	36.46	41.39	mA	
		—	38.21	44.67	mA	
I <sub>DD_WAIT</sub>	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	15.0	—	mA	2
I <sub>DD_WAIT</sub>	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.67	—	mA	5
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.878	—	mA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.23	—	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.538	—	mA	8
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V <ul style="list-style-type: none"> <li>@ –40 to 25 °C</li> <li>@ 70 °C</li> <li>@ 105 °C</li> </ul>	—	0.458	1.068	mA	
		—	0.964	3.544	mA	
		—	2.12	9.22	mA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> <li>@ –40 to 25 °C</li> <li>@ 70 °C</li> <li>@ 105 °C</li> </ul>	—	50.6	210.57	μA	
		—	225.24	908.25	μA	
		—	619.98	2273.88	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V <ul style="list-style-type: none"> <li>@ –40 to 25 °C</li> <li>@ 70 °C</li> <li>@ 105 °C</li> </ul>	—	3.68	13.03	μA	9
		—	14.14	49.34	μA	
		—	51.57	183.11	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> <li>@ –40 to 25 °C</li> <li>@ 70 °C</li> <li>@ 105 °C</li> </ul>	—	3.02	5.53	μA	
		—	12.06	37.57	μA	
		—	43.59	140.76	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> <li>@ –40 to 25 °C</li> <li>@ 70 °C</li> <li>@ 105 °C</li> </ul>	—	1.73	2.26	μA	
		—	3.98	9.36	μA	
		—	13.09	37.68	μA	

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25 °C</li> <li>• @ 70 °C</li> <li>• @ 105 °C</li> </ul>	—	0.777	0.97	μA	
		—	2.14	4.7	μA	
		—	8.52	25.22	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> <li>• @ -40 to 25 °C</li> <li>• @ 70 °C</li> <li>• @ 105 °C</li> </ul>	—	0.360	0.56	μA	
		—	1.67	4.29	μA	
		—	7.91	24.37	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> <li>• @ -40 to 25 °C</li> <li>• @ 70 °C</li> <li>• @ 105 °C</li> </ul>	—	0.173	0.246	μA	
		—	1.41	2.25	μA	
		—	7.42	17.02	μA	
I <sub>DD_VBAT</sub>	Average current with RTC and 32kHz disabled at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25 °C</li> <li>• @ 70 °C</li> <li>• @ 105 °C</li> </ul>	—	0.18	0.21	μA	
		—	0.66	0.81	μA	
		—	2.92	3.92	μA	
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers <ul style="list-style-type: none"> <li>• @ 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25 °C</li> <li>• @ 70 °C</li> <li>• @ 105 °C</li> </ul> </li> </ul>	—	0.71	0.86	μA	10
		—	1.22	1.66	μA	
		—	3.50	5.53	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 120 MHz core and system clock, 60 MHz bus, clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
3. 120 MHz core and system clock, 60 MHz bus clock, and 24 MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 0.5 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1.0 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1.0 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 256 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

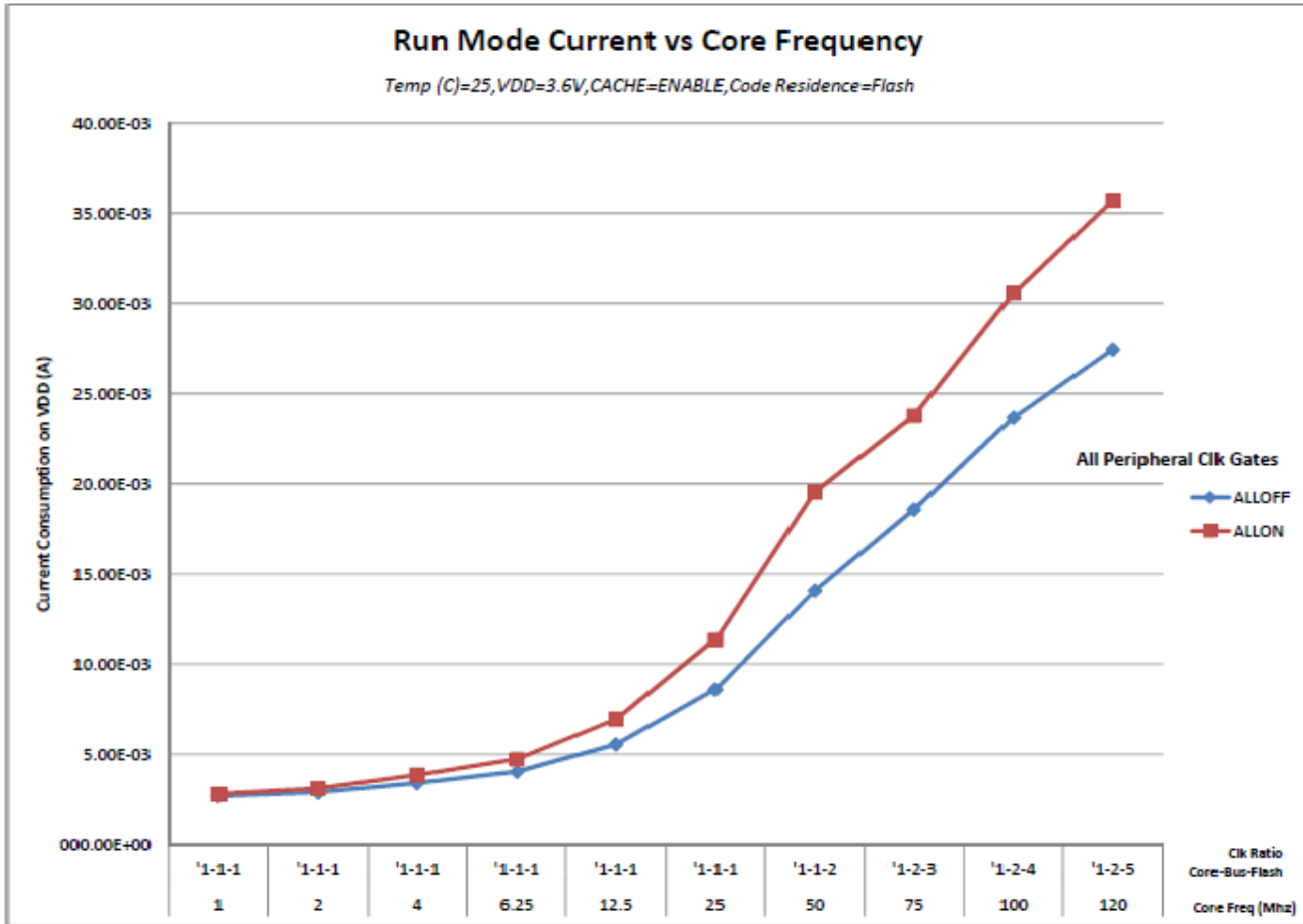
**Table 7. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)				Unit
		-10	25	50	85	
I <sub>IREFSTEN4MHz</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	μA
I <sub>IREFSTEN32KHz</sub>	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	μA
I <sub>EREFSTEN4MHz</sub>	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	uA
I <sub>EREFSTEN32KHz</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.					
	VLLS1	440	490	540	560	nA
	VLLS3	440	490	540	560	
	LLS	490	490	540	560	
	VLPS	510	560	560	560	
	STOP	510	560	560	560	
I <sub>48MIRC</sub>	48 Mhz internal reference clock	350	350	350	350	
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	μA
I <sub>BG</sub>	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	μA
I <sub>ADC</sub>	ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>D<sub>DA</sub></sub> by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	μA

### 2.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 3. Run mode supply current vs. core frequency**

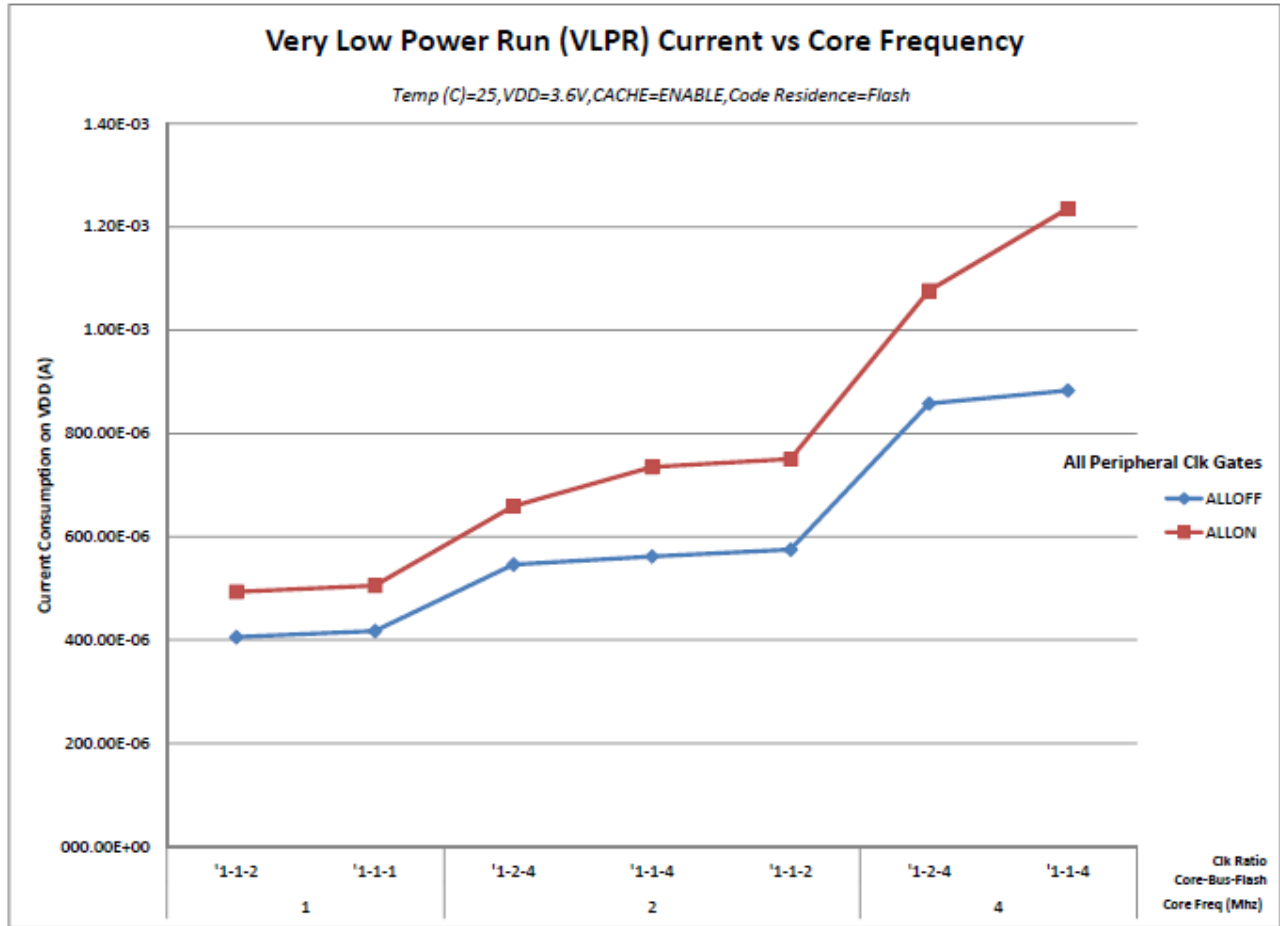


Figure 4. VLPR mode supply current vs. core frequency

## 2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
			121 XFBGA		
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	16	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	22	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	21	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	16	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic

## General

application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2.  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $f_{OSC} = 12\text{ MHz}$  (crystal),  $f_{SYS} = 120\text{ MHz}$ ,  $f_{BUS} = 60\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

### 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

### 2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

Table 10. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	120	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
$f_{BUS}$	Bus clock	—	60	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	
$f_{LPTMR}$	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
$f_{SYS}$	System and core clock	—	4	MHz	
$f_{BUS}$	Bus clock	—	4	MHz	
$f_{FLASH}$	Flash clock	—	0.8	MHz	

Table continues on the next page...



**Table 10. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
f <sub>ERCLK</sub>	External reference clock	—	16	MHz	
f <sub>LPTMR_pin</sub>	LPTMR clock	—	25	MHz	
f <sub>LPTMR_ERCLK</sub>	LPTMR external reference clock	—	16	MHz	
f <sub>I2S_MCLK</sub>	I2S master clock	—	12.5	MHz	
f <sub>I2S_BCLK</sub>	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

**Table 11. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>• Slew disabled <ul style="list-style-type: none"> <li>• 1.71 ≤ V<sub>DD</sub> ≤ 2.7 V</li> <li>• 2.7 ≤ V<sub>DD</sub> ≤ 3.6 V</li> </ul> </li> <li>• Slew enabled <ul style="list-style-type: none"> <li>• 1.71 ≤ V<sub>DD</sub> ≤ 2.7 V</li> <li>• 2.7 ≤ V<sub>DD</sub> ≤ 3.6 V</li> </ul> </li> </ul>	—	10	ns	4
		—	5	ns	
		—	30	ns	
		—	16	ns	
	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> <li>• Slew disabled</li> </ul>				5

**Table 11. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7 V</math></li> </ul>	—	10	ns	
	<ul style="list-style-type: none"> <li>• <math>2.7 \leq V_{DD} \leq 3.6 V</math></li> </ul>	—	5	ns	
	<ul style="list-style-type: none"> <li>• Slew enabled</li> </ul>	—	30	ns	
	<ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7 V</math></li> </ul>	—	16	ns	
	<ul style="list-style-type: none"> <li>• <math>2.7 \leq V_{DD} \leq 3.6 V</math></li> </ul>	—			

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 25 pF load

## 2.4 Thermal specifications

### 2.4.1 Thermal operating requirements

**Table 12. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	105	°C

### 2.4.2 Thermal attributes

Board type	Symbol	Description	121 XFBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	33.3	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	21.1	°C/W	1

*Table continues on the next page...*

Board type	Symbol	Description	121 XFBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	26.2	$^{\circ}\text{C}/\text{W}$	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	17.8	$^{\circ}\text{C}/\text{W}$	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	16.3	$^{\circ}\text{C}/\text{W}$	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	12	$^{\circ}\text{C}/\text{W}$	3
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	$^{\circ}\text{C}/\text{W}$	4

## NOTES:

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 3 Peripheral operating requirements and behaviors

### 3.1 Core modules

### 3.1.1 JTAG electricals

**Table 13. JTAG full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 20 33	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	50 25 15	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.0	—	ns
J7	TCLK low to boundary scan output data valid	—	32.8	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	26.5	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

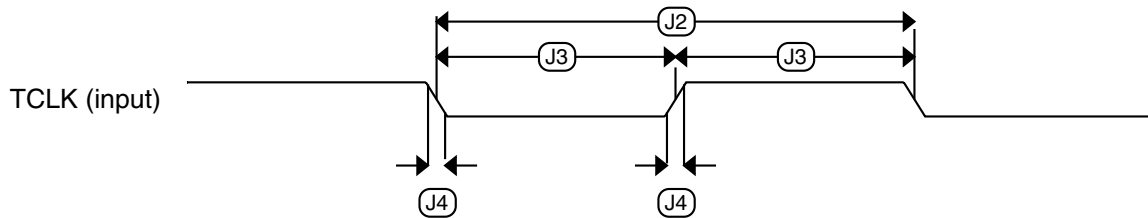
**Table 14. JTAG limited voltage electricals**

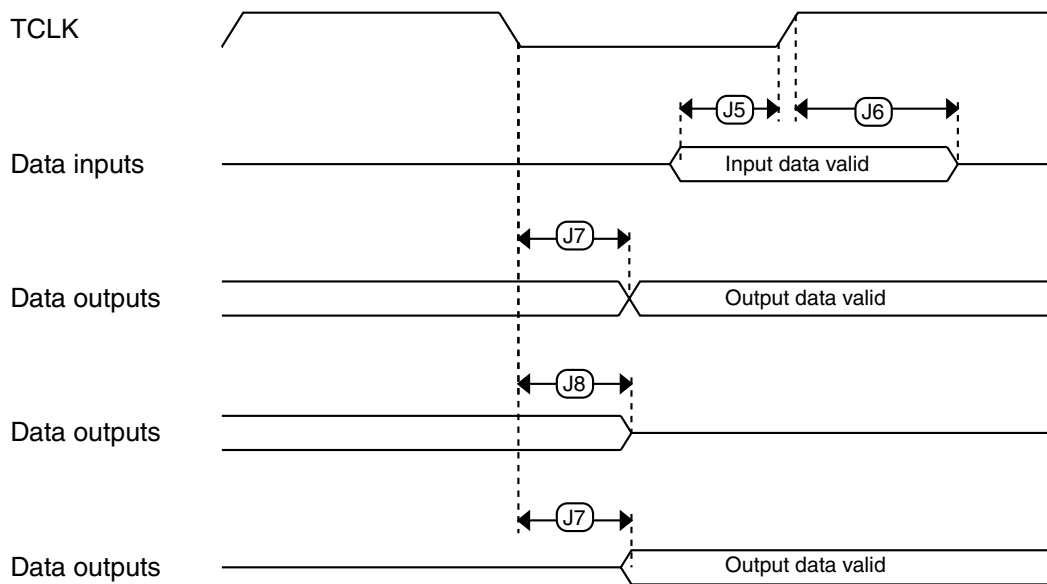
Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 20 33	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> </ul>	50	—	ns

*Table continues on the next page...*

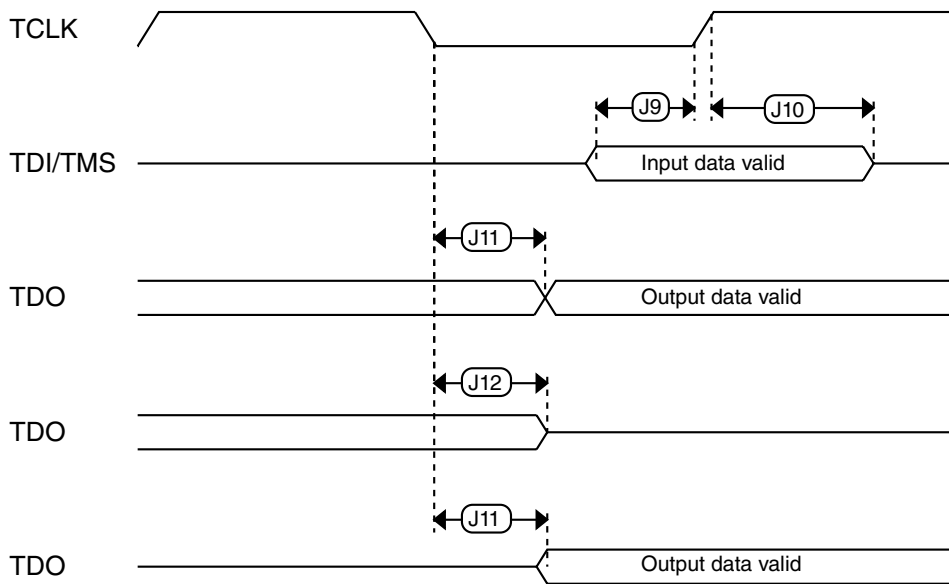
**Table 14. JTAG limited voltage electricals (continued)**

Symbol	Description	Min.	Max.	Unit
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	15	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

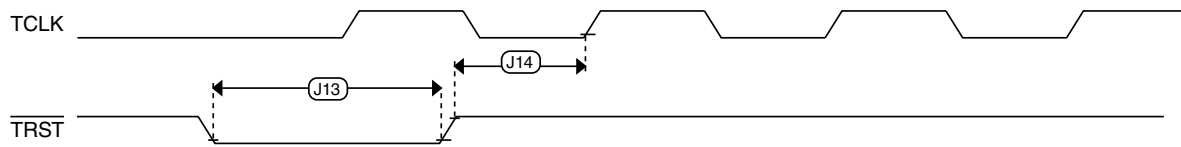

**Figure 5. Test clock input timing**



**Figure 6. Boundary scan (JTAG) timing**



**Figure 7. Test Access Port timing**


**Figure 8. TRST timing**

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG specifications

**Table 15. MCG specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$I_{ints}$	Internal reference (slow clock) current	—	20	—	μA	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% $f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	% $f_{dco}$	1
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	± 0.5	± 2	% $f_{dco}$	1 ,
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1	% $f_{dco}$	1
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$I_{intf}$	Internal reference (fast clock) current	—	25	—	μA	

Table continues on the next page...

**Table 15. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
f <sub>loc_low</sub>	Loss of external clock minimum frequency — RANGE = 00	(3/5) x f <sub>ints_t</sub>	—	—	kHz		
f <sub>loc_high</sub>	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	(16/5) x f <sub>ints_t</sub>	—	—	kHz		
FLL							
f <sub>fill_ref</sub>	FLL reference frequency range	31.25	—	39.0625	kHz		
f <sub>dco</sub>	DCO output frequency range	Low range (DRS=00) 640 × f <sub>fill_ref</sub>	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f <sub>fill_ref</sub>	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f <sub>fill_ref</sub>	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f <sub>fill_ref</sub>	80	83.89	100	MHz	
f <sub>dco_t_DMx3</sub> 2	DCO output frequency	Low range (DRS=00) 732 × f <sub>fill_ref</sub>	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f <sub>fill_ref</sub>	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f <sub>fill_ref</sub>	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f <sub>fill_ref</sub>	—	95.98	—	MHz	
J <sub>cyc_fill</sub>	FLL period jitter • f <sub>DCO</sub> = 48 MHz • f <sub>DCO</sub> = 98 MHz	—	180 150	—	ps		
t <sub>fill_acquire</sub>	FLL target frequency acquisition time	—	—	1	ms	6	
PLL							
f <sub>vco</sub>	VCO operating frequency	48.0	—	120	MHz		
I <sub>pll</sub>	PLL operating current • PLL @ 96 MHz (f <sub>osc_hi_1</sub> = 8 MHz, f <sub>pll_ref</sub> = 2 MHz, VDIV multiplier = 48)	—	1060	—	μA	7	
		—	600	—	μA	7	
f <sub>pll_ref</sub>	PLL reference frequency range	2.0	—	4.0	MHz		
J <sub>cyc_pll</sub>	PLL period jitter (RMS) • f <sub>vco</sub> = 48 MHz • f <sub>vco</sub> = 120 MHz	—	120	—	ps	8	
		—	—	—	ps		
J <sub>acc_pll</sub>	PLL accumulated jitter over 1 μs (RMS)	—	—	—	—	8	

Table continues on the next page...



**Table 15. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li><math>f_{vco} = 48 \text{ MHz}</math></li> <li><math>f_{vco} = 120 \text{ MHz}</math></li> </ul>	—	1350	—	ps	
		—	600	—	ps	
$D_{lock}$	Lock entry frequency tolerance	$\pm 1.49$	—	$\pm 2.98$	%	
$D_{unl}$	Lock exit frequency tolerance	$\pm 4.47$	—	$\pm 5.97$	%	
$t_{pll\_lock}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

### 3.3.2 IRC48M specifications

**Table 16. IRC48M specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DD48M}$	Supply current	—	400	500	$\mu\text{A}$	
$f_{irc48m}$	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage ( $V_{DD}=1.71\text{V}-1.89\text{V}$ ) over temperature <ul style="list-style-type: none"> <li>• Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0)</li> <li>• Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)</li> </ul>	—	$\pm 0.5$	$\pm 1.0$	$\%f_{irc48m}$	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage ( $V_{DD}=1.89\text{V}-3.6\text{V}$ ) over temperature <ul style="list-style-type: none"> <li>• Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)</li> </ul>	—	$\pm 0.5$	$\pm 1.0$	$\%f_{irc48m}$	
$\Delta f_{irc48m\_cl}$	Closed loop total deviation of IRC48M frequency over voltage and temperature	—	—	$\pm 0.1$	$\%f_{host}$	1

Table continues on the next page...

**Table 16. IRC48M specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$J_{cyc\_irc48m}$	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	$\mu$ s	2

1. Closed loop operation of the IRC48M is only feasible for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting IRC48M as USB clock source, and enabling the clock recover function (USB\_CLK\_RECOVER\_IRC\_CTRL[CLOCK\_RECOVER\_EN]=1, USB\_CLK\_RECOVER\_IRC\_EN[IRC\_EN]=1).
2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting USB\_CLK\_RECOVER\_IRC\_EN[IRC\_EN]=1.

### 3.3.3 Oscillator electrical specifications

#### 3.3.3.1 Oscillator DC electrical specifications

**Table 17. Oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DDOSC}$	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
$I_{DDOSC}$	Supply current — high-gain mode (HGO=1) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	$\mu$ A	1
$C_x$	EXTAL load capacitance	—	—	—		2, 3
$C_y$	XTAL load capacitance	—	—	—		2, 3
$R_F$	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M $\Omega$	

Table continues on the next page...

**Table 17. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	

1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C<sub>x</sub> and C<sub>y</sub> can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

### 3.3.3.2 Oscillator frequency specifications

**Table 18. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f <sub>osc_lo</sub>	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f <sub>osc_hi_1</sub>	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	

Table continues on the next page...

**Table 18. Oscillator frequency specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{ec\_extal}$	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

**NOTE**

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

### 3.3.4 32 kHz oscillator electrical characteristics

#### 3.3.4.1 32 kHz oscillator DC electrical specifications

**Table 19. 32kHz oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{BAT}$	Supply voltage	1.71	—	3.6	V
$R_F$	Internal feedback resistor	—	100	—	MΩ
$C_{para}$	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
$V_{pp}^1$	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 3.3.4.2 32 kHz oscillator frequency specifications

**Table 20. 32 kHz oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal	—	32.768	—	kHz	
$t_{start}$	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$V_{ec\_extal32}$	Externally provided input clock amplitude	700	—	$V_{BAT}$	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and  $V_{IH}$  and  $V_{IL}$  specifications do not apply. The voltage of the applied clock must be within the range of  $V_{SS}$  to  $V_{BAT}$ .

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 21. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp4}$	Longword Program high-voltage time	—	7.5	18	$\mu$ s	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

#### 3.4.1.2 Flash timing specifications — commands

**Table 22. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{pgmchk}$	Program Check execution time	—	—	45	$\mu$ s	1
$t_{rdsrc}$	Read Resource execution time	—	—	30	$\mu$ s	1

*Table continues on the next page...*

**Table 22. Flash command timing specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu$ s	—
$t_{ersscr}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	1.8	ms	—
$t_{rdonce}$	Read Once execution time	—	—	30	$\mu$ s	1
$t_{pgmonce}$	Program Once execution time	—	100	—	$\mu$ s	—
$t_{ersall}$	Erase All Blocks execution time	—	500	3000	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	30	$\mu$ s	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 3.4.1.3 Flash high voltage current behaviors

**Table 23. Flash high voltage current behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{DD\_PGM}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{DD\_ERS}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 3.4.1.4 Reliability specifications

**Table 24. NVM reliability specifications**

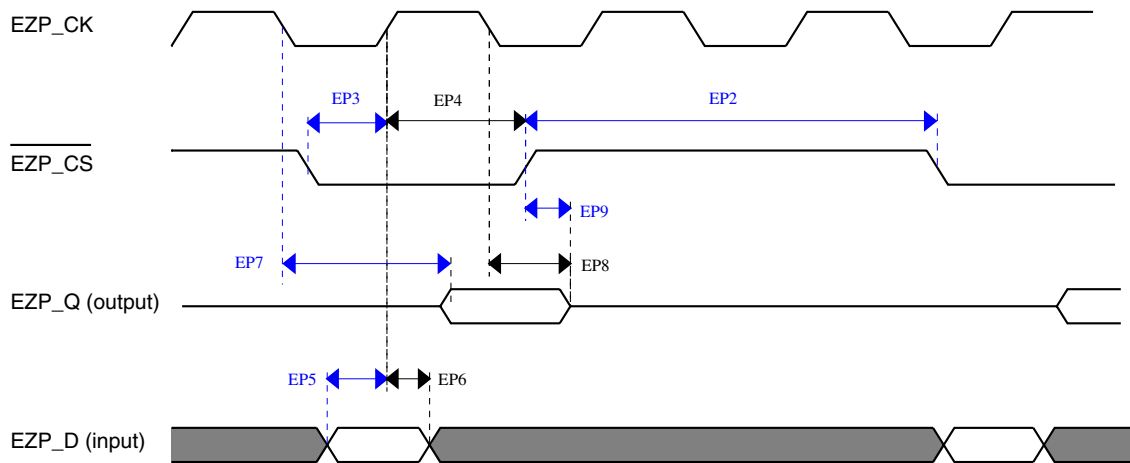
Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40\text{ °C} \leq T_j \leq 125\text{ °C}$ .

### 3.4.2 EzPort switching specifications

**Table 25. EzPort full voltage range switching specifications**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	$2 \times t_{\text{EZP\_CK}}$	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	18	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns



**Figure 9. EzPort Timing Diagram**

## 3.5 Analog

### 3.5.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 26](#) and [Table 27](#) are achievable on the differential pins ADCx\_DP0, ADCx\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 3.5.1.1 16-bit ADC operating conditions

**Table 26. 16-bit ADC operating conditions**

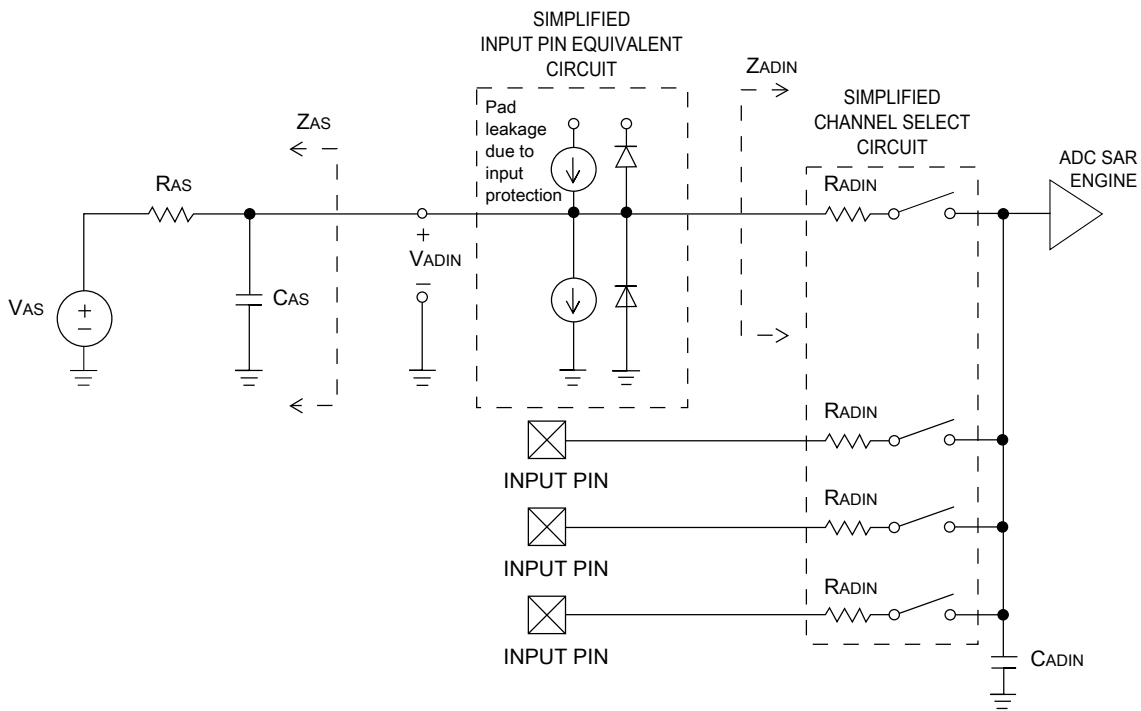
Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )	-100	0	+100	mV	<a href="#">2</a>
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )	-100	0	+100	mV	<a href="#">2</a>
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	ADC reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage	<ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>	V <sub>REFL</sub> V <sub>REFL</sub>	— —	31/32 * V <sub>REFH</sub> V <sub>REFH</sub>	V	
V <sub>ADIN</sub>	Input voltage		V <sub>REFL</sub>	—	V <sub>REFH</sub>	V	
C <sub>ADIN</sub>	Input capacitance	<ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>	— —	8 4	10 5	pF	
R <sub>ADIN</sub>	Input series resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance (external)	13-bit / 12-bit modes f <sub>ADCK</sub> < 4 MHz	—	—	5	kΩ	<a href="#">3</a>
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	<a href="#">4</a>
f <sub>ADCK</sub>	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	<a href="#">4</a>
C <sub>rate</sub>	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	<a href="#">5</a>
C <sub>rate</sub>	ADC conversion rate	16-bit mode No ADC hardware averaging	37.037	—	461.467	Ksps	<a href="#">5</a>



**Table 26. 16-bit ADC operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
		Continuous conversions enabled, subsequent conversion time					

1. Typical values assume  $V_{DDA} = 3.0\text{ V}$ ,  $\text{Temp} = 25\text{ }^\circ\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$ , unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had  $< 8\ \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $< 1\text{ ns}$ .
4. To use the maximum ADC conversion clock frequency,  $\text{CFG2}[\text{ADHSC}]$  must be set and  $\text{CFG1}[\text{ADLPC}]$  must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).



**Figure 10. ADC input impedance equivalency diagram**

### 3.5.1.2 16-bit ADC electrical characteristics

**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

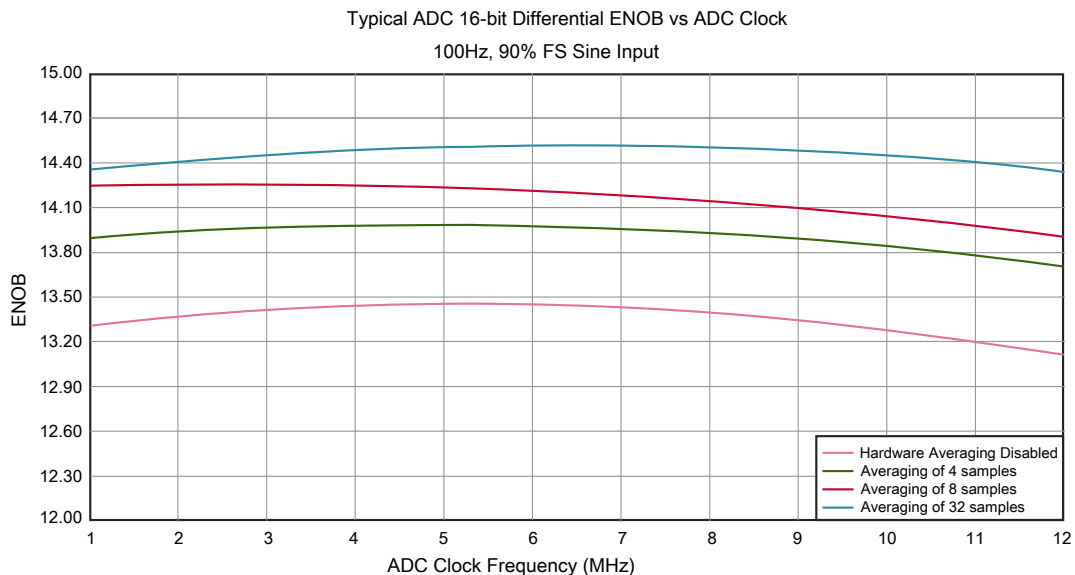
Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$f_{ADACK}$	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	$\pm 4$ $\pm 1.4$	$\pm 6.8$ $\pm 2.1$	LSB <sup>4</sup>	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	$\pm 0.7$ $\pm 0.2$	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5
INL	Integral non-linearity	• 12-bit modes • <12-bit modes	— —	$\pm 1.0$ $\pm 0.5$	-2.7 to +1.9 -0.7 to +0.5	LSB <sup>4</sup>	5
$E_{FS}$	Full-scale error	• 12-bit modes • <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ <sup>5</sup>
$E_Q$	Quantization error	• 16-bit modes • $\leq 13$ -bit modes	— —	-1 to 0 —	— $\pm 0.5$	LSB <sup>4</sup>	
ENOB	Effective number of bits	16-bit differential mode	12.8	14.5	—	bits	6
		• Avg = 32	11.9	13.8	—	bits	
		• Avg = 4	12.2	13.9	—	bits	
		16-bit single-ended mode	11.4	13.1	—	bits	
		• Avg = 32 • Avg = 4					
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode	—	-94	—	dB	7
		• Avg = 32	—	-85	—	dB	
		16-bit single-ended mode					
		• Avg = 32					
SFDR	Spurious free dynamic range	16-bit differential mode	82	95	—	dB	7
		• Avg = 32	78	90	—	dB	

Table continues on the next page...

**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
		16-bit single-ended mode • Avg = 32					
$E_{IL}$	Input leakage error		$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
$V_{TEMP25}$	Temp sensor voltage	25 °C	706	716	726	mV	8

- All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
- Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$
- ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
- Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
- Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
- ADC conversion clock < 3 MHz


**Figure 11. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**

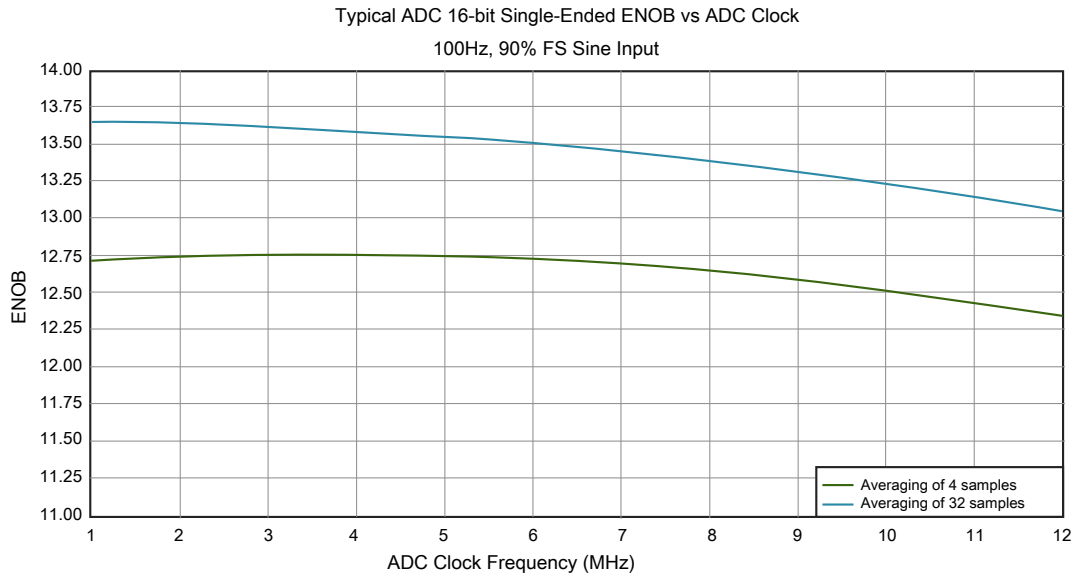


Figure 12. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode

### 3.5.2 CMP and 6-bit DAC electrical specifications

Table 28. Comparator and 6-bit DAC electrical specifications

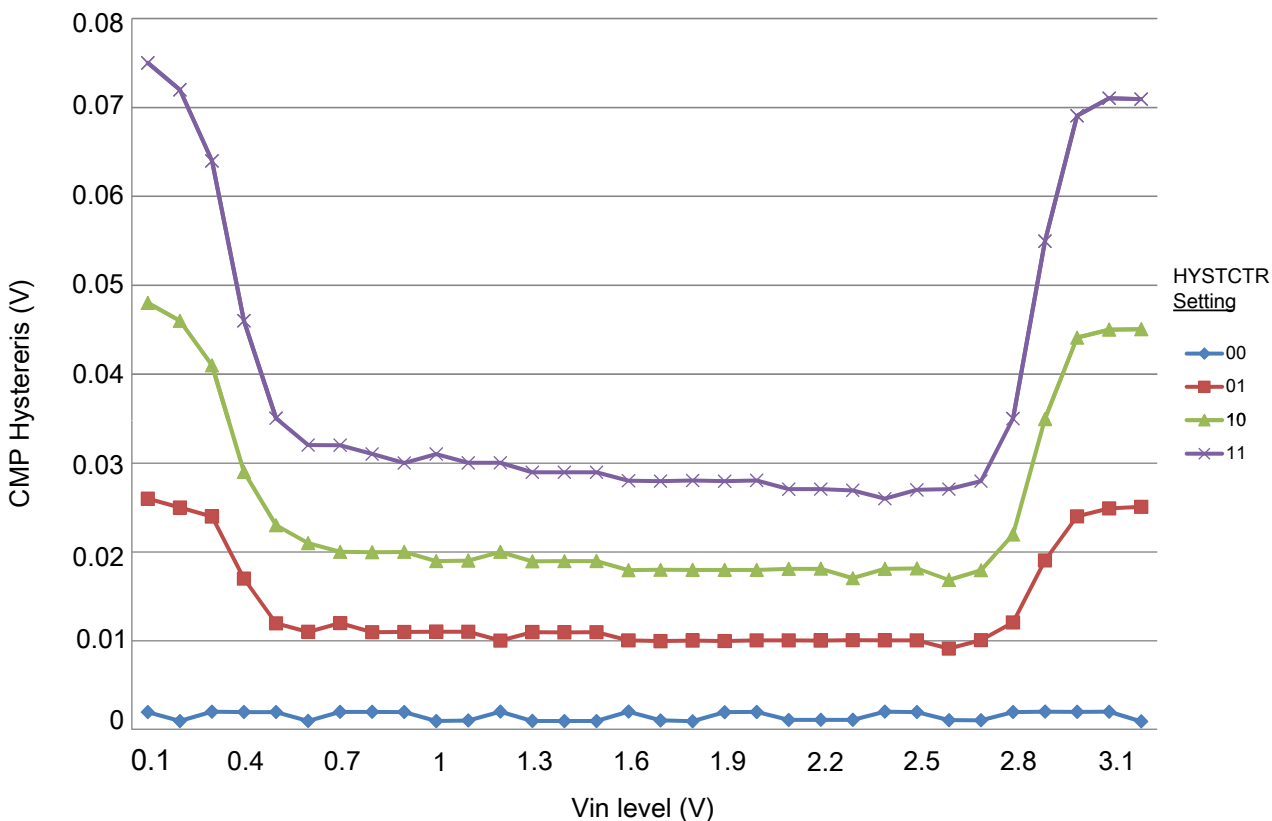
Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V
I <sub>DDHS</sub>	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I <sub>DDL</sub>	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V <sub>AIN</sub>	Analog input voltage	V <sub>SS</sub> - 0.3	—	V <sub>DD</sub>	V
V <sub>AIO</sub>	Analog input offset voltage	—	—	20	mV
V <sub>H</sub>	Analog comparator hysteresis <sup>1</sup> <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul>	—	5 10 20 30	—	mV
V <sub>CMPOh</sub>	Output high	V <sub>DD</sub> - 0.5	—	—	V
V <sub>CMPOl</sub>	Output low	—	—	0.5	V
t <sub>DHS</sub>	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t <sub>DLS</sub>	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	μs
I <sub>DAC6b</sub>	6-bit DAC current adder (enabled)	—	7	—	μA

Table continues on the next page...

**Table 28. Comparator and 6-bit DAC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6$  V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$



**Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**

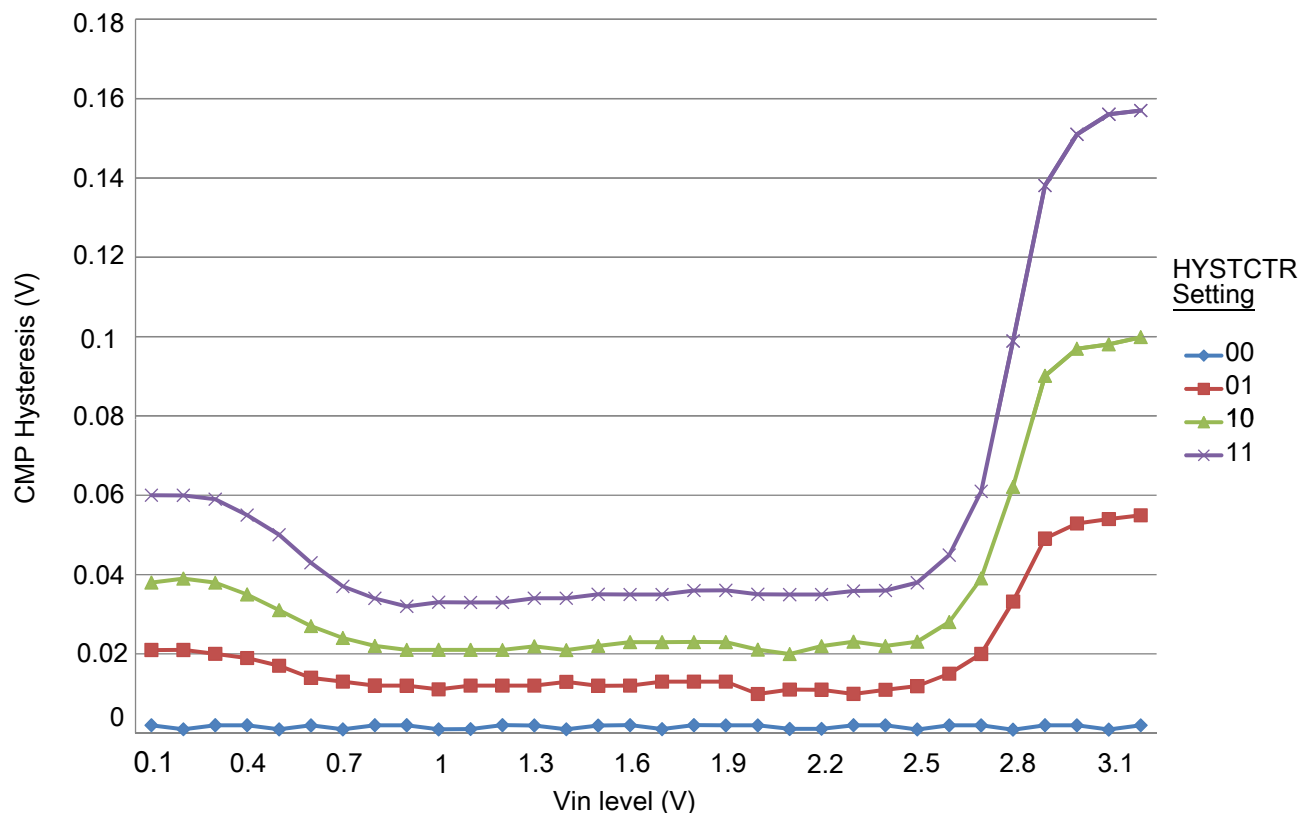


Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

### 3.5.3 12-bit DAC electrical characteristics

#### 3.5.3.1 12-bit DAC operating requirements

Table 29. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be  $V_{DDA}$  or  $V_{REFH}$ .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

### 3.5.3.2 12-bit DAC operating behaviors

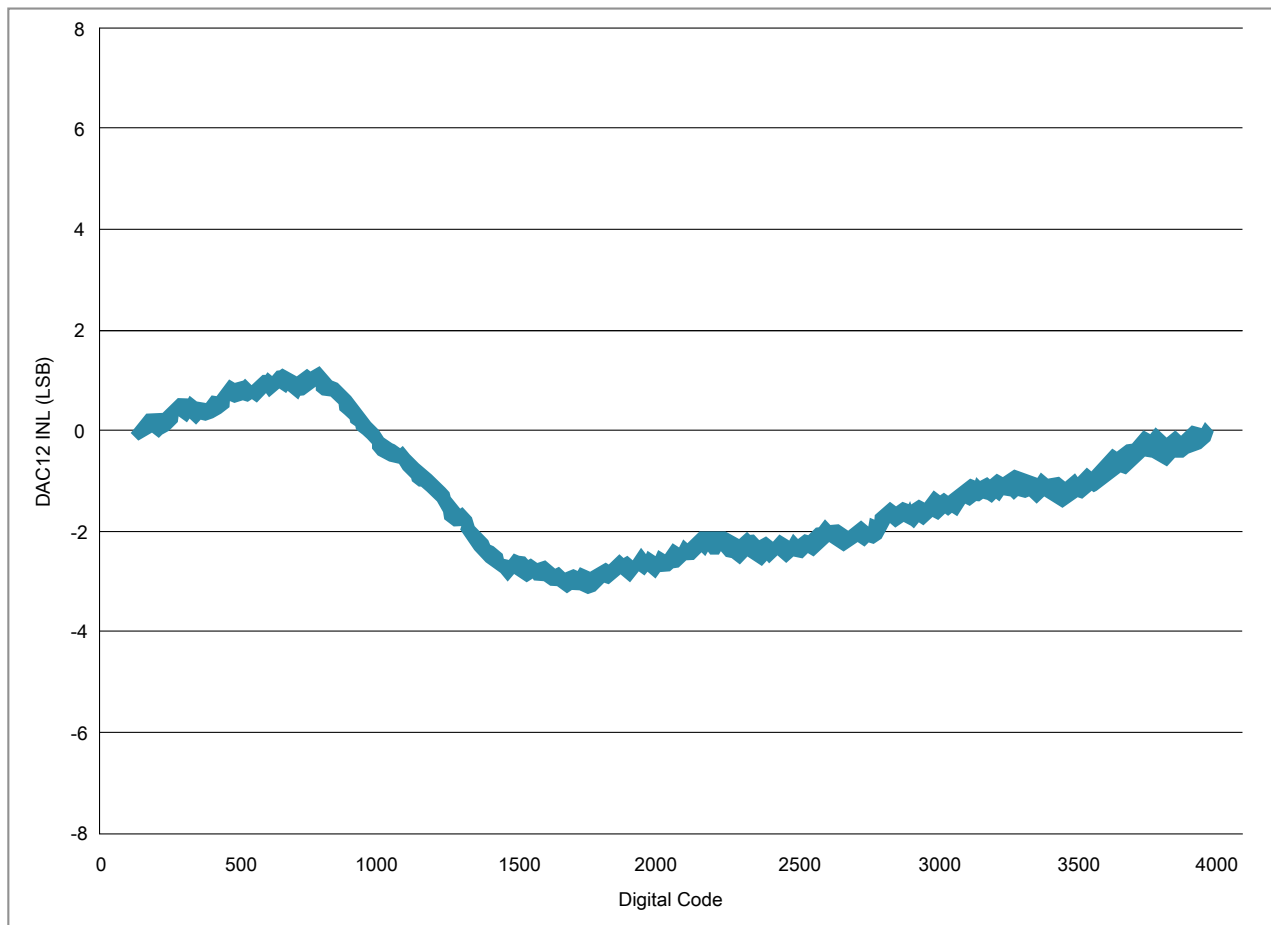
Table 30. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	330	$\mu\text{A}$	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	1200	$\mu\text{A}$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu\text{s}$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu\text{s}$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	$\pm 0.8$	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$A_C$	Offset aging coefficient	—	—	100	$\mu\text{V}/\text{yr}$	
$R_{op}$	Output resistance (load = 3 k $\Omega$ )	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>• High power (<math>SP_{HP}</math>)</li> <li>• Low power (<math>SP_{LP}</math>)</li> </ul>	1.2 0.05	1.7 0.12	— —	$\text{V}/\mu\text{s}$	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>• High power (<math>SP_{HP}</math>)</li> <li>• Low power (<math>SP_{LP}</math>)</li> </ul>	550 40	— —	— —	kHz	

1. Settling within  $\pm 1$  LSB
2. The INL is measured for 0 + 100 mV to  $V_{DACR} - 100\text{ mV}$
3. The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100\text{ mV}$
4. The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100\text{ mV}$  with  $V_{DDA} > 2.4\text{ V}$
5. Calculated by a best fit curve from  $V_{SS} + 100\text{ mV}$  to  $V_{DACR} - 100\text{ mV}$

**Peripheral operating requirements and behaviors**

- 6.  $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  (DACx\_CO:DACRFS = 1), high power mode (DACx\_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device



**Figure 15. Typical INL error vs. digital code**



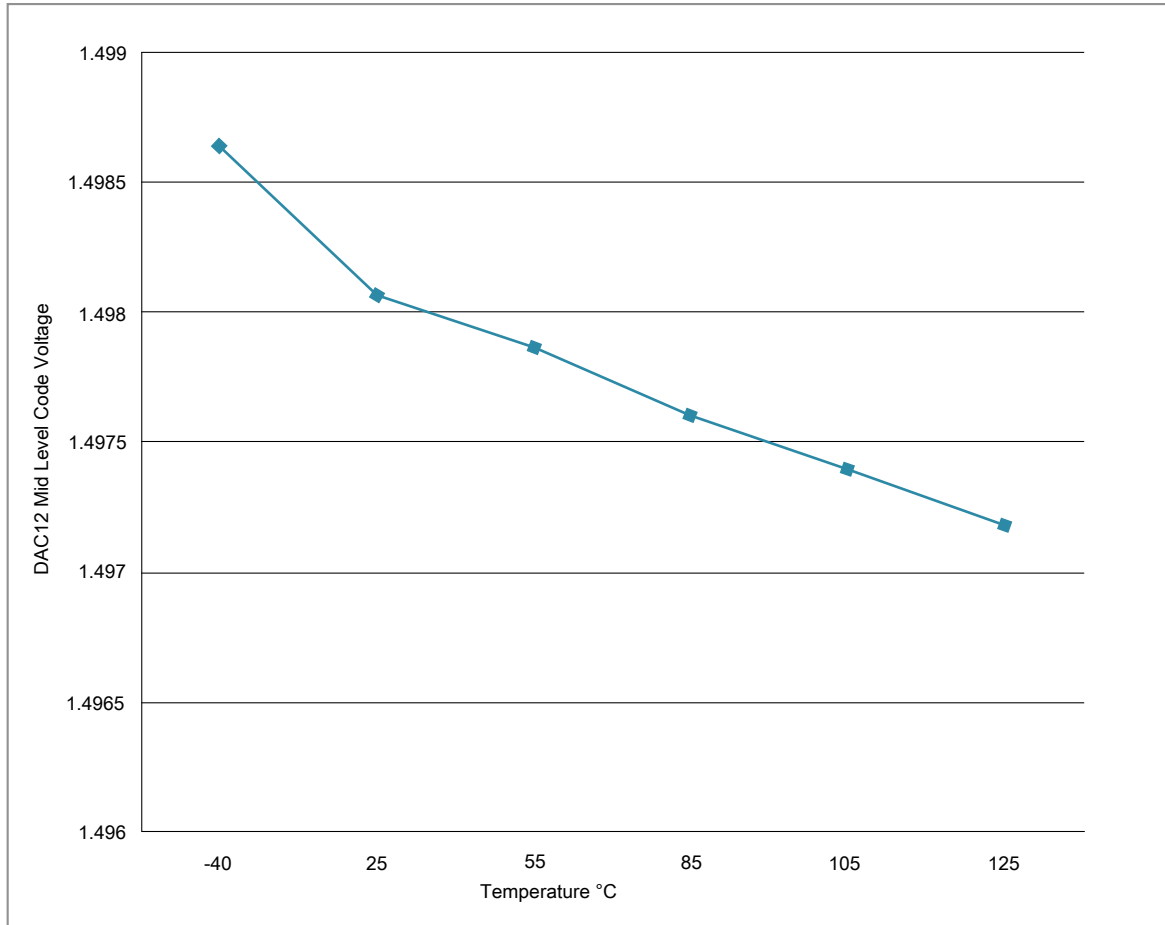


Figure 16. Offset at half scale vs. temperature

### 3.5.4 Voltage reference electrical specifications

Table 31. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	—
$T_A$	Temperature	Operating temperature range of the device		°C	—
$C_L$	Output load capacitance	100		nF	1, 2

1.  $C_L$  must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified  $C_L$  value over the operating temperature range of the device.

**Table 32. VREF full-range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C	1.1915	1.195	1.1977	V	1
$V_{out}$	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
$V_{out}$	Voltage reference output — user trim	1.193	—	1.197	V	1
$V_{step}$	Voltage reference trim step	—	0.5	—	mV	1
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	1
$I_{bg}$	Bandgap only current	—	—	80	$\mu A$	1
$\Delta V_{LOAD}$	Load regulation <ul style="list-style-type: none"> <li>current = <math>\pm 1.0</math> mA</li> </ul>	—	200	—	$\mu V$	1, 2
$T_{stup}$	Buffer startup time	—	—	100	$\mu s$	—
$V_{vdrift}$	Voltage drift ( $V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 33. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	50	$^{\circ}C$	—

**Table 34. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	1.173	1.225	V	—

## 3.6 Timers

See [General switching specifications](#).

## 3.7 Communication interfaces

### 3.7.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit [usb.org](http://usb.org).

#### NOTE

The MCGFLLCLK and IRC48M do not meet the USB jitter specifications for certification for Host mode operation.

### 3.7.2 USB DCD electrical specifications

Table 35. USB0 DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DP_SRC</sub>	USB_DP source voltage (up to 250 $\mu$ A)	0.5	—	0.7	V
V <sub>LGC</sub>	Threshold voltage for logic high	0.8	—	2.0	V
I <sub>DP_SRC</sub>	USB_DP source current	7	10	13	$\mu$ A
I <sub>DM_SINK</sub>	USB_DM sink current	50	100	150	$\mu$ A
R <sub>DM_DWN</sub>	D- pulldown resistance for data pin contact detect	14.25	—	24.8	k $\Omega$
V <sub>DAT_REF</sub>	Data detect voltage	0.25	0.33	0.4	V

### 3.7.3 USB VREG electrical specifications

Table 36. USB VREG electrical specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I <sub>DDon</sub>	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	$\mu$ A	
I <sub>DDstby</sub>	Quiescent current — Standby mode, load current equal zero	—	1.1	10	$\mu$ A	
I <sub>DDoff</sub>	Quiescent current — Shutdown mode	—	650	—	nA	
		—	—	4	$\mu$ A	
I <sub>LOADrun</sub>	Maximum load current — Run mode	—	—	120	mA	
I <sub>LOADstby</sub>	Maximum load current — Standby mode	—	—	1	mA	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (VREGIN) > 3.6 V					

Table continues on the next page...

**Table 36. USB VREG electrical specifications (continued)**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>Run mode</li> <li>Standby mode</li> </ul>	3 2.1	3.3 2.8	3.6 3.6	V V	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C <sub>OUT</sub>	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I <sub>LIM</sub>	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I<sub>Load</sub>.

### 3.7.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 37. Master mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t <sub>BUS</sub>	—	ns	
DS2	DSPI_SCK output high/low time	(t <sub>SCK</sub> /2) – 2	(t <sub>SCK</sub> /2) + 2	ns	
DS3	DSPI_PCS <sub>n</sub> valid to DSPI_SCK delay	(t <sub>BUS</sub> x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS <sub>n</sub> invalid delay	(t <sub>BUS</sub> x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].

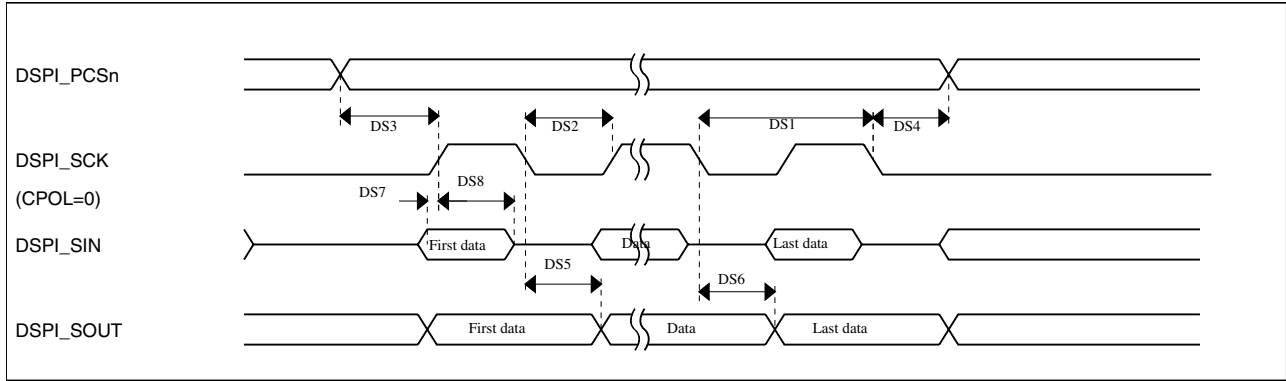


Figure 17. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI\_SS}$ active to DSPI_SOUT driven	—	20	ns
DS16	$\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven	—	20	ns

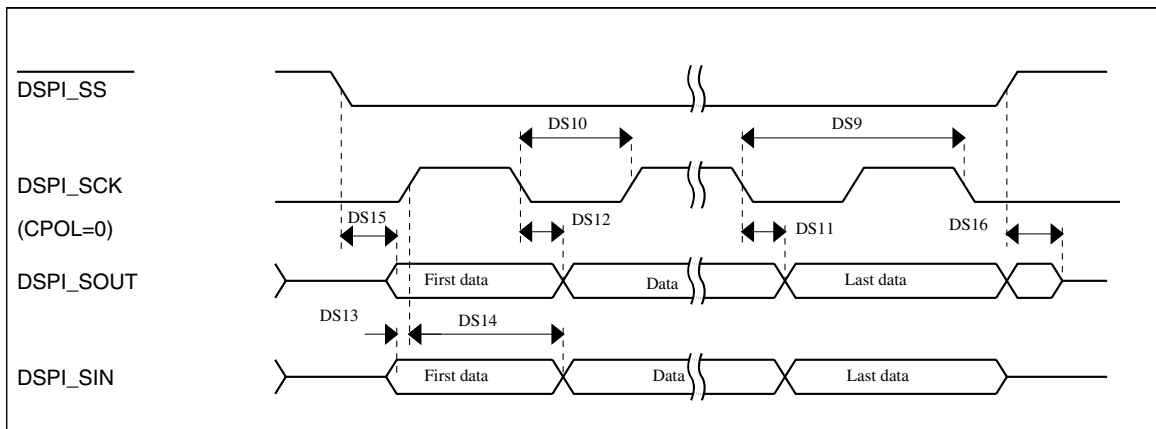


Figure 18. DSPI classic SPI timing — slave mode

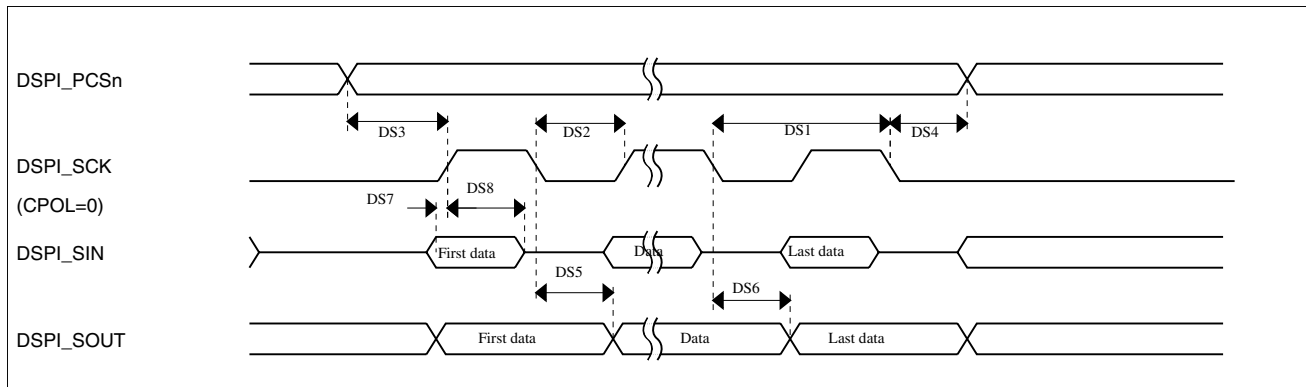
### 3.7.5 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 39. Master mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 2$	$(t_{SCK/2}) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

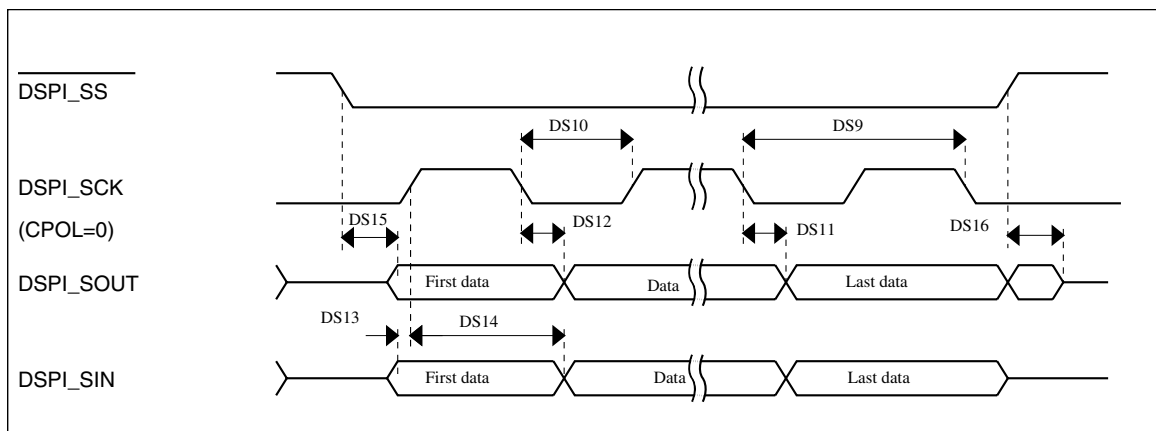
1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 19. DSPI classic SPI timing — master mode**

**Table 40. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK/2}) - 2$	$(t_{SCK/2}) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	28.3	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI\_SS}$ active to DSPI_SOUT driven	—	27	ns
DS16	$\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven	—	27	ns


**Figure 20. DSPI classic SPI timing — slave mode**

### 3.7.6 Inter-Integrated Circuit Interface (I<sup>2</sup>C) timing

**Table 41. I<sup>2</sup>C timing**

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	$f_{SCL}$	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD}; STA$	4	—	0.6	—	$\mu s$
LOW period of the SCL clock	$t_{LOW}$	4.7	—	1.3	—	$\mu s$
HIGH period of the SCL clock	$t_{HIGH}$	4	—	0.6	—	$\mu s$
Set-up time for a repeated START condition	$t_{SU}; STA$	4.7	—	0.6	—	$\mu s$

Table continues on the next page...

**Table 41. I<sup>2</sup>C timing (continued)**

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Data hold time for I <sup>2</sup> C bus devices	t <sub>HD</sub> ; DAT	0 <sup>1</sup>	3.45 <sup>2</sup>	0 <sup>3</sup>	0.9 <sup>1</sup>	μs
Data set-up time	t <sub>SU</sub> ; DAT	250 <sup>4</sup>	—	100 <sup>25</sup>	—	ns
Rise time of SDA and SCL signals	t <sub>r</sub>	—	1000	20 + 0.1C <sub>b</sub> <sup>6</sup>	300	ns
Fall time of SDA and SCL signals	t <sub>f</sub>	—	300	20 + 0.1C <sub>b</sub> <sup>5</sup>	300	ns
Set-up time for STOP condition	t <sub>SU</sub> ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t <sub>BUF</sub>	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t <sub>SP</sub>	N/A	N/A	0	50	ns

1. The master mode I<sup>2</sup>C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum t<sub>HD</sub>; DAT must be met only if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I<sup>2</sup>C bus device can be used in a Standard mode I<sup>2</sup>C bus system, but the requirement t<sub>SU</sub>; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t<sub>rmax</sub> + t<sub>SU</sub>; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I<sup>2</sup>C bus specification) before the SCL line is released.
6. C<sub>b</sub> = total capacitance of the one bus line in pF.

**Table 42. I<sup>2</sup>C 1MHz timing**

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f <sub>SCL</sub>	0	1	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t <sub>HD</sub> ; STA	0.26	—	μs
LOW period of the SCL clock	t <sub>LOW</sub>	0.5	—	μs
HIGH period of the SCL clock	t <sub>HIGH</sub>	0.26	—	μs
Set-up time for a repeated START condition	t <sub>SU</sub> ; STA	0.26	—	μs
Data hold time for I <sup>2</sup> C bus devices	t <sub>HD</sub> ; DAT	0	—	μs
Data set-up time	t <sub>SU</sub> ; DAT	50	—	ns
Rise time of SDA and SCL signals	t <sub>r</sub>	20 + 0.1C <sub>b</sub> <sup>1</sup>	120	ns
Fall time of SDA and SCL signals	t <sub>f</sub>	20 + 0.1C <sub>b</sub> <sup>2</sup>	120	ns
Set-up time for STOP condition	t <sub>SU</sub> ; STO	0.26	—	μs
Bus free time between STOP and START condition	t <sub>BUF</sub>	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t <sub>SP</sub>	0	50	ns

1. C<sub>b</sub> = total capacitance of the one bus line in pF.
2. A Fast mode I<sup>2</sup>C bus device can be used in a Standard mode I<sup>2</sup>C bus system, but the requirement t<sub>SU</sub>; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t<sub>rmax</sub> + t<sub>SU</sub>; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I<sup>2</sup>C bus specification) before the SCL line is released.



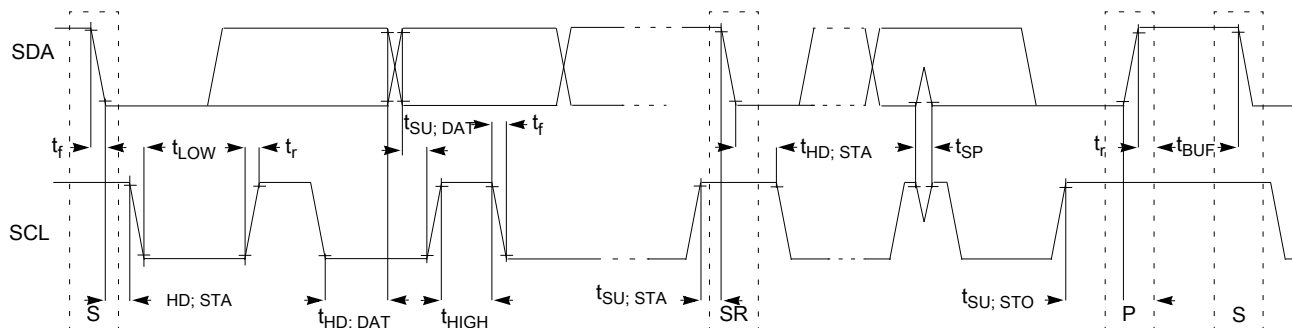


Figure 21. Timing definition for fast and standard mode devices on the I<sup>2</sup>C bus

### 3.7.7 UART switching specifications

See [General switching specifications](#).

### 3.7.8 I<sup>2</sup>S switching specifications

This section provides the AC timings for the I<sup>2</sup>S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S\_BCLK) and/or the frame sync (I2S\_FS) shown in the figures below.

Table 43. I<sup>2</sup>S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	80	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	0	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	18	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

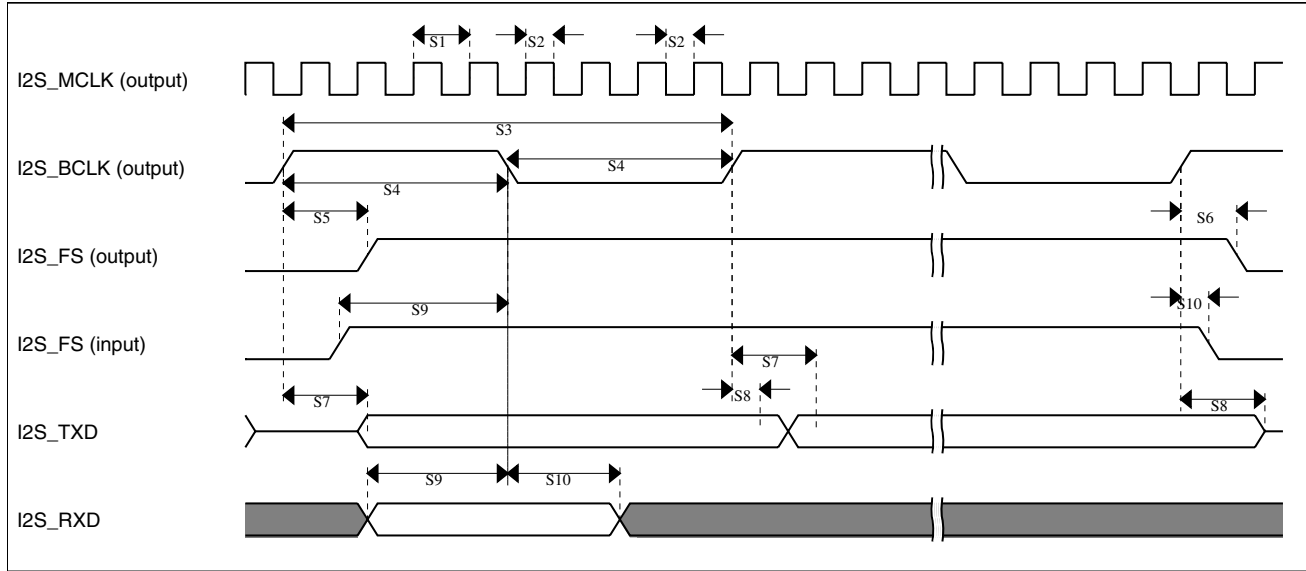


Figure 22. I<sup>2</sup>S timing — master mode

Table 44. I<sup>2</sup>S slave mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	80	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	2	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>		25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

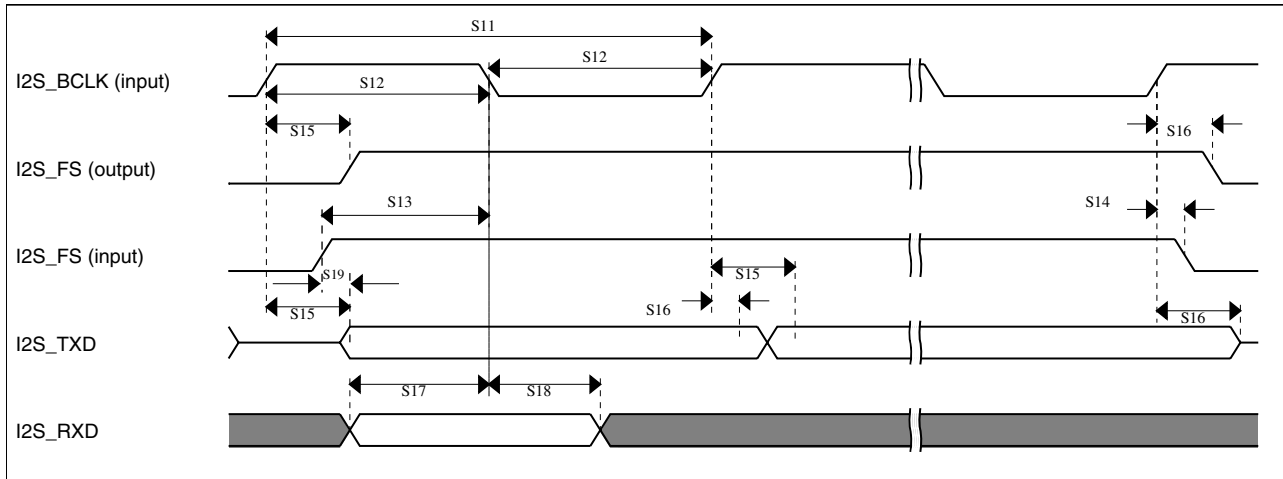


Figure 23. I<sup>2</sup>S timing — slave modes

### 3.7.8.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 45. I2S/SAI master mode timing (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	16.2	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-0.5	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	17	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

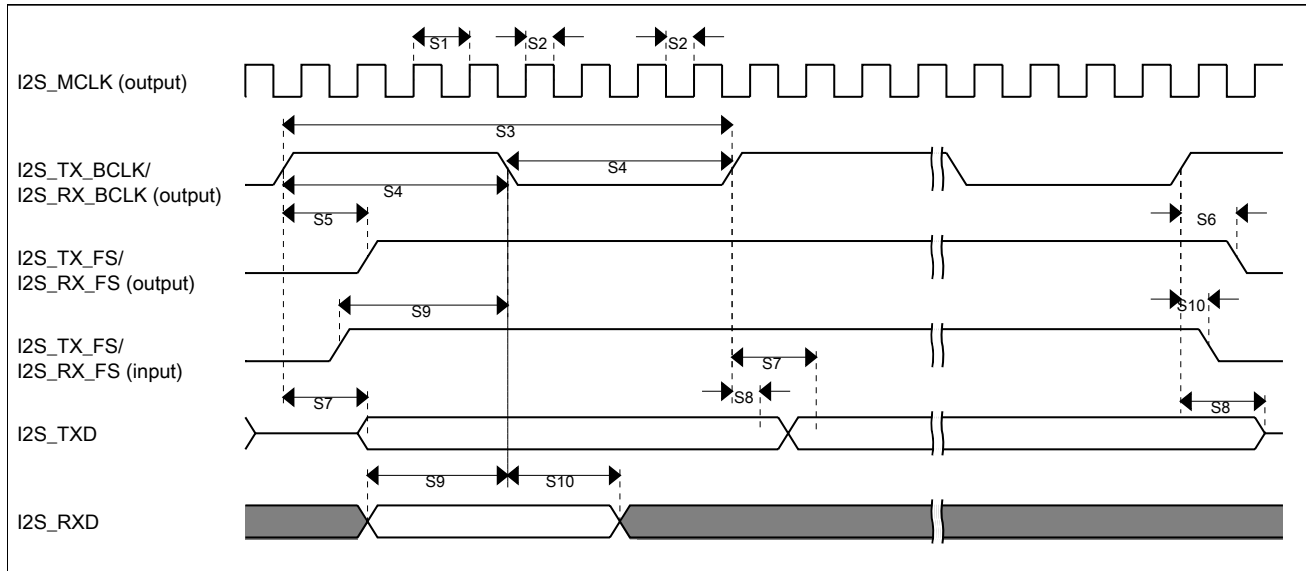


Figure 24. I2S/SAI timing — master modes

Table 46. I2S/SAI slave mode timing (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	26.9	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	26.6	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

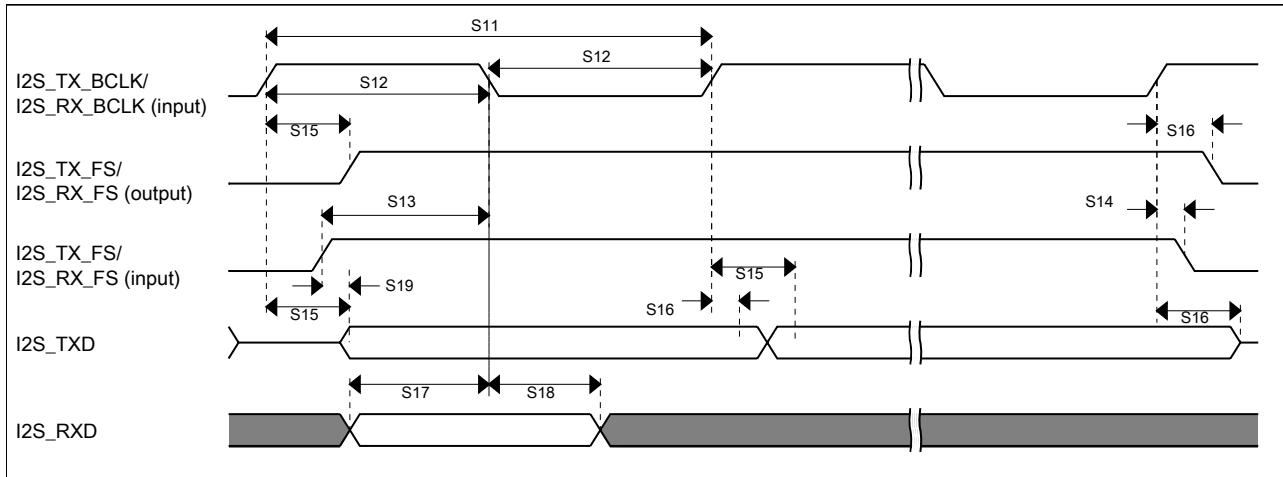


Figure 25. I2S/SAI timing — slave modes

### 3.7.8.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 47. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

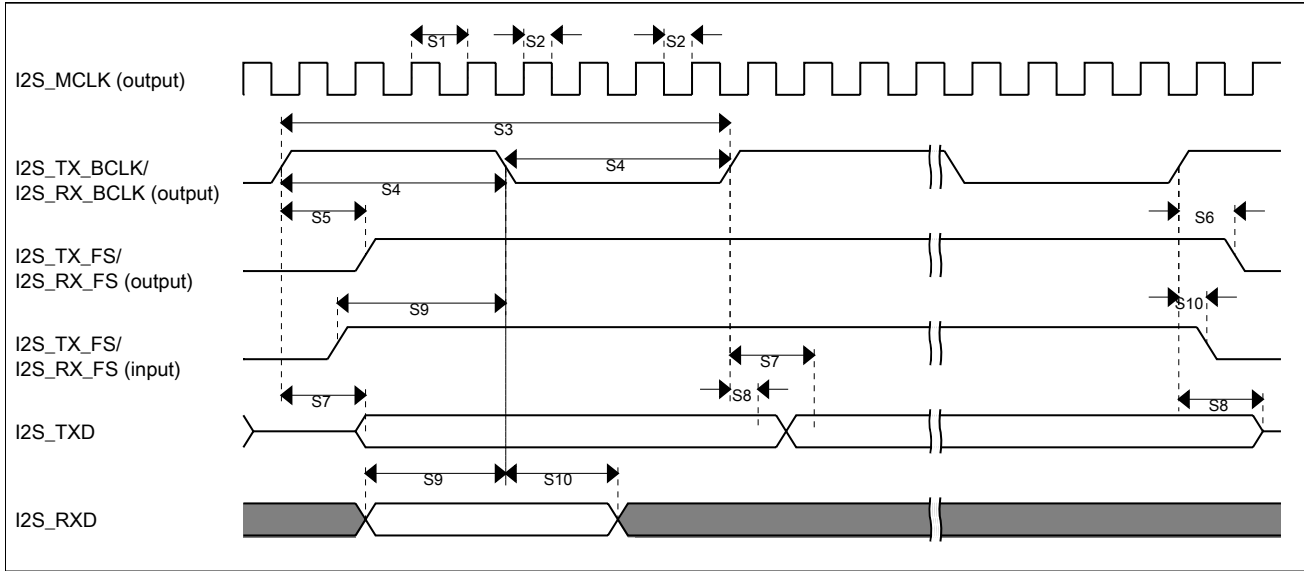


Figure 26. I2S/SAI timing — master modes

Table 48. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	5	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	56.5	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

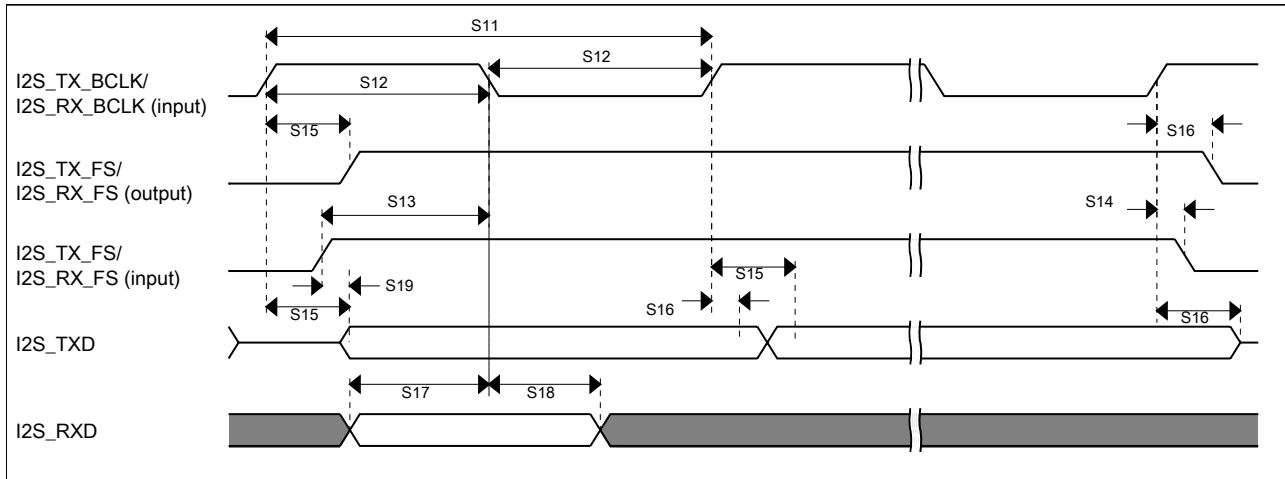


Figure 27. I2S/SAI timing — slave modes

## 4 Dimensions

### 4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
121-pin XFBGA	98ASA00595D

## 5 Pinout

### 5.1 K24 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

### Warning

The SIM\_SOPT2[CLKOUTSEL] field must be configured to select a valid clock output before enabling the CLKOUT pin function.

121 XFB GA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX			I2C1_SDA	RTC_CLKOUT	
E3	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			I2C1_SCL	SPI1_SIN	
E2	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b					
F4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b				SPI1_SOUT	
E7	VDD	VDD	VDD								
F7	VSS	VSS	VSS								
H7	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX					
G4	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX			FTM3_CH0		
E6	VDDIO_E	VDDIO_E	VDDIO_E								
G7	VSS	VSS	VSS								
F3	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		FTM3_CH1	USB_SOF_OUT	
E6	VDD	VDD	VDD								
G7	VSS	VSS	VSS								
L6	VSS	VSS	VSS								
F1	USB0_DP	USB0_DP	USB0_DP								
F2	USB0_DM	USB0_DM	USB0_DM								
G1	VOUT33	VOUT33	VOUT33								
G2	VREGIN	VREGIN	VREGIN								
H1	ADC0_DP1	ADC0_DP1	ADC0_DP1								
H2	ADC0_DM1	ADC0_DM1	ADC0_DM1								
J1	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2								
J2	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2								
K1	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3								
K2	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3								
L1	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3								
L2	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3								



121 XFB GA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
F5	VDDA	VDDA	VDDA								
G5	VREFH	VREFH	VREFH								
G6	VREFL	VREFL	VREFL								
F6	VSSA	VSSA	VSSA								
J3	ADC1_SE16/ ADC0_SE22	ADC1_SE16/ ADC0_SE22	ADC1_SE16/ ADC0_SE22								
H3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								
L3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
K5	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
K4	CMP0_IN4/ ADC1_SE23	CMP0_IN4/ ADC1_SE23	CMP0_IN4/ ADC1_SE23								
L7	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
L4	XTAL32	XTAL32	XTAL32								
L5	EXTAL32	EXTAL32	EXTAL32								
K6	VBAT	VBAT	VBAT								
L10	VDD	VDD	VDD								
K10	VSS	VSS	VSS								
H5	PTE24	ADC0_SE17	ADC0_SE17	PTE24		UART4_TX		I2C0_SCL	EWM_OUT_b		
J5	PTE25	ADC0_SE18	ADC0_SE18	PTE25		UART4_RX		I2C0_SDA	EWM_IN		
H6	PTE26	DISABLED		PTE26		UART4_CTS_ b			RTC_ CLKOUT	USB_CLKIN	
J6	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
H8	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
J7	PTA2	JTAG_TDO/ TRACE_ SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
H9	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
J8	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
K7	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2			I2S0_TX_ BCLK	JTAG_TRST_ b	
E5	VDD	VDD	VDD								



## Pinout

121 XFB GA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G3	VSS	VSS	VSS								
J9	PTA10	DISABLED		PTA10		FTM2_CH0			FTM2_QD_PHA		
J4	PTA11	DISABLED		PTA11		FTM2_CH1		I2C2_SDA	FTM2_QD_PHB		
K8	PTA12	DISABLED		PTA12		FTM1_CH0		I2C2_SCL	I2S0_TXD0	FTM1_QD_PHA	
L8	PTA13/ LLWU_P4	DISABLED		PTA13/ LLWU_P4		FTM1_CH1		I2C2_SDA	I2S0_TX_FS	FTM1_QD_PHB	
K9	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX		I2C2_SCL	I2S0_RX_BCLK	I2S0_TXD1	
L9	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
J10	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b			I2S0_RX_FS	I2S0_RXD1	
H10	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		
L10	VDD	VDD	VDD								
K10	VSS	VSS	VSS								
L11	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
K11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
J11	RESET_b	RESET_b	RESET_b								
H11	PTA29	DISABLED		PTA29							
G11	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8	ADC0_SE8/ ADC1_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA		
G10	PTB1	ADC0_SE9/ ADC1_SE9	ADC0_SE9/ ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
G9	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
G8	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b			FTM0_FLT0		
K10	VSS	VSS	VSS								
L10	VDD	VDD	VDD								
F11	PTB6	ADC1_SE12	ADC1_SE12	PTB6							
E11	PTB7	ADC1_SE13	ADC1_SE13	PTB7							
D11	PTB8	DISABLED		PTB8		UART3_RTS_b					
E10	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_CTS_b					
D10	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1		
C10	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2		
B11	PTB12	DISABLED		PTB12	UART3_RTS_b	FTM1_CH0	FTM0_CH4		FTM1_QD_PHA		



121 XFB GA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C11	PTB13	DISABLED		PTB13	UART3_CTS_b	FTM1_CH1	FTM0_CH5		FTM1_QD_PHB		
K10	VSS	VSS	VSS								
L10	VDD	VDD	VDD								
B10	PTB16	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0		EWM_IN		
E9	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1		EWM_OUT_b		
D9	PTB18	DISABLED		PTB18		FTM2_CH0	I2S0_TX_BCLK		FTM2_QD_PHA		
C9	PTB19	DISABLED		PTB19		FTM2_CH1	I2S0_TX_FS		FTM2_QD_PHB		
F10	PTB20	DISABLED		PTB20	SPI2_PCS0				CMP0_OUT		
F9	PTB21	DISABLED		PTB21	SPI2_SCK				CMP1_OUT		
F8	PTB22	DISABLED		PTB22	SPI2_SOUT						
E8	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5					
B9	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG	USB_SOF_OUT		I2S0_TXD1		
D8	PTC1/ LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
C8	PTC2	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
B8	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
K10	VSS	VSS	VSS								
L10	VDD	VDD	VDD								
A8	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
D7	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	FTM0_CH2	
C7	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
B7	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS				
A7	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK				
D6	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_BCLK		FTM2_FLT0		
C6	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS				
C5	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1				
B6	PTC12	DISABLED		PTC12		UART4_RTS_b	FTM_CLKIN0		FTM3_FLT0		
A6	PTC13	DISABLED		PTC13		UART4_CTS_b	FTM_CLKIN1				
A5	PTC14	DISABLED		PTC14		UART4_RX					



## Pinout

121 XFB GA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B5	PTC15	DISABLED		PTC15		UART4_TX					
K10	VSS	VSS	VSS								
L10	VDD	VDD	VDD								
D5	PTC16	DISABLED		PTC16		UART3_RX					
C4	PTC17	DISABLED		PTC17		UART3_TX					
B4	PTC18	DISABLED		PTC18		UART3_RTS_b					
A4	PTC19	DISABLED		PTC19		UART3_CTS_b					
D4	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0				
D3	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1				
C3	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2			I2C0_SCL	
B3	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3			I2C0_SDA	
A3	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN	SPI1_PCS0	
A2	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5		EWM_OUT_b	SPI1_SCK	
B2	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0	SPI1_SOUT	
K10	VSS	VSS	VSS								
L10	VDD	VDD	VDD								
A1	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1	SPI1_SIN	
A10	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX					
A9	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX					
B1	PTD10	DISABLED		PTD10		UART5_RTS_b					
C2	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b					
C1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0					
D2	PTD13	DISABLED		PTD13	SPI2_SOUT						
D1	PTD14	DISABLED		PTD14	SPI2_SIN						
E1	PTD15	DISABLED		PTD15	SPI2_PCS1						
A11	NC	NC	NC								
K3	NC	NC	NC								
H4	NC	NC	NC								

## 5.2 Unused analog interfaces

**Table 49. Unused analog interfaces**

Module name	Pins	Recommendation if unused
ADC	ADC0_SE8, ADC0_SE9, ADC1_SE8, ADC1_SE9	Ground
USB	VREGIN, VOUT33	Float
	USB0_DM, USB0_DP	Float
RTC	VBAT	Float
	EXTAL32	VSS
	XTAL32	Float
	RTC_WAKEUP_B	Float

## 5.3 K24 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	PTC19	PTC14	PTC13	PTC8	PTC4/ LLWU_P8	PTD9	PTD8	NC	A
B	PTD10	PTD6/ LLWU_P15	PTD3	PTC18	PTC15	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	PTB12	B
C	PTD12	PTD11	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	PTB13	C
D	PTD14	PTD13	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	PTB8	D
E	PTD15	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	VDD	VDDIO_E VDD	VDD	PTB23	PTB17	PTB9	PTB7	E
F	USB0_DP	USB0_DM	PTE6	PTE3	VDDA	VSSA	VSS	PTB22	PTB21	PTB20	PTB6	F
G	VOUT33	VREGIN	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	ADC0_DP1	ADC0_DM1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	NC	PTE24	PTE26	PTE4/ LLWU_P2	PTA1	PTA3	PTA17	PTA29	H
J	ADC1_DP1/ ADC0_DP2	ADC1_DM1/ ADC0_DM2	ADC1_SE16/ ADC0_SE22	PTA11	PTE25	PTA0	PTA2	PTA4/ LLWU_P3	PTA10	PTA16	RESET_b	J
K	ADC0_DP0/ ADC1_DP3	ADC0_DM0/ ADC1_DM3	NC	CMP0_IN4/ ADC1_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	ADC1_DP0/ ADC0_DP3	ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	XTAL32	EXTAL32	VSS	RTC_ WAKEUP_B	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 28. 121 XFBGA Pinout Diagram

## 5.4 Ordering parts

### 5.4.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers:

PK24 and MK24

## 5.5 Part identification

### 5.5.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 5.5.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

### 5.5.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> <li>SC = Fully qualified, special part</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K24</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>32 = 32 KB</li> <li>64 = 64 KB</li> <li>128 = 128 KB</li> <li>256 = 256 KB</li> <li>512 = 512 KB</li> <li>1M0 = 1 MB</li> <li>2M0 = 2 MB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>Z = Initial</li> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> <li>C = -40 to 85</li> <li>U = -10 to +70 °C</li> </ul>

*Table continues on the next page...*

Field	Description	Values
PP	Package identifier	<ul style="list-style-type: none"> <li>• FM = 32 QFN (5 mm x 5 mm)</li> <li>• FT = 48 QFN (7 mm x 7 mm)</li> <li>• LF = 48 LQFP (7 mm x 7 mm)</li> <li>• LH = 64 LQFP (10 mm x 10 mm)</li> <li>• MP = 64 MAPBGA (5 mm x 5 mm)</li> <li>• LK = 80 LQFP (12 mm x 12 mm)</li> <li>• LL = 100 LQFP (14 mm x 14 mm)</li> <li>• MC = 121 MAPBGA (8 mm x 8 mm)</li> <li>• DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm)</li> <li>• LQ = 144 LQFP (20 mm x 20 mm)</li> <li>• MD = 144 MAPBGA (13 mm x 13 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>• 5 = 50 MHz</li> <li>• 7 = 72 MHz</li> <li>• 10 = 100 MHz</li> <li>• 12 = 120 MHz</li> <li>• 15 = 150 MHz</li> <li>• 16 = 168 MHz</li> <li>• 18 = 180 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>• R = Tape and reel</li> <li>• (Blank) = Trays</li> </ul>

### 5.5.4 Example

This is an example part number:

MK24FN256VDC12

## 5.6 Terminology and guidelines

### 5.6.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 5.6.1.1 Example

This is an example of an operating requirement:



Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

## 5.6.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 5.6.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	130	μA

## 5.6.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 5.6.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

## 5.6.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

## Pinout

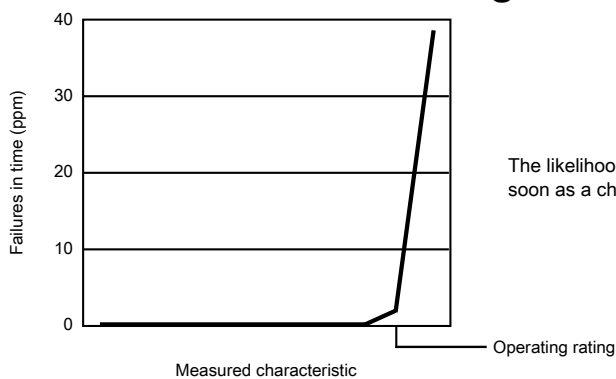
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 5.6.4.1 Example

This is an example of an operating rating:

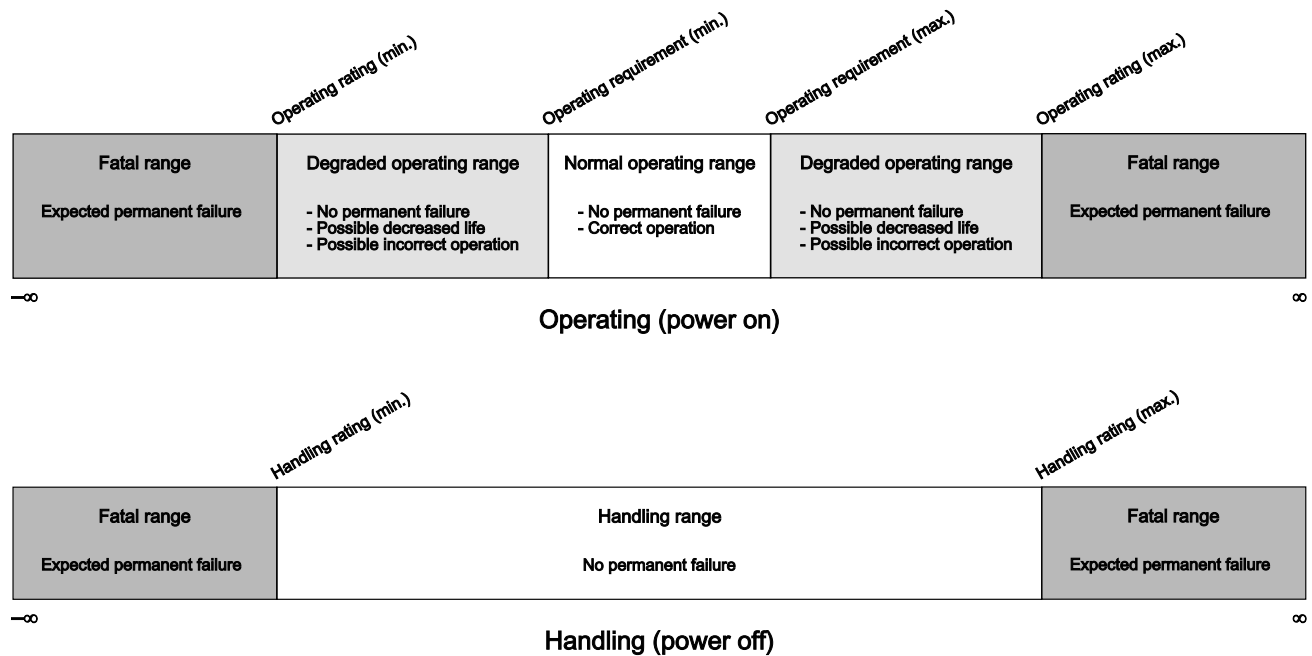
Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

### 5.6.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

## 5.6.6 Relationship between ratings and operating requirements



## 5.6.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 5.6.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

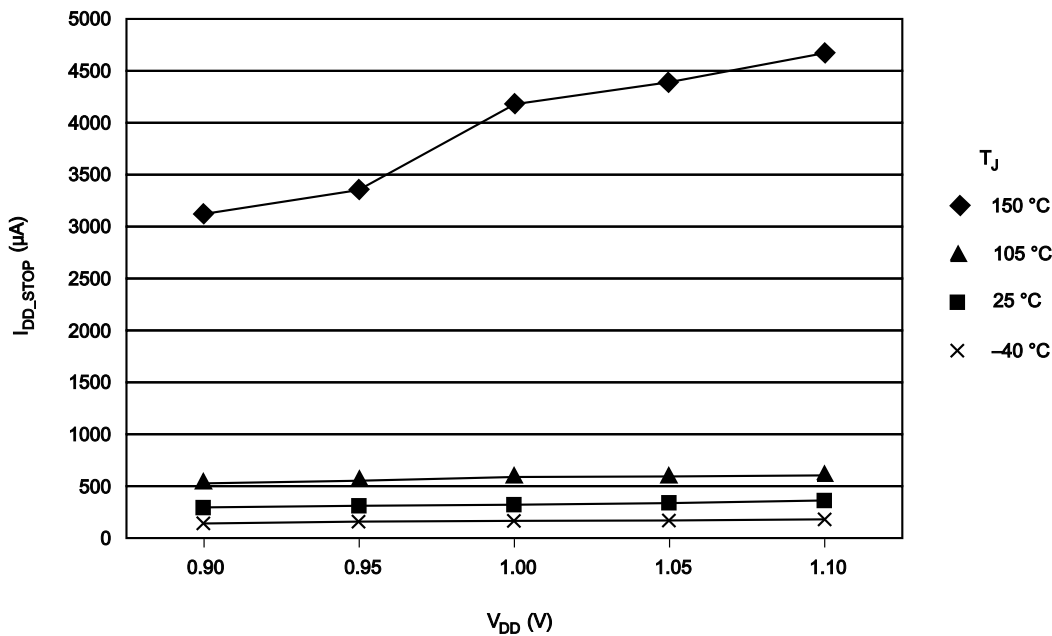
### 5.6.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu A$

### 5.6.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



### 5.6.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
$T_A$	Ambient temperature	25	$^{\circ}C$
$V_{DD}$	3.3 V supply voltage	3.3	V

## 6 Revision History

**Table 50. Revision history**

Revision number	Date	Substantial changes
1	05/2014	<ul style="list-style-type: none"> <li>• Initial NDA release</li> </ul>
2	08/2014	<ul style="list-style-type: none"> <li>• Added flashloader information to the feature list</li> <li>• Added run and static power consumption specifications</li> </ul>

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