MIC2103/4

75V Synchronous Buck Controllers Featuring Adaptive ON-Time Control

Features

- Hyper Speed Control® Architecture Enables:
  - High Delta V Operation (V_{IN} = 75V and V_{OUT} = 1.2V)
  - Any Capacitor™ Stable
- 4.5V to 75V Input Voltage
- Adjustable Output Voltage from 0.8V to 24V (Also Limited by Duty Cycle)
- 200 kHz to 600 kHz Programmable Switching Frequency
- HyperLight Load® Control (MIC2103 Only)
- Hyper Speed Control® (MIC2104 Only)
- Enable Input, Power-Good Output
- Built-In 5V Regulator for Single-Supply Operation
- Programmable Current-Limit and Fold-Back "Hiccup" Mode Short-Circuit Protection
- 5 ms Internal Soft-Start, Internal Compensation, and Thermal Shutdown
- Supports Safe Start-Up into a Pre-Biased Output
- –40°C to +125°C Junction Temperature Range
- Available in 16-Pin 3 mm x 3 mm QFN Package

Applications

- Distributed Power Systems
- Networking/Telecom Infrastructure
- Printers, Scanners, Graphic Cards, and Video Cards

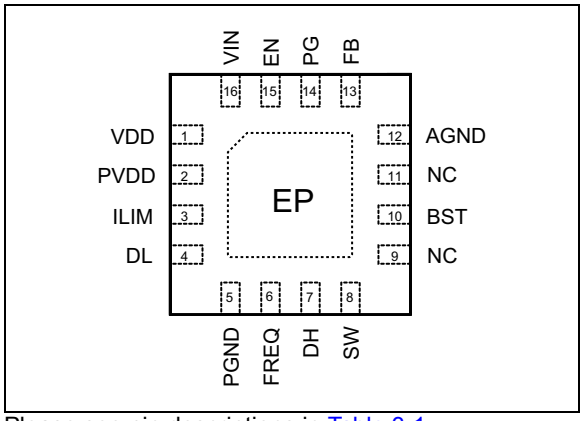
General Description

The MIC2103/4 are constant-frequency, synchronous buck controllers that feature a unique adaptive ON-time control architecture. The MIC2103/4 operates over an input supply range from 4.5V to 75V and can be used to supply up to 15A of output current. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of ±1%. The device operates with programmable switching frequency from 200 kHz to 600 kHz.

The HyperLight Load® architecture provides the same high-efficiency and ultra-fast transient response as the Hyper Speed Control architecture under medium to heavy loads, but also maintains high efficiency under light load conditions by transitioning to variable frequency, discontinuous-mode operation.

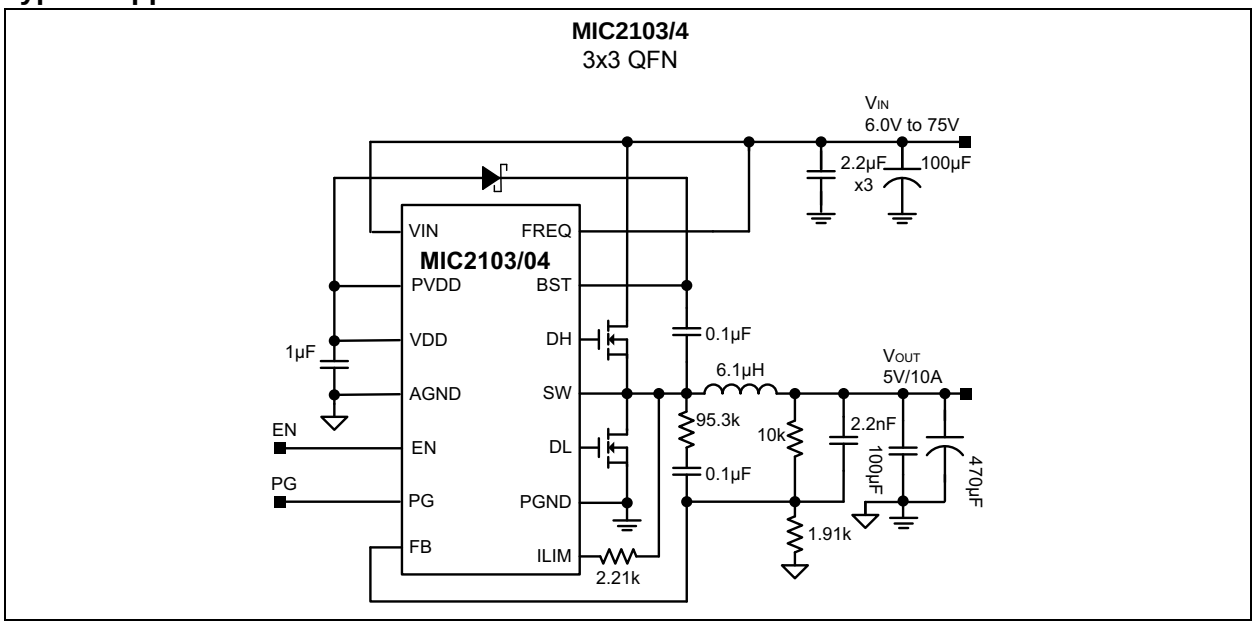
The MIC2103/4 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, fold-back current-limit, "hiccup" mode short-circuit protection, and thermal shutdown.

Package Type

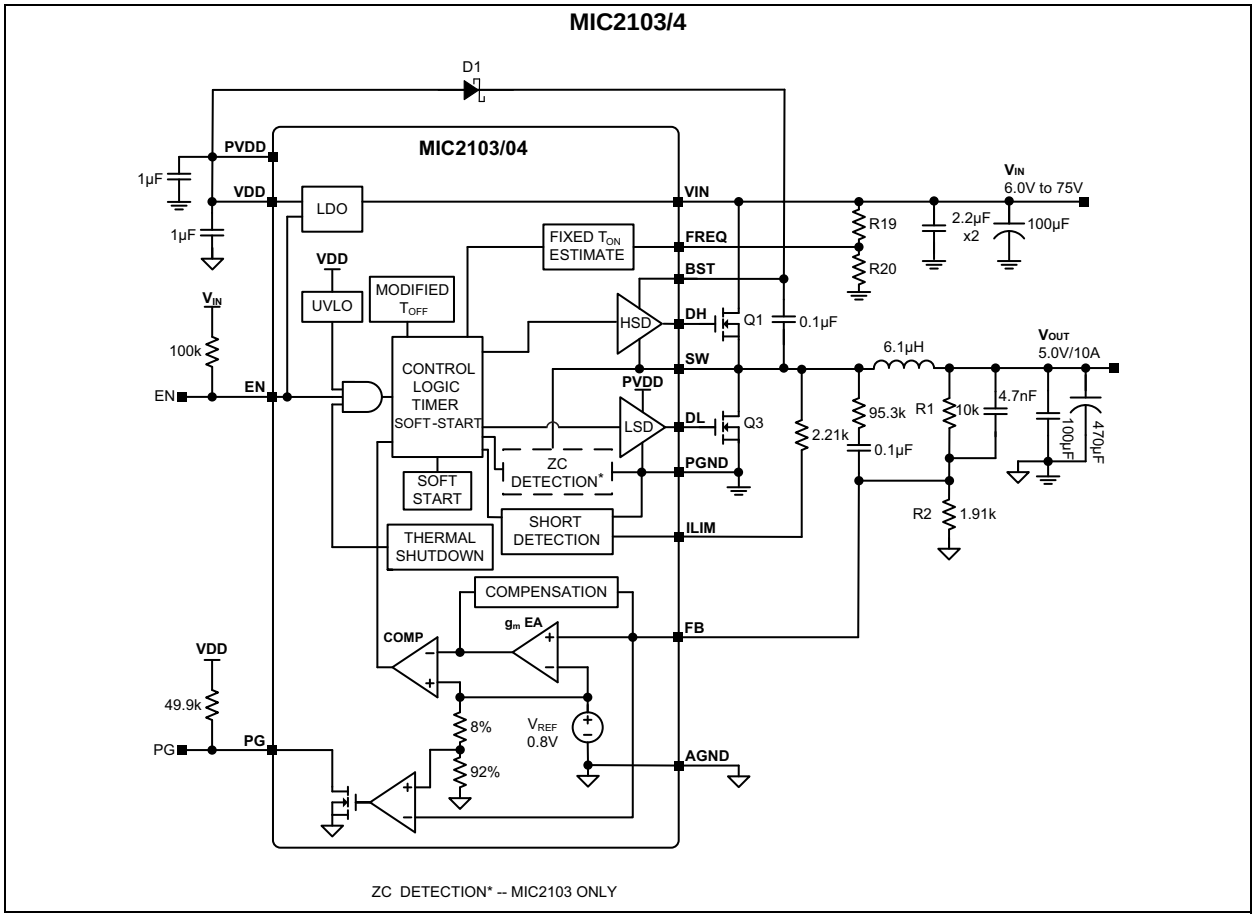


Please see pin descriptions in Table 3-1.

Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} ..... –0.3V to +76V
V_{DD}, V_{PVDD} ..... –0.3V to +6V
V_{FREQ}, V_{ILIM}, V_{EN} ..... –0.3V to (V_{IN} + 0.3V)
V_{SW} (DC) ..... –0.3V to (V_{IN} + 0.3V)
V_{SW} (Transient <100 ns) ..... –5.0V
V_{BST} to V_{SW} ..... –0.3V to +6V
V_{BST} ..... –0.3V to +82V
V_{PG} ..... –0.3V to (V_{DD} + 0.3V)
V_{FB} ..... –0.3V to (V_{DD} + 0.3V)
PGND to AGND ..... –0.3V to +0.3V
ESD Rating ..... Note 1

Operating Ratings ‡

Supply Voltage (V_{IN}) ..... +4.5V to +75V
Enable Input (V_{EN}) ..... 0V to V_{IN}
V_{SW}, V_{FREQ}, V_{ILIM} ..... 0V to V_{IN}

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 48V, V_{OUT} = 5V, $V_{BST} - V_{SW}$ = 5V; T_A = +25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range	V_{IN}	**4.5**	—	**75**	V	Note 2
Quiescent Supply Current	I_Q	—	400	**750**	µA	MIC2103, V_{FB} = 1.5V
		—	2.1	**3**	mA	MIC2104, V_{FB} = 1.5V
Shutdown Supply Current	I_{SHDN}	—	0.1	**10**	µA	SW unconnected, V_{EN} = 0V
V_{DD} Supply						
V_{DD} Output Voltage	V_{DD}	**4.8**	5.2	**5.4**	V	V_{IN} = 7V to 75V, I_{DD} = 10 mA
V_{DD} UVLO Upper Threshold	$V_{DDUV,R}$	**3.8**	4.2	**4.6**	V	V_{DD} rising
V_{DD} UVLO Hysteresis	ΔV_{DDUV}	—	400	—	mV	—
Load Regulation	$\Delta V_{DD,LOAD}$	0.6	2	3.6	%	I_{DD} = 0 mA to 40 mA
Reference						
Feedback Reference Voltage	V_{FB}	0.792	0.8	0.808	V	T_J = 25°C (±1.0%)
		0.784	**0.8**	**0.816**		–40°C ≤ T_J ≤ +125°C (±2%)
FB Bias Current	I_{FB}	—	5	**500**	nA	V_{FB} = 0.8V
Enable Control						
EN Logic Level High	$V_{EN(HI)}$	**1.8**	—	—	V	—
EN Logic Level Low	$V_{EN(LO)}$	—	—	**0.6**	V	—
EN Hysteresis	$V_{EN(HYS)}$	—	200	—	mV	—
EN Bias Current	I_{EN}	—	23	**40**	µA	V_{EN} = 48V
Oscillator						
Switching Frequency	f_{SW}	**400**	600	**750**	kHz	$V_{FREQ} = V_{IN}$
		—	300	—		V_{FREQ} = 50%V_{IN}
Maximum Duty Cycle	D_{MAX}	—	85	—	%	—
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{FB} > 0.8V
Minimum Off-Time	$t_{OFF(MIN)}$	140	200	260	ns	—
Soft-Start						
Soft-Start Time	t_{SS}	—	5	—	ms	—
Short-Circuit Protection						
Current-Limit Threshold	V_{CL}	–30	–14	0	mV	V_{FB} = 0.79V
Short-Circuit Threshold	$V_{CL(FB)}$	–23	–7	9	mV	V_{FB} = 0V
Current-Limit Source Current	I_{CL}	60	80	100	µA	V_{FB} = 0.79V
Short-Circuit Source Current	$I_{CL(FB)}$	27	36	47	µA	V_{FB} = 0V
FET Drivers						
DH, DL Output Low Voltage	V_{LO}	—	—	**0.1**	V	I_{SINK} = 10 mA
DH, DL Output High Voltage	V_{HI}	V_{PVDD} – 0.1V or V_{BST} – 0.1V	—	—	V	I_{SOURCE} = 10 mA
DH On-Resistance, High State	$R_{ON(DHH)}$	—	2.1	**3.3**	Ω	—
DH On-Resistance, Low State	$R_{ON(DHL)}$	—	1.8	**3.3**	Ω	—
DL On-Resistance, High State	$R_{ON(DLH)}$	—	1.8	**3.3**	Ω	—

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 48V, V_{OUT} = 5V, $V_{BST} – V_{SW}$ = 5V; T_A = +25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
DL On-Resistance, Low State	$R_{ON(DLL)}$	—	1.2	**2.3**	Ω	—
SW, BST Leakage Current	I_{LEAK}	—	—	50	µA	—
Power Good						
Power Good Threshold Voltage	V_{PGTH}	**85**	90	**95**	$\%V_{OUT}$	Sweep V_{FB} from Low to High
Power Good Hysteresis	V_{PGHYS}	—	6	—	$\%V_{OUT}$	Sweep V_{FB} from High to Low
Power Good Delay Time	$t_{d(PG)}$	—	100	—	µs	Sweep V_{FB} from Low to High
Power Good Low Voltage	$V_{PG(LO)}$	—	70	**200**	mV	V_{FB} < 90% x V_{NOM}, I_{PG} = 1 mA
Thermal Protection						
Overtemperature Shutdown Threshold	T_{SD}	—	160	—	°C	T_J rising
Overtemperature Shutdown Hysteresis	$T_{SD(HYS)}$	—	4	—	°C	—

Note 1: Specification for packaged product only

2: The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH}.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Maximum Junction Temperature	—	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10s
Package Thermal Resistances						
Thermal Resistance 3x3 QFN-16Ld	θ_{JA}	—	50.8	—	°C/W	—
Thermal Resistance 3x3 QFN-16Ld	θ_{JC}	—	25.3	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

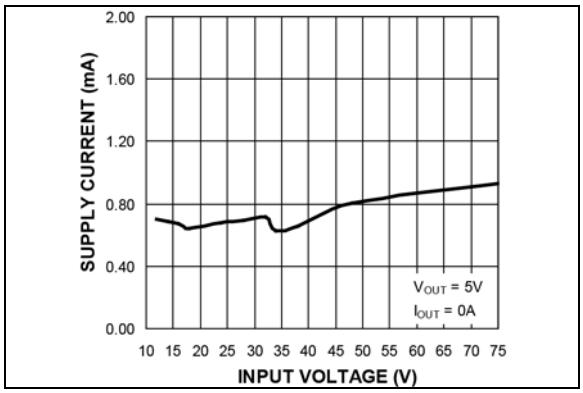


FIGURE 2-1: *V_{IN} Operating Supply Current vs. Input Voltage (MIC2103).*

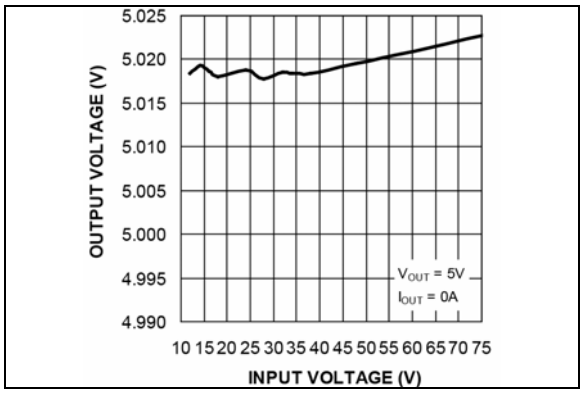


FIGURE 2-4: *Output Voltage vs. Input Voltage (MIC2103).*

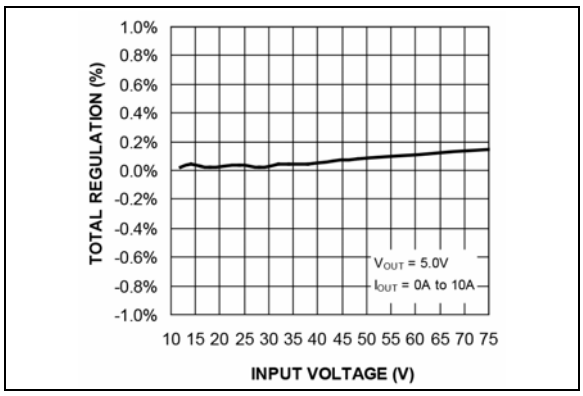


FIGURE 2-2: *Output Regulation vs. Input Voltage (MIC2103).*

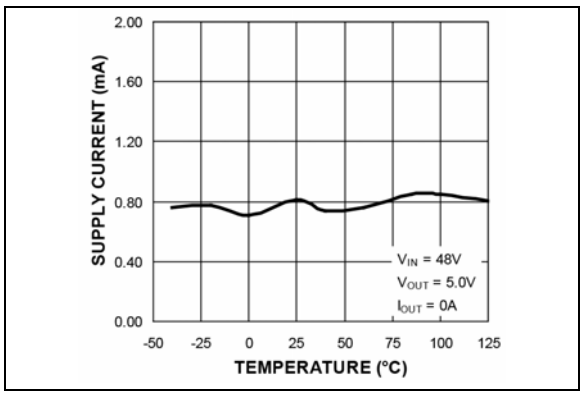


FIGURE 2-5: *V_{IN} Operating Supply Current vs. Temperature (MIC2103).*

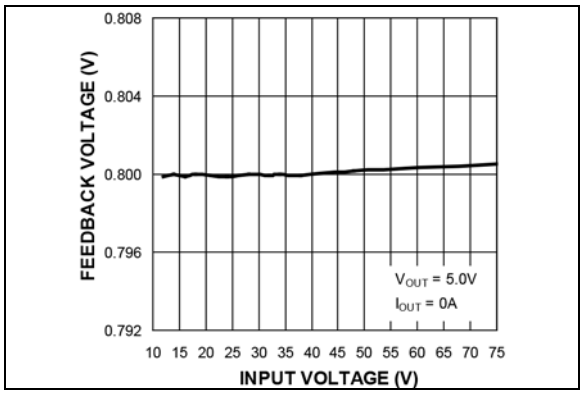


FIGURE 2-3: *Feedback Voltage vs. Input Voltage (MIC2103).*

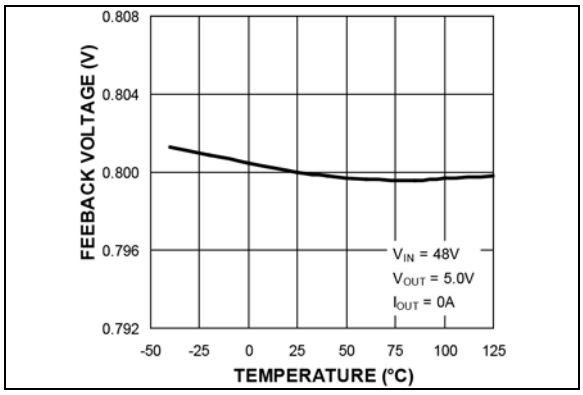


FIGURE 2-6: *Feedback Voltage vs. Temperature (MIC2103).*

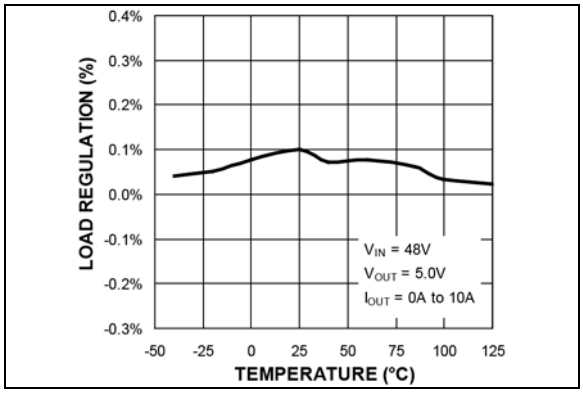


FIGURE 2-7: *Load Regulation vs. Temperature (MIC2103).*

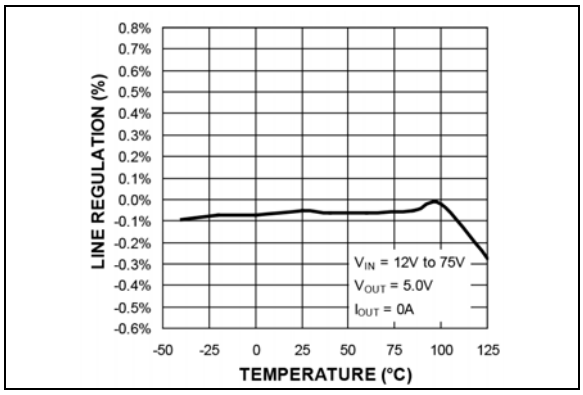


FIGURE 2-8: *Line Regulation vs. Temperature (MIC2103).*

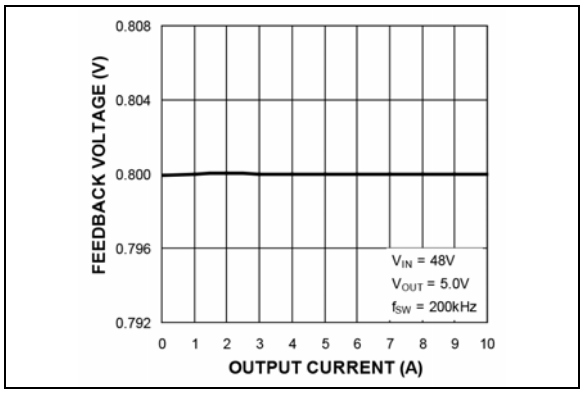


FIGURE 2-9: *Feedback Voltage vs. Output Current (MIC2103).*

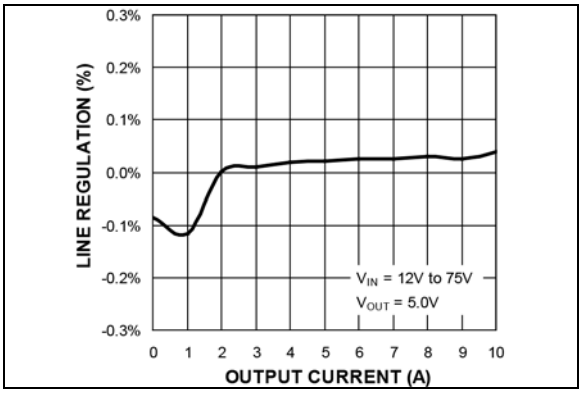


FIGURE 2-10: *Line Regulation vs. Output Current (MIC2103).*

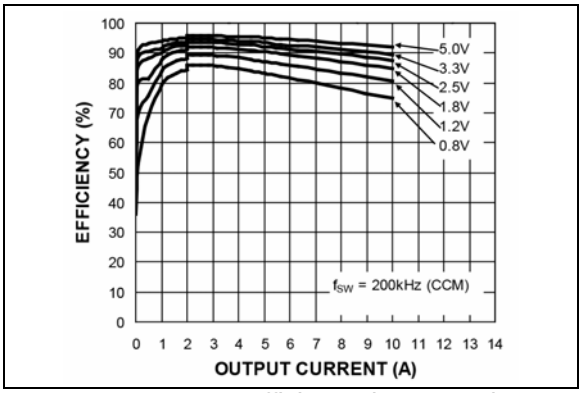


FIGURE 2-11: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC2103).*

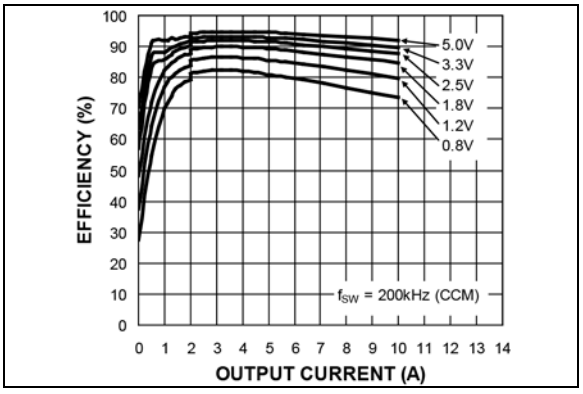


FIGURE 2-12: *Efficiency (V_{IN} = 18V) vs. Output Current (MIC2103).*

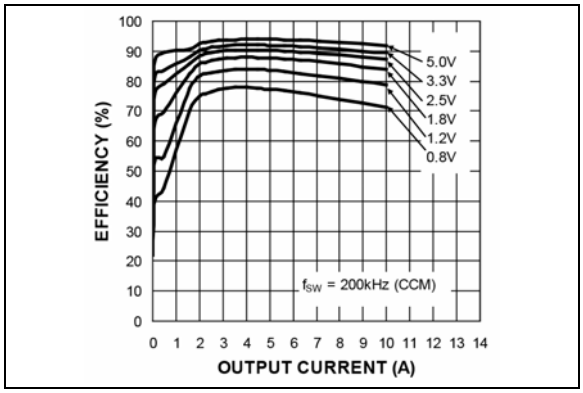


FIGURE 2-13: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC2103).*

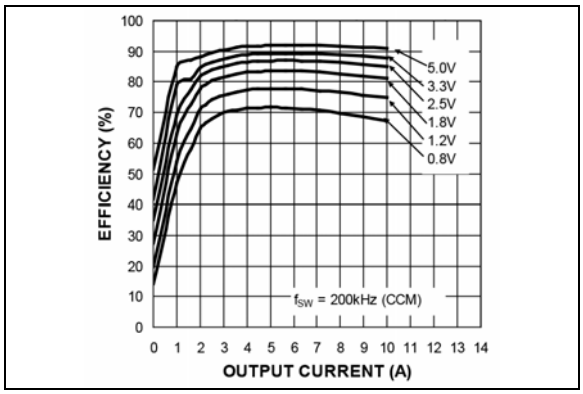


FIGURE 2-14: *Efficiency (V_{IN} = 38V) vs. Output Current (MIC2103).*

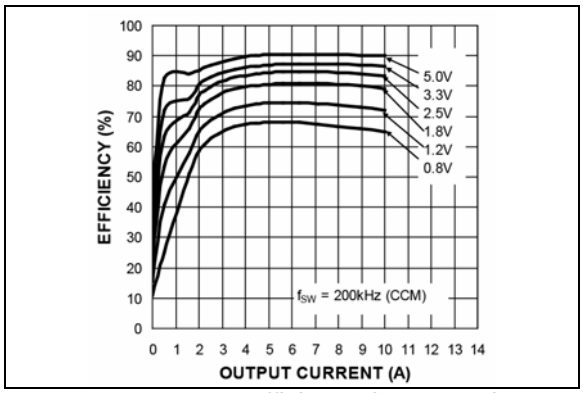


FIGURE 2-15: *Efficiency (V_{IN} = 48V) vs. Output Current (MIC2103).*

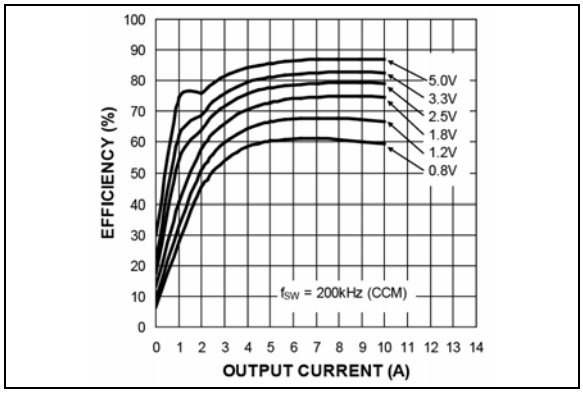


FIGURE 2-16: *Efficiency (V_{IN} = 75V) vs. Output Current (MIC2103).*

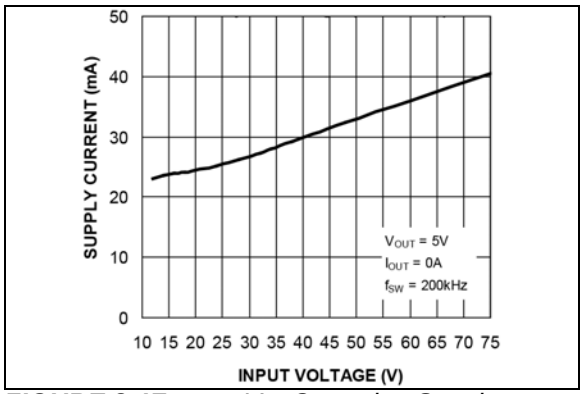


FIGURE 2-17: *V_{IN} Operating Supply Current vs. Input Voltage (MIC2104).*

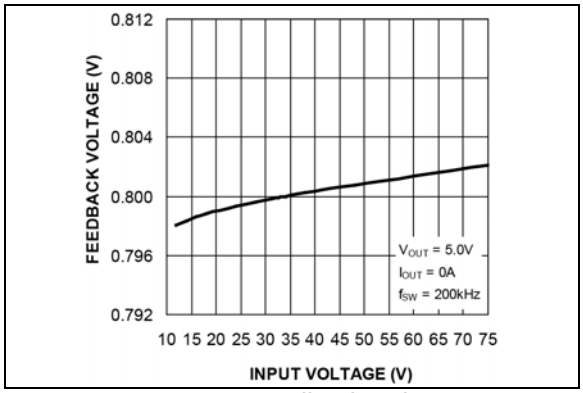


FIGURE 2-18: *Feedback Voltage vs. Input Voltage (MIC2104).*

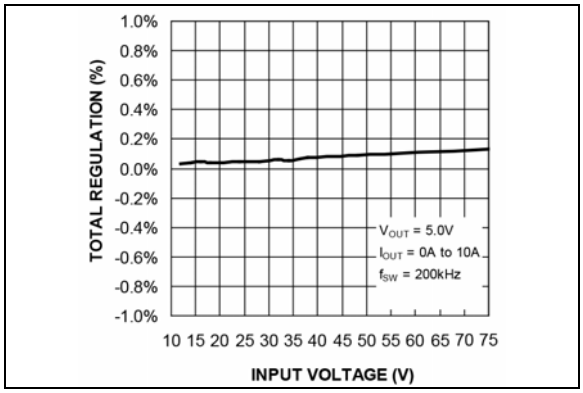


FIGURE 2-19: *Output Regulation vs. Input Voltage (MIC2104).*

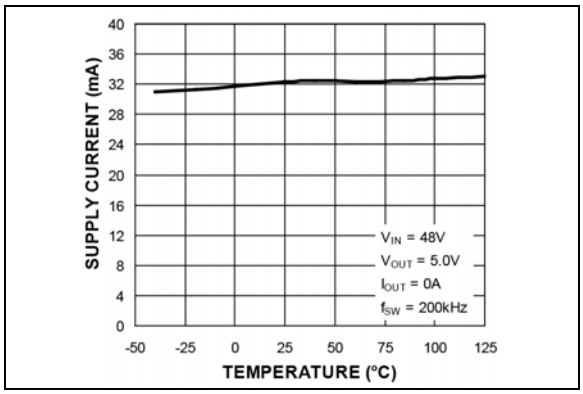


FIGURE 2-20: *V_{IN} Operating Supply Current vs. Temperature (MIC2104).*

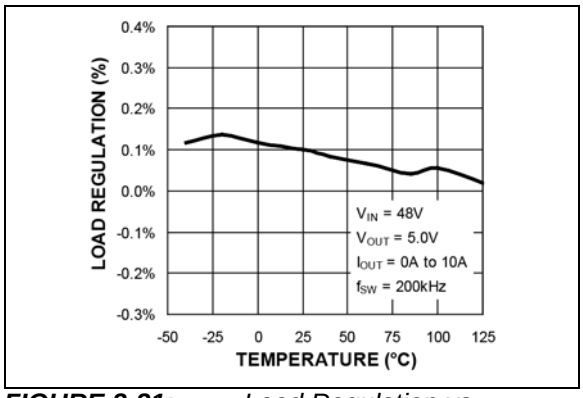


FIGURE 2-21: *Load Regulation vs. Temperature (MIC2104).*

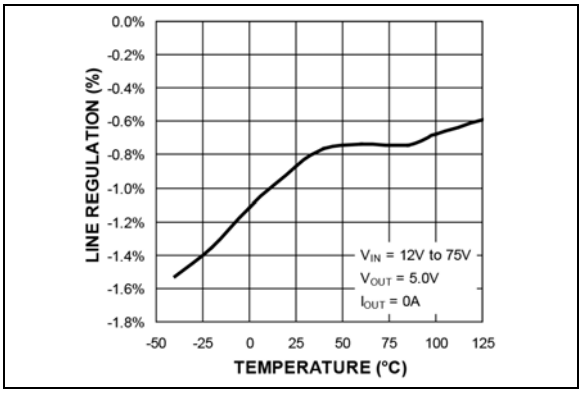


FIGURE 2-22: *Line Regulation vs. Temperature (MIC2104).*

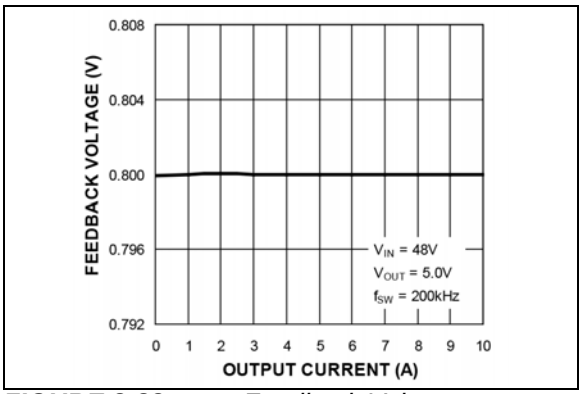


FIGURE 2-23: *Feedback Voltage vs. Output Current (MIC2104).*

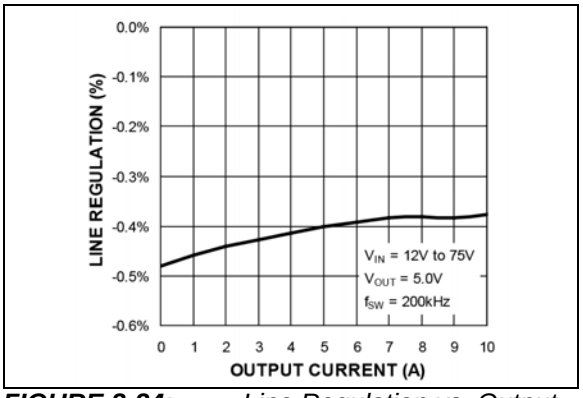


FIGURE 2-24: *Line Regulation vs. Output Current (MIC2104).*

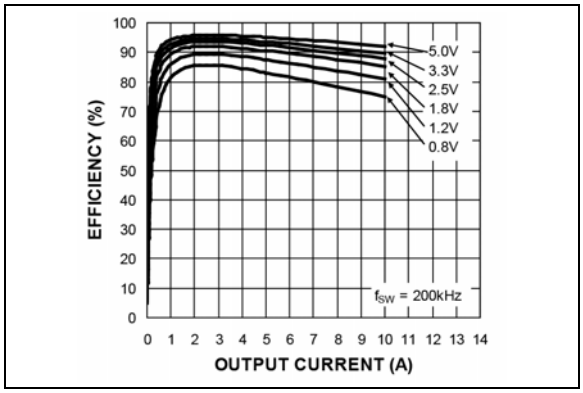


FIGURE 2-25: *Efficiency (V_{IN} = 12V) vs. Output Current (MIC2104).*

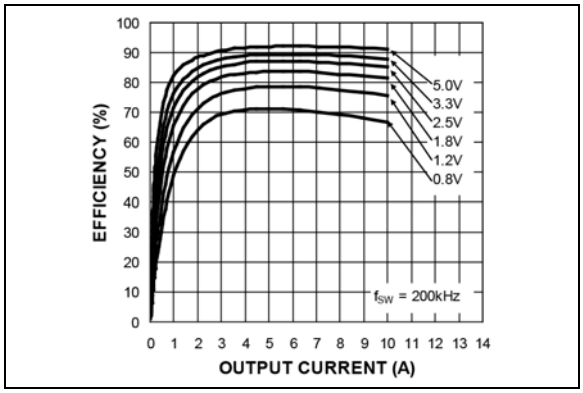


FIGURE 2-28: *Efficiency (V_{IN} = 38V) vs. Output Current (MIC2104).*

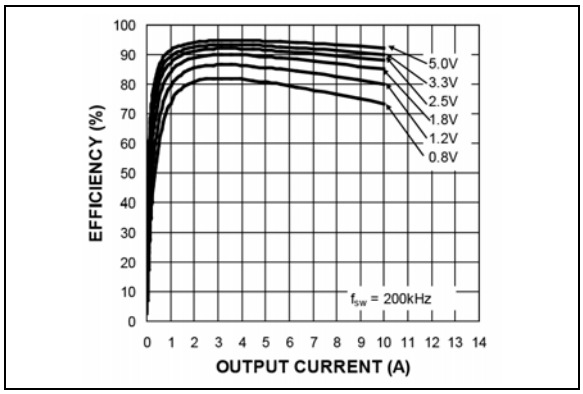


FIGURE 2-26: *Efficiency (V_{IN} = 18V) vs. Output Current (MIC2104).*

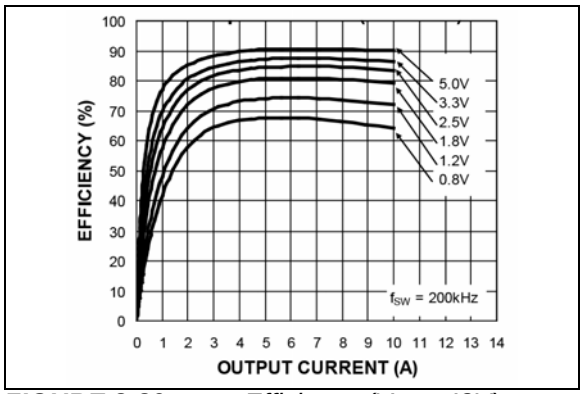


FIGURE 2-29: *Efficiency (V_{IN} = 48V) vs. Output Current (MIC2104).*

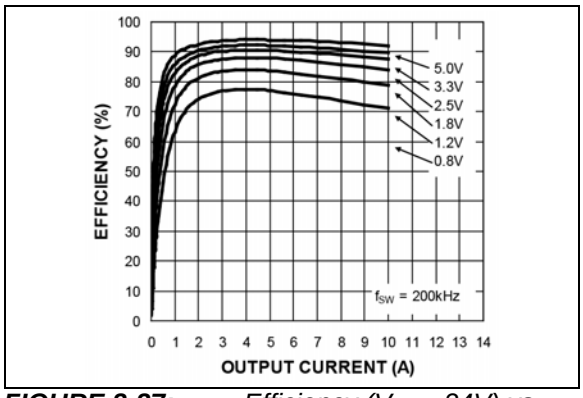


FIGURE 2-27: *Efficiency (V_{IN} = 24V) vs. Output Current (MIC2104).*

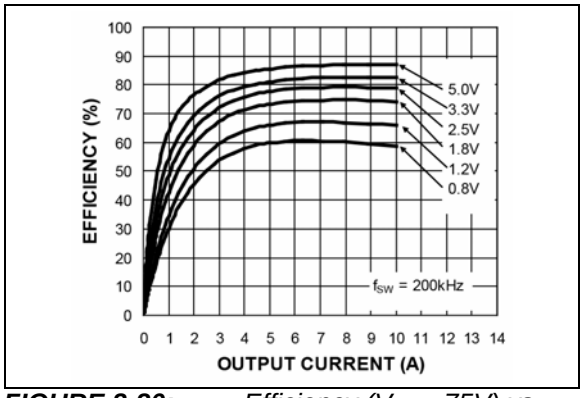


FIGURE 2-30: *Efficiency (V_{IN} = 75V) vs. Output Current (MIC2104).*

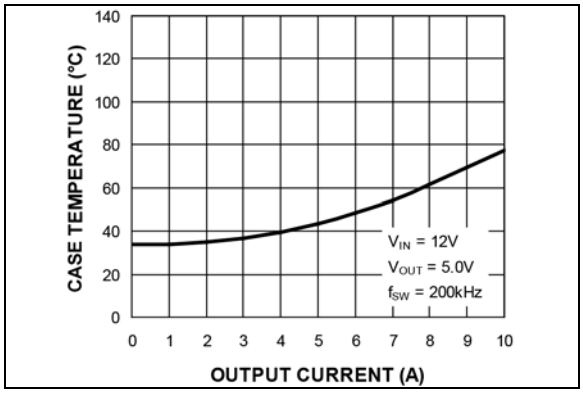


FIGURE 2-31: *Case Temperature* (V_{IN} = 12V) vs. Output Current.*

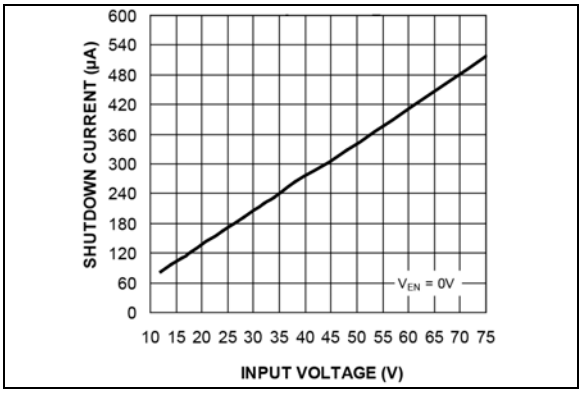


FIGURE 2-34: *V_{IN} Shutdown Current vs. Input Voltage.*

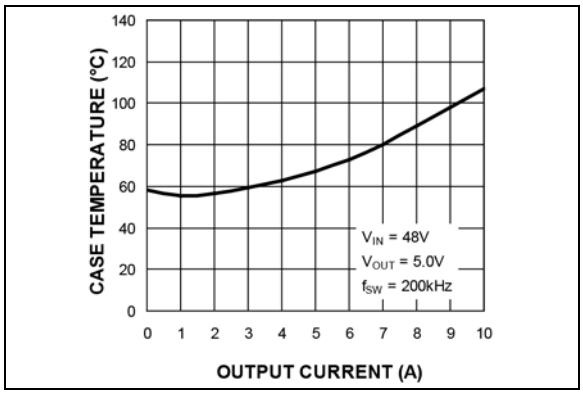


FIGURE 2-32: *Case Temperature* (V_{IN} = 48V) vs. Output Current.*

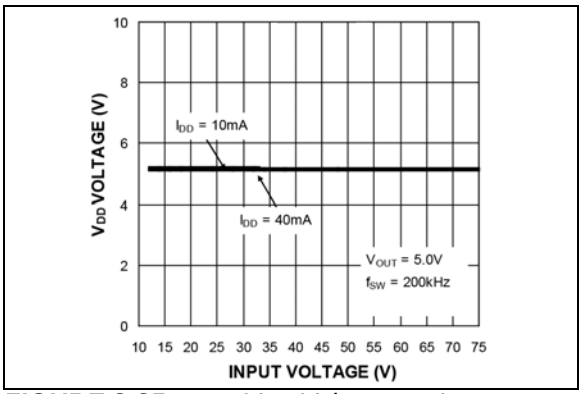


FIGURE 2-35: *V_{DD} Voltage vs. Input Voltage.*

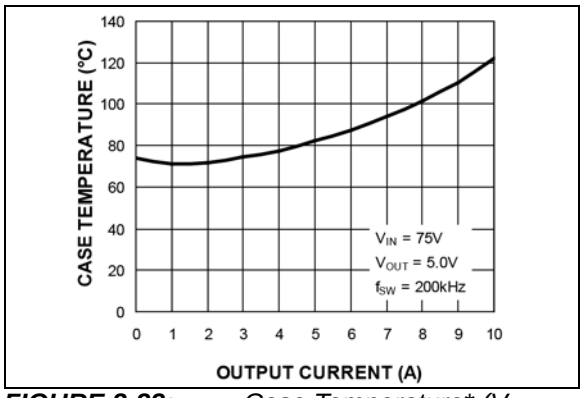


FIGURE 2-33: *Case Temperature* (V_{IN} = 75V) vs. Output Current.*

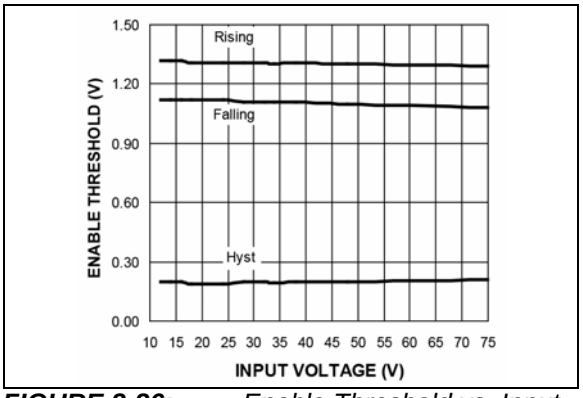


FIGURE 2-36: *Enable Threshold vs. Input Voltage.*

Note: ***Case Temperature:** The temperature measurement was taken at the hottest point on the MIC2103 case mounted on a 5 square inch PCB. Actual results will depend upon the size of the PCB, ambient temperature, and proximity to other heat-emitting components.

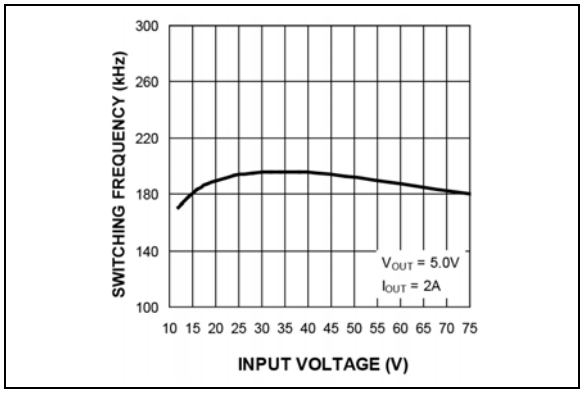


FIGURE 2-37: *Switching Frequency vs. Input Voltage*.

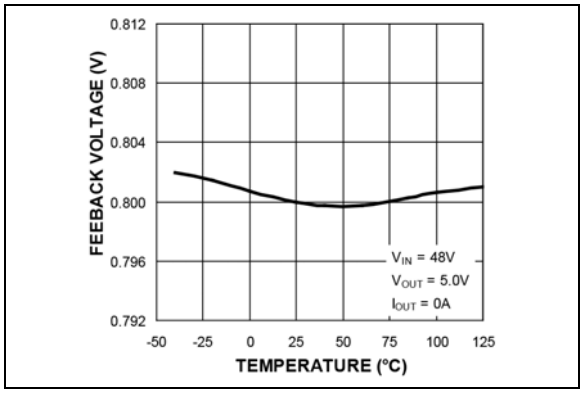


FIGURE 2-40: *Feedback Voltage vs. Temperature.*

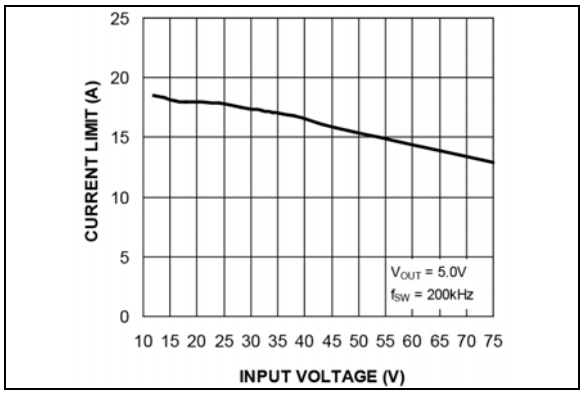


FIGURE 2-38: *Output Peak Current Limit vs. Input Voltage*.

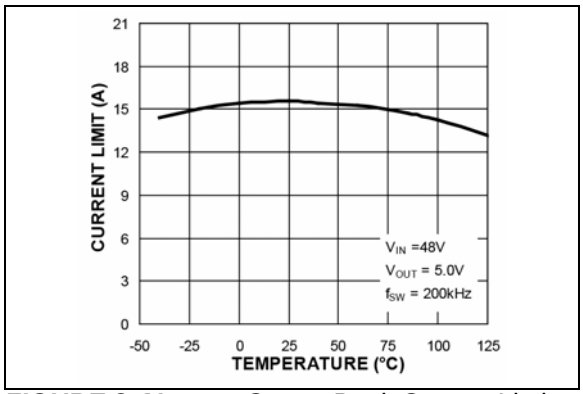


FIGURE 2-41: *Output Peak Current Limit vs. Temperature.*

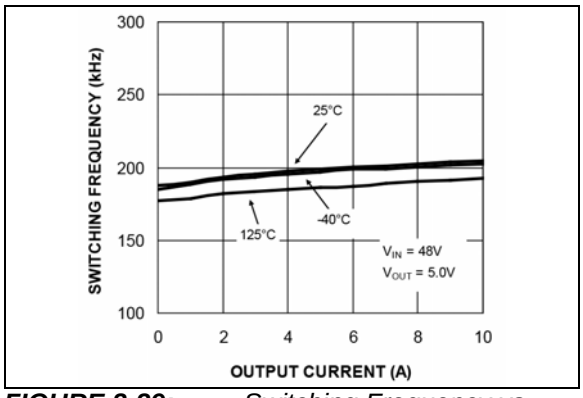


FIGURE 2-39: *Switching Frequency vs. Output Current.*

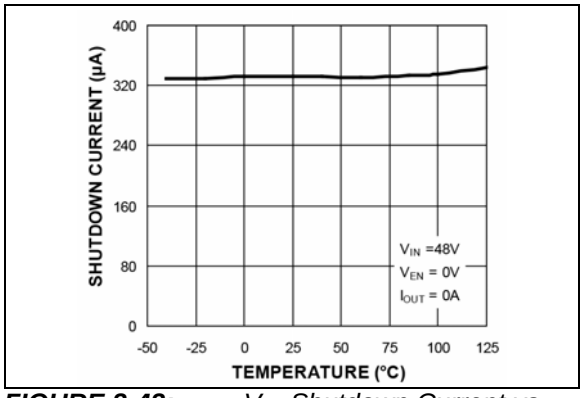


FIGURE 2-42: *V_{IN} Shutdown Current vs. Temperature.*

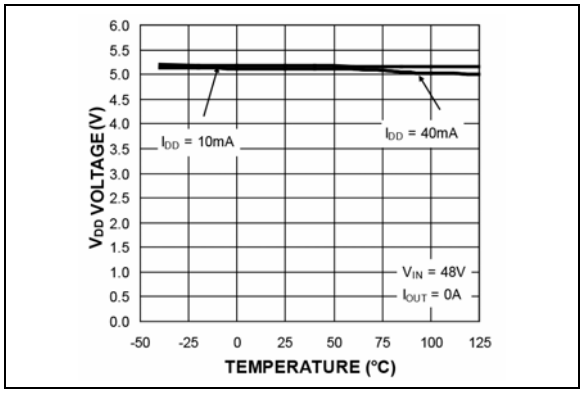


FIGURE 2-43: *V_{DD} Voltage vs. Temperature.*

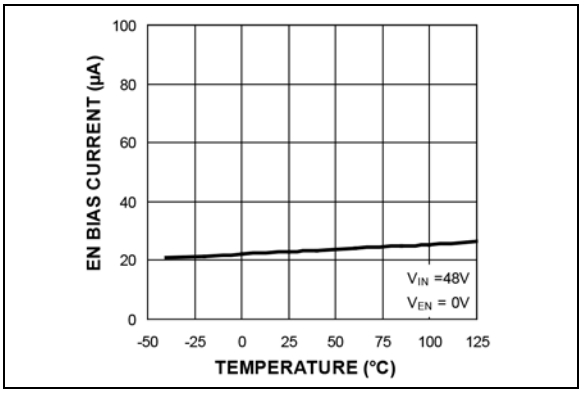


FIGURE 2-46: *EN Bias Current vs. Temperature.*

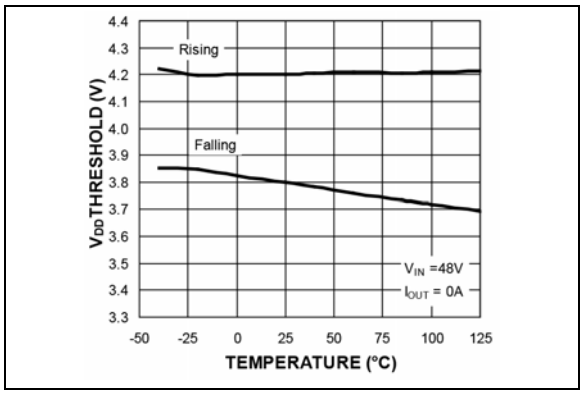


FIGURE 2-44: *V_{DD} UVLO Threshold vs. Temperature.*

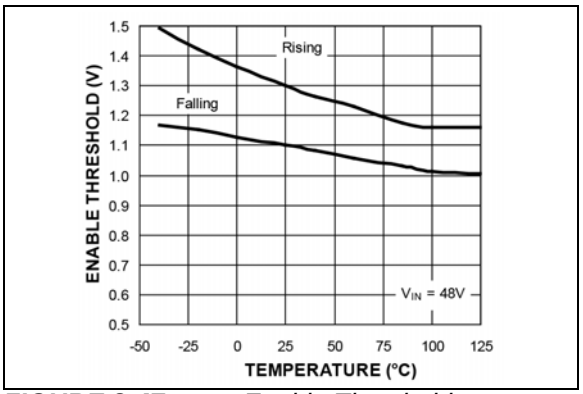


FIGURE 2-47: *Enable Threshold vs. Temperature.*

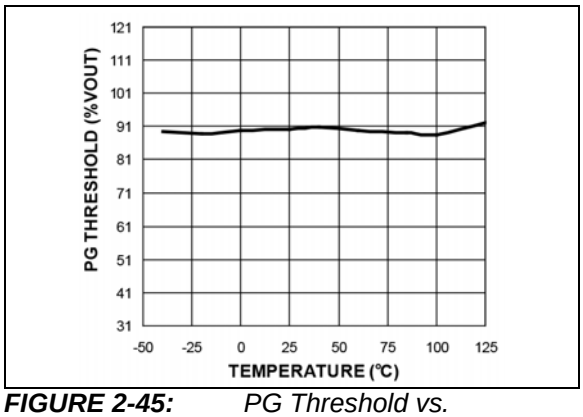


FIGURE 2-45: *PG Threshold vs. Temperature.*

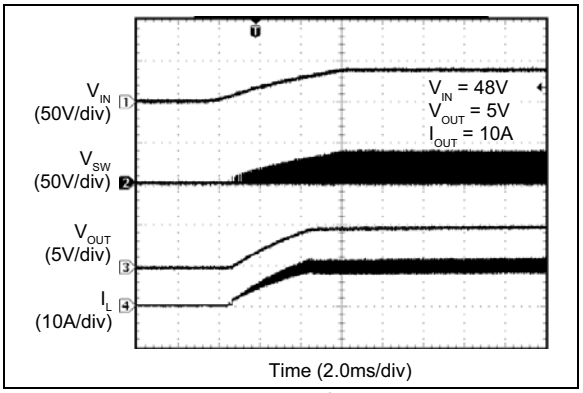


FIGURE 2-48: *V_{IN} Soft Turn-On.*

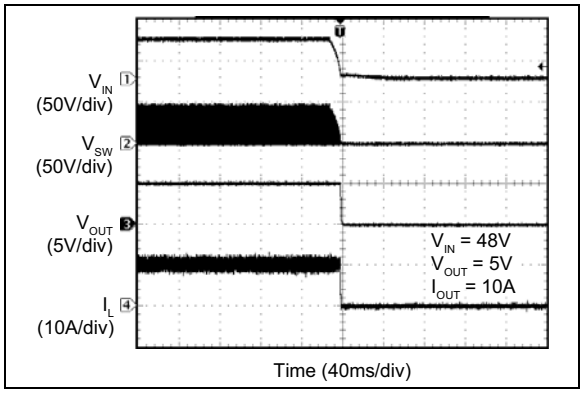


FIGURE 2-49: *V_{IN} Soft Turn-Off.*

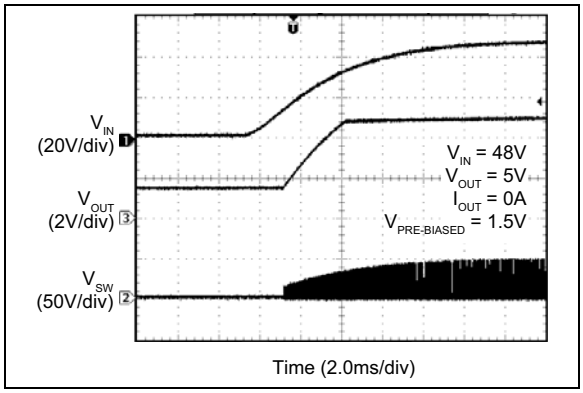


FIGURE 2-52: *MIC2104 V_{IN} Start-Up with Pre-Biased Output.*

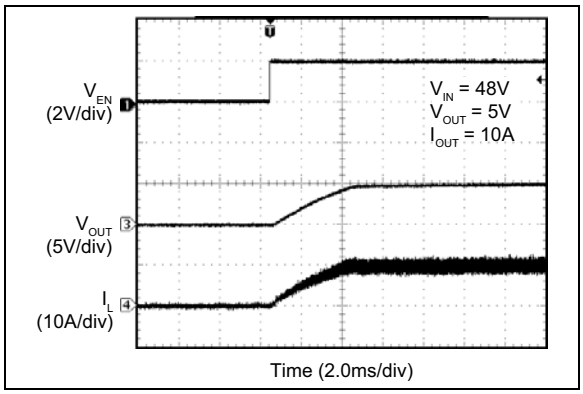


FIGURE 2-50: *Enable Turn-On Delay and Rise Time.*

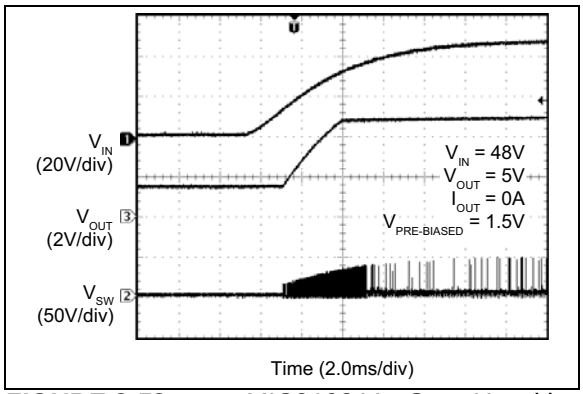


FIGURE 2-53: *MIC2103 V_{IN} Start-Up with Pre-Biased Output.*

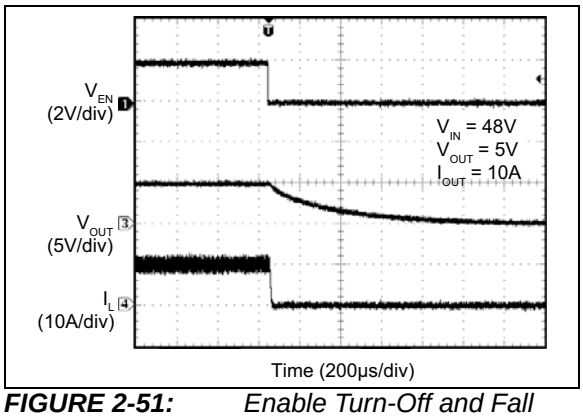


FIGURE 2-51: *Enable Turn-Off and Fall Time.*

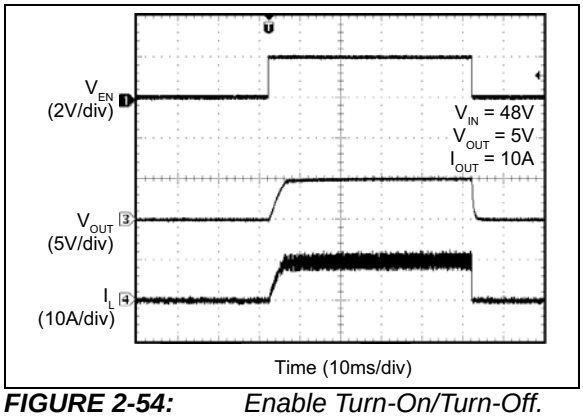


FIGURE 2-54: *Enable Turn-On/Turn-Off.*

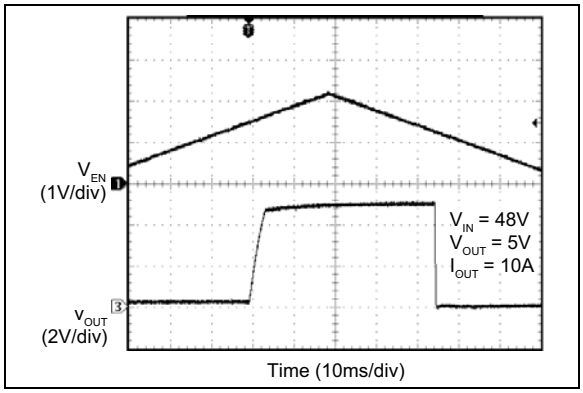


FIGURE 2-55: *Enable Thresholds.*

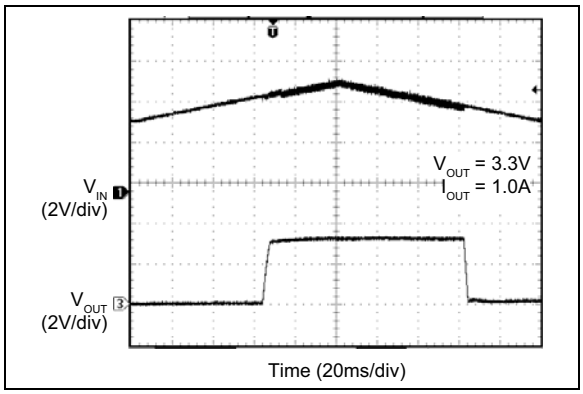


FIGURE 2-56: *V_{IN} UVLO Thresholds.*

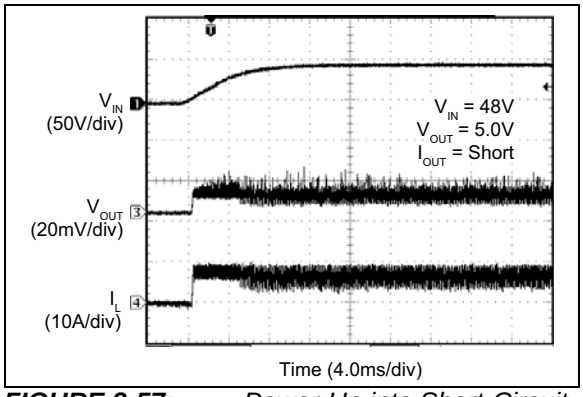


FIGURE 2-57: *Power-Up into Short-Circuit.*

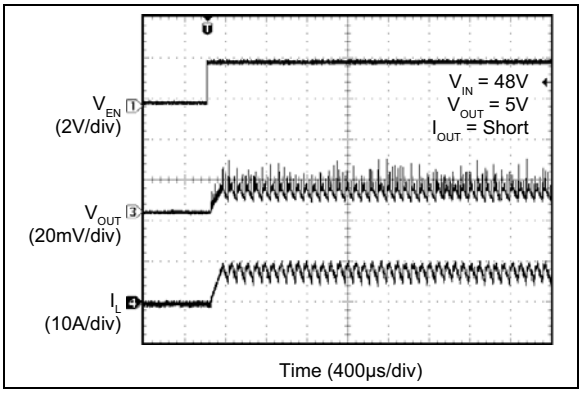


FIGURE 2-58: *Enabled into Short-Circuit.*

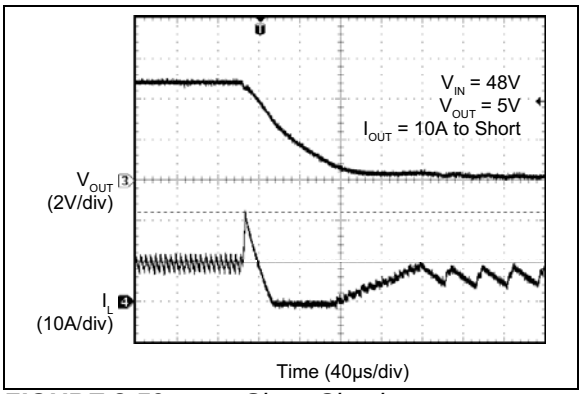


FIGURE 2-59: *Short-Circuit.*

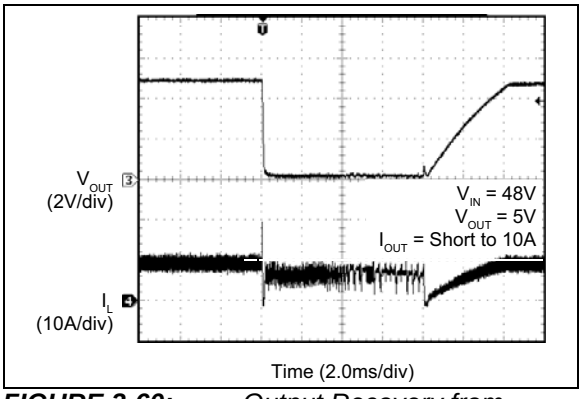


FIGURE 2-60: *Output Recovery from Short-Circuit.*

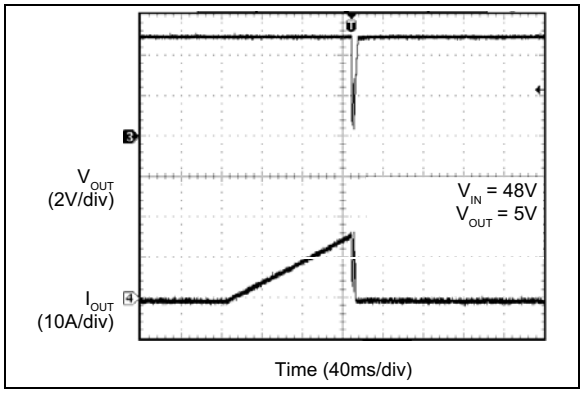


FIGURE 2-61: *Output Peak Current-Limit Threshold.*

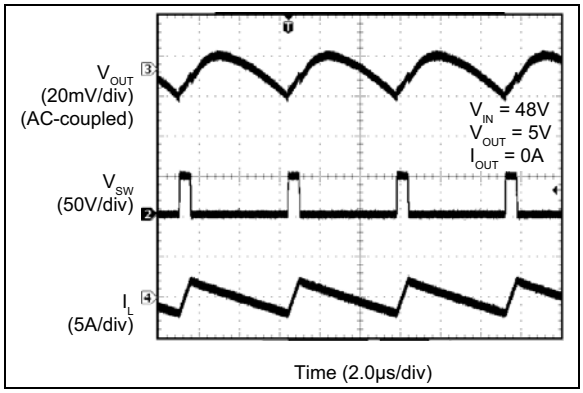


FIGURE 2-64: *MIC2104 Switching Waveforms (I_{OUT} = 0A).*

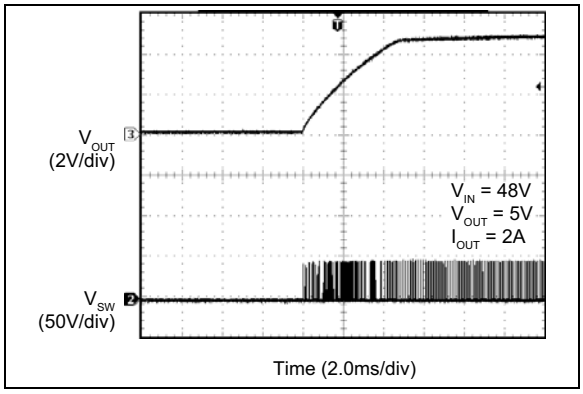


FIGURE 2-62: *Output Recovery from Thermal Shutdown.*

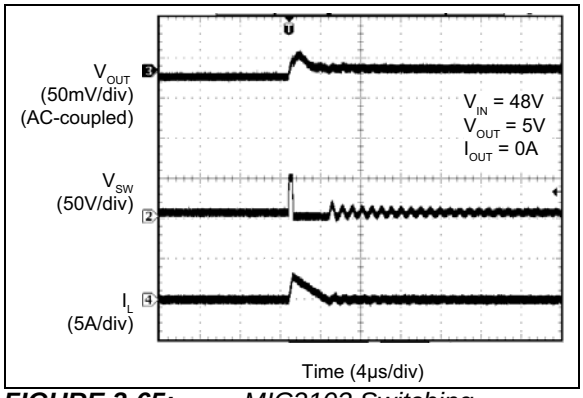


FIGURE 2-65: *MIC2103 Switching Waveforms (I_{OUT} = 0A, DCM).*

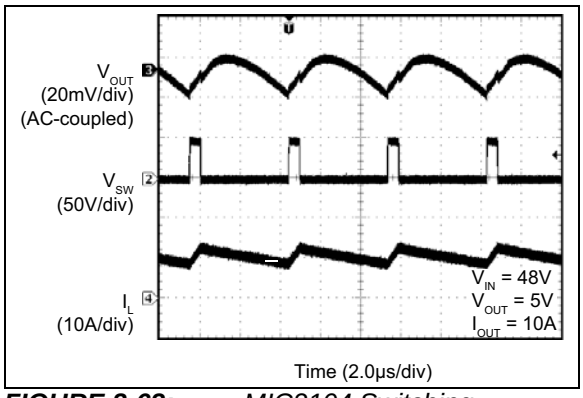


FIGURE 2-63: *MIC2104 Switching Waveforms (I_{OUT} = 10A).*

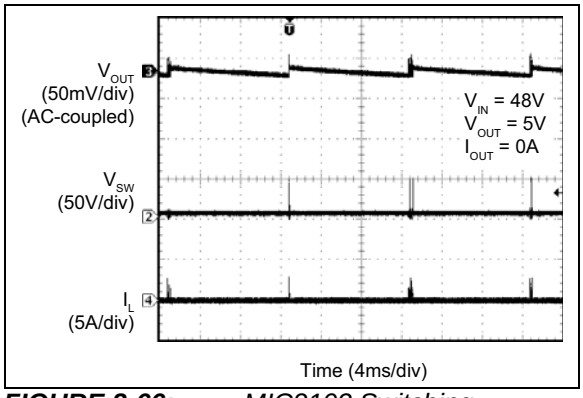


FIGURE 2-66: *MIC2103 Switching Waveforms (I_{OUT} = 0A, DCM).*

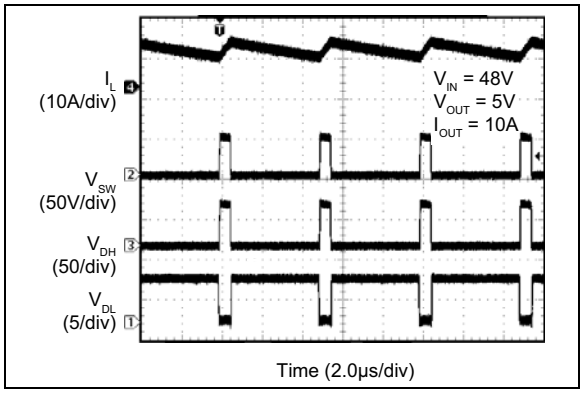


FIGURE 2-67: *MIC2103 Switching Waveforms (I_{OUT} = 10A).*

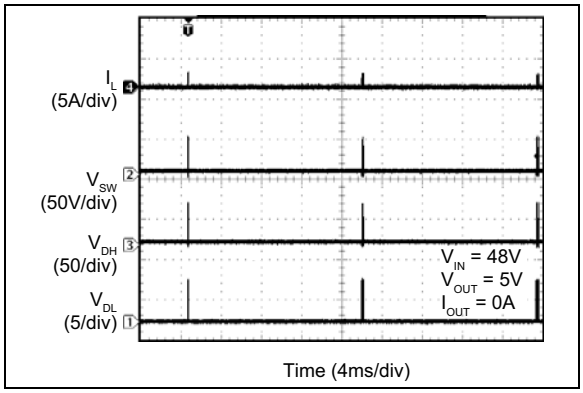


FIGURE 2-68: *MIC2103 Switching Waveforms (I_{OUT} = 0A, DCM).*

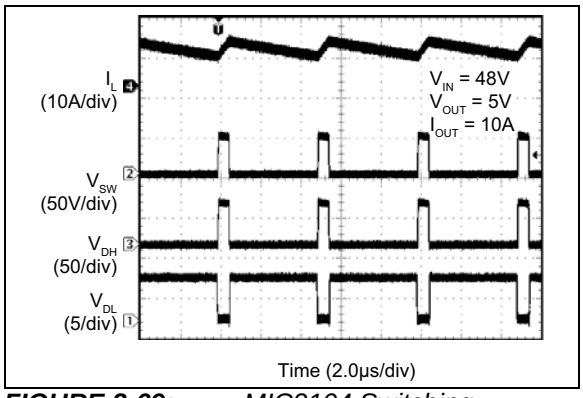


FIGURE 2-69: *MIC2104 Switching Waveforms (I_{OUT} = 10A).*

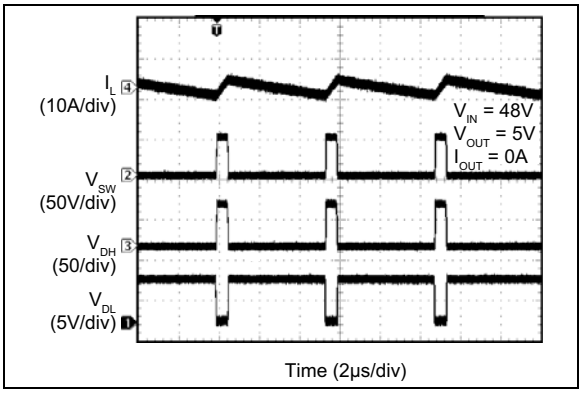


FIGURE 2-70: *MIC2104 Switching Waveforms (I_{OUT} = 0A).*

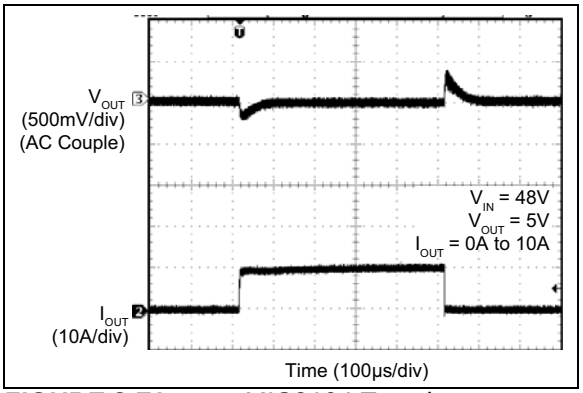


FIGURE 2-71: *MIC2104 Transient Response.*

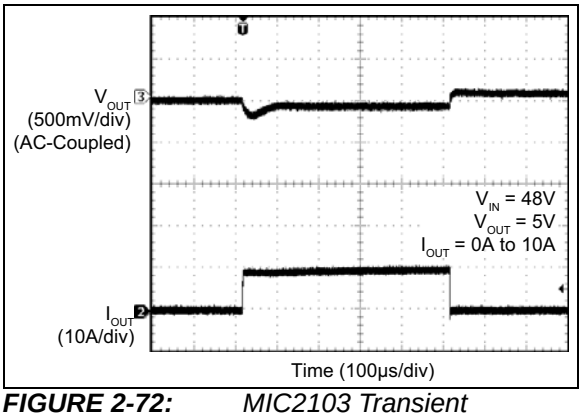


FIGURE 2-72: *MIC2103 Transient Response.*

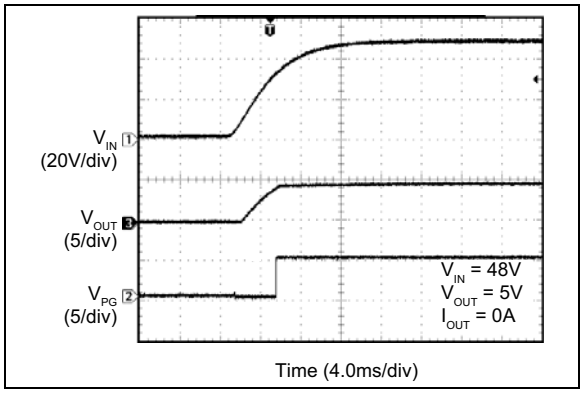


FIGURE 2-73: *Power Good at V_{IN} Soft Turn-On.*

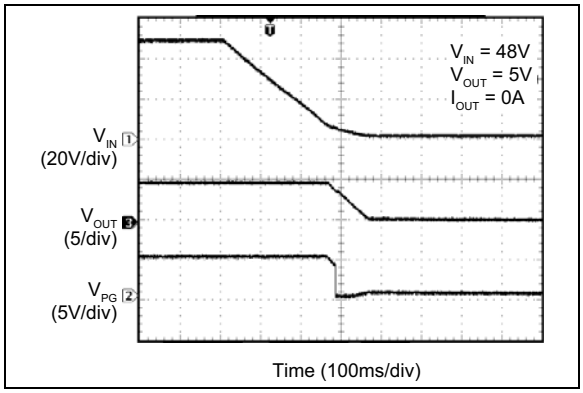


FIGURE 2-74: *Power Good at V_{IN} Soft Turn-Off.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VDD	Internal +5V linear regulator output. V_{DD} is the internal supply bus for the device. A 1 µF ceramic capacitor from V_{DD} to AGND is required for decoupling. In the applications with V_{IN} < +5.5V, V_{DD} should be tied to V_{IN} to bypass the linear regulator.
2	PVDD	5V supply input for the low-side N-channel MOSFET driver, which can be tied to V_{DD} externally. A 1 µF ceramic capacitor from PV_{DD} to PGND is recommended for decoupling.
3	ILIM	Current-Limit Setting. Connect a resistor from SW to ILIM to set the overcurrent threshold for the converter.
4	DL	Low-Side Drive output. High-current driver output for external low-side MOSFET of a buck converter. The DL driving voltage swings from ground to V_{DD}. Adding a small resistor between DL pin and the gate of the low-side N-channel MOSFET can slow down the turn-on and turn-off speed of the MOSFET.
5	PGND	Power Ground. PGND is the return path for the buck converter power stage and the low-side MOSFET driver. The PGND pin connects to the sources of low-side N-channel external MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors. The return path for the power ground should be as small as possible and separate from the Signal ground (AGND) return path.
6	FREQ	Switching Frequency Adjust input. Tie this pin to V_{IN} to operate at 600 kHz and place a resistor divider to reduce the frequency.
7	DH	High-Side Drive output. High-current driver output for external high-side MOSFET of a buck converter. The DH driving voltage is floating on the switch node voltage (V_{SW}). Adding a small resistor between DH pin and the gate of the high-side N-channel MOSFET can slow down the turn-on and turn-off speed of the MOSFET.
8	SW	Switch node, current-sense input, and high-current high-side MOSFET driver return path. The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to the SW pin using a Kelvin connection.
9, 11	NC	No connection.
10	BST	Voltage Supply Pin input for the high-side N-channel MOSFET driver, which can be powered by a bootstrapped circuit connected between V_{DD} and SW, using a Schottky diode and a 0.1 µF ceramic capacitor. Adding a small resistor at BST pin can slow down the turn-on speed of the high-side MOSFET.
12	AGND	Signal ground for V_{DD} and the control circuitry, which is connected to Thermal Pad electronically. The signal ground return path should be separate from the power ground (PGND) return path.
13	FB	Feedback input. Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage.
14	PG	Power Good output. Open-Drain Output, an external pull-up resistor to V_{DD} or external power rail is required.
15	EN	Enable input. A logic signal to enable or disable the buck converter operation. The EN pin is CMOS compatible. Logic high enables the device, logic low disables the regulator. In the disable mode, the V_{DD} supply current for the device is minimized to 0.7 mA typically.
16	VIN	Supply voltage. The V_{IN} operating voltage range is from 4.5V to 75V. A 1 µF ceramic capacitor from V_{IN} to AGND is required for decoupling.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
EP	ePAD	Exposed Pad. Connect the EPAD to PGND plain on the PCB to improve the thermal performance.

4.0 FUNCTIONAL DESCRIPTION

The MIC2103/4 are adaptive on-time synchronous buck controllers built for high-input voltage to low-output voltage conversion applications. They are designed to operate over a wide input voltage range, from 4.5V to 75V, and the output is adjustable with an external resistive divider. An adaptive on-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Overcurrent protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown.

4.1 Theory of Operation

The Functional Block Diagram illustrates the block diagram of the MIC2103/4. The output voltage is sensed by the MIC2103/4 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the amplifier output is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT} = Output voltage.
V_{IN} = Power stage input voltage.
f_{SW} = Switching frequency.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 200 ns, the MIC2103/4 control logic will apply the $t_{OFF(min)}$ instead. $t_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 200 ns $t_{OFF(min)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{200ns}{t_S}$$

Where:

$t_S = 1/f_{SW}$.

It is not recommended to use MIC2103/4 with a OFF-time close to $t_{OFF(min)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC2103/4. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the external MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, one must analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 4-1 shows the MIC2103/4 control loop timing during steady-state operation. During steady-state, the gm amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

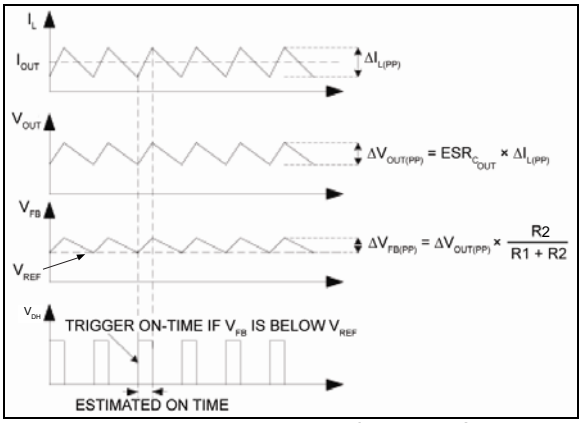


FIGURE 4-1: *MIC2103/4 Control Loop Timing.*

Figure 4-2 shows the operation of the MIC2103/4 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be

less than V_{REF}. This causes the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} because the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC2103/4 converter.

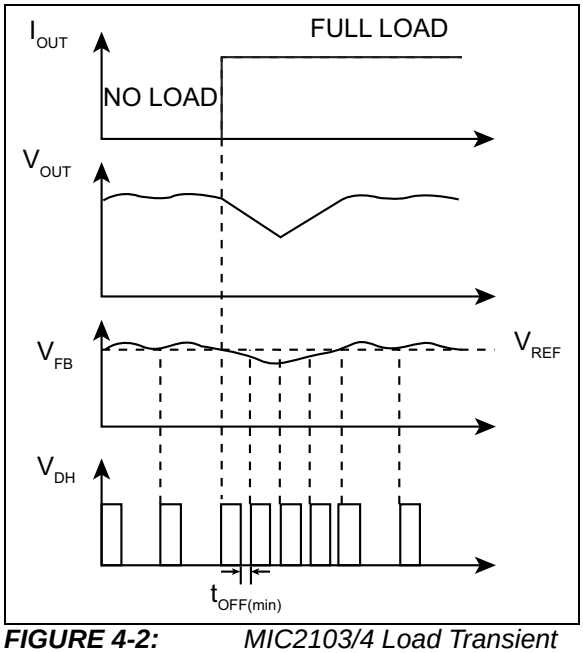


FIGURE 4-2: *MIC2103/4 Load Transient Response.*

Unlike true current-mode control, the MIC2103/4 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC2103/4 feedback voltage ripple should be in phase with the inductor current ripple and are large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV~100 mV over full input voltage range. If a low ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to the Ripple Injection subsection in Application Information for more details about the ripple injection technique.

4.2 Discontinuous Mode (MIC2103 Only)

In continuous mode, the inductor current is always greater than zero. However, at light loads, the MIC2103 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 4-3. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC2103 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC2103 has a zero crossing comparator (ZC Detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC2103 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC2103 goes into discontinuous mode, both DH and DL are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 4-3 shows the control loop timing in discontinuous mode.

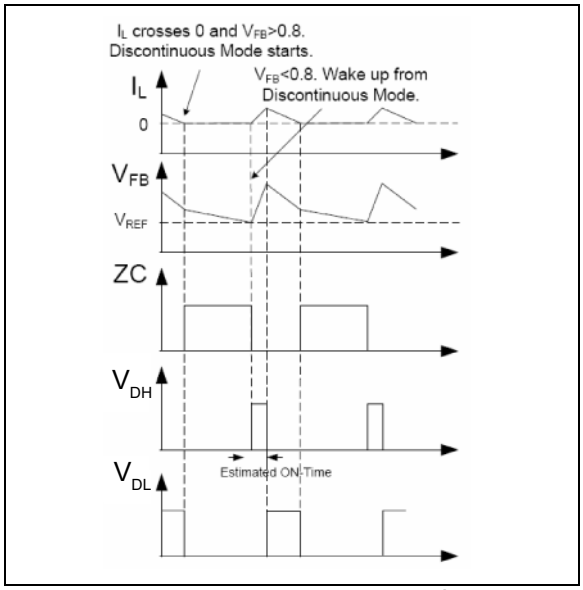


FIGURE 4-3: *MIC2103 Control Loop Timing (Discontinuous Mode).*

During discontinuous mode, the bias current of most circuits are reduced. As a result, the total power supply current during discontinuous mode is only about 400 µA, allowing the MIC2103 to achieve high efficiency in light load applications.

4.3 Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC2103/4 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 6 ms with 9.7 mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

4.4 Current-Limit

The MIC2103/4 uses the $R_{DS(ON)}$ and external resistor connected from ILIM pin to SW node to decide the current limit.

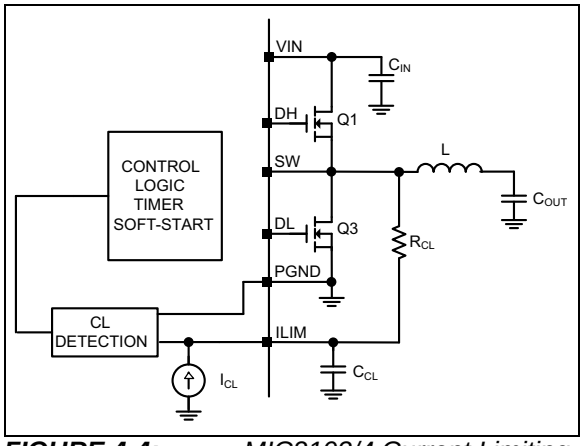


FIGURE 4-4: *MIC2103/4 Current Limiting Circuit.*

In each switching cycle of the MIC2103/4 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage $V_{(ILIM)}$ is compared with the power ground (PGND) after a blanking time of 150 ns. In this way the drop voltage over the resistor R_{CL} (V_{RCL}) is compared with the drop over the bottom FET generating the short current-limit. The small capacitor (C_{CL}) connected from the ILIM pin to PGND filters the switching node ringing during the off time allowing a better short limit measurement. The time constant created by R_{CL} and C_{CL} should be much less than the minimum off time.

The V_{RCL} drop allows programming of short limit through the value of the resistor (R_{CL}), If the absolute value of the voltage drop on the bottom FET is greater than V_{RCL} in that case the $V_{(ILIM)}$ is lower than PGND and a short-circuit event is triggered. A hiccup cycle to treat the short event is generated. The hiccup sequence including the soft-start reduces the stress on the switching FETs and protects the load and supply for severe short conditions.

The short-circuit current-limit can be programmed by using the following formula:

EQUATION 4-3:

$$R_{CL} = \frac{(I_{CLIM} + \Delta I_{L(PP)} \times 0.5) \times R_{DS(ON)} + V_{CL}}{I_{CL}}$$

Where:

I_{CLIM} = Desired output current limit.
$\Delta I_{L(PP)}$ = Inductor current, peak-to-peak.
$R_{DS(ON)}$ = On resistance of low-side power MOSFET.
V_{CL} = Current-limit threshold. Typical value is 14 mV.
I_{CL} = Current-limit source current. Typical value is 80 µA.

In case of a hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft start is under the folded short limit, otherwise the supply will go in hiccup mode and may not be finishing the soft-start successfully.

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add a 50% margin to the calculated R_{CL} in Equation 4-3 to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

4.5 MOSFET Gate Drive

The MIC2103/4 high-side drive circuit is designed to switch an N-channel MOSFET. The Functional Block Diagram shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10 mA, so a 0.1 µF to 1 µF is sufficient to hold

the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e., ΔBST = 10 mA x 3.33 µs/0.1 µF = 333 mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G, which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately $V_{DD} – V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximate 30 ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

5.0 APPLICATION INFORMATION

5.1 Setting the Switching Frequency

The MIC2103/4 are adjustable-frequency, synchronous buck controllers that feature a unique adaptive on-time control architecture. The switching frequency can be adjusted between 200 kHz and 600 kHz by changing the resistor divider network consisting of R19 and R20.

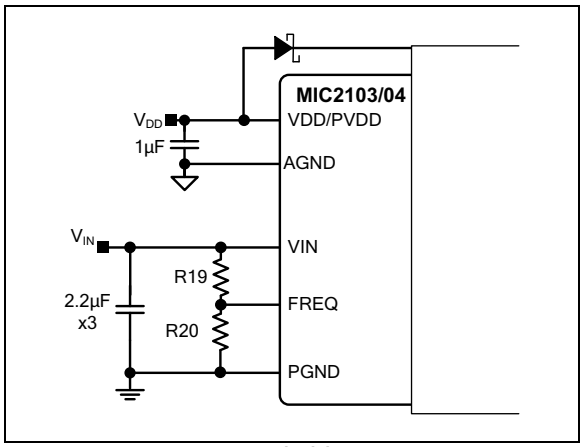


FIGURE 5-1: *Switching Frequency Adjustment.*

The following formula gives the estimated switching frequency:

EQUATION 5-1:

$$f_{SW\_ADJ} = f_O \times \frac{R20}{R19 + R20}$$

Where:

f_O = Switching frequency when R19 is 100 kΩ and R20 is open. Typically 550 kHz.

For a more precise setting, it is recommended to use the following graph:

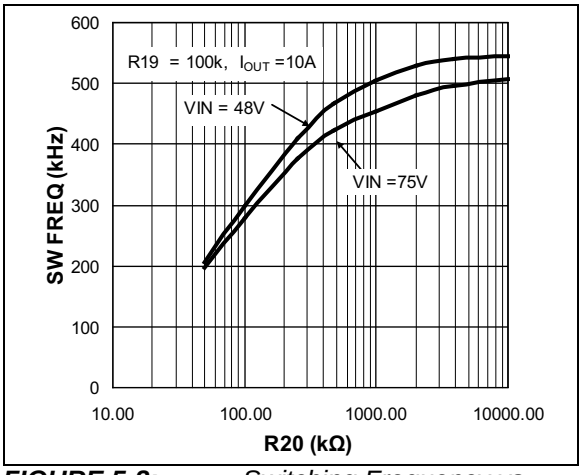


FIGURE 5-2: *Switching Frequency vs. R20.*

5.2 MOSFET Selection

The MIC2103/4 controllers work from input voltages of 4.5V to 75V and have an internal 5V V_{DD} LDO. This internal V_{DD} LDO provides power to turn on the external N-channel power MOSFETs for the high-side and low-side switches. For applications where V_{DD} < 5V, it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for V_{GS} of 2.5V. For applications when V_{DD} > 5V; logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used.

There are different criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles. In such an application, the high-side MOSFET is then required to switch as quickly as possible in order to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty cycle approaches 50%, the current carrying capability of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current limit. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2103/4 gate-drive circuit. At 200 kHz switching frequency, the gate charge can be a significant source of power dissipation in the

MIC2103/4. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

EQUATION 5-2:

$$I_{G(HIGH-SIDE(AVG))} = Q_G \times f_{SW}$$

Where:

$I_{G(HIGH-SIDE(AVG))}$ = Average high-side MOSFET gate current.
Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for $V_{GS} = V_{DD}$.
f_{SW} = Switching frequency.

The low-side MOSFET is turned on and off at $V_{DS} = 0$ because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at $V_{DS} = 0$ instead of gate charge.

For the low-side MOSFET:

EQUATION 5-3:

$$I_{G(LOW-SIDE(AVG))} = C_{ISS} \times V_{GS} \times f_{SW}$$

Because the current from the gate drive comes from the V_{DD}, which is the output of the internal linear regulator powered by V_{IN}, the power dissipated in the MIC2103/4 due to gate drive is:

EQUATION 5-4:

$$P_{GATEDRIVE} = V_{IN} \times (I_{G(HIGH-SIDE(AVG))} + I_{G(LOW-SIDE(AVG))})$$

A convenient figure of merit for switching MOSFETs is the on resistance multiplied by the total gate charge; $R_{DS(ON)} \times Q_G$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2103/4. Also, the $R_{DS(ON)}$ of the low-side MOSFET will determine the current-limit value. Please refer to the Current-Limit subsection in the Functional Description for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{HSD}. A safety factor of 20% should be added to the $V_{DS(max)}$ of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses during the period of time when the MOSFETs turn on and off (P_{AC}).

EQUATION 5-5:

$$P_{SW} = P_{CONDUCTION} + P_{AC}$$

$$P_{CONDUCTION} = I_{SW(RMS)}^2 \times R_{DS(ON)}$$

$$P_{AC} = P_{AC(OFF)} + P_{AC(ON)}$$

Where:

$I_{SW(RMS)}$ = RMS current of the MOSFET switch.
$R_{DS(ON)}$ = On-resistance of the MOSFET switch.

The high-side MOSFET and low-side MOSFET RMS currents can be calculated by Equation 5-6:

EQUATION 5-6:

$$I_{SWHS(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D}$$

$$I_{SWLS(RMS)} \approx I_{OUT(MAX)} \times \sqrt{(1-D)}$$

Where:

D = Duty cycle = V_{OUT}/V_{HSD}.

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

EQUATION 5-7:

$$t_T = \frac{C_{ISS} \times V_{DD} + C_{OSS} \times V_{HSD}}{I_G}$$

Where:

C_{ISS} and C_{OSS} are measured at V_{DS} = 0.
I_G = Gate drive current.

The total high-side MOSFET switching loss is:

EQUATION 5-8:

$$P_{AC} = (V_{HSD} + V_D) \times I_{L(PK)} \times t_T \times f_{SW}$$

Where:

t_T = Switching transition time.
V_D = Body diode drop (0.5V).
f_{SW} = Switching frequency.

The high-side MOSFET switching losses increase with the switching frequency and the power stage input voltage V_{HSD}. The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

5.3 Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor.

A good compromise among size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current.

The inductance value is calculated by Equation 5-9:

EQUATION 5-9:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times 20\% \times I_{OUT(MAX)}}$$

Where:

f_{SW} = Switching frequency.
20% = Ratio of AC ripple current to DC output current.
$V_{IN(MAX)}$ = Max. power stage input voltage.

The peak-to-peak inductor current ripple is:

EQUATION 5-10:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

EQUATION 5-11:

$$I_{L(PK)} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

EQUATION 5-12:

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{\Delta I_{L(PP)}^2}{12}}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2103/4 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the buck converter. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper

losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetic vendor.

Copper loss in the inductor is calculated by Equation 5-13:

EQUATION 5-13:

$$P_{INDUCTOR(Cu)} = I_{L(RMS)}^{2} \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

EQUATION 5-14:

$$R_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C}))$$

Where:

T_H = Temp. of wire under full load.
$T_{20°C}$ = Ambient temperature.
$R_{WINDING(20°C)}$ = Room temperature winding resistance (usually specified by the manufacturer).

5.4 Output Capacitor Selection

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

EQUATION 5-15:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}}$$

Where:

$\Delta V_{OUT(PP)}$ = Peak-to-peak output voltage ripple.
$\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple.

The total output ripple is a combination of voltage ripples caused by the ESR and output capacitance. The total ripple is calculated in Equation 5-16:

EQUATION 5-16:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + (\Delta I_{L(PP)} \times ESR_{COUT})^2}$$

Where:

C_{OUT} = Output capacitance value.
f_{SW} = Switching frequency.

As described in the Theory of Operation subsection in Functional Description, the MIC2103/4 requires at least 20 mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to the Ripple Injection subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 5-17:

EQUATION 5-17:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-18:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^{2} \times ESR_{COUT}$$

5.5 Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when

subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating.

The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-19:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

EQUATION 5-20:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 5-21:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^{2} \times ESR_{CIN}$$

5.6 Voltage Setting Components

The MIC2103/4 requires two resistors to set the output voltage as shown in Figure 5-3:

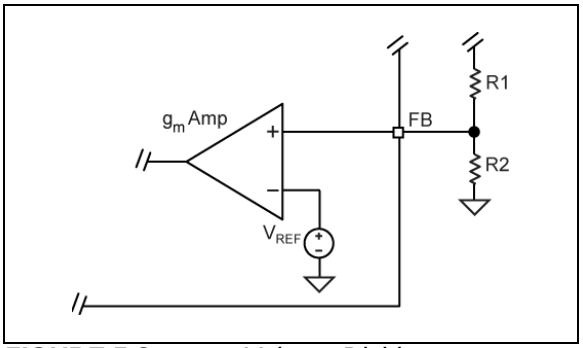


FIGURE 5-3: *Voltage-Divider Configuration.*

The output voltage is determined by the following equation:

EQUATION 5-22:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{FB} = 0.8V.

A typical value of R1 can be between 3 kΩ and 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the buck converter, especially at light loads. Once R1 is selected, R2 can be calculated using Equation 5-23:

EQUATION 5-23:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

5.7 Ripple Injection

The V_{FB} ripple required for proper operation of the MIC2103/4 g_m amplifier and error comparator is 20 mV to 100 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10 mV to 20 mV, and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator cannot sense it, then the MIC2103/4 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

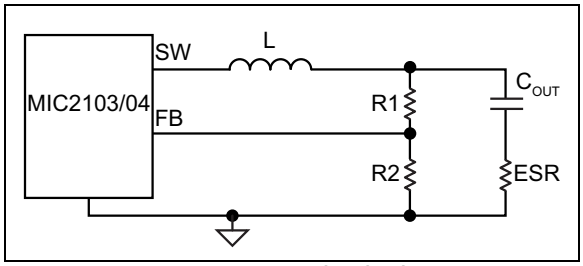


FIGURE 5-4: *Enough Ripple at FB.*

As shown in Figure 5-4, the converter is stable without any ripple injection. The feedback voltage ripple is:

EQUATION 5-24:

$$\Delta V_{FB(PP)} = \frac{R2}{R1 + R2} \times ESR_{COUT} \times \Delta I_{L(PP)}$$

Where:

$\Delta I_{L(PP)}$ = Peak-to-peak inductor current ripple.

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

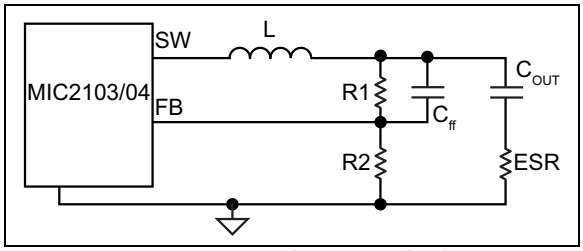


FIGURE 5-5: *Inadequate Ripple at FB.*

The output voltage ripple is fed into the FB pin through a feed-forward capacitor C_{ff} in this situation, as shown in Figure 5-5. The typical C_{ff} value is between 1 nF and 100 nF. With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

EQUATION 5-25:

$$\Delta V_{FB(PP)} \approx ESR \times \Delta I_{L(PP)}$$

3. Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors:

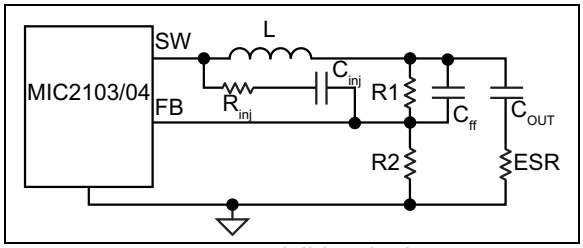


FIGURE 5-6: *Invisible Ripple at FB.*

In this situation, the output voltage ripple is less than 20 mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{inj} and a capacitor C_{inj}, as shown in Figure 5-6. The injected ripple is:

EQUATION 5-26:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1 - D) \times \frac{1}{f_{SW} \times \tau}$$

Where:

V_{IN} = Power stage input voltage.
D = Duty cycle.
f_{SW} = Switching frequency.
$\tau = (R1//R2//R_{inj}) \times C_{ff}$.

EQUATION 5-27:

$$K_{DIV} = \frac{R1//R2}{R_{inj} + R1//R2}$$

In Equation 5-26 and Equation 5-27, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

EQUATION 5-28:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

If the voltage divider resistors R1 and R2 are in the kΩ range, then a C_{ff} of 1 nF to 100 nF can easily satisfy the large time constant requirements. Also, a 100 nF injection capacitor C_{inj} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1 nF to 100 nF if R1 and R2 are in kΩ range.
2. Select R_{inj} according to the expected feedback voltage ripple using Equation 5-29:

EQUATION 5-29:

$$K_{DIV} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1 - D)}$$

Then the value of R_{inj} is obtained as:

EQUATION 5-30:

$$R_{inj} = (R1 // R2) \times \left(\frac{1}{K_{DIV}} - 1\right)$$

3. Select C_{inj} as 100 nF, which could be considered as short for a wide range of the frequencies.

6.0 PCB LAYOUT GUIDELINES

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power and signal return paths.

The following guidelines should be followed to insure proper operation of the MIC2103/4 buck controllers.

6.1 IC

- The 1 µF ceramic capacitors, which are connected to the V_{DD} and PV_{DD} pins, must be located right at the IC. The V_{DD} pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the V_{DD}, PV_{DD}, AGND, and PGND pins.
- The signal ground pin (AGND) must be connected directly to the ground planes. Do not route the AGND pin to the PGND pin on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

6.2 Input Capacitor

- Place the input capacitors on the same side of the board and as close to the MOSFETs as possible.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric ceramic input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

6.3 RC Snubber

- Place the RC snubber on the same side of the board and as close to the SW pin as possible.

6.4 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The SW pin should be connected directly to the drain of the low-side MOSFET to accurately sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

6.5 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

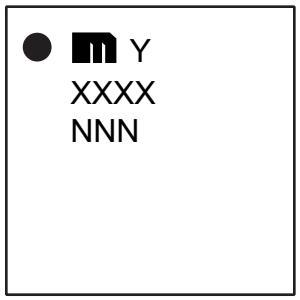
6.6 MOSFETs

- Low-side MOSFET gate drive trace (DL pin to MOSFET gate pin) must be short and routed over a ground plane. The ground plane should be the connection between the MOSFET source and PGND.
- Choose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance to minimize the effect of dv/dt inducted turn-on.
- Do not put a resistor between the low-side MOSFET gate drive output and the gate.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than 4.5V V_{GS} should not be used.

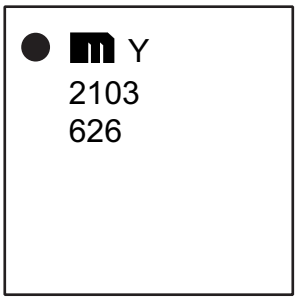
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

16-Pin QFN*



Example

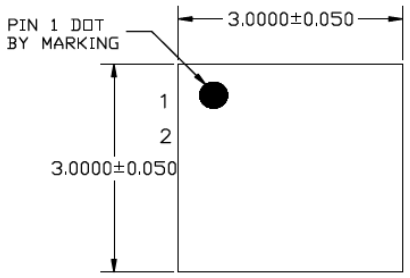


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

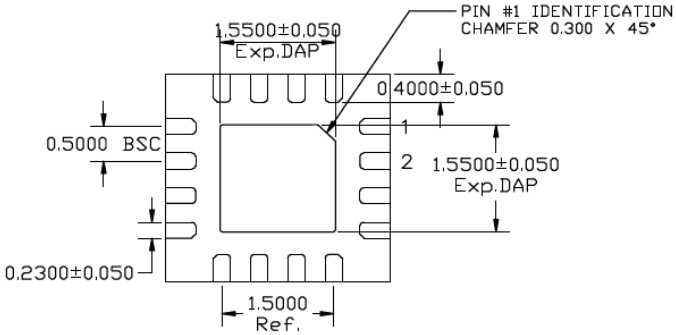
16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

TITLE
16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

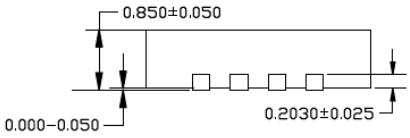
DRAWING #	QFN33-16LD-PL-1	UNIT	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3

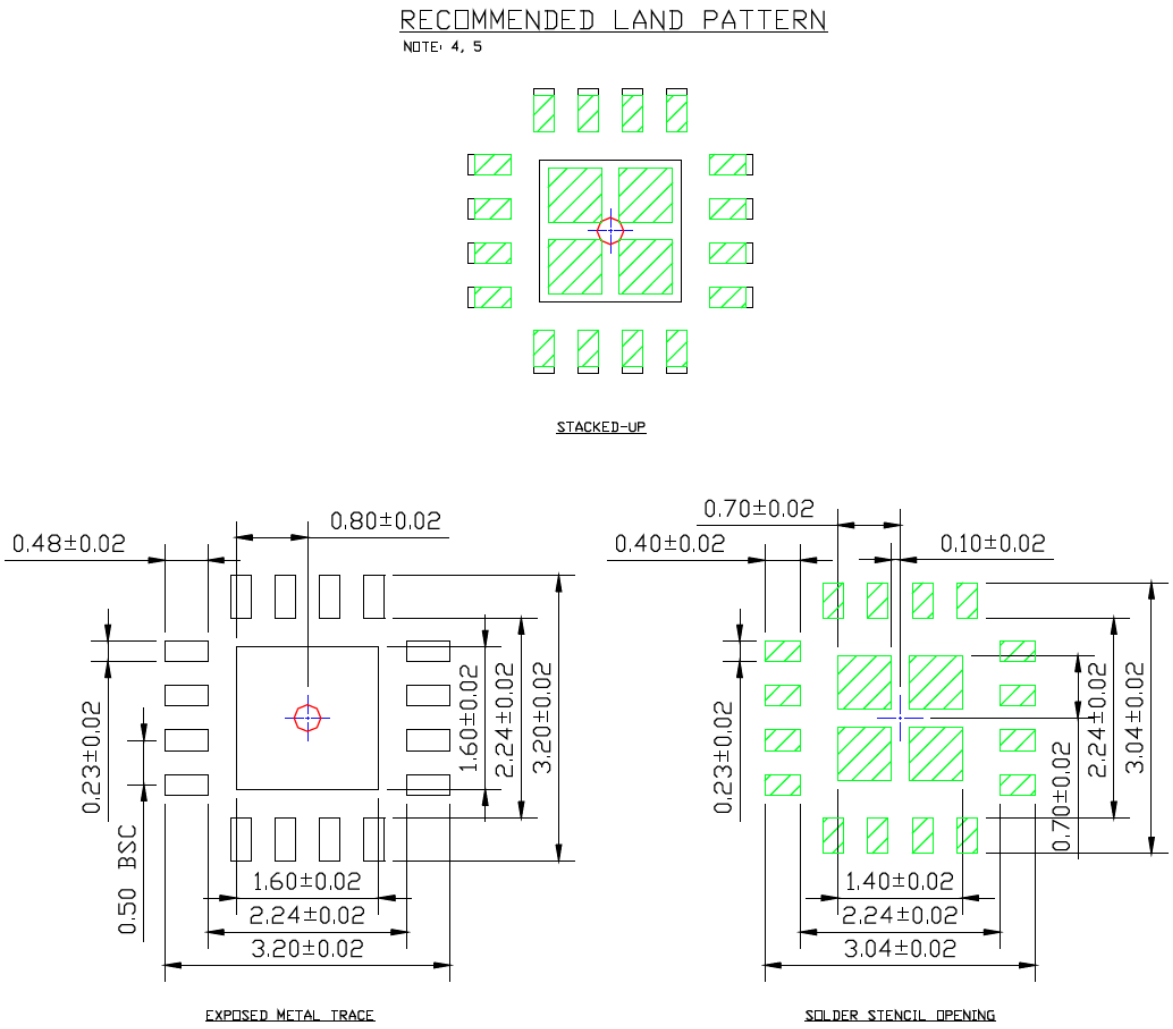


SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30–0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern drawing # QFN33-16LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (December 2017)

- Converted Micrel document MIC2103/4 to Microchip data sheet DS20005899A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	XX	–XX
Device	Features	Junction Temp. Range	Package	Media Type

Device:	MIC210_:		75V, Synchronous Buck Controller featuring Adaptive On-Time Control
Features:	3	=	HyperLight Load®
	4	=	Hyper Speed Control®
Junction Temperature Range:	Y	=	–40°C to +125°C, RoHS-Compliant
Package:	ML	=	16-Lead 3 mm x 3 mm QFN
Media Type:	TR	=	5,000/Reel

Examples:

a) MIC2103YML-TR: 75V, Synchronous Buck Controller featuring Adaptive On-Time Control, HyperLight Load, –40°C to +125°C Temp. Range, 16-Lead 3 mm x 3 mm QFN, 5,000/Reel

b) MIC2104YML-TR: 75V, Synchronous Buck Controller featuring Adaptive On-Time Control, Hyper Speed Control, –40°C to +125°C Temp. Range, 16-Lead 3 mm x 3 mm QFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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