

MCR703A Series

Preferred Device

Sensitive Gate Silicon Controlled Rectifiers Reverse Blocking Thyristors

PNPN devices designed for high volume, low cost consumer applications such as temperature, light and speed control; process and remote control; and warning systems where reliability of operation is critical.

Features

- Small Size
- Passivated Die Surface for Reliability and Uniformity
- Low Level Triggering and Holding Characteristics
- Recommend Electrical Replacement for C106
- Surface Mount Package – Case 369C
- To Obtain “DPAK” in Straight Lead Version (Shipped in Sleeves): Add '1' Suffix to Device Number, i.e., MCR706A1
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- Pb-Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Max	Unit
Peak Repetitive Off-State Voltage (Note 1) (T _C = -40 to +110°C, Sine Wave, 50 to 60 Hz, Gate Open)	V _{DRM} , V _{RRM}	100 400 600	V
Peak Non-Repetitive Off-State Voltage (Sine Wave, 50 to 60 Hz, Gate Open, T _C = -40 to +110°C)	V _{RSM}	150 450 650	V
On-State RMS Current (180° Conduction Angles; T _C = 90°C)	I _{T(RMS)}	4.0	A
Average On-State Current (180° Conduction Angles) T _C = -40 to +90°C T _C = +100°C	I _{T(AV)}	2.6 1.6	A
Non-Repetitive Surge Current (1/2 Sine Wave, 60 Hz, T _J = 110°C) (1/2 Sine Wave, 1.5 ms, T _J = 110°C)	I _{TSM}	25 35	A
Circuit Fusing (t = 8.3 msec)	I ² t	2.6	A ² sec
Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec, T _C = 90°C)	P _{GM}	0.5	W
Forward Average Gate Power (t = 8.3 msec, T _C = 90°C)	P _{G(AV)}	0.1	W
Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec, T _C = 90°C)	I _{GM}	0.2	A
Operating Junction Temperature Range	T _J	-40 to +110	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.



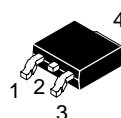
ON Semiconductor®

<http://onsemi.com>

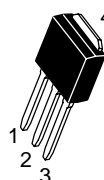
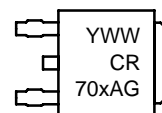
SCRs
4.0 AMPERES RMS
100 – 600 VOLTS



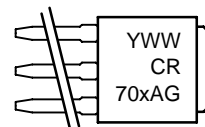
MARKING DIAGRAMS



DPAK
CASE 369C
STYLE 2



DPAK-3
CASE 369D
STYLE 2



Y = Year
WW = Work Week
70xA = Device Code
x = 3, 6 or 8
G = Pb-Free Package

PIN ASSIGNMENT

Pin	Assignment
1	Gate
2	Anode
3	Cathode
4	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	8.33	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	80	$^{\circ}\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	T_L	260	$^{\circ}\text{C}$

2. Case 369C when surface mounted on minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current ($V_{AK} = \text{Rated } V_{DRM}$ or V_{RRM} ; $R_{GK} = 1 \text{ k}\Omega$)	I_{DRM}, I_{RRM}	-	-	10 200	μA
					$T_C = 25^{\circ}\text{C}$ $T_C = 110^{\circ}\text{C}$

ON CHARACTERISTICS

Peak Forward "On" Voltage ($I_{TM} = 8.2 \text{ A}$ Peak, Pulse Width = 1 to 2 ms, 2% Duty Cycle)	V_{TM}	-	-	2.2	V
Gate Trigger Current (Continuous dc) (Note 3) ($V_{AK} = 12 \text{ Vdc}$, $R_L = 24 \Omega$)	I_{GT}	-	25	75	μA
		-	-	300	
					$T_C = 25^{\circ}\text{C}$ $T_C = -40^{\circ}\text{C}$
Gate Trigger Voltage (Continuous dc) (Note 3) ($V_{AK} = 12 \text{ Vdc}$, $R_L = 24 \Omega$)	V_{GT}	-	-	0.8 1.0	V
		-	-		$T_C = 25^{\circ}\text{C}$ $T_C = -40^{\circ}\text{C}$
Gate Non-Trigger Voltage (Note 3) ($V_{AK} = 12 \text{ Vdc}$, $R_L = 100 \Omega$, $T_C = 110^{\circ}\text{C}$)	V_{GD}	0.2	-	-	V
Holding Current ($V_{AK} = 12 \text{ Vdc}$, Gate Open) $T_C = 25^{\circ}\text{C}$ (Initiating Current = 200 mA) $T_C = -40^{\circ}\text{C}$	I_H	-	-	5.0 10	mA
		-	-		
Peak Reverse Gate Blocking Voltage ($I_{GR} = 10 \mu\text{A}$)	V_{RGM}	10	12.5	18	V
Peak Reverse Gate Blocking Current ($V_{GR} = 10 \text{ V}$)	I_{RGM}	-	-	1.2	μA
Total Turn-On Time (Source Voltage = 12 V, $R_S = 6 \text{ k}\Omega$) ($I_{TM} = 8.2 \text{ A}$, $I_{GT} = 2 \text{ mA}$, Rated V_{DRM}) (Rise Time = 20 ns, Pulse Width = 10 μs)	t_{gt}	-	2.0	-	μs

DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage ($V_D = \text{Rated } V_{DRM}$; $R_{GK} = 1 \text{ k}\Omega$, Exponential Waveform, $T_C = 110^{\circ}\text{C}$)	dv/dt	-	10	-	$\text{V}/\mu\text{s}$
Repetitive Critical Rate of Rise of On-State Current ($C_f = 60 \text{ Hz}$, $I_{PK} = 30 \text{ A}$, $PW = 100 \mu\text{s}$, $diG/dt = 1 \text{ A}/\mu\text{s}$)	di/dt	-	-	100	$\text{A}/\mu\text{s}$

3. R_{GK} current not included in measurement.

ORDERING INFORMATION

Device	Package Type	Package	Shipping [†]
MCR703AT4	DPAK	369C	2500 Tape & Reel
MCR703AT4G	DPAK	369C (Pb-Free)	2500 Tape & Reel
MCR706AT4	DPAK	369C	2500 Tape & Reel
MCR706AT4G	DPAK	369C (Pb-Free)	2500 Tape & Reel
MCR708A	DPAK	369C	2500 Tape & Reel
MCR708AG	DPAK	369C (Pb-Free)	2500 Tape & Reel
MCR708A1	DPAK-3	369D	75 Units / Rail
MCR708A1G	DPAK-3	369D (Pb-Free)	75 Units / Rail
MCR708AT4	DPAK	369C	2500 Tape & Reel
MCR708AT4G	DPAK	369C (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off-State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off-State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak On-State Voltage
I_H	Holding Current

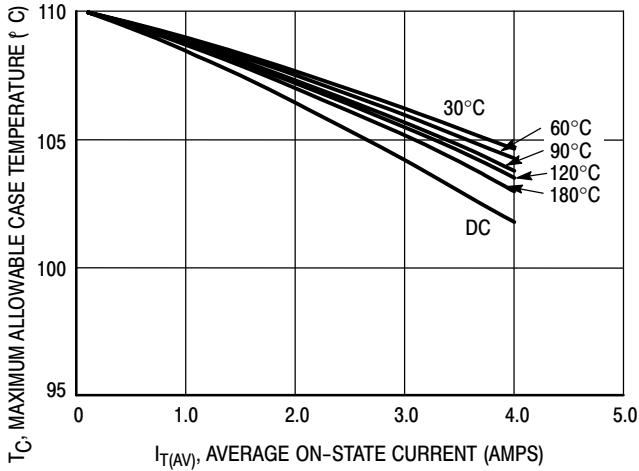
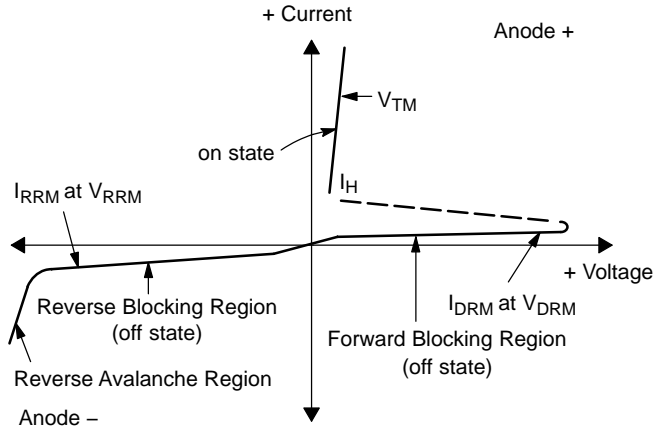


Figure 1. Average Current Derating

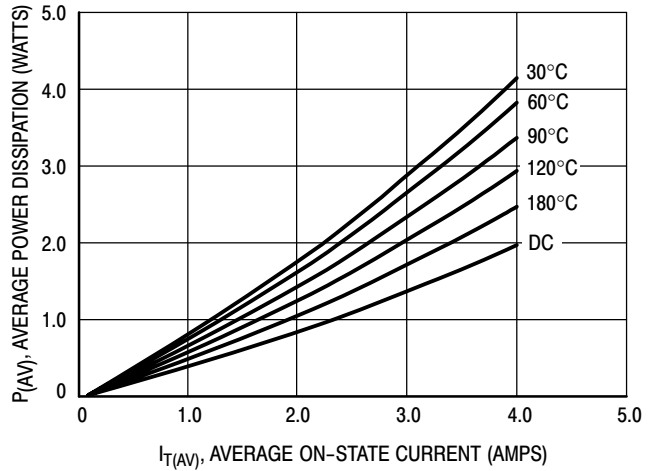


Figure 2. On-State Power Dissipation

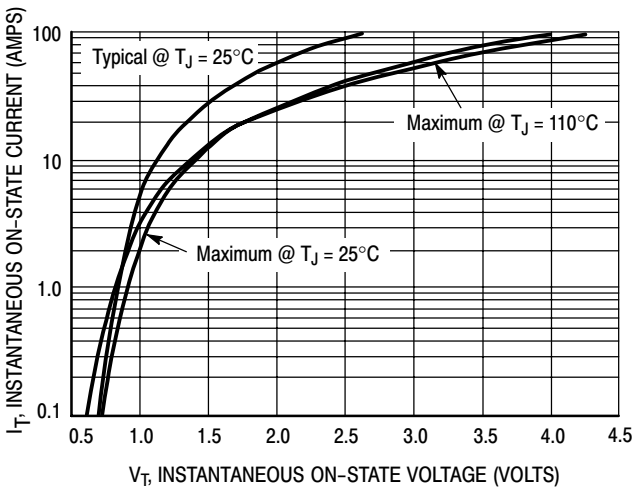


Figure 3. On-State Characteristics

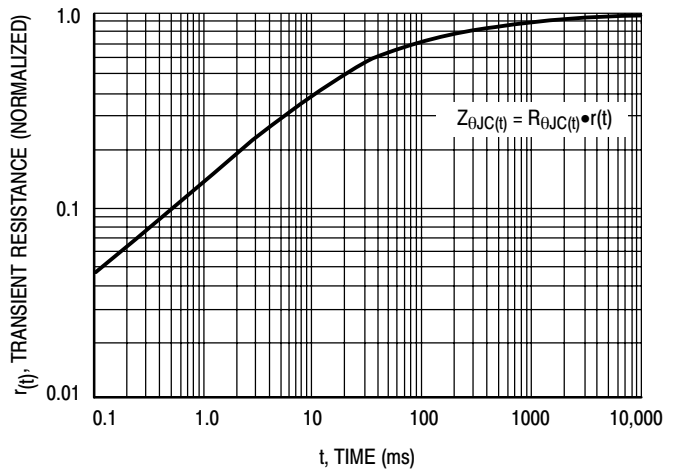


Figure 4. Transient Thermal Response

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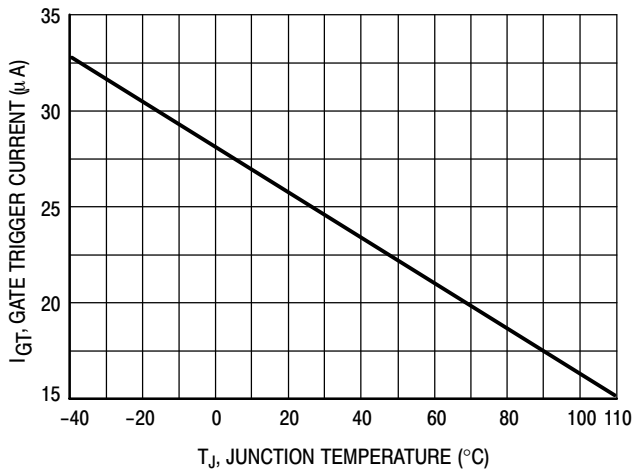


Figure 5. Typical Gate Trigger Current versus Junction Temperature

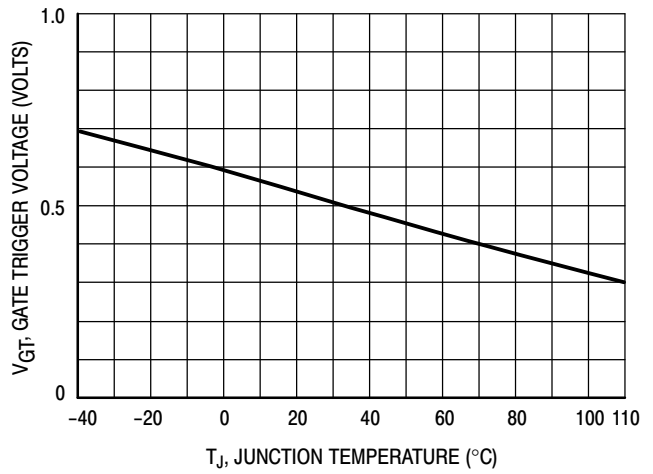


Figure 6. Typical Gate Trigger Voltage versus Junction Temperature

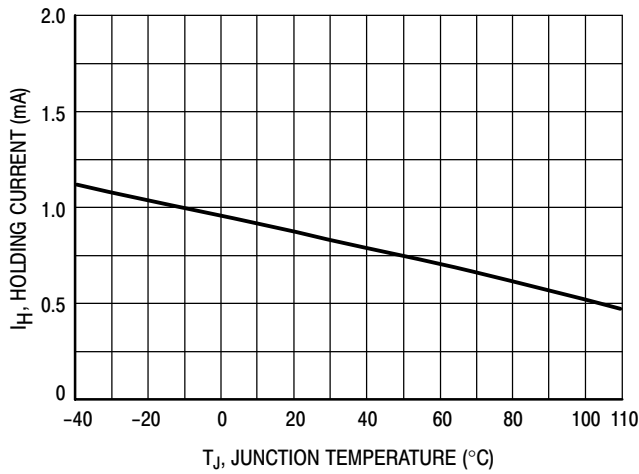


Figure 7. Typical Holding Current versus Junction Temperature

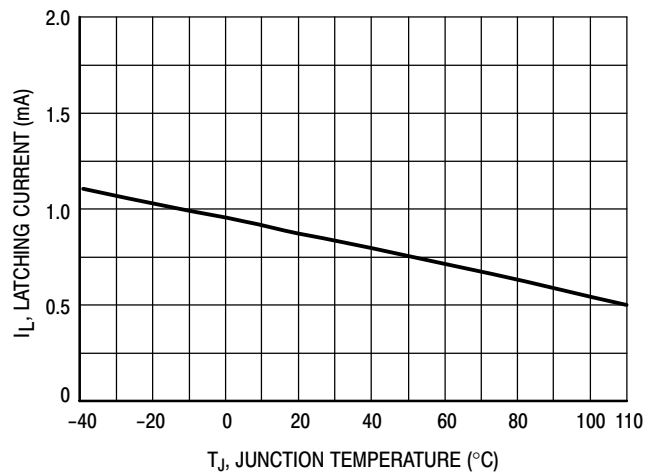
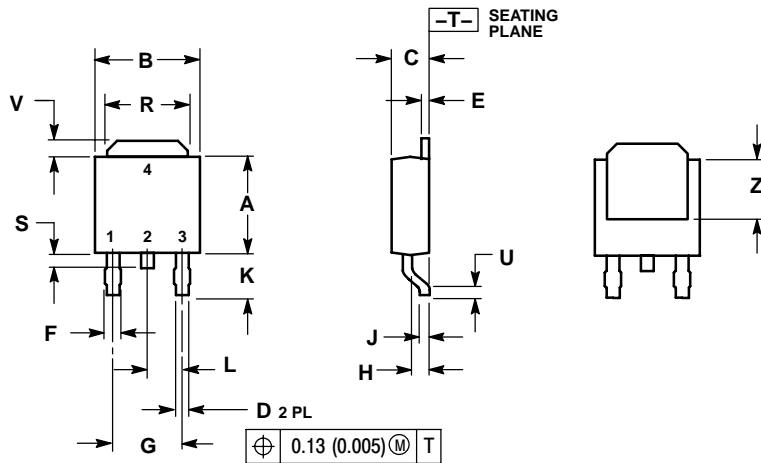


Figure 8. Typical Latching Current versus Junction Temperature

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PACKAGE DIMENSIONS

DPAK
CASE 369C
ISSUE O

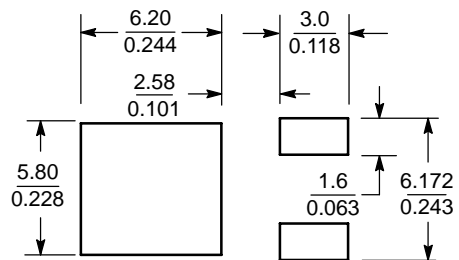


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



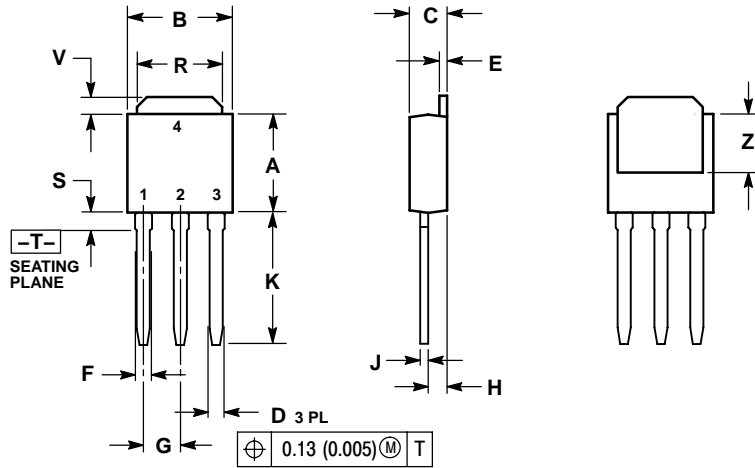
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

DKPAK-3
CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

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