Two cylinder small engine control IC

Powered by SMARTMOS technology, the 33814 delivers a cost-optimized IC solution for managing one and two-cylinder engines. With six drivers, three pre-drivers, a 5.0 V regulator for the MCU, a protected external sensor supply, and a high level of integration, the IC offers an ideal response to contemporary market requirements. The innovative VRS system optimizes noise immunity under cranking conditions. Diagnostic and protection features present on all outputs allow applications to operate with greater safety.

Features:

- Operates over supply voltage range of 4.5 V < V_{PWR} < 36 V
- Start-up/shutdown control and power sequence logic with KEYSW input
- MCU supply: V_{CC} is a 5.0 V (±2.0 %, 200 mA) regulated supply
- Sensor supply: V_{PROT} (100 mA) is a V_{CC} tracking protected sensor supply
- Three configurable pre-drivers for IGBT or general purpose gate MOSFETs for ignition and O_2 sensor (HEGO) heater:
  - PWM
  - Overcurrent shutdown
  - Short-to-battery shutdown
- Six low-side drivers with full diagnostics, self-protection and PWM control:
  - Two fuel injector drivers, $R_{DS(on)}$ = 0.6 Ω, I_{LIMIT} = 1.8 A, to drive typical 12 Ω high-impedance injectors
  - Relay 1 driver, $R_{DS(on)}$ = 0.4 Ω, I_{LIMIT} = 3.0 A, to drive fuel pump
  - Relay 2 driver, $R_{DS(on)}$ = 1.5 Ω, I_{LIMIT} = 1.2 A, to drive power relay
  - Lamp driver, $R_{DS(on)}$ = 1.5 Ω, I_{LIMIT} = 1.2 A, to drive warning lamp or an LED
  - Programmable Tachometer Driver, $R_{DS(on)}$ = 20 Ω, $I_{shutdown}$ = 60 mA, to drive a Tachometer display
- Innovative configurable VRS conditioning circuit, with two different parameter settings for engine cranking and running mode and an optional automatic mode to improve noise immunity in cranking conditions
- K-line (ISO9141)
- MCU reset generator and programmable watchdog
- MCU Interface: 16-bit SPI and parallel interface with 5.0 V IO capability

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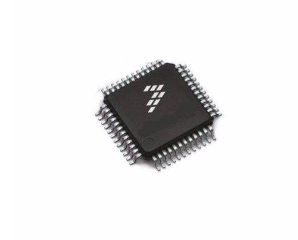
33814

TWO CYLINDER SMALL ENGINE CONTROL IC



98ASA00737D
AE SUFFIX (PB-FREE)
48-PIN LQFP-EP

Applications:

Small Engine Control for:

- Motor scooters
- Small motorcycles
- Lawn mowers
- Lawn trimmers
- Snow blowers
- Chain saws
- Gasoline-driven electrical generators
- Outboard motors

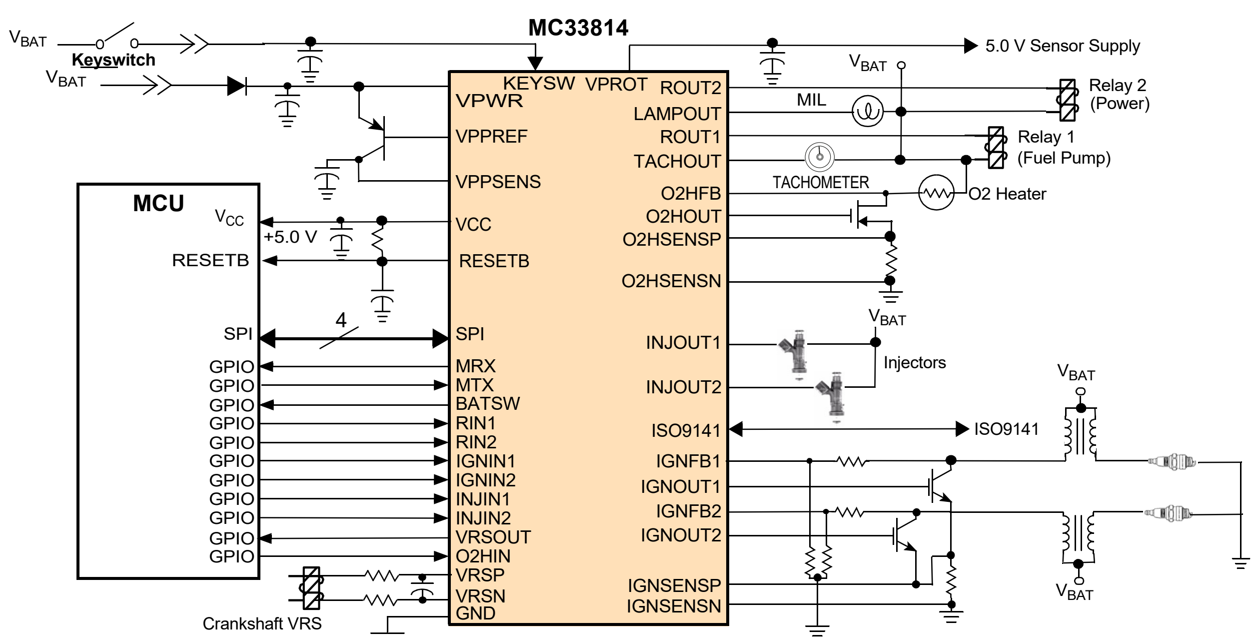


Figure 1. 33814 simplified application diagram

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1 Orderable parts

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	Package
MC33814AE	-40 °C to 125 °C	48 LQFP-EP

Notes

1. To order parts in tape and reel, add the R2 suffix to the part number.

2 Internal block diagram

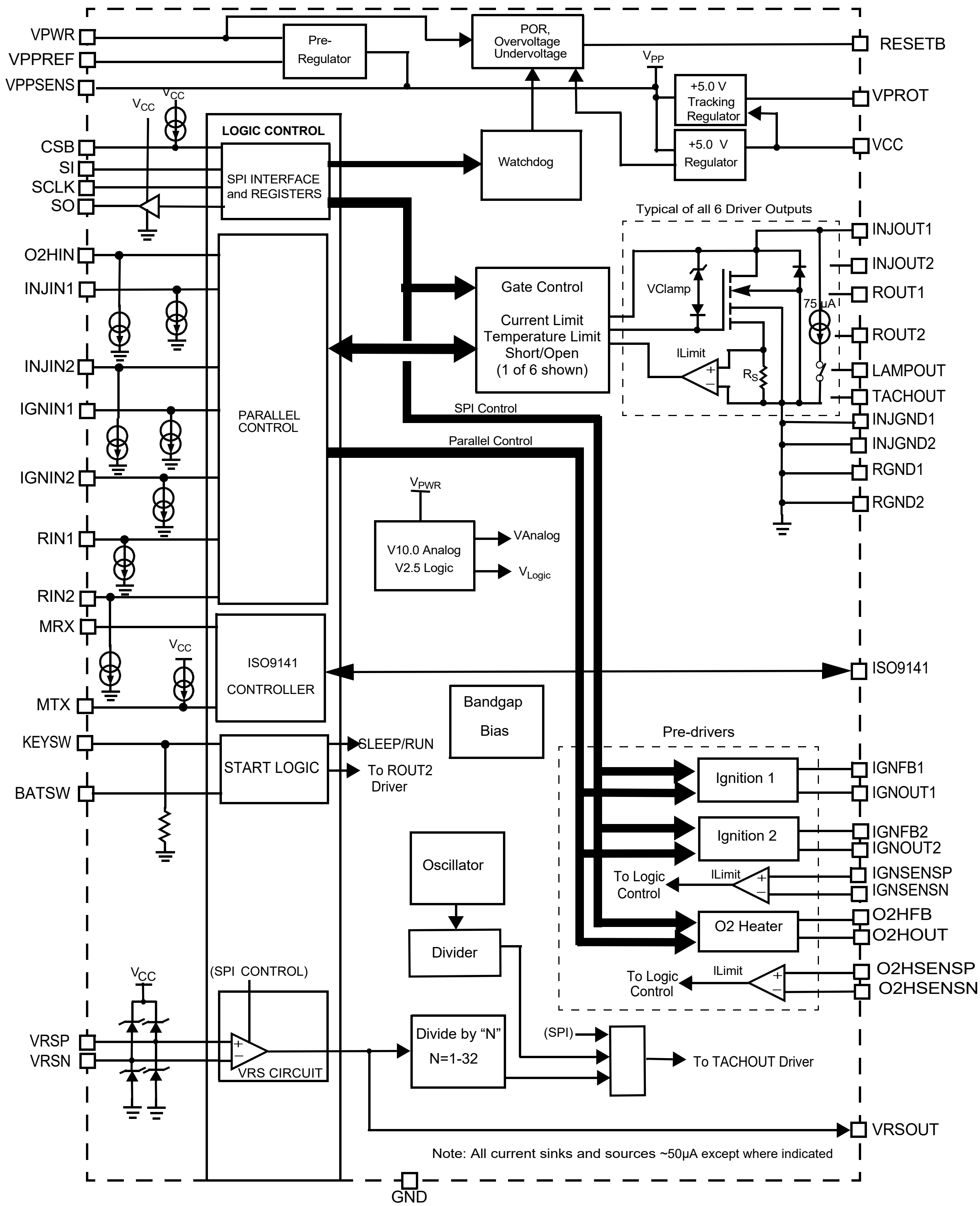


Figure 2. Simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

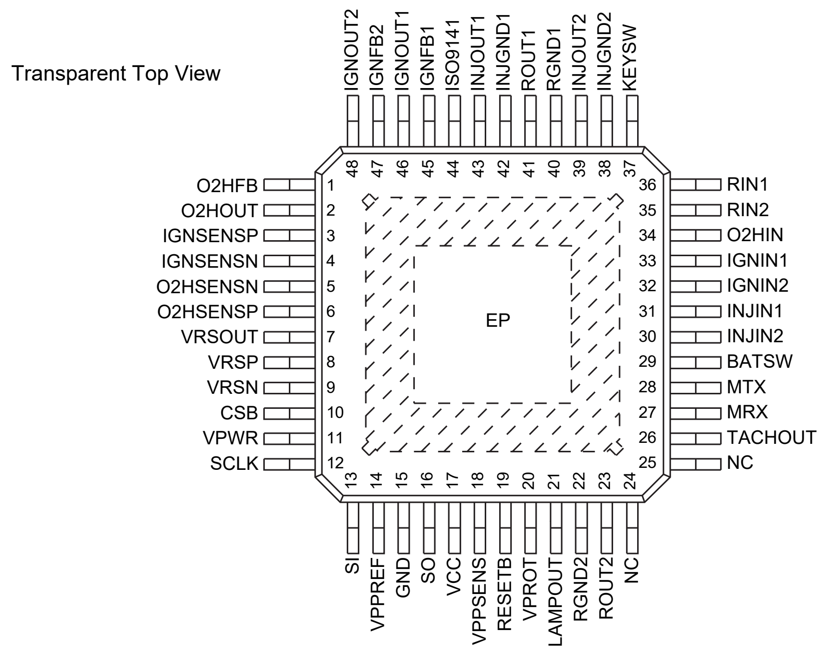


Figure 3. 33814 pin connections

3.2 Pin definitions

Table 2. 33814 pin definitions

Pin	Pin name	Pin function	Formal name	Description
1	O2HFB	Input	O2 Sensor Heater Feedback Input	Voltage feedback from drain of O2 Sensor Heater driver FET. If used as IGBT driver, voltage feedback from collector of IGBT through 10:1 voltage divider (9R:1R).
2	O2HOUT	Output	O2 Sensor Heater Output	Pre-driver output for O2 Sensor Heater driven by SPI input or O2HIN pin
3	IGNSENSP	Input	Ignition Current Sense Input Positive	Positive input to the ignition current sense differential amplifier. Measures current in IGBT emitter resistor (or MOSFET source resistor) for IGNOUT1 and IGNOUT2, if used
4	IGNSENSN	Input	Ignition Current Sense Input Negative	Negative input to the ignition current sense differential amplifier. Measures current in IGBT emitter resistor (or MOSFET source resistor) for IGNOUT1 and IGNOUT2, if used
5	O2HSENSN	Input	O2 Heater Current Sense Input Negative	Negative input to the O2 heater current sense differential amplifier. Measures current in of O2 heater driver MOSFET source resistor (or IGBT emitter resistor), if used
6	O2HSENSP	Input	O2 Heater Current Sense Input Positive	Positive input to the O2 heater current sense differential amplifier. Measures current in of O2 heater driver MOSFET source resistor (or MOSFET source resistor) for IGNOUT1 and IGNOUT2, if used
7	VRSOUT	Output	VRS Conditioned Output	5.0 V Logic Level Output from conditioned VRS differential inputs VRSP, VRSN

Table 2. 33814 pin definitions

Pin	Pin name	Pin function	Formal name	Description
8	VRSP	Input	Variable Reluctance Sensor Positive Input	The VRSP and VRSN form a differential input for the Variable Reluctance Sensor attached to the crankshaft toothed wheel.
9	VRSN	Input	Variable Reluctance Sensor Negative Input	The VRSP and VRSN form a differential input for the Variable Reluctance Sensor attached to the crankshaft toothed wheel.
10	CSB	Input	SPI Chip Select	The Chip Select input pin is an active low signal sent by the MCU to indicate that the device is being addressed.
11	VPWR	Supply Input	Main Voltage Supply Input	VPWR is the main voltage supply input for the device. Should be connected to a 12 Volt battery with reverse battery protection and adequate transient protection.
12	SCLK	Input	SPI Clock Input	The SCLK input pin is used to clock in and out the serial data on the SI and SO pins while being addressed by the CSB.
13	SI	Input	SPI Data Input	The SI input pin is used to receive serial data into the device from the MCU.
14	VPPREF	Output	VPP Reference Base Drive	Base drive for external PNP pass transistor
15	GND	Ground	Ground	Ground pin, return for all voltage supplies
16	SO	Output	SPI Data Output	The SO output pin is used to transmit serial data from the device to the MCU.
17	VCC	Supply	VCC Supply Protected Output	5.0 Volt supply output for MCU V_{CC}. This output supplies the V_{CC} voltage for 5.0 Volt MCUs. It is short-circuit and overcurrent protected.
18	VPPSENS	Input	Voltage Sense from VPP	Feedback to internal V_{PP} 6.5 Volt regulator from external pass transistor
19	RESETB	Output	RESETB Output to MCU	5.0 V Logic level reset signal used to reset the MCU during under and overvoltage conditions and for initial power-up, down and watchdog timeouts
20	VPROT	Output	Sensor Supply Protected Output	The VPROT Output is a protected 5.0 Volt output that tracks the V_{CC} voltage but isolates the VCC output against shorts to ground and to battery. It is intended to supply sensors which are located off of the ECU board.
21	LAMPOUT	Output	Warning Lamp Output	Low-side driver output for MIL (warning lamp) driven by SPI input command
22	RGND2	Ground	ROUT2 Power Ground	Ground connection for ROUT 2 low-side driver. Must be tied to VPWR Ground.
23	ROUT2	Output	Relay Driver 2 Output	Low-side relay driver output # 2 driven by SPI input command or RIN2 logic input
24, 25	N.C.	No Connect	Unused pin	
26	TACHOUT	Output	Tachometer output	This pin provides the low-side drive for a tachometer gauge or alternatively as a SPI controlled low-side driver, or oscillator output.
27	MRX	Output	Low-side Driver Output	Output 5.0 V logic level ISO9141 data to the MCU from the ISO9141 IN/OUT pin
28	MTX	Input	ISO9141 MCU Data Input	Input 5.0 V logic level ISO9141 data from the MCU to the ISO9141 IN/OUT pin
29	BATSW	Output	Battery Switch	This output is a 5.0 V logic level that is high when KEYSW is high. It is only low when KEYSW is low. It can also be controlled via the SPI.
30	INJIN2	Input	Injector Driver Input 2	5.0 V logic level input from the MCU to control the injector 2 driver output. (Can also be controlled via the SPI)
31	INJIN1	Input	Injector Driver Input 1	5.0 V logic level input from the MCU to control the injector 1 driver output. (Can also be controlled via the SPI)
32	IGNIN2	Input	Ignition Input 2	5.0 V logic level input from MCU controlling the ignition coil # 2 current flow and spark. (Can also be controlled via the SPI)
33	IGNIN1	Input	Ignition Input 1	5.0 V logic level input from MCU controlling the ignition coil # 1 current flow and spark. (Can also be controlled via the SPI)
34	O2HIN	Input	O2 Sensor Heater Input	5.0 V logic level input used to turn on and off the O2HOUT driver. The O2HOUT driver can also be turned on and off via the SPI if this pin is not present in a different package.
35	RIN2	Input	Relay Driver Input 2	5.0 V logic level input from the MCU to control the relay 2 driver output ROUT2. The ROUT2 driver can also be turned on and off via the SPI if this pin is not present in a different package.

Table 2. 33814 pin definitions

Pin	Pin name	Pin function	Formal name	Description
36	RIN1	Input	Relay Driver Input 1	5.0 V logic level input from the MCU to control the relay 1 driver output ROUT1. The ROUT1 driver can also be turned on and off via the SPI if this pin is not present in a different package.
37	KEYSW	Input	Key Switch Input	The Key Switch Input is a V_{PWR} level signal that indicates that the Key is inserted and turned to the ON/OFF position. In the ON position the (KEYSW = V_{BAT}) the IC is enabled and BATSW = HIGH (Relay 2 ON if programmed in the SPI). In the OFF position the IC is in Sleep mode, only when the PWREN bit in the SPI register is also low.
38	INJGND2	Ground	Injector Driver 2 Ground	Ground connection for injector 2 low-side driver. Must be tied to VPWR ground
39	INJOUT2	Output	Injector Driver 2 Output	Low-side driver output for injector 2 driven by the SPI input or by parallel input INJIN2
40	RGND1	Ground	ROUT1 Power Ground	Ground connection for ROUT 1 low-side driver. Must be tied to VPWR ground
41	ROUT1	Output	Relay Driver 1 Output	Low-side relay driver output # 1 driven by the SPI input command or RIN1 logic input
42	INJGND1	Ground	Injector Driver 1 Ground	Ground connection for injector 1 low-side driver. Must be tied to VPWR ground
43	INJOUT1	Output	Injector Driver 1 Output	Low-side driver output for injector 1 driven by the SPI input or by parallel input INJIN1
44	ISO9141	Input/Output	ISO9141 K-Line Bidirectional Serial Data Signal	ISO9141 pin is V_{PWR} level IN/OUT signal which is connected to an external ECU tester that uses the ISO9141 protocol.The output is open drain with an internal 32 kΩ pull-up resistor and the Input is a ratiometric V_{PWR} level threshold comparator.
45	IGNFB1	Input	Feedback from Collector 1	Voltage feedback from collector of ignition # 1 driver IGBT through 10:1 voltage divider (9R:1R)(or voltage feedback from the drain of the FET connected to IGNOUT1, if selected)
46	IGNOUT1	Output	Ignition Output 1	Output to gate of IGBT or GPGD for ignition # 1
47	IGNFB2	Input	Feedback from Collector 2	Voltage feedback from collector of ignition # 2 driver IGBT through 10:1 voltage divider (9R:1R)(or voltage feedback from the drain of the IGNOUT2 FET, if selected)
48	IGNOUT2	Output	Ignition Output 2	Output to gate of IGBT or GPGD for ignition # 2

4 General product characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

Symbol	Parameter	Min.	Max.	Unit	Notes
ELECTRICAL RATINGS					
V_{PWR}	V_{PWR} Supply Voltage	-0.3	45	V_{DC}	
V_{PP_Ext}	V_{PP} Supply Voltage (If supplied externally and not using internal VPP regulator) • VPP_{REF} • VPP_{SENSE}	 -0.3 -0.3	 45 10	V_{DC}	
V_{CC}	V_{CC} Regulator	-0.3	7.0	V_{DC}	
V_{PROT}	V_{PROT} Regulator	-0.3	V_{PWR}	V_{DC}	
V_{IL}, V_{IH}	SPI Interface and Logic Input Voltage (V_{SI}, V_{SCLK}, V_{CSB}, V_{RIN1}, V_{RIN2}, V_{INJIN1}, V_{INJIN2}, V_{IGNIN1}, V_{IGNIN2}, V_{O2HIN}, V_{MTX})	-0.3	V_{CC}	V_{DC}	
V_{IL}, V_{IH}	SPI Interface and Logic Output Voltage (V_{SO}, V_{BATSW}, V_{MRX}, V_{VRSOUT})	-0.3	V_{CC}	V_{DC}	
V_{OUTX}	All Low-side Drivers Drain Voltage ($V_{INJOUT1}$, $V_{INJOUT2}$, V_{ROUT1}, V_{ROUT2}, $V_{LAMPOUT}$, $V_{TACHOUT}$)	-0.3	V_{CLAMP}	V_{DC}	
V_{GDX}	All Pre-drivers Output Voltage ($V_{IGNOUT1}$, $V_{IGNOUT2}$, V_{O2HOUT})	-0.3	10	V_{DC}	
V_{GDFB}	All Pre-driver Feedback Inputs Voltage (V_{IGNFB1}, V_{IGNFB2}, V_{O2HFB})	-1.5	60	V_{DC}	
V_{ISENS}	All Pre-driver Current Sense Inputs Voltage ($V_{IGNSENSN}$, $V_{IGNSENSP}$, $V_{O2HSENSN}$, $V_{O2HSENSP}$)	-0.3	1.0	V_{DC}	
V_{KEYSW}	KEYSW Input Voltage (V_{KEYSW})	-18	V_{PWR}	V_{DC}	
V_{RESETB}	RESETB Output Voltage (V_{RESETB})	-0.3	V_{CC}	V_{DC}	
$V_{ISO9141}$	ISO9141 Input/Output Voltage ($V_{ISO9141}$)	-18	V_{PWR}	V_{DC}	
V_{VRS_IN}	Maximum Voltage for VRSN and VRSP inputs to ground	-0.5	6.0	V_{DC}	
I_{VRSX_IN}	Maximum Current for VRSN and VRSP inputs (internal diodes limit voltage)	-	15	mA	
E_{CLAMP}	Output Clamp Energy (INJOUT1, INJOUT2, ROUT1, ROUT2) • $T_{JUNCTION}$ = 150 °C, I_{OUT} = 1.0 A	-	100	mJ	
E_{CLAMP_LAMP}	Output Clamp Energy (LAMPOUT) • $T_{JUNCTION}$ = 150 °C, I_{OUT} = 0.5 A	-	35	mJ	
V_{ESD1} V_{ESD2} V_{ESD3}	ESD Voltage • Human Body Model (HBM) • Charge Device Model (CDM) (corner pins) • Charge Device Model (CDM)	 - - -	 ±2000 ±750 ±500	V	(2)

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model.

Table 3. Maximum ratings

All voltages are with respect to ground, unless mentioned otherwise. Exceeding these ratings may cause malfunction or permanent device damage.

Symbol	Parameter	Min.	Max.	Unit	Notes
THERMAL RATINGS					
T_A T_J T_C	Operating Temperature (Automotive grade version) • Ambient • Junction • Case	-40 -40 -40	125 150 125	°C	
T_{STG}	Storage Temperature	-55	150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	-	Note 4	°C	(3), (4)
Thermal Resistance and Package Dissipation Ratings					
$R_{\theta JA}$ $R_{\theta JC}$	Thermal Resistance • Junction-to-Ambient (LQFP-48-EP Package) (Single Layer Board) • Junction-to-Case (LQFP-48-EP Package)	29 2.4	29 2.4	°C/W	

Notes

3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. NXP’s Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes), enter the core ID to view all orderable parts and review parametrics.

4.2 Static electrical characteristics

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
POWER INPUT (VPWR)						
$V_{PWR(LS)}$ $V_{PWR(FO)}$ $V_{PWR(FP)}$	Supply Voltage (measured at VPWR pin) • Logic Stable Range • Full Operational Range • Full Parameter Specification Range	2.5 4.5 6.0	- - -	45 36 18	V	(5)
$I_{VPWR(ON)}$	Supply Current • All Outputs Disabled (Normal Mode), excludes base current to the external pnp	-	10.0	14.0	mA	
$I_{VPWR(SS)}$	Sleep State Supply Current (Must have PWREN = 0 and KEYSW ≤ 0.8 V for sleep state) • V_{PWR} = 18 V	-	10	20	µA	
$V_{PWR(OV)}$	V_{PWR} Overvoltage Shutdown Threshold Voltage (OV Reset)	37.5	39	42	V	(6)
$V_{PWR(OV-HYS)}$	V_{PWR} Overvoltage Shutdown Hysteresis Voltage	0.5	1.5	3.0	V	
$V_{CC(POR)}$	V_{CC} Power On Reset Voltage Threshold (POR), (rising voltage)	3.9	-	4.9	V	
$V_{CC(UV)}$	V_{CC} Undervoltage Shutdown Threshold Voltage (UV Reset), (falling voltage)	2.9	-	3.9	V	(7)
$V_{CC(UV/POR-HYS)}$	V_{CC} POR and Undervoltage Shutdown Hysteresis Voltage	100	-	-	mV	
$V_{CC,NONOVERLAP}$	V_{CC} POR and Undervoltage Non-overlap (POR-UV)	0.8	1.0	1.2	V	
VOLTAGE PRE-REGULATOR OUTPUT (VPPREF, VPPSENS)						
V_{PPSENS}	VPPSENS Output Voltage	5.85	6.5	7.15	V	(8)
I_{VPPREF_CL}	VPPREF Current Limit	-5.0	-15	-20	mA	
V_{OCE}	Output Capacitance External (ceramic)	2.2	-	25	µF	
$I_{VPPSENS}$	VPPSENS Quiescent Current (excluding external PNP current)	-	-	3	mA	
$REGLINE_{\_VPP}$	Line Regulation I_{VCC} = 100 mA, I_{VPROT} = 50 mA, 9.0 V < V_{PWR} < 18 V and Diodes Inc. FZT753TA PNP	-	2.0	25	mV	
$V_{DROPOUT\_VPP}$	Dropout Voltage (Minimal Input/Output Voltage, tracks input below) I_{VCC} = 100 mA, I_{VPROT} = 50 mA and Diodes Inc. FZT753TA PNP	-	-	500	mV	
VOLTAGE REGULATOR OUTPUTS (VCC, VPROT)						
V_{CC}	VCC Output Voltage 0 ≤ I_{VCC} ≤ I_{VCC_C}	4.9	5.0	5.1	V	
I_{VCC_C}	VCC Output Current Continuous	-	-	200	mA	
$\|V_{CC}-V_{PROT}\|$	VPROT Output Voltage (tracks VCC) I_{VCC} = 100 mA, I_{VPROT} = 50 mA 9.0 V < V_{PWR} < 18 V	-	-	25	mV	
I_{VPROT_C}	VPROT Output Current Continuous	-	-	100	mA	
I_{VCC_CL}	VCC Output Current Limiting	200	-	500	mA	(8)
I_{VPROT_CL}	VPROT Output Current Limiting	110	-	260	mA	
V_{OCE}	Output Capacitance External (V_{CC} and V_{PROT}) without reverse protection diode	2.2	-	47	µF	

Notes
5. This parameter is guaranteed by design but is not production tested.
6. Overvoltage thresholds minimum and maximum include hysteresis.
7. Undervoltage thresholds minimum and maximum include hysteresis
8. Guaranteed at 9.0 V ≤ V_{PWR} ≤ 18 V

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VOLTAGE REGULATOR OUTPUTS (VCC, VPROT) (CONTINUED)						
V_{CC}	VCC Output Voltage 0 ≤ I_{VCC} ≤ I_{VCC_C}	4.9	5.0	5.1	V	
REG_{LINE_VB}	Line Regulation (Both V_{CC} and V_{PROT}) I_{VCC} =100 mA, I_{PROT} = 50 mA, 9.0 V< V_{PWR} < 18 V	-	2.0	25	mV	
REG_{LOAD_VB}	Load Regulation (Both V_{CC} and V_{PROT}) measured from 10 % to 90 % of I_{VCC_C} and I_{PROT_C}, V_{PWR} = 13 V	-	20	35	mV	
$V_{DROPOUT\_VCC/VPROT}$	Dropout Voltage (Both V_{CC} and V_{PROT}) (Minimal Input/Output Voltage I_{VCC} = 100 mA, I_{VPROT} = 50 mA, tracks input below)	-	-	500	mV	
ALL LOW-SIDE DRIVERS (INJOUT1, INJOUT2, ROUT1, ROUT2, LAMPOUT, TACHOUT)						
$V_{OUT(FLT-TH)}$	Output Fault Detection Voltage Threshold used for Short to battery and open load detections	2.0	2.5	3.0	V	(9)
$I_{(OFF)OCO}$	Output OFF Open Load Detection Current (INJ1, INJ2, RELAY1, RELAY2 AND LAMP) • V_{DRAIN} = 18 V, Outputs Programmed OFF	40	75	115	µA	
$I_{(OFF)TACH}$	Output OFF Open Load Detection Current TachOut	10	-	30	µA	
$I_{OUT(LKG)}$	Output Leakage Current • V_{DRAIN} = 24 V, Open Load Detection Disabled and Output commanded OFF	-	-	20	µA	
T_{LIM}	Overtemperature Shutdown (OT)	155	-	185	°C	(9)
$T_{LIM(HYS)}$	Overtemperature Shutdown Hysteresis	5.0	10	15	°C	(9)
V_{OC}	Output Clamp Voltage • I_D = 20 mA	48	53	60	V	
INJOUT1, INJOUT2						
$R_{DS(ON)\_INJx}$	Drain-to-Source ON Resistance • I_{OUT} = 1.0 A T_J = 150 °C, V_{PWR} = 13 V	-	-	0.6	Ω	
$I_{OUT(LIM)\_INJx}$	Output Self Limiting Current	1.8	-	3.0	A	
ROUT1						
$R_{DS(ON)\_R1}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 700 mA, T_J = 150 °C, V_{PWR} = 13 V	-	-	0.4	Ω	
$I_{OUT(LIM)\_R1}$	Output Self-limiting Current (Has inrush current timer)	3.0	-	6.0	A	
ROUT2						
$R_{DS(ON)\_R2}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 350 mA, T_J = 150 °C, V_{PWR} = 13 V	-	-	1.5	Ω	
$I_{OUT(LIM)\_R2}$	Output Self-limiting Current	1.2	-	2.4	A	
LAMPOUT						
$R_{DS(ON)\_LAMP}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 1.0 A, T_J = 150 °C, V_{PWR} = 13 V	-	-	1.5	Ω	
$I_{OUT(LIM)\_LAMP}$	Output Self-limiting Current (Has inrush current timer)	1.2	-	2.4	A	

Notes
9. This parameter is guaranteed by design, however it is not production tested.

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
TACHOUT						
$R_{DS(ON)\_TACH}$	Driver Drain-to-Source ON Resistance • I_{OUT} = 50 mA, T_J = 150 °C, V_{PWR} = 13 V	-	-	20	Ω	
$I_{OUT(SHUTDOWN)\_TACH}$	Output Current Shutdown	60	-	110	mA	
ALL PRE-DRIVERS (IGNOUT1, IGNOUT2 AND O2HOUT)						
$V_{GS(ON)}$ $V_{GS(OFF)}$	Pre-driver Output Voltage, V_{PWR} = 13 V • I_{GD} = 500 µA • I_{GD} = -500 µA	7.0 0.0	8.0 0.375	9.0 0.5	V	
$I_{IGN\_GD\_H}$	IGNOUTx Output Source Current (IGNOUT1 and IGNOUT2 by default) • 1.0 ≤ V_{GD} ≤ 3.0, V_{PWR} = 13 V	10	-	-	mA	
$I_{(OFF)OCO}$	Output OFF Open Load Detection Current • V_{DRAIN} = 18 V, Outputs Programmed OFF	40	75	115	µA	
$I_{GPGD\_GD\_H}$	GPGD Output Source Current (O2HOUT by default) at 1.0 ≤ V_{GD} ≤ 3.0, V_{PWR} = 13 V	10	-	-	mA	
$V_{IGNFB(FLT-TH)}$ $V_{GPGD(FLT\_TH)}$	Pre-driver Fault Detection Voltage Threshold, Outputs programmed OFF (open load), Outputs programmed ON (short to battery) • I_{GD} = 500 µA • I_{GD} = -500 µA	100 1.0	250 2.5	400 4.0	mV V	
V_{CLAMP}	Output Clamp Voltage	48	53	60	V	
$V_{SENS-TH}$	Overcurrent Voltage Threshold for O2HOUT • $V_{O2HSENSN}$ to $V_{O2HSENSP}$	180	200	220	mV	
$V_{SENS-TH}$ $V_{SENS-TH}$	Overcurrent Voltage Threshold for IGNOUT1 and IGNOUT2 • $V_{IGNSENSN}$ to $V_{IGNSENSP}$ • $V_{IGNSENSN}$ to $V_{IGNSENSP}$ (if both IGNOUT1 and IGNOUT2 are configured as IGBT gate drivers and both IGNOUT1 and IGNOUT2 are ON)	180 360	200 400	220 440	mV	(10)
$I_{SENS-OFFSET}$	Current Sense Input Offset Current (IGNSENSP, IGNSENSN, O2HSENSN, O2HSENSP)	-	-	15	µA	
$I_{SENS-BIAS}$	Current Sense Input Bias Current	-	-	15	µA	
ISO-9141 TRANSCEIVER PARAMETERS (8.0 V < V_{PWR} < 18 V)						
V_{IL_ISO}	Input Low Voltage at ISO I/O pin	-	-	0.3xV_{PWR}	V	
V_{IH_ISO}	Input High Voltage at ISO I/O pin	0.7*V_{PWR}	-	-	V	
V_{HYST_ISO}	Input Hysteresis at ISO I/O pin	0.15x V_{PWR}	-	-	V	
V_{OL_ISO}	Output Low-voltage at ISO I/O pin	-	-	0.2xV_{PWR}	V	
V_{OH_ISO}	Output High-voltage at ISO I/O pin	0.8x V_{PWR}R	-	-	V	
I_{PU}	Internal pull-up resistor to V_{PWR}	-	32	-	kΩ	
I_{LIM_ISO}	Output current limit at ISO I/O pin (MTX = 0)	50	100	150	mA	

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
C_{L_ISO}	Load capacitance at ISO I/O pin	0.01	3.0	10	nF	(11)
$I_{\_ISO}$	Output load current at ISO I/O pin (MTX = 0, RLOAD = 1.0 kΩ, ±10 %)	-	12	-	mA	
T_{LIM}	Overtemperature Shutdown (OT)	155	-	185	°C	(11)
$T_{LIM(HYS)}$	Overtemperature Shutdown Hysteresis	5.0	10	15	°C	(11)

Notes

10. 400 mV threshold is only valid when both IGNOUT are configured as IGBT gate drivers and both IGNOUT1 and IGNOUT2 are ON.
11. This parameter is guaranteed by design, however it is not production tested.

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
VRS CONDITIONER INPUT						
V_{VRS_THRESH}	Comparator Thresholds	-	See Table variable via SPI or dynamically		mV	
$Accu_{THRESH}$	Threshold Accuracy Steady State Condition (±20 % only valid for VRS DAC thresholds 110 mV and higher.All other thresholds guaranteed monotonic only.)	-	-	±20	%	
$I_{BIASRSX}$	Input Bias Current VRSP and VRSN (2.5 V common mode must be off)	-5.0		5.0	µA	
V_{CLAMP_P}	VRS Positive Clamp Voltage at I_{CLAMP} = 10 mA	5.5	-	5.8	V	
V_{CLAMP_N}	VRS Negative Clamp Voltage at I_{CLAMP} = 10 mA	-0.45	-	-0.22	V	
DIGITAL INTERFACE (MRX, MTX,CSB, SI, SCLK, SO, RINX,O2HIN, INJINX, IGNINX, BATSW, VRSOUT, RESETB)						
V_{IH}	Input Logic High-voltage Thresholds	0.7 x V_{CC}	-	V_{CC} + 0.3	V	
V_{IL}	Input Logic Low-voltage Thresholds	GND - 0.3	-	0.2 x V_{CC}	V	
V_{HYS}	Input Logic Voltage Hysteresis	500	-	-	mV	
C_{IN}	Input Logic Capacitance	-	-	20	pF	
I_{LOGIC_SS}	Sleep Mode Input Logic Current • KEYSW = 0 V	-10	-	10	µA	(12)
I_{LOGIC_PD}	Input Logic Pull-down Current INJIN1, INJIN2, RIN1, RIN2, SI, SCLK, IGNIN1, IGNIN2, O2HIN • 0.8 V to 5.0 V	30	50	100	µA	(12)
I_{TRISO}	SO Tri-state Output (in Tri-state mode, CSB = 1) • 0 V to 5.0 V	-10	-	10	µA	
I_{CSB}	CSB Input Current • CSB = V_{CC}	-10	-	10	µA	
I_{LOGIC_PU}	Input Logic Pull-up Current - CSB and MTX • 0.0 to 4.2 V	-20	-40	-90	µA	
$I_{CSB(LKG)}$	CSB Leakage Current to V_{CC} • CSB = 5.0 V, KEYSW = 0.0 V	-	-	10	µA	
V_{SO_HIGH} V_{MRX_HIGH}	SO, MRX High-state Output Voltage (CSB =0 for SO) • $I_{SO\text{-}HIGH}$ = -1.0 mA	V_{CC} - 0.4	-	-	V	
V_{SO_LOW} V_{MRX_LOW}	SO, MRX Low-state Output Voltage (CSB =0 for SO) • $I_{SO\text{-}LOW}$ = 1.0 mA	-	-	0.4	V	
V_{BATSW_HIGH}	BATSW High-state Output Voltage • $I_{SO\text{-}HIGH}$ = -10 mA	V_{CC} - 1.0	-	-	V	
V_{BATSW_LOW}	BATSW Low-state Output Voltage • $I_{SO\text{-}LOW}$ = 10 mA	-	-	1.0	V	
V_{KEYSW_HIGH}	KEYSW High-state Input Voltage	4.5	-	V_{PWR}	V	
V_{KEYSW_LOW}	KEYSW Low-state Input Voltage	-0.3	-	2.5	V	
V_{KEYSW_HYS}	KEYSW Hysteresis	100	-	-	mV	

Notes

12. This parameter is guaranteed by design, however it is not production tested.

Table 4. Power input static electrical characteristics

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter’s approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
DIGITAL INTERFACE (MRX, MTX,CSB, SI, SCLK, SO, RINX,O2HIN, INJINX, IGNINX, BATSW, VRSOUT, RESETB) (CONTINUED)						
V_{VRSOUT_LOW}	VRS Low-state Output Voltage • $I_{VRS-LOW}$ = 1.0 mA	-	-	0.4	V	
V_{VRSOUT_HIGH}	VRS High-state Output Voltage • $I_{VRS-HIGH}$ = 1.0 mA	V_{CC} -0.4	-	5.0	V	
V_{RESET_LOW}	RESET Low-state Output Voltage • $I_{RESET-LOW}$ = 1.0 mA	-	-	0.4	V	
$I_{RESET\_LEAKAGE\_HIGH}$	RESET High-state Leakage Current	-	-	25	µA	
$R_{RESET\_PULDOWN}$	RESET Pull-down Resistor	200	-	500	kΩ	

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics [14]

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
POWER INPUT						
t_{RESET}	Required Low State Duration on V_{CC} for power-on reset • V_{CC} ≤ 0.2 V	1.0	-	-	µs	
$t_{(POR)}$	Power on RESET pulse width	100	-	-	µs	
$t_{(KEYSW\_FILTER)}$	KEYSW Filter Time	-	12.7	-	ms	(13)
WATCHDOG TIMER						
WDMAX	Maximum Time Value Watchdog can be loaded with (default time)	-	-	10	sec.	
WD_{MIN}	Minimum Time Value Watchdog can be loaded with	1.0	-	-	ms	
WD_{RESET}	Reset Pulse Width when Watchdog time is out	100	-	-	µs	
VRS CONDITIONING INPUT						
$OUTPUT_{BLANK}$	Output Blanking Time Programming Range (% of previous out pulse 0 to 15/32 in 1/32 steps, 15/32 = 46.9 %)	0	-	50	%	
$OUTPUT_{DEGLITCH}$	Output Deglitch Filter Time (1/128 of the previous output pulse)	-	1.0	-	%	
$DELAY_{THRESH}$	Delay from CSB to Change in VRS Comparator Threshold	-	-	10	µs	(13)
$DELAY_{OBT}$	Delay from CSB to Change in VRS Output Blank Time	-	-	10	µs	(13)
ISO9141 TRANSCEIVER						
ISO_{BR}	Typical ISO9141 Data Rate	-	10	-	kbps	
t_{TXDF}	Turn OFF Delay MTX Input to ISO Output	-	-	2.0	µs	
t_{RXDF}, t_{RXDR}	Turn ON/OFF Delay ISO Input to MRX Output	-	-	1.0	µs	
t_{RXR}, t_{RXF}	Rise and Fall Time MRX Output (measured from 10 % to 90 %)	-	-	1.0	µs	
t_{TXR}, t_{TXF}	Maximum Rise and Fall Time MTX Input (measured from 10 % to 90 %)	-	-	1.0	µs	
ALL LOW-SIDE DRIVERS						
t_{SC1}	Output ON Current Limit Fault Filter Timer	30	60	90	µs	
t_{REF}	Output Retry Timer	7.0	10	13	ms	
t_{INRUSH}	Inrush Current Delay Timer	7.0	10	13	ms	(13)
$t_{(OFF)OC}$	Output OFF Open-circuit Fault Filter Timer	100	-	400	µs	
$t_{SR(RISE)}$	Output Slew Rate, INJOUT1, INJOUT2, ROUT1, ROUT2 and LAMPOUT • R_{LOAD} = 500 Ω, V_{LOAD} = 14 V	1.0	5.0	10	V/µs	
$t_{SR(FALL)}$	Output Slew Rate, INJOUT1, INJOUT2, ROUT1, ROUT2 and LAMPOUT • R_{LOAD} = 500 Ω, V_{LOAD} = 14 V	1.0	5.0	10	V/µs	
t_{PHL}	Propagation Delay (Input Rising Edge OR CSB to Output Falling Edge) • Input at 50 % V_{DD} to Output voltage 90 % of V_{LOAD} (INJ1, INJ2, ROUT1, ROUT2, LAMP)	-	1.0	5.0	µs	
t_{PHL}	Propagation Delay (Input Rising Edge OR CSB to Output Falling Edge) • Input at 50 % V_{DD} to Output voltage 90 % of V_{LOAD} (TACHOMETER)	-	1.0	6.0	µs	

Notes
13. Guaranteed by design
14. internal oscillator of 4.0 MHz ±10 % typical for V_{PWR} = 13 V, at room temp.

Table 5. Dynamic electrical characteristics [14]

Characteristics noted under conditions of 6.0 V ≤ V_{PWR} ≤ 18 V, -40 °C ≤ T_{CASE} ≤ 125 °C and Calibrated Timers, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 14 V, T_A = 25 °C.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
ALL LOW-SIDE DRIVERS (CONTINUED)						
t_{PLH}	Propagation Delay (Input Falling Edge OR CSB to Output Rising Edge) • Input at 50 % V_{DD} to Output voltage 10 % of V_{LOAD} (INJ1, INJ2, ROUT1, ROUT2, LAMP)	-	1.0	5.0	µs	
t_{PLH}	Propagation Delay (Input Falling Edge OR CSB to Output Rising Edge) • Input at 50 % V_{DD} to Output voltage 10 % of V_{LOAD} (TACHOMETER)	-	1.0	6.0	µs	
$t_{SR(FALL)}$	Output Slew Rate, Tachout • R_{LOAD} = 500 Ω, V_{LOAD} = 14 V	6.0	-	14	V/µs	
ALL GATE PRE-DRIVER (IGN1, IGN2 AND O2H)						
$t_{(OFF)OC}$	Output OFF Open-circuit Fault Filter Timer	100	-	400	µs	
t_{SC1}	Overcurrent (short-circuit) Fault Filter Timer	30	-	90	µs	
t_{PLH}	Propagation Delay (Input Rising Edge OR CSB to Output Rising Edge) • Input at 50 % V_{DD} to Output voltage 10 % of $V_{GS(ON)}$	-	1.0	5.0	µs	
t_{PHL}	Propagation Delay (Input Falling Edge OR CSB to Output Falling Edge) • Input at 50 % V_{DD} to Output voltage 90 % of $V_{GS(ON)}$	-	1.0	5.0	µs	
SPI DIGITAL INTERFACE TIMING [15]						
t_{LEAD}	Falling Edge of CSB to Rising Edge of SCLK • Required Setup Time	100	-	-	ns	
t_{LAG}	Falling Edge of SCLK to Rising Edge of CSB • Required Setup Time	50	-	-	ns	
$t_{SI(SU)}$	SI to Rising Edge of SCLK • Required Setup Time	16	-	-	ns	
$t_{SI(HOLD)}$	Rising Edge of SCLK to SI • Required Hold Time	20	-	-	ns	
$t_{R(SI)}$	SI, CSB, SCLK Signal Rise Time [16]	-	5.0	-	ns	
$t_{F(SI)}$	SI, CSB, SCLK Signal Fall Time [16]	-	5.0	-	ns	
$t_{SO(EN)}$	Time from Falling Edge of CSB to SO Low-impedance [17]	-	-	55	ns	
$t_{SO(DIS)}$	Time from Rising Edge of CSB to SO High-impedance	-	-	55	ns	
t_{VALID}	Time from Falling Edge of SCLK to SO Data Valid [18]	-	25	55	ns	
t_{STR}	Sequential Transfer Rate [15] • Time required between data transfers	-	-	1.0	µs	

Notes

15. These parameters are guaranteed by design. Production test equipment uses 1.0 MHz, 5.0 V SPI interface (variable with magnitude input frequency).
16. Rise and Fall time of incoming SI, CSB and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
17. Time required for output states data to be terminated at SO pin.
18. Time required to obtain valid data out from SO following the fall of SCLK with 200 pF load.

4.4 Timing diagrams

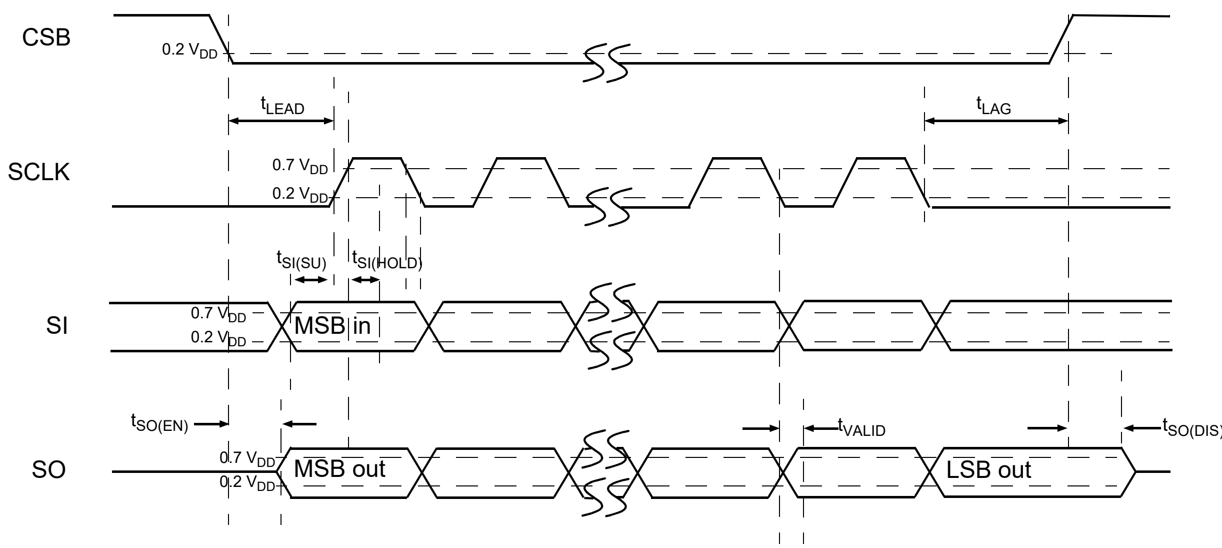


Figure 4. Timing diagram

4.5 Typical electrical characteristics

4.5.1 Driver and gate driver characteristics

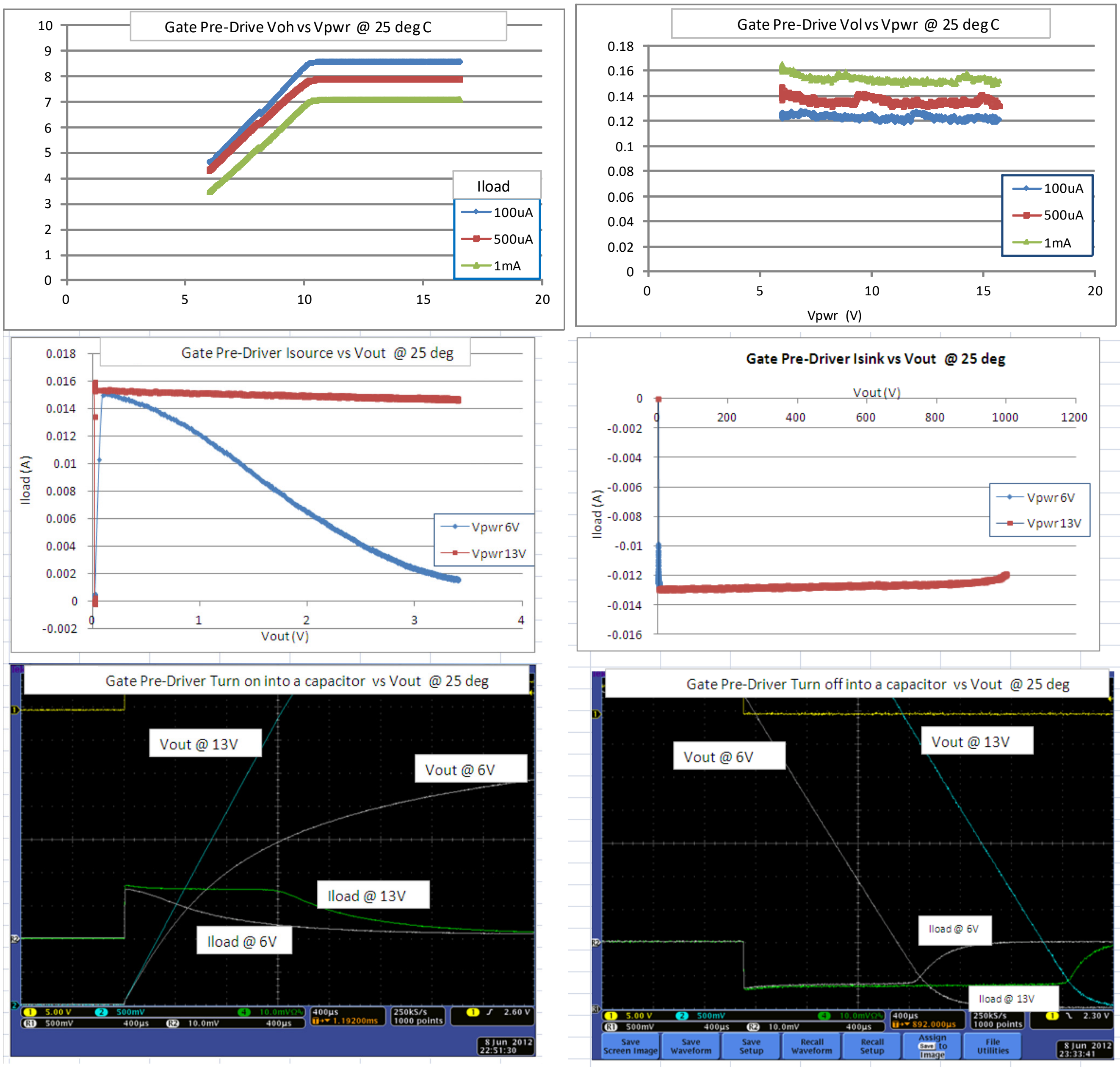


Figure 5. Typical electrical specifications

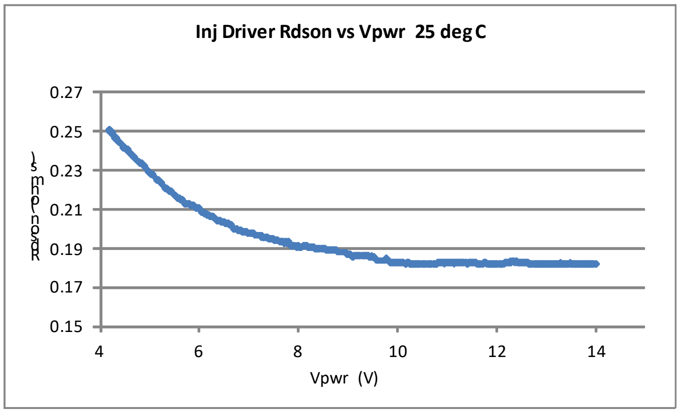


Figure 6. Typical electrical specifications (continued)

4.5.2 V_{CC} and V_{PROT} characteristics

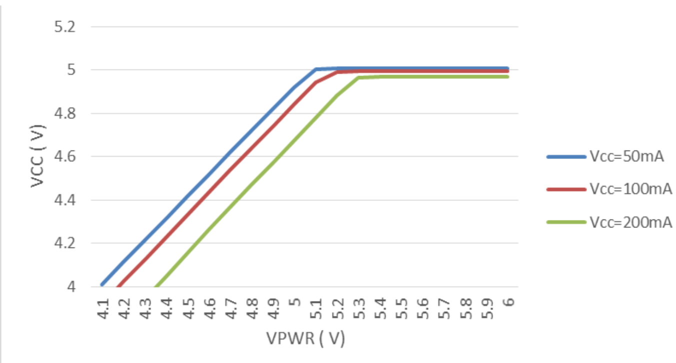


Figure 7. V_{CC} voltage vs. V_{PWR} at 125 °C

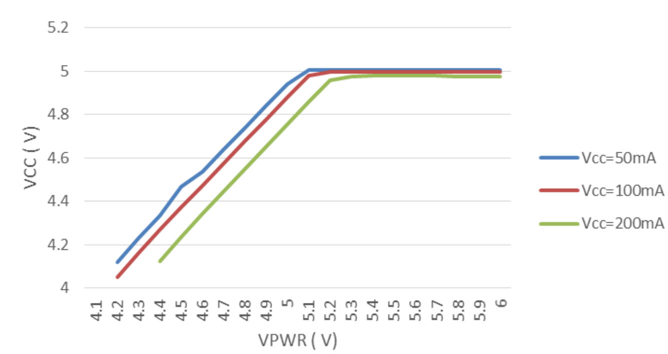


Figure 8. V_{CC} voltage vs. V_{PWR} at 25 °C

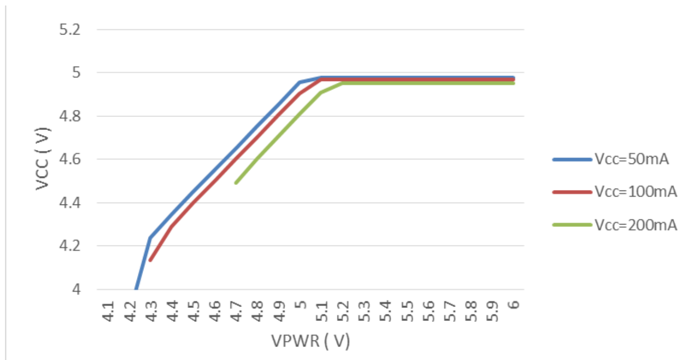


Figure 9. V_{CC} voltage vs. V_{PWR} at -40 °C

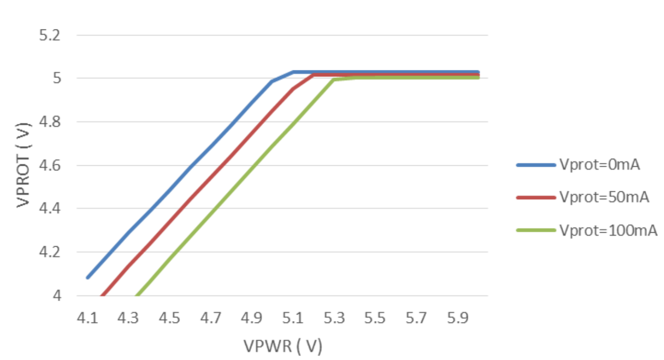


Figure 10. V_{PROT} voltage vs. V_{PWR} at 125 °C

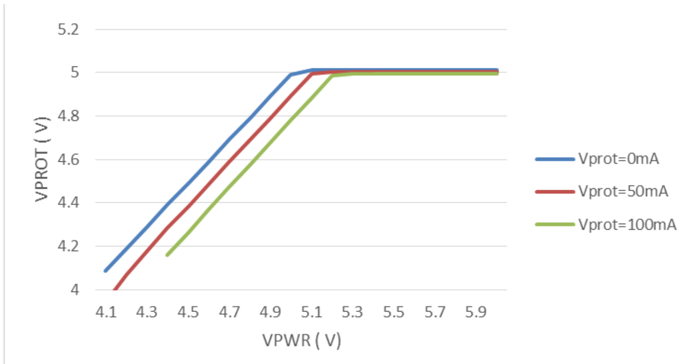


Figure 11. V_{PROT} voltage vs. V_{PWR} at 25 °C

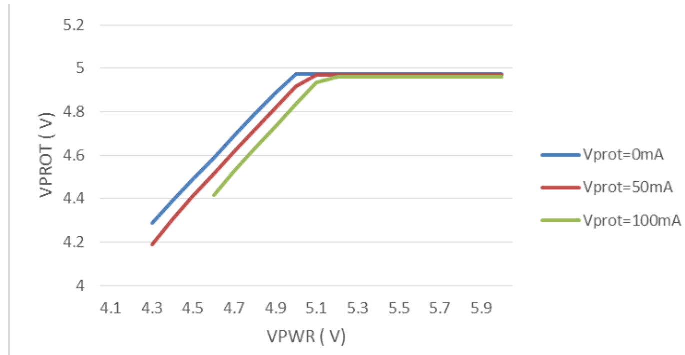


Figure 12. V_{PROT} voltage vs. V_{PWR} at -40 °C

5 General IC functional description and application information

5.1 System controller

5.1.1 System control signals

5.1.1.1 KEYSW input pin

KEYSW is the input from the vehicle ignition key switch. This signal is at V_{BAT} (12 V) when the key is inserted and turned to the ON position. When the key is in the OFF position and/or removed from the key switch, this input is pulled to ground by an internal pull-down resistor. This pin is internally protected against a reverse battery condition by an internal diode. The state of the KEYSW input is also available as a bit in the SPI Status Register.

5.1.1.2 BATSW output pin

The BATSW output pin is a 5.0 V logic level output, which by default is an indication of the state of the KEYSW input.

5.1.1.3 PWREN SPI control register BIT

The PWREN signal is a bit in the SPI Control Register #1 allowing “Prepare to shutdown” state transition.

5.1.2 Operating modes

5.1.2.1 Power On Reset (POR)

Applying V_{PWR} and bringing KEYSW high (VBAT), longer than the KEYSW filter time, generates a Power On Reset (POR) and places the device in the Normal operating state. The Power On Reset circuit incorporates a timer to prevent high frequency transients from causing an erroneous POR. Upon enabling the device (KEYSW High), outputs are activated based on the initial state of the control register or parallel input. All three supplies, V_{PP}, V_{CC} and V_{PROT}, are enabled when KEYSW is brought high.

Table 6. Operational states

KEYSW Input	PWREN SPI Bit Input	BATSWB Output	All Supplies	STATE
L	L	L	OFF	Sleep
H	L	H	ON	NORMAL
H	H	H	ON	NORMAL
L	H	L	ON	Prepare to shutdown

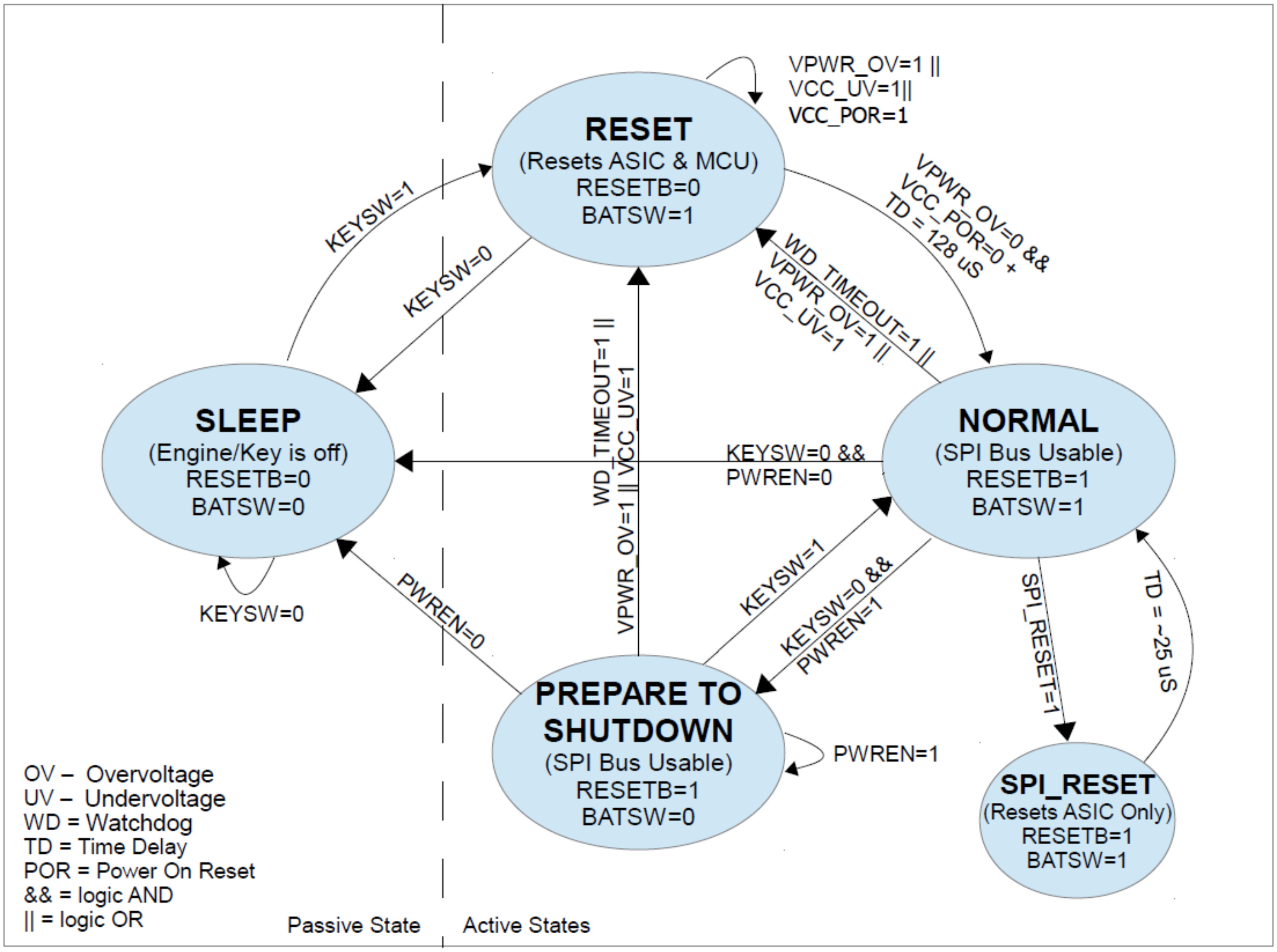


Figure 13. 33814 functional state diagram

5.1.2.2 Normal state

The default Normal state is entered when power is applied to the VPWR and KEYSW pins. Note that the device is designed to have VPWR present before KEYSW is brought high. It is acceptable to bring VPWR and KEYSW high simultaneously. However it is not recommended to bring KEYSW high while VPWR is low.

SPI register settings from Power On Reset (POR) are as follows:

- All outputs turned off
- Off State open load detection enabled (LSD)
- Default values in the SPI Configuration, Control and Status registers

5.1.2.3 Sleep state

When KEYSW signal is low and the PWREN SPI Control register bit is also low, the 33814 enters into Sleep mode. In the Sleep state, all outputs, current sources and sinks are off and the device consumes less than $I_{VPWR(SS)}$. When KEYSW signal goes high, it wakes up the IC, turns on the V_{PP} regulator and a Power On Reset signal is generated.

5.1.2.4 Prepare to shutdown state

The purpose of the PWREN signal is to allow the MCU to control the shutdown of power to itself when the user turns off the KEYSW. This may be necessary to allow the MCU the time required to perform its pre-shutdown routines. When the MCU wants to shutdown the power supplies in the 33814, it must write a logic zero (0) to the PWREN bit in the SPI Control register. Only the state of the PWREN bit in the SPI Control register controls the shutdown of the 33814 power supplies. In this state, only the outputs are turned off (except ROUT2 if the Shutdown Disable bit is set. See 5.5.3.3. Using ROUT2 as a power relay, page 37).

Note: In case of KEYSW =1 condition, 33814 goes back in Normal mode, retrieving the last register configuration. This suggests that before entering in Prepare to Shutdown mode, user needs to configure registers as appropriate (switching off drivers and pre-drivers for example).

5.1.2.5 Power On Self-test (POST)

When a power on occurs after a POR, it may be desired to go through an initial Power On Self-test routine to ensure the SPI is working correctly and the status registers in the 33814 are viable. After a POR, all the registers in the 33814 contain their ‘default’ values, as indicated in the SPI register tables later in this document. The watchdog is also set to its default timeout value of 10 seconds, so any POST routine must be accomplished within this time frame or a WD reset may occur.

To perform a POST routine, the MCU should first send a SPI message to set the POST enable bit in the SPI control register 1, bit 6. Once this bit is set, the status registers are disconnected from the analog and logic portions of the 33814 and are connected only to the SPI circuitry. The POST can then write various data patterns to the status registers and verify that none of the bits are ‘stuck’ and state of the bit is accurately reflected. Note that bits in the status register labeled ‘x’ are not implemented and testing these bits may result in erroneous data. After testing all the status registers and confirming they are viable, the status registers can be set back to their default values by clearing the POST Enable bit back to 0. The POST enable bit allows the MCU to write ones (1s) to the Status registers.

Normally, the status register can only be cleared to zeros by the MCU and ones can be written to the status register only by the 33814 internal logic. This is designed to prevent the MCU from missing any reported fault bits and, for the 33814, to prevent system status errors resulting from the MCU erroneously writing a one (1) to a fault bit.

Once the POST enable bit is set back to a zero (0) by the MCU, the status register returns to the condition where the 33814 can only write ones (1s) to it and the MCU can only write zeros (0s) to it. Again, it is important to note that any POST routine should be designed to take less than 10 seconds to avoid a watchdog reset from occurring and truncating the POST routine, because the WD reset clears the POST Enable bit as well.

5.1.3 BATSW output functionality

The BATSW output pin has several functionalities:

- By default, the BATSW output pin is an indication of the state of the KEYSW input.
- The BATSW output can also be used to control an LS driver, such as the Relay ROUT2 driver by connecting the BATSW output to the RIN2 input.
- The BATSW output can also be configured as a low current LED high-side driver controlled through the SPI interface.

5.1.3.1 BATSW pin as a KEYSW input indication

When KEYSW is at V_{BAT} (12 V) level, the BATSW output is a logic 1 (5.0 V) and when KEYSW is at ground (0 V) level, BATSW is at a logic 0. The BATSW output may be used to inform the MCU the user is trying to shutdown the vehicle.

5.1.3.2 BATSW pin as an LS driver control

The BATSW output can also be used to control an LS driver, such as the Relay ROUT2 driver, by connecting the BATSW output to the RIN2 input. (see 5.5.3.3. Using ROUT2 as a power relay, page 37)

5.1.3.3 BATSW pin as an LED driver

If the BATSW signal is not needed by the MCU or to control the Relay 2 output, it can be configured as a low current LED high-side driver controlled through the SPI interface. As a high-side driver, BATSW can be PWM’d to allow an LED to be dimmed. A bit in the SPI Battery Switch Logic Output Configuration register called ‘HSD’, controls whether the BATSW output is a simple high-side driver, or controlled by KEYSW as indicated previously.

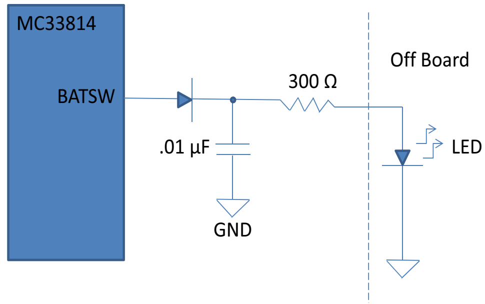


Figure 14. Recommended circuit to use BATSW as an LED driver

If the BATSW output is used to control an LED, the LED cathode should be tied to ground and the LED anode should be connected to the BATSW pin through an external resistor. The value of the external resistor should be 340 Ω or greater. Care must be taken if the BATSW output is sent off-board due to the chance of shorts to the battery or shorts to ground, for which the output is not protected. At a minimum, this output should be protected by a diode, a current limit resistor and an ESD capacitor (0.01 µF ceramic).

5.1.4 System SPI registers

5.1.4.1 SPI configuration registers

Table 7. Battery switch logic output configuration register

Reg #	Hex			7	6	5	4	3	2	1	0
6	6	Battery Switch Logic Output		HSD Mode	x	x	x	x	x	PWM Freq.1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 8. Battery switch logic output configuration register field

Field	Description
7-HSD Mode	BATSW Mode selection 0 - BATSW is controlled by KEYSW 1 - BATSW is used as a high-side driver
1-0 PWM Freq.x	PWM Frequency and Duty Cycle Mode [19] 00 - PWM Freq.: None 01 - PWM Freq.:100 Hz-D/C: Internal 10 - PWM Freq.: 1 KHz-D/C: Internal

Notes
19. See 5.5.2.2. Pulse Width Modulation mode, page 35

5.1.4.2 SPI control registers

Table 9. Other OFF/ON control register

Reg #	Hex			7	6	5	4	3	2	1	0
1	1	Other OFF/ON Control		Pwren **OFF**/ON	POST Enable **OFF**/ON	X	VProt **ON**/OFF	X	Batsw **OFF**/ON	Tach OFF/**ON**	RESET internal only
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(1)	(0)
8	8	Batsw		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 10. Other OFF/ON control register field description

Field	Description
7-Pwren OFF/ON	Power Enable 0-Power Disable (allowing sleep mode entry) 1-Power Enable (allowing Prepare to Shutdown mode entry)
6-POST Enable OFF/ON	Power On Self Test Enable 0-POST Disable 1-POST Enable
2-BATSW OFF/ON	BATSW Output Control 0-BATSW Output OFF 1-BATSW Output ON

Table 11. BATSW control register field description

Field	Description
6-0 PWM x	PWM Duty Cycle Setting with 1 % increment 0000000 to 1100100 (Dec. 100) represent 0 % to 100 % 1100100 (Dec. 100) to 1111111 (Dec.127) all map to 100 %.

5.1.4.3 SPI status registers

Table 12. Power supply and any system fault status register

Reg #	Hex			7	6	5	4	3	2	1	0
13	D	Power Supply and Any System Faults		Any System Faults	Keysw	Pwren	Batsw	SPI Error	V_{PROT} Short to Battery	V_{PROT} Overtemp OT	V_{PROT} Short to Ground
			Reset	(0)	(1)	(0)	(0)	(0)	(0)	(0)	(0)

Table 13. Power supply and any system fault status register field description

Field	Description
7-Any System Fault	System-wide any fault bit whose stats is the OR of all the other “Any fault” bits in the other status 0-No Fault reported 1-At least one Fault is reported [20]
6-Keysw	KEYSW Pin Status: 0-KEYSW is high (V_{BAT} Present) 1-KEYSW is low (Prepare to Shutdown mode)
5-PWREN	PWREN Status 0-PWREN Control bit is low 1-PWREN Control bit is high
4-Batsw	BATSW Pin Status 0-BATSW Pin is low 1-BATSW Pin is high

Notes

20. The MCU must interrogate all the other status registers to determine the actual fault(s) present.

5.2 Watchdog

5.2.1 Watchdog Normal operation

The watchdog is a programmable timer used to monitor the operation of the MCU. The timer programming is done by the Watchdog Parameters SPI Configuration Register by selection the Time Multiplier Value (bit 6-4) and the Time Value (bit 3-0).

Watchdog Timer = Time Multiplier Value (1.0 s,100 ms, or 10 ms) X Time Value (1 to 10)

Using this technique, time values from 1.0 ms. to 10 seconds can be programmed into the watchdog (default value is 10 s).

When the MCU is executing code properly, its program code should contain instructions to periodically send a SPI message to the watchdog SPI control register to refresh the watchdog. The watchdog timer, once refreshed, reloads the time interval value stored in the SPI watchdog configuration register and begins counting time again. Under normal operating conditions this sequence continues until the MCU shuts down, typically, when the KEYSW is turned off.

5.2.2 Watchdog Fault operation

In the event that something goes wrong during the MCU program execution, such as an unexpected breakpoint or some other program hang-up such as the execution of a HALT instruction, the watchdog may not be refreshed. When the WD time interval value programmed in the SPI Configuration register elapses, the watchdog issues a RESETB pulse. This RESETB pulse causes the MCU to restart its program and correct operation should be restored. After any RESETB (power-on or other), the watchdog SPI configuration register contains the default value for the refresh time (10 seconds). The watchdog is also enabled by default. The MCU, in its initialization (start-up) code, can choose to change this default value and/or disable the watchdog by sending a SPI command to write new information in the watchdog SPI configuration register.

5.2.3 Disabling the Watchdog timer

A watchdog reset occurs, by default, 10 seconds after the POR. If the MCU needs to be programmed in-circuit, a means of disabling the watchdog must be provided to avoid interrupting the MCU programming procedure. This disable mechanism can be a jumper between the RESETB pin of the 33814 and the MCU's Reset input pin. Alternatively, an isolation resistor can be placed between the RESETB pin on the 33814 and the MCU's reset input pin, allowing the MCU's reset pin to be pulled high independently of the 33814 RESETB. The watchdog can also be disabled via a bit in the SPI WD configuration register.

5.2.4 Watchdog SPI register

5.2.4.1 Watchdog SPI configuration register

Table 14. Watchdog parameters configuration registers

Reg #	Hex			7	6	5	4	3	2	1	0
10	A	Watchdog Parameters		Disable/ **Enable**	Load Time x1 sec	Load Time x100 ms	Load Time x10 ms	Load Time 8	Load Time 4	Load Time 2	Load Time 1
			Reset	(1)	(1)	(0)	(0)	(1)	(0)	(1)	(0)

Table 15. Watchdog parameter - register field descriptions

Field	Description
7-Disable/Enable	Watchdog Enable/Disable 0-Watchdog Disable 1-Watchdog Enable (Default State)
6-Load Time x1 sec	Time Multiplier Value [(21)] 0- Disable 1- Multiplier value = 1.0 sec (Default State)
5-Load Time x100 ms	Time Multiplier Value [(21)] 0- Disable (Default State) 1- Multiplier value = 100 ms

Table 15. Watchdog parameter - register field descriptions

Field	Description
4-Load Time x10 ms	Time Multiplier Value (21) 0- Disable (Default State) 1- Multiplier value = 10 ms
3-0 Load Time Value	Bits 3, 2, 1, 0 are a binary coded decimal (BCD) value from 1 to 10. (11 to 16 are mapped to 10 and 0 is mapped to 1) Default state = 1010 = X10

Notes

21. There are three time multiplier values so only one bit, 6, 5, or 4 may be set at one time. Setting more than one bit results in the highest multiplier value getting precedence.

5.2.4.2 Watchdog SPI control register

Table 16. Watchdog control registers

Reg #	Hex			7	6	5	4	3	2	1	0
12	C	Watchdog		WDRFSH	Load Time x1 sec	Load Time x100 ms	Load Time x10 ms	Load Time 8	Load Time 4	Load Time 2	Load Time 1
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 17. Watchdog control - register field descriptions

Field	Description
7-WDRFSH	Watchdog Refresh 0-No Watchdog refresh action 1-Refresh the watchdog timer. (reload the time value from the Watchdog Parameters Register)
6-Load Time x1 sec	Temporary Time Multiplier Value (22) 0- Disable 1- Multiplier value = 1.0 sec
5-Load Time x100 ms	Temporary Time Multiplier Value (22) 0- Disable 1- Multiplier value = 100 ms
4-Load Time x10 ms	Temporary Time Multiplier Value (22) 0- Disable 1- Multiplier value = 10 ms
3-0 Load Time Value	Bits 3, 2, 1, 0 are a Temporary Binary coded decimal (BCD) value from 1 to 10. (11 to 16 are mapped to 10 and 0 is mapped to 1)

Notes

22. There are three time multiplier values so only one bit, 6, 5, or 4 may be set at one time. Setting more than one bit results in the highest multiplier value getting precedence.

Note: The watchdog SPI Control Register can also be loaded with a time value to temporarily set a different value in the watchdog timer for the next cycle. When Bits 6 through 0 in the watchdog SPI control register are zero, the value stored in the watchdog SPI configuration register loads into the watchdog timer. If there is a temporary time value written into the watchdog SPI control register, the value loads into the watchdog. The watchdog SPI control register is automatically cleared to zero when the watchdog timer is loaded. Unless a new temporary time value is again written to the watchdog SPI Control Register, the next watchdog timer load is from the value stored in the watchdog SPI configuration register.

5.2.4.3 Watchdog SPI status register

Table 18. Watchdog status register

Reg #	Hex			7	6	5	4	3	2	1	0
10	A	Watchdog State		Enable/ Disable	WD timer bit 6	WD timer bit 5	WD timer bit 4	WD timer bit 3	WD timer bit 2	WD timer bit 1	WD timer bit 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 19. Watchdog status - register field descriptions

Field	Description
7-Enable/Disable	Watchdog Enable/Disable Status 0-Watchdog disable 1-Watchdog Enable
6-0 WD Timer bit x	Reflecting the Watchdog Timer value Each step represents the WD timer/127

Bits [6:0] represent the value stored in the watchdog timer. If the watchdog is enabled, this value read on the fly represents the time left before a watchdog reset.

Table 20. Watchdog timer values

Status register							
WD timer bit6	**WD timer bit5**	**WD timer bit4**	**WD timer bit3**	**WD timer bit2**	**WD timer bit1**	**WD timer bit0**	**Value in ms**
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
0	0	0	0	1	0	1	5
0	0	0	0	1	1	0	6
0	0	0	0	1	1	1	7
0	0	0	1	0	0	0	8
0	0	0	1	0	0	1	9
0	0	1	0	0	0	1	10
0	0	1	0	0	1	0	20
0	0	1	0	0	1	1	30
0	0	1	0	1	0	0	40
0	0	1	0	1	0	1	50
0	0	1	0	1	1	0	60
0	0	1	0	1	1	1	70
0	0	1	1	0	0	0	80
0	0	1	1	0	0	1	90
0	1	0	0	0	0	1	100
0	1	0	0	0	1	0	200
0	1	0	0	0	1	1	300
0	1	0	0	1	0	0	400
0	1	0	0	10	0	1	500
0	1	0	0	1	1	0	600
0	1	0	0	1	1	1	700

Table 20. Watchdog timer values (continued)

0	1	0	1	0	0	0	800
0	1	0	1	0	0	1	900
1	0	0	0	0	0	1	1000
1	0	0	0	0	1	0	2000
1	0	0	0	0	1	1	3000
1	0	0	0	1	0	0	4000
1	0	0	0	1	0	1	5000
1	0	0	0	1	1	0	6000
1	0	0	0	1	1	1	7000
1	0	0	1	0	0	0	8000
1	0	0	1	0	0	1	9000
1	0	0	1	0	1	0	10000

5.3 System reset

5.3.1 RESETB output pin

The RESETB pin is a 5.0 volt logic, low level output used to reset the MCU.The RESETB pin is an open drain output. Without power on the 33814 circuit, the RESETB pin is held low by an internal pull-down resistor. In a typical application, the RESETB pin must be pulled up externally by a pull-up resistor to VCC.

5.3.2 Reset sources

When power is applied to the circuit and the voltage on the VCC pin reaches the lower voltage threshold, the RESETB pin remains at a low level (open drain FET turned on) for a period of time equal to the time value WD_{RESET}. After this time period, the RESETB pin goes high and stays high until a reset pulse is generated due to any of the following events:

- A watchdog timer timeout event occurs
- An undervoltage event on VCC occurs
- An overvoltage event on VPWR occurs

A Power On Reset (POR) is always provided upon power ON (anytime the IC goes from sleep state to active state).

5.3.3 Internal reset

The SPI control register includes a bit labeled ‘Reset’. When this bit is set to a one (1) by the MCU, it instructs the 33814 to perform an internal reset. This reset does NOT toggle the RESETB output pin. However, it causes all internal registers to be initialized back to their default values (including clearing the reset bit in the SPI control register).

Table 21. Other OFF/ON control register

Reg #	**Hex**			**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	1	Other OFF/ON Control		Pwren **OFF**/ON	POST Enable **OFF**/ON	X	VProt **ON**/OFF	X	Batsw **OFF**/ON	Tach OFF/**ON**	RESET internal only
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(1)	(0)

Table 22. Other OFF/ON register field descriptions

Field	Description
0-RESET Internal Only	Reset Internal Only Command 0-Do not perform an internal reset 1-Perform an internal reset

5.4 Power supplies

5.4.1 Pin description

5.4.1.1 PWR supply input

The VPWR pin is the battery input to the 33814 IC. The VPWR pin requires an external reverse battery and adequate transient voltage protection. The VPWR pin should be bypassed to ground, as close to the IC as possible, with a 0.1 μF ceramic capacitor.

5.4.1.2 VPPREF output

The VPPREF output pin is used to drive the base of an external regulator PNP pass transistor. It is not recommended that this voltage be brought off of the module PC board, because it may not have adequate protection to prevent damage to the PNP pass transistor under short-to-ground or short-to-battery conditions.

5.4.1.3 VPPSENS input

The VPPSENS pin is used to monitor the V_{PP} pre-regulator output voltage from the external pass transistor's collector and to supply the input voltage to the V_{CC} and V_{PROT} regulators. The VPPSENS pin should be bypassed to ground, as close to the IC as possible, with a 0.1 μF ceramic capacitor and a higher value electrolytic capacitor in parallel. The VPPSENS pin should not be used to supply other components. The external regulator PNPN pass transistor should be dedicated to the 33814.

5.4.1.4 VCC output (5.0 V supply)

The VCC output supplies 5.0 V power to the system MCU and other on-board peripherals. An external capacitor V_{OCE} is recommended.

5.4.1.5 VPROT output (5.0 V protected supply)

The VPROT output is a protected 5.0 Volt output that tracks the V_{CC} voltage. The VPROT output should be protected against ESD by means of a 0.1 μF ceramic capacitor on the output and a higher value electrolytic capacitor in parallel. An external capacitor V_{OCE} is also recommended.

5.4.1.6 GND

The GND pin provides the ground reference for the V_{PWR}, V_{PP}, V_{PROT} and V_{CC} supplies. The GND pin is used as a return for both the power supplies, as well as power a ground for some of the lower current output drivers. The higher current output drivers have their own ground pins. All ground pins (INJGND1, INJGND2, RGND1 and RGND2) and the exposed pad must be directly connected to this pin and to the negative battery terminal. There is no separate ground pin associated with the LAMPOUT driver. It shares a ground with ROUT2.

5.4.2 Power supplies functions

5.4.2.1 Power supply

The 33814 is designed to operate from $VPWR_{MIN}$ to $VPWR_{MAX}$ on the VPWR pin. The VPWR pin supplies power to all internal regulators and analog and logic circuit blocks. All IC analog current and internal logic current is provided from the VPWR pin. An overvoltage comparator monitors this pin. When an overvoltage condition is present, all outputs and voltage regulators are shut off for protection.

5.4.2.2 V_{PP} pre-regulator

The V_{PP} pre-regulator supplies the input voltage to the V_{CC} and V_{PROT} regulators. The V_{PP} regulator is a low drop-out (LDO) regulator. It provides a regulated output voltage when the input is greater than its specified voltage level and it follows the input voltage when it is below its specified voltage level.

The V_{PP} regulator uses an external PNP transistor as a pass element. This allows the user to choose the PNP's size and package considerations to meet the system requirements. The amount of power the external PNP transistor has to dissipate depends on the maximum voltage the system can be expected to run at and the maximum expected current drawn from the V_{CC} and V_{PROT} regulators. The VPPSENS pin is used to feedback the value of the V_{PP} voltage for regulation. Since the V_{PP} regulator is not intended to supply off-the-board loads, there is no short-to-ground or short-to-battery protection on the output of the external PNP.

5.4.2.3 V_{CC} regulator

The V_{CC} regulator obtains its input voltage from the V_{PP} pre-regulator. The V_{CC} regulator output is used for supplying 5.0 V to the MCU and for setting communication threshold levels via the internal SPI SO driver. The V_{CC} regulator contains an internal pass transistor protecting against overcurrent.

A Power On Reset (POR) circuit monitors the VCC output voltage level. When the V_{CC} voltage exceeds the $V_{CC(POR)}$ threshold, the RESETB line is held low for an additional delay time $t_{(POR)}$ before being brought to a logic one level. An undervoltage (UV) circuit monitors the output of the V_{CC} regulator. When the voltage goes below the $V_{CC(UV)}$ threshold for more than the V_{CC} filter time, $t_{(VCC-UV)}$, the RESETB line is asserted to a logic zero state and remains there until the POR condition is met.

5.4.2.4 V_{PROT} regulator

The protected output V_{PROT} is a tracking regulator using the V_{CC} output as a reference. Because the V_{PROT} regulator is expected to supply 5.0 V to external sensors and other off-board peripherals in the vehicle, it is well protected against shorts-to battery, shorts-to-ground, overcurrent and overtemperature.The V_{PROT} supply is enabled at power-on, but can be disabled via the SPI Control Register.

5.4.2.5 Power up sequence

Table 23. Power up sequence

t	Actions
t0	Battery connected to VPWR Pin
t1	User turns on ignition switch, KeySw => High • Internal regulators, band gap reference and bias current generator are enabled
t2 = t1+ ~5.0 µs	Internal PORb de-asserted after internal 2.5 V regulator to the logic core stabilizes • Logic and oscillator are enabled • Start KeySw filter time
t3 = t2+ ~12.7 ms	KeySW filter time period expires • Enable V_{PP} pre-regulator • Soft start sets turn on ramp to ~ 400 µs
t4 = t3+ (< 400 µs)	V_{PPSENS} exceeds 4.8 V, enables V_{CC} & V_{PROT} regulators • Soft start sets turn on ramps to ~ 2.0 ms • BatSw buffer receives power • Output rises with V_{CC}
t5 = t4+ (< 2.0 ms)	V_{CC} exceed POR Threshold ~4.6 V • Start POR Timing ~128 µs
t6 = t5+ ~128 µs	POR Time period expires • Release RESETB pin

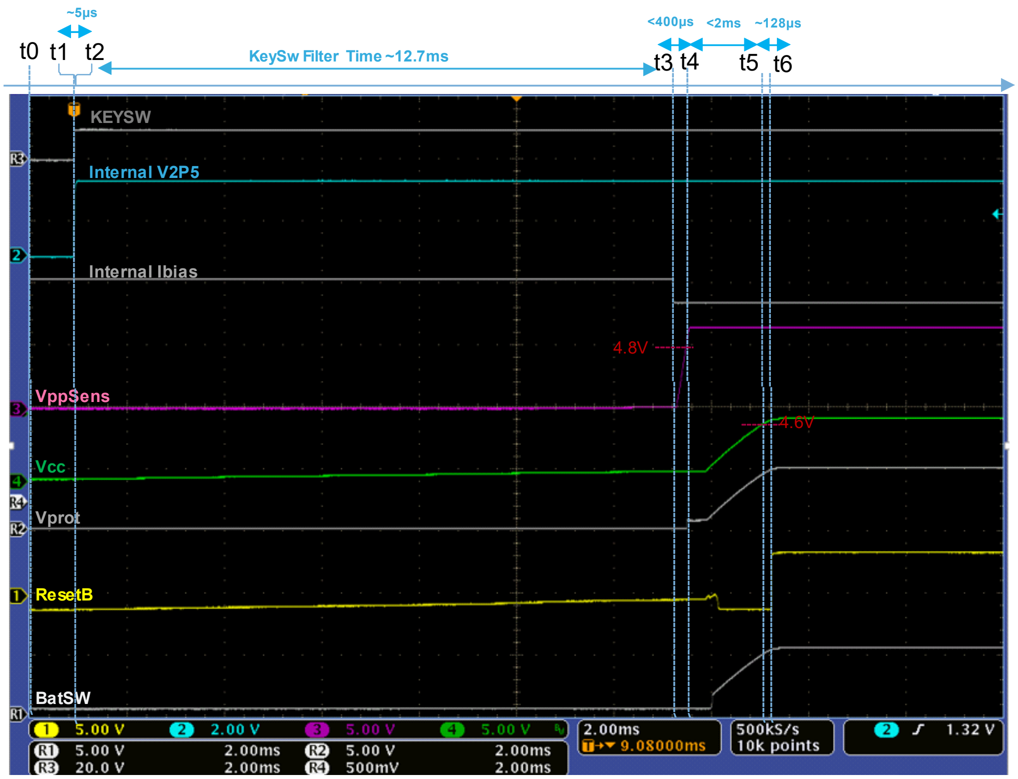


Figure 15. Power up sequence

5.4.3 Power supply SPI register

5.4.3.1 SPI control registers

Table 24. OFF/ON control register

Reg #	Hex			7	6	5	4	3	2	1	0
1	1	Other OFF/ON Control		Pwren **OFF**/ON	POST Enable **OFF**/ON	X	VProt OFF/**ON**	X	Batsw **OFF**/ON	Tach OFF/**ON**	RESET internal only
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(1)	(0)

Table 25. Other OFF/ON register field descriptions

Field	Description
4-VPROT OFF/ON	VPROT Regulator Enable 0-Disable 1-Enable (Default)

5.4.3.2 SPI status registers

Table 26. Power supply and any system fault status register

Reg #	Hex			7	6	5	4	3	2	1	0
13	D	Power Supply and Any System Faults		Any System Faults	Keysw	Pwren	Batsw	SPI Error	V_{PROT} Short to Battery	V_{PROT} Overtemp OT	V_{PROT} Short to Ground
			Reset	(0)	(1)	(0)	(0)	(0)	(0)	(0)	(0)

Table 27. Power supply and any system fault status register field description

Field	Description
2-V_{PROT} Short to Battery	V_{PROT} Short to Battery Status: 0-No Fault reported 1-Fault reported
1-V_{PROT} Overtemp OT	V_{PROT} Overtemp: 0-No Fault reported 1-Fault reported
0-V_{PROT} Short to Ground	V_{PROT} Short To Ground: 0-No Fault reported 1-Fault reported

5.5 Drivers blocks

5.5.1 Pin description

5.5.1.1 INJIN1, INJIN2 inputs

The INJIN1 and INJIN2 pins are the parallel inputs controlling the Injector outputs, INJOUT1 and INJOUT2 respectively. The INJIN1 and INJIN2 pins are 5.0 V logic level inputs with built-in pull-downs to ground that prevent accidental actuation of an injector if the connection to the pin is lost.

5.5.1.2 RIN1, RIN2 inputs

The RIN1and RIN2 pins are the parallel inputs controlling the relay outputs ROUT1 and ROUT2 respectively. The RIN1 and RIN2 pins are 5.0 V logic level inputs with built-in pull-downs to ground to prevent accidental actuation of a relay if the connection to the pin is lost.

5.5.1.3 INJOUT1, INJOUT2 driver outputs

These are outputs pins for INJOUT1 and INJOUT2 low-side drivers. Theses outputs can be used as injector driver outputs for the two Injectors the IC supports. If the two injectors are not needed, one INJOUT can be used as a general purpose low-side driver for relays, motors, lamps, gauges, etc. Injector outputs are forced off during all RESET events.

5.5.1.4 ROUT1, ROUT2 driver outputs

These are output pins for ROUT1 and ROUT2 low-side drivers and have different current ratings and can be used to drive relays (like fuel pump, main power relay, …) or other inductive loads.

5.5.1.5 LAMPOUT driver output

The Lamp driver output, LAMPOUT is a low-side driver capable of driving an incandescent lamp even under cold filament conditions and can also be used to drive a LED if the open load feature is disabled.

5.5.1.6 Tachometer (TACHOUT)

The TACHOUT pin is a low-side driver which can used to drive a tachometer meter movement and can be programmed via the SPI to:

- Output the same signal as VRSOUT divided by a 1 to 32 programmable divider
- Output a PWM signal with a frequency and duty cycle programmable via the SPI
- Output one of eight fixed frequencies

5.5.2 Common functionality

The six open drain low-side drivers (LSDs) are designed to control various automotive loads, such as injectors, fuel pumps, solenoids, lamps and relays, etc. Each driver includes off-state open load detection, on-state short-to-ground detection, short-circuit to battery protection, overcurrent protection, overtemperature protection and diagnostic fault reporting via the SPI. The LSD outputs can be Pulse Width Modulated (PWM'd) based on an internal and/or external frequency for use as variable speed motor drivers, LED/lamp dimming drivers, or as a fuel pump driver.

All outputs except ROUT2 are disabled when the KEYSW input pin is brought low regardless of the state of the input pins. All outputs, including ROUT2 are disabled when the RESETB pin is low.

5.5.2.1 LSD input logic control

The four LSDs (INJOUT1, INJOUT2, ROUT1 and ROUT2) are controlled individually using a combination of the external pin input (respectively INJIN1, INJIN2, RIN1 and RIN2) and/or a SPI On/Off Control bit. The two LSDs (LAMPOUT and TACHOUT) are controlled individually using a SPI On/Off Control bit. The logic can be made to turn the outputs on or off by:

- a logical combination of the external pin **OR**ed with the SPI Control On/Off Bit (Default State)
- a logical combination of the external pin **AND**ed with the SPI Control On/Off Bit

A separate OR/AND select bit is found in the SPI configuration registers to accomplish this selection.

5.5.2.2 Pulse Width Modulation mode

Alongside just turning the outputs ON or OFF, the six LSD outputs can be Pulse Width Modulated (PWM'd) to control the outputs with a variable 0 to 100 % duty cycle at a selection of different frequencies. There are two built-in PWM frequencies (100 HZ and 1.0 kHz) and the external input pin can also be used as either an external PWM frequency input (divided by 100) or a total PWM (frequency and duty cycle) input.

Two bits (Bits 1, 0) in the SPI configuration register control which mode of input control is selected. The internal PWM duty cycles (D/C) are controlled by the lower seven bits in the corresponding SPI control register with a 1 % increment. The external PWM duty cycles (D/C) are provided by the MCU on the input pin of the corresponding output driver.

5.5.2.3 Overcurrent (OC) protection

Output protection uses two strategies—overcurrent (OC) protection and/or overtemperature (OT) protection—to detect a fault. When a fault occurs, the output protection feature automatically controls the output to prevent damage to the output device.

The overcurrent protection scheme senses an overcurrent condition by monitoring the voltage on the individual output device drain.

5.5.2.3.1 Inrush delay

The Inrush Delay bit in the SPI Configuration Register for each output, when set to a one(1), prevents the overcurrent fault bit from being set and the overcurrent protection from shutting off the output for t_{INRUSH} time (Typ.10 ms) rather than $t_{SC1.}$(Typ. 60 μs).

This means that during this fixed time period, the device enters into current limitation, and the output is switched off when the fixed period expires.

Note that for the Lampout Driver, the default state is Inrush Delay equal to 1 (t_{INRUSH}).

5.5.2.3.2 Retry feature

When the Retry feature is enabled (Retry Bit for each output) during an overcurrent condition at the end of the Inrush period, the output device turns off and waits until a delay time (t_{Ref}) has passed. After this off time, the output tries to turn on again. If the short is still present, the process starts again. This on/off cycling continues until the output is shut off by command or the overtemperature (OT) on the output device is reached. Note that the Inrush delay resets to its default state for this on/off cycling. See Figure 16.

If the SPI configuration register retry enable bit is set to a zero (0), this on/off cycling does not occur and the output turns off if the overcurrent threshold is reached. The output does not turn on again until the output is shut off and then on again by command.

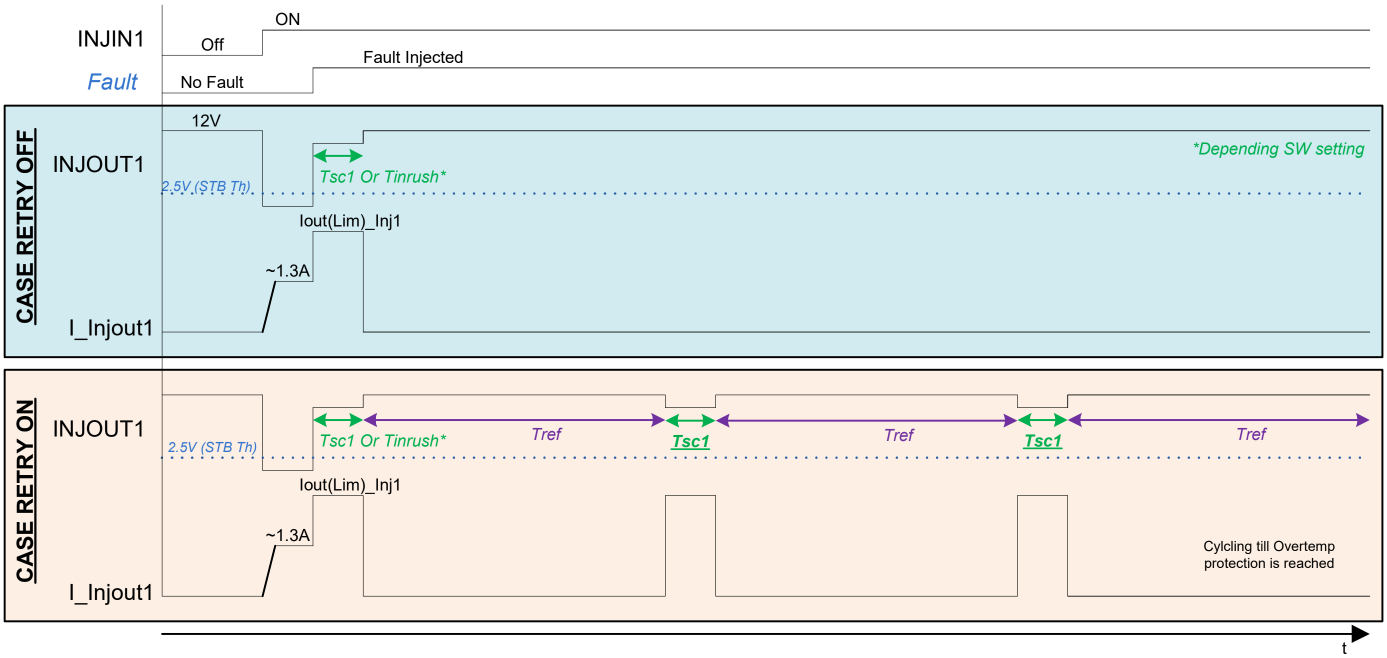


Figure 16. Retry and Inrush feature

5.5.2.4 Temperature limit (OT) protection

The second output protection scheme works by sensing the local temperature of the individual output device. During an overcurrent event, the device enters the current limit and remains there until the output driver maximum temperature limit is exceeded (OT). At this point, the device shuts down automatically regardless of the input state. The output tries to turn on again only when the junction temperature falls below the maximum temperature minus the T_{LIM} hysteresis temperature value and the input state is commanding the output to be on. The T_{LIM} hysteresis value is specified in the static parameter table.

The temperature limit (T_{LIM}) protection is independent of the overcurrent protection and is not controlled by the SPI. T_{LIM} is always enabled and is always a retry operation. Outputs may be used in parallel to drive higher current loads as long as the turn-off energy of the load does not exceed the energy rating of a single output driver.

5.5.2.5 Open load (OL) and short-to-battery (OC) strategy

The injectors, lamps, relays and tachometer low-side outputs are capable of detecting an open load in the off state and short-to-battery condition in the on state. All faults are reported through the SPI status register communication (OL bit for open load fault and OC bit for short-to-battery fault).

For open load detection, a current source is placed between the MOSFET drain pin and the ground of the IC. An open load fault is reported when the drain voltage is less than the listed threshold. A shorted load fault is reported if the drain pin voltage is greater than the programmed short threshold voltage when the device is in the on state. The open load and short-to-battery fault threshold voltage is fixed and cannot be modified via the SPI.

The open load feature could be disabled (to allow the outputs to be used as LED drivers) by clearing the appropriate bit in the in the LSD configuration register.

5.5.2.6 Short-to-ground (SG) strategy

The injectors, lamps and relays (but not the Tachometer) low-side driver outputs are capable of detecting a short-to-ground by measuring the current flow in the output device and comparing it to a known current value. If a short-to-ground is detected, it is annunciated via a bit in the appropriate SPI status register.

5.5.2.7 Output driver diagnostics

Overcurrent (OC), temperature limit (OT) exceeded, short-to-ground (SG) and open load (OL) conditions are reported through the status register for each driver (no SG for the tachometer). A bit in the SPI status register indicates when any of the LSDs or pre-drivers are reporting a fault and when a particular output has any of the four possible fault conditions present. The MCU polls for fault conditions by looking for a single bit in one register to detect the presence of any fault in the circuit.

5.5.3 Special features

5.5.3.1 LAMP OUT

The Inrush delay bit is set to 1 by default to allow the driver to handle the inrush current of a cold lamp filament. It waits an additional time before annunciating an overcurrent condition. A pull-down current sink is provided to allow the IC to detect when the bulb is burned out (open filament). The LAMP is switched on and off via the SPI ON/OFF Control register word. It also has the ability to be PWM'd for advanced diagnostic (dimming) purposes via the SPI Lamp Control register. The output can also drive an LED if the open load detect current sink is commanded off via the SPI to prevent 'ghosting'.

5.5.3.2 TACHOUT

The TACHOUT pin is a low-side driver used to drive a tachometer meter movement. TACHOUT can be programmed via the SPI to:

- Output the same signal as VRSOUT divided by a 1 to 32 programmable divider
- Output a PWM signal with a frequency and duty cycle programmable via the SPI
- Output one of eight fixed frequencies, as indicated in Table 30

If a tachometer is not required, the TACHOUT output can also be used as a low current, SPI controlled, low-side driver to drive an LED or other low current load. The SPI Configuration register for the tachometer is used to determine for which mode this output is used. The TACHOUT output handles overcurrent (OC) differently than the other low-side drivers. When an overcurrent limit is reached, the TACHOUT output does not enter a current limiting state, but rather shuts the output off to protect the output device. The retry option works similarly to the other low-side drivers. In the LSD mode, bit 4 of the SPI Configuration register controls the turn on or turn off of the open load detect current sink.

5.5.3.3 Using ROUT2 as a power relay

The ROUT2 (Relay 2 Output) can be used to drive a power relay. The RIN2 input or the RIN2 bit in the SPI Control register can be used to turn the ROUT2 output on or off as desired. The BATSW output can be connected to the RIN2 input to control the power relay, or the MCU can chose to control the RIN2 bit in the SPI Control register to actuate the power relay. The ROUT2 output is unique in that it can be kept turned on even after KEYSW is turned off (as long as the PWREN bit is still set to a one), by setting the shutdown disable (SDD) bit in the ROUT2 Configuration register.

5.5.4 SPI drivers registers

5.5.4.1 SPI configuration registers

Table 28. Injector 1/2, Relay1/2,Lampout configuration registers

Reg #	Hex			7	6	5	4	3	2	1	0
0	0	Injector 1 Driver		Retry Enable	x	x	**OL Current Sink Enable**	In-Rush Delay	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
1	1	Injector 2 Driver		Retry Enable	x	x	**OL Current Sink Enable**	In-Rush Delay	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)

Table 28. Injector 1/2, Relay1/2,Lampout configuration registers (continued)

Reg #	Hex			7	6	5	4	3	2	1	0
2	2	Relay 1 Driver		Retry Enable	x	x	OL Current Sink Enable	In-Rush Delay	OR/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
3	3	Relay 2 Driver		Retry Enable	Shutdown DisableSD D	x	OL Current Sink Enable	In-Rush Delay	OR/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
5	5	Lamp Driver		Retry Enable	x	x	OL Current Sink Enable	In-Rush Delay	x	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(1)	(0)	(0)	(0)

Table 29. Injector 1/2 and Relay 1/2 Lampout configuration. Field description

Field	Description
7-Retry Enable	Retry Enable 0-Disable 1-Enable
6-Shutdown Disable SDD	Shutdown Disable Mode selection (23) allowing to keep ROUT2 ON even after KEYSW =0 0- SDD Mode Disable 1- SDD Mode Enable
4-OL Current Sink Enable	Open Load Current Sink Enable 0- Disable (OL Flag in status register will be forced to 0) 1- Enable (Default)
3-In-Rush Delay	In-rush Delay Time disabling overcurrent protection 0-t_{SC1} (Default) 1- t_{INRUSH} (24)
2-OR/AND	OR/AND logical action to control LS Output (25) 0- OR between Input pin and Control bit (Default) 1-AND between Input pin and Control bit
1/0- PWM Freq1/0	PWM Frequency and Duty Cycle Mode (26) 00-PWM Freq.: None or Ext.Pin - D/C: None or ext.Pin 01-PWM Freq.:100 Hz-D/C: Internal 10-PWM Freq.: 1 KHz-D/C: Internal 11-PWM Freq.:On ext. pin /100 -D/C: Internal

Notes

23. Valid only for Relay 2 Driver.
24. Default For Lampout Driver
25. NA for Lampout Driver
26. No ext Pin for Lampout Driver

Table 30. Tachometer driver configuration registers

Reg #	Hex			7	6	5	4	3	2	1	0
4	4	Tachometer Driver		Retry Enable	Vrsout/ LSD	Vrsout/ Osc. mode	N16/OL Current Sink Enable	N8/In-Rush Delay	N4/Osc 2	N2/Osc 1/ PWM Freq. 1	N1/Osc 0/ PWM Freq. 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(1)

Table 31. Tachometer driver configuration registers. Field description

Field	Description
7-Retry Enable	Retry Enable 0-Disable 1-Enable
6-V_{RSOUT}/LSD 5-V_{RSOUT}/ Osc.mode	VRSOUT/LSD/OSC Mode selection 00 (Default) - VRSOUT Output divided by N 01- Oscillator Output 10- Low-side Driver mode 11- Same as 10 (LSD)
4-N16/ OL Current Sink Enable	N16 or Open Load Current Sink Enable -When used as VRSOUT, see Table 32. . -When used as LSD: 0- Disable (Open Load Flag in status register will be forced to 0) 1- Enable (Default)
3-N8/In-Rush Delay	N8 / In-Rush Delay Time disabling overcurrent protection -When used as VRSOUT, see Table 32. -When used as LSD: 0-t_{SC1} 1- t_{INRUSH}
2-1-0:N(4,2,1), Osc (2,1,0) PWM freq (x,1,0)	N(4,2,1) or Output Frequency or PWM Output -When used as VRSOUT, see Table 32. -When used as Oscillator Output, see Table 33 -When used as PWM output, see Table 34

Table 32. Tachout mode configuration when used as VSROUT

SPI Configuration Register Bits 4, 3, 2, 1, 0 (N16, N8, N4, N2, N1)	TACHOUT Mode VRSOUT divided by ‘N’ where ‘N’ is defined by bits 0 thru 4 of SPI
00000	N=32
00001 (default)	N=1
00010	N=2
......	....
11111	N=31

Table 33. Fixed oscillator frequencies configuration when used as an oscillator output

SPI Configuration Register Bits 2,1,0 (Osc2, Osc1, Osc0)	Oscillator Frequencies MODE
000	10 Hz
001 (default)	100 Hz
010	1.0 kHz
011	5.0 kHz
100	10 kHz
101	20 kHz
110	40 kHz
111	100 kHz (not recommended for use)

Table 34. PWM frequency configuration when used as LSD

SPI Configuration Register Bits 1, 0 PWM Frequency	PWM MODE
x00	None
x01 (default)	PWM Freq: 100 Hz - D/C: Internal
x10	PWM Freq: 1.0 kHZ - D/C: Internal
x11	None

5.5.4.2 SPI control registers

Table 35. Main OFF/ON control register

Reg #	Hex			7	6	5	4	3	2	1	0
0	0	Main OFF/ON Control		INJ1	INJ2	REL1	REL2	LAMP	IGN1	IGN2	O2H
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 36. Main OFF/ON control register field description

Field	Description
7-INJ1	INJOUT1 Bit Control 0-OFF 1-ON
6-INJ2	INJOUT2 Bit Control 0-OFF 1-ON
5-REL1	ROUT1 Bit Control 0-OFF 1-ON
4-REL2	ROUT2 Bit Control 0-OFF 1-ON
1-LAMP	LAMP Bit Control 0-OFF 1-ON

Table 37. Other OFF/ON control register

Reg #	Hex			7	6	5	4	3	2	1	0
1	1	Other OFF/ON Control		Pwren **OFF**/ON	POST Enable **OFF**/ON	X	VProt **ON**/OFF	X	Batsw **OFF**/ON	Tach OFF/**ON**	RESET internal only
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(1)	(0)

Table 38. Other OFF/ON control register field description

Field	Description
1-Tach OFF/ON	TACHOUT Bit Control 0-OFF 1-ON

Table 39. PWM duty cycle setting control register

Reg #	Hex			7	6	5	4	3	2	1	0
2	2	Injector 1 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
3	3	Injector 2 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
4	4	Relay 1 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
5	5	Relay 2 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
6	6	Tachometer Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
7	7	Lamp Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 40. PWM duty cycle setting control register field description

Field	Description
6-0 -PWMx	PWM Duty Cycle Setting with 1 % increment 0000000 to 1100100 (Dec. 100) represent 0 % to 100 % 1100100(Dec. 100) to 1111111 (Dec.127) all map to 100 %.

5.5.4.3 SPI status registers

s

Table 41. LS driver status register

Reg #	Hex			7	6	5	4	3	2	1	0
0	0	Injector 1 Driver Faults		Faults	x	x	x	Open Load OL	Over - current OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
1	1	Injector 2 Driver Faults		Faults	x	x	x	Open Load OL	Overcurren t OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
2	2	Relay 1 Driver Faults		Faults	x	x	x	Open Load OL	Overcurren t OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
3	3	Relay 2 Driver Faults		Faults	x	x	x	Open Load OL	Overcurren t OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
4	4	Tachometer Driver Faults		Faults	x	x	x	Open Load OL	Overcurren t OC	Overtemp OT	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
5	5	Lamp Driver Faults		Faults	x	x	x	Open Load OL	Overcurren t OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 42. LS driver status register description field

Field	Description
7-Faults	Global Driver Fault bit (by driver) Logical OR of bit 0-3 0-No Fault 1-Fault detected
3-Open Load OL	Open Load Fault Flag 0-No Fault (Forced to 0 if OL feature disabled) 1-Fault detected
2-Overcurrent OC	Overcurrent Fault Flag 0-No Fault 1-Fault detected
1-Over Temp OT	Over Temp Limit Fault Flag 0-No Fault 1-Fault detected
0-Short GND SG	Over Temp Limit Fault Flag [27] 0-No Fault 1-Fault detected

Notes
27. Not present on Tachometer Driver

Table 43. System On/Off indicators status register

Reg #	Hex			7	6	5	4	3	2	1	0
14	E	System On/Off Indicators		INJ1 Off/On	INJ2 Off/On	REL1 Off/On	REL2 Off/On	LAMP Off/On	IGN1 Off/On	IGN2 Off/On	O2H Off/On
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 44. System On/Off indicators status register field description

Field	Description
7-3 Driver Off/On	Driver On/Off Status 0- Off 1- On

5.6 Pre-driver

5.6.1 Pin description

5.6.1.1 IGNIN1 and IGNIN2 inputs

The IGNIN1 and IGNIN2 pins are the parallel inputs controlling the IGNOUT1 and IGNOUT2 pre-driver outputs respectively. The IGNIN1 and IGNIN2 pins are 5.0 V logic level inputs with built-in pull-downs to ground that prevents accidental actuation of a pre-driver output if the connection to the pin is lost.

5.6.1.2 O2HIN input

The O2HIN pin is the parallel input controlling the O2HOUT pre-driver output. The O2HIN pin is a 5.0 V logic level input with a built-in pull-down to ground that prevents accidental actuation of the pre-driver output if the connection to the pin is lost.

5.6.1.3 IGNOUT1 and IGNOUT2 Pre-driver outputs, with feedback IGNFB1 and IGNFB2 and current sense inputs IGNSENSP and IGNSENSN

The IGNOUT1 and IGNOUT2 outputs are pre-driver outputs driving either an ignition (IGBT) pre-driver or a general purpose gate driver (GPGD). INGOUT1 and IGNOUT2 are configured by default as an IGBT driver to control the ignition coil current to produce a spark.

The IGNOUTx outputs and their associated feedback pins IGNFBx provide short-to-battery and one shared current sense resistor provides overcurrent protection for the external driver transistors. When used as an IGBT driver, a 10:1 voltage divider (9R:1R) must be used on the feedback pins to prevent the 400 V flyback from damaging the IC. More accurate current control can be provided by placing a current sense resistor between the IGNSENSP and IGNSENSN pins.

5.6.1.4 O2HOUT Pre-driver output with drain feedback input O2HFB and current sense inputs O2HSENSP and O2HSENSN

The O2HOUT output is a pre-driver output driving either an ignition (IGBT) pre-driver or a general purpose gate driver (GPGD). O2HOUT is configured by default as GPDC to control the gate of a MOSFET to drive a heater on an O2 (Lamda) sensor. The pre-driver is capable of driving most power MOSFETs. The O2HOUT output and associated drain feedback pin O2HFB provide short-to-battery, overcurrent protection for the external driver MOSFET. When used as an IGBT driver, a 10:1 voltage divider (9R:1R) must be used on the feedback pins to prevent the 400 V flyback from damaging the IC. More accurate current control can be provided by placing a current sense resistor between the O2HSENSP and O2HSENSN pins.

5.6.2 Functions description

There are three identical pre-drivers in the 33814. Each pre-driver can be configured as either an ignition (IGBT) pre-driver or a general purpose gate driver (GPGD). By default, one pre-driver is configured as a GPGD (O2HOUT) and two pre-drivers are configured as ignition (IGNOUT1, IGNOUT2) pre-drivers. A bit in each pre-driver’s SPI Configuration register defines whether the pre-driver behaves as an ignition or a GPGD pre-driver.

It should be noted that there are only two current measurement circuits: ISGNSENSP/N and O2HSENSP/N. Each pre-driver includes off-state open load detection and can be Pulse Width Modulated (PWM’d) based on an internal and/or external frequency for use as variable speed motor drivers, LED/lamp dimming drivers, or as a fuel pump driver.

5.6.2.1 Pre-driver input logic control

The three Pre-drivers (IGNOUT1, IGNOUT2 and O2HOUT) are controlled individually using a combination of the external pin input (respectively IGNIN1, IGNIN2 and O2HIN) and/or a SPI On/Off Control bit.

The logic can be made to turn the outputs on or off by:

- a logical combination of the external pin **OR**ed with the SPI Control On/Off Bit (Default State)
- a logical combination of the external pin **AND**ed with the SPI Control On/Off Bit

A separate OR/AND select bit is found in the SPI configuration registers to accomplish this selection.

5.6.2.2 Pulse Width Modulation mode

See 5.5.2.2. Pulse Width Modulation mode, page 35.

5.6.2.3 Open load (OL) and short-to-battery (OC) strategy

The Pre-drivers are capable of detecting an open load in the off state and short-to-battery condition in the on state. All faults are reported through the SPI status register communication (OL bit for open load fault and OC bit for short-to-battery fault).

For open load detection, a current source is placed between the MOSFET drain pin and ground of the IC. An open load fault is reported when the drain voltage is less than the specified threshold. A shorted load fault is reported when the drain pin voltage is greater than the programmed short threshold voltage when the device is in the on state. The open load and short-to-battery fault threshold voltage is fixed and cannot be modified via the SPI.

The Open Load feature could be disabled (current source disable) by clearing the appropriate bit in the in the pre-driver configuration register.

5.6.2.4 Current sense protection (OC) strategy

Two current measurement circuits, ISGNSENSP/N and O2HSENSP/N, are available for more accurate current control and better protection of pre-driver. A current sense resistor should be place between the IGNSENSP and IGNSENSN pins for IGNOUT1 and IGNOUT2 and between O2HSENSEP and O2HSENSEN for O2HOUT.

When both IGNOUT1 and IGNOUT2 pre-drivers are used as ignition (IGBT) pre-drivers, both pre-drivers can share one current sense resistor. The pre-driver configuration determines the value of the current sense threshold voltage across the current sense resistor. The voltage threshold is $V_{sense\text{-}th}$ typically 200 mV. It is changed to typically 400 mV when both IGNOUT1 and IGNOUT2 are configured as IGBT gate drivers and both IGNOUT1 and IGNOUT2 are ON. The IGNOUT2 pre-driver does not have an associated current sense circuit and relies on short-to-battery (drain voltage sense) protection only.

When one pre-driver is used as an ignition pre-driver and the other pre-driver is used as a GPGD, the current sense circuit is connected only to the ignition driver channel.

When both pre-drivers are designated as GPGD pre-drivers, only pre-driver #1 has use of the current sense circuit, the other pre-driver, #2, only has short-to-battery protection via the drain sense voltage comparator. The O2HOUT has its own current sense circuit, O2HSENSP/N.

Table 45. Current sense protection strategy overview

Output mode configuration		Current sense measurement circuit available on	Protection available	
IGN1OUT	IGN2OUT		for IGNOUT1	for IGNOUT2
IGBT	IGBT	IGNOUT1 and IGNOUT2 (shared)	SVBAT and current sense	SVBAT and current sense
IGBT	GPGD	IGNOUT1	SVBAT and current sense	SVBAT
GPGD	IGBT	IGNOUT2	SVBAT	SVBAT and current sense
GPGD	GPGD	IGNOUT1	SVBAT and current sense	SVBAT

5.6.2.5 Retry feature

See 5.5.2.3.2. Retry feature, page 35

5.6.2.6 Output pre-driver diagnostics

Overcurrent (OC) and open load (OL) conditions are reported through the status register for each pre-driver. There is also a bit in the SPI status register to indicate when any of the pre-drivers report a fault and when a particular output has any of the four possible fault conditions present. The MCU polls for fault conditions by looking for a single bit in one register to detect the presence of any fault in the circuit.

5.6.3 SPI drivers registers

5.6.3.1 SPI configuration registers

Table 46. Pre-driver configuration registers

Reg #	Hex			7	6	5	4	3	2	1	0
7	7	O2 Heater Pre-driver		**GPGD**/IGN Select	Retry Enable	x	**OL Current Sink**	x	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
8	8	Ignition 1 Pre-driver		GPGD/**IGN** Select	Retry Enable	x	OL Current Sink	x	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
9	9	Ignition 2 Pre-driver		GPGD/**IGN** Select	Retry Enable	x	OL Current Sink	x	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 47. Pre-driver configuration registers field description

Field	Description
7-GPGD/IGN	GPGD/IGN mode selection 0- General Purpose Gate Driver (Default for O2HOUT) 1-IGBT Driver (Default for IGNOUT1and2)
6-Retry Enable	Retry Enable 0-Disable 1-Enable
4-OL Current Sink	Open Load Current Sink Enable 0- Disable (Open Load Flag in status register will be forced to 0) 1- Enable (Default for O2Heater Pre-driver)
2-OR/AND	OR/AND logical action to control Output 0- OR between Input pin and Control bit (Default) 1-AND between Input pin and Control bit
1/0 -PWM Freq1/0.	PWM Frequency and Duty Cycle Mode 00-PWM Freq.: None or Ext.Pin - D/C: None or ext.Pin 01-PWM Freq.:100 HZ-D/C: Internal 10-PWM Freq.: 1 KHZ-D/C: Internal 01-PWM Freq.:On ext. pin /100 -D/C: Internal

5.6.3.2 SPI control registers

Table 48. Main OFF/ON control register

Reg #	Hex			7	6	5	4	3	2	1	0
0	0	Main OFF/ON Control		INJ1	INJ2	REL1	REL2	LAMP	IGN1	IGN2	O2H
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 49. Main OFF/ON control register field description

Field	Description
2-IGN1	IGN1 Bit Control 0-OFF 1-ON
1-IGN2	IGN2 Bit Control 0-OFF 1-ON
0-O2H	O2H Bit Control 0-OFF 1-ON

Table 50. PWM D/C configuration register

Reg #	Hex			7	6	5	4	3	2	1	0
9	9	O2 Heater Pre-driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
10	A	Ignition 1 Pre-driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
11	B	Ignition 2 Pre-driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 51. PWM D/C configuration register field description

Field	Description
6-0 -PWMx	PWM Duty Cycle Setting with 1 % increment 0000000 to 1100100 (Dec. 100) represent 0 % to 100 % 1100100(Dec. 100) to 1111111 (Dec.127) all map to 100 %.

5.6.3.3 SPI status registers

Table 52. Pre-driver status registers

Reg #	Hex			7	6	5	4	3	2	1	0
7	7	O2 Heater Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
8	8	Ignition 1 Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
9	9	Ignition 2 Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 53. Pre-driver status registers field description

Field	Description
7-Faults	Global Driver Fault bit (by driver) Logical OR of bit 3-2 0-No Fault 1-Fault detected
3-Open Load OL	Open Load Fault Flag 0-No Fault (Forced to 0 if OL feature disabled) 1-Fault detected
2-Overcurrent OC	Overcurrent Fault Flag (including Short To V_{BAT} Fault) 0-No Fault 1-Fault detected

Table 54. System On/Off indicators status register

Reg #	Hex			7	6	5	4	3	2	1	0
14	E	System On/Off Indicators		INJ1 **Off**/On	INJ2 **Off**/On	REL1 **Off**/On	REL2 **Off**/On	LAMP **Off**/On	IGN1 **Off**/On	IGN2 **Off**/On	O2H **Off**/On
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 55. System On/Off indicators status register field description

Field	Description
2-0 xxx Off/On	Pre-driver On/Off Status 0- Off 1- On

5.7 VRS circuitry

5.7.1 Pin description

5.7.1.1 VRSP and VRSN inputs

The VRSP and VRSN form a differential input for the Variable Reluctance Sensor attached to the crankshaft toothed wheel. It is important to provide an external 15 kΩ current limiting resistors to prevent damage to the VRSP and VRSN inputs (See **Figure 17**).The VRS can be connected to the 33814 in either a differential or single-ended fashion.The use of a differential filtering capacitor and grounded capacitors of at least 100 nF are also advisable. In some applications, placing a damping resistor of approximately 5.0 kΩ directly across the pickup coil is also useful to minimize high frequency ringing.

5.7.1.2 VRSOUT output

The VRSOUT Pin is the output of the VRS circuit, which is a 5.0 Volt logic level signal provided to the MCU.

5.7.2 Functions description

The 33814 contains a VRS input conditioning circuit employing a differential input. VRSP and VRSN are the positive and negative inputs from the VRS (See **Figure 17**). An internal zener diode clamps to ground and V_{CC} limits the input voltage to within the safe operating range of the circuit.

The VRS circuit conditions and digitizes the input from the crankshaft mounted toothed wheel to provide an angle clock and RPM data to the MCU. This circuit provides a comparator with multiple thresholds programmed via the SPI. This allows the VRS circuit to handle different sensors and a dynamic range of VRS output at engine speeds ranging from cranking to running. The output of this circuit is provided on the VRSOUT pin to the MCU. The comparator threshold values can also be controlled automatically based on the input signal amplitude.

The output of the comparator contains a programmable one shot, noise blanking circuit. The time value of this blanking pulse can be selected via the SPI as a percentage of the last input high (or low) pulse.The VRSOUT output can also be divided and sent to the TACHOUT pin to drive a tachometer.

Two different SPI registers are provided to control the VRS circuit values in the manual mode. The SPI VRS configuration register is used to set the ‘engine running’ values for the threshold and blanking filter, and the SPI VRS control register is used to provide the ‘engine cranking’ threshold and blanking filter values. Once the engine is running, the MCU clears the SPI VRS control register (engine cranking) and the 33814 uses the values found in the SPI VRS configuration register (engine running).

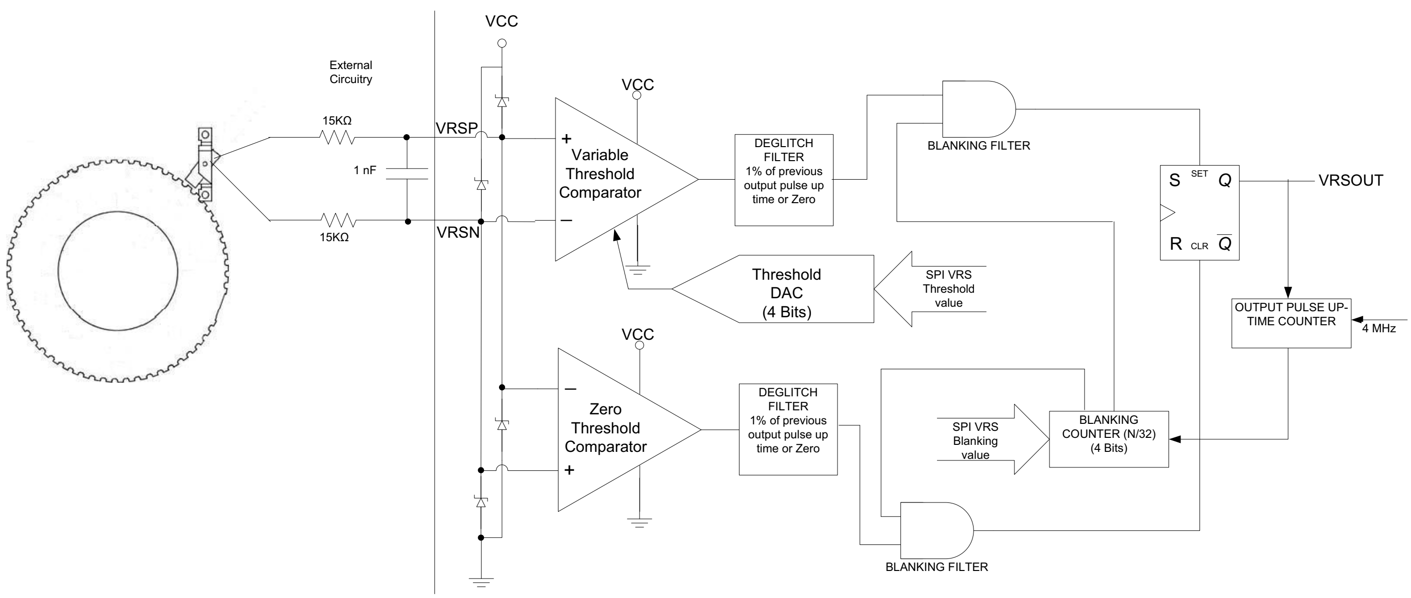


Figure 17. VRS schematic

5.7.2.1 ‘Engine Running’ and ‘Engine Cranking’ parameters

Two different SPI registers are provided to define two different sets of parameters (Input Threshold and Blanking Time) for ‘engine running’ and ‘engine cranking’ conditions, in the manual mode. The SPI VRS Engine Running Parameters register is used to set the ‘engine running’ values for the threshold and blanking filter. The SPI VRS Engine Cranking Parameters register is used to set the ‘engine cranking’ values for the threshold and blanking filter.

When the contents of the SPI VRS Engine Cranking Parameters register contains all zeros, the value for parameters is taken from the value in the SPI VRS Engine Running Parameters register.

When the contents of the SPI VRS Engine Cranking Parameters register is non-zero, the value for parameters is taken from this register. So from system point of view, once the engine is running, the MCU should clear the SPI VRS Engine Cranking Parameters register and the 33814 uses the values found in the SPI VRS Engine Running Parameters.

5.7.2.1.1 Input comparator threshold values

The threshold voltage for the input comparator is produced by a 4-bit D/A converter. The SPI VRS Engine Cranking Parameters register or SPI VRS Engine Running Parameters register controls the output value of the D/A.The values output by this D/A, using one or the other register, are listed in the below threshold values table.

Table 56. Input comparator threshold value table

SPI VRS Manual Parameter Configuration Registers Bits 7, 6, 5, 4	Min. Threshold Value	Threshold Values (Nominal)	Max. Threshold Value	Comment
0000	—	10 mv	28 mv	Tolerance not specified, for information only. Monotonicity not guaranteed.
0001	—	14 mv	36 mv	
0010	3.0 mv	20 mv	38 mv	Tolerance not specified, for information only. Only specified for monotonicity.
0011	5.0 mv	28 mv	50 mv	
0100	21 mv	40 mv	55 mv	
0101 (default)	25 mv	56 mv	80 mv	
0110	56 mv	80 mv	92 mv	
0111	-20%	110 mv	+20%	Tolerance and monotonicity specified.
1000	-20%	150 mv	+20%	
1001	-20%	215 mv	+20%	
1010	-20%	300 mv	+20%	
1011	-20%	425 mv	+20%	
1100	-20%	600 mv	+20%	
1101	-20%	850 mv	+20%	
1110	-20%	1.21 V	+20%	
1111	-20%	1.715 V	+20%	

5.7.2.1.2 Blanking time definitions

The values for the one shot blanking as a percentage of the last high output pulse period is shown in Table 57.

Table 57. SPI VRS manual configuration register

SPI VRS Configuration/Control Register Bits 3,2,1,0	Blanking Time in % (of last pulse high period)
0000 (default)	0.0
0001	3.12
0010	6.25
0011	9.37
0100	12.5
0101	15.62
0110	18.75
0111	21.87
1000	25
1001	28.1
1010	31.3
1011	34.4
1100	37.5
1101	40.6
1110	43.8
1111	46.9

5.7.2.2 Manual and Automatic modes

The SPI VRS miscellaneous configuration register has a bit to enable the automatic selection of the comparator threshold (bit 7). At this time, the operation of automatic mode remains.

Under cranking conditions in Manual mode, the selected threshold value is fixed (VT Selected) by the SPI VRS Engine Cranking Parameters register. To avoid invalid detection due to noise close to the selected threshold, Automatic mode allows the VRS system to be less sensitive to noise in the cranking mode.

As soon as the VRS Input signal crosses zero, the VRS system selects the highest Input Comparator Threshold (VT Max 1.715 V Typ.). A decay circuitry ensures the VRS system decays from VT Max to VT Selected with the correct timing. The setting of the decay timing is done through the SPI VRS Automatic Parameters Configuration Register.

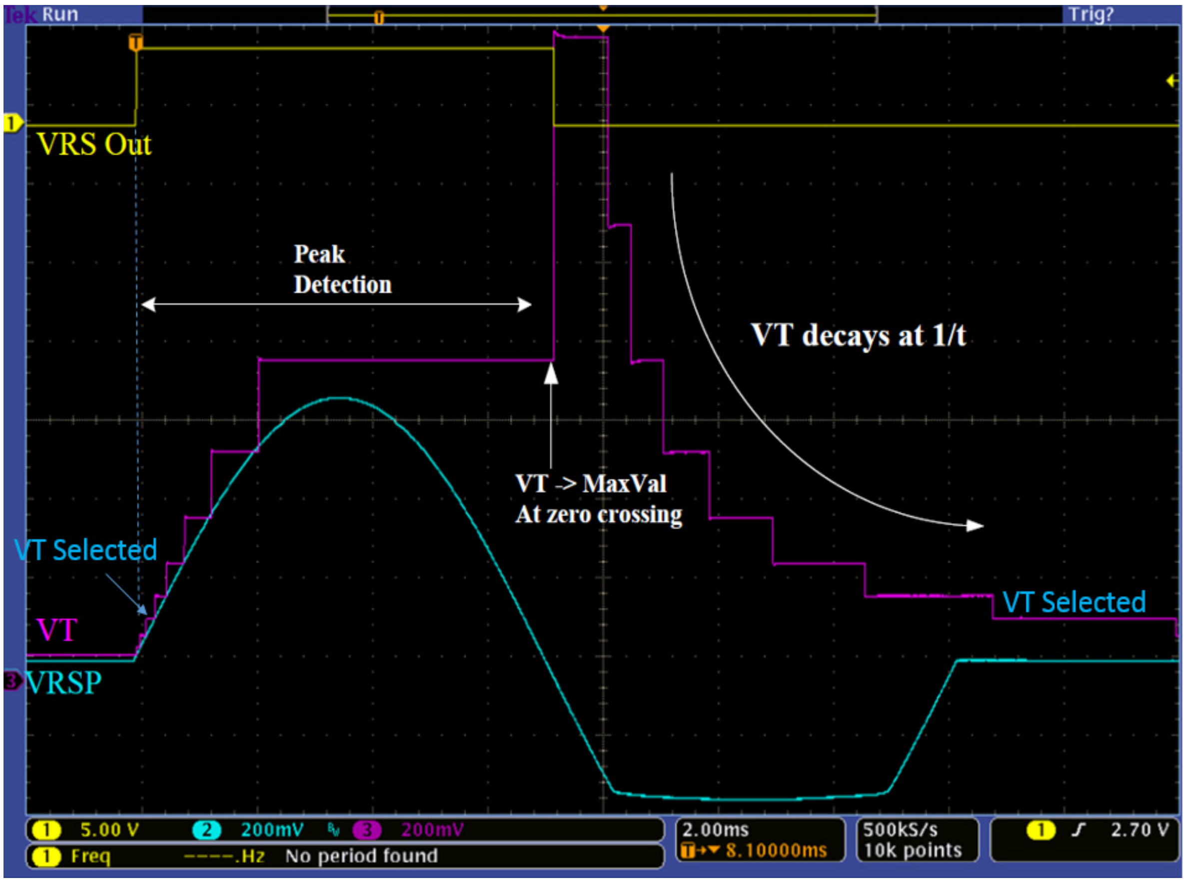


Figure 18. Automatic mode illustration (VT signal in pink is internal IC signal not observable in application)

Mantissa and Exponent parameters defined in the VRS Automatic mode parameters register set the decay time of the system.

The mathematical formula is:

E = $\log_2[(V_{peak} \times Tau)/18.1] - 4$ truncated

M = $\{[(V_{peak} \times Tau)/18.1]/2^{E}\} - 16$ rounded to nearest integer

So Tau (timing between zero crossing and V_{PEAK}) and the V_{PEAK} value are required to determine M and E parameters. Tau and V_{PEAK} could be calculated, based on system specification (number of teeth, minimum RPM,…). However, NXP recommends measuring physical parameters on the real application to define the best setting. A dedicated application note is available to explain the mathematical principle and measurement instructions.

5.7.2.3 Disable VRS bit

The disable VRS bit in the SPI VRS miscellaneous configuration register is used to disable the VRS input circuitry when there is no need for a VRS input conditioning circuit. This would be the case, for example, if the crankshaft wheel sensor was a hall effect device whose output could be directly input to the MCU. The default for this bit is zero (0) indicating the VRS input conditioning circuitry is active.

5.7.2.4 High/Low reference bit

The High/Low reference bit in the SPI VRS miscellaneous configuration register is used to change the use of the input high pulse timing to input low pulse timing, in cases where an elongated tooth wheel is being used rather than the missing tooth wheel. The default for this bit is zero (0), indicating the use of a crankshaft wheel with a missing tooth (or teeth).

5.7.2.5 VRS deglitching filters

The VRS input circuit has additional filters on the rising and falling edges of the input waveforms to reduce the effect of short transitions occurring during noise sensitive times. The deglitching filters are approximately 1 % of the last positive pulse period. The deglitch filters are enabled by setting the deglitch bit (bit 3) in the SPI VRS miscellaneous parameters configuration register. This bit is, by default, zero (0), meaning the deglitch filters are disabled.

5.7.2.6 GND VRSN bit

To use the VRS inputs in a single-ended configuration, the “GND VRSN” bit in the SPI Configuration register must be set to indicate to the 33814 that this mode is being used. The VRS is then connected between the VRSP input and ground. The default for this bit is zero (0), indicating the differential mode is selected. Note that in the single ended configuration, the 2.5 Volt reference should be disconnected (Disable 2.5V CM bit should be set to 1) when using a Variable Reluctance Sensor.

Note that a hall effect sensor can be used instead of a VRS. To do so, the bits GND VRSN and disable 2.5 V ref must be 0 and the VRSN pin must not be connected. In this case, the voltage on VRSN is 2.5 V and the 0 crossing can be done even if low state output of the hall effect is 0 V or little higher.

5.7.2.7 Inverting inputs

The Inv. Inputs Bit in the SPI VRS Miscellaneous Parameter Register is used to make a logical inversion of all functions. This is swapping the VRSP and VRSN signals.

5.7.2.8 2.5 Volt reference disconnect bit

The disconnect 2.5 V reference bit in the SPI VRS configuration register is used to disconnect the internal 2.5 V reference signal from the VRSN and VRSP inputs so an external reference voltage can be employed. The default state of this bit is zero (0), indicating the internal 2.5 Volt reference voltage is connected to the VRSN and VRSP inputs.

5.7.2.9 VRS peak detector

The VRS peak detector determines the magnitude of the positive peak of the VRS input signal and digitizes it. The value of the VRS peak voltage is reported in the VRS SPI status register bits 7, 6, 5 and 4. The MCU reads the input pulse peak voltage value after the zero crossing time and uses this information to set the threshold and blanking parameters for subsequent input pulses. Status bits reflect the last detected peak and only read 0000 after a POR or SPI reset command.

Table 58. Peak detector output in SPI VRS status register

SPI VRS Status Register Bits 7,6,5,4	Peak Values (nominal)
0000	10 mV
0001	14 mV
0010	20 mV
0011	28 mV
0100	40 mV
0101	56 mV
0110	80 mV
0111	110 mV
1000	150 mV
1001	215 mV

Table 58. Peak detector output in SPI VRS status register (continued)

1010	300 mV
1011	425 mV
1100	600 mV
1101	850 mV
1110	1.210 V
1111	1.715 V

5.7.2.10 Clamp active status bits

There are two clamp active status bits in the SPI VRS status register. One is for the low pulse clamp and the other is for the high pulse clamp. When either of these bits are a one (1), it indicates the peak voltage for the part of the input waveform which has exceeded the clamp voltage and is clamped to the high or low voltage limit. These status bits can be used to indicate the engine has attained the speed necessary to switch from 'cranking' values for the threshold and blanking (in the SPI VRS control register) to the 'running' values (in the SPI VRS configuration register).

5.7.3 SPI drivers registers

5.7.3.1 SPI configuration registers

Table 59. VRS configuration registers

Reg #	Hex			7	6	5	4	3	2	1	0
11	B	VRS Engine Running Parameters		Threshold 3	**Threshold 2**	Threshold 1	Threshold 0	Filter Time 3	Filter Time 2	**Filter Time 1**	**Filter Time 0**
			Reset	(0)	(1)	(0)	(1)	(0)	(0)	(1)	(1)
12	C	VRS Automatic Parameters		mantiss 8	mantiss 4	**mantiss 2**	mantiss 1	exponent 8	exponent 4	exponent 2	**exponent 1**
			Reset	(0)	(0)	(1)	(0)	(0)	(0)	(0)	(1)
13	D	VRS Miscellaneous Parameters		**Man.**/Auto	Disable VRS	x	**High**/ Low Ref	De-glitch	Gnd VRSN	Inv Inputs	Disable 2.5 V CM
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 60. VRS engine running parameters register field description

Field	Description
7-4 Threshold x	Input Comparator Threshold Value Selection, Table 56
3-0 Filter Time x	Blanking Time Selection, Table 57

Table 61. VRS automatic parameters register field

Field	Description
7-5 Mantissa x	Mantissa parameter to set the decay timing in Automatic mode
3-0 Exponent x	Exponent parameter to set the decay timing in Automatic mode

Table 62. VRS miscellaneous parameters register field

Field	Description
7-MAN/Auto	Manual/Automatic Mode Selection 0-Manual Mode (Default) 1-Automatic Mode
6-Disable VRS	Disabling the VRS System 0- VRS Enable (Default) 1-VRS disable
4-High/Low Ref	High/Low reference 0-High Pulse Timing (Missing tooth Wheel) 1-Low Pulse Timing (Elongated Tooth Wheel)
3-De-glitch	Additional Deglitching Filter 0-De-glitch Disable 1-De-glitch enable
2-Gnd VRSN	Single Ended Configuration (VRSN = GND) or Differential mode configuration 0-Differential Mode Configuration 1-Single Ended Configuration
1-Inv inputs	Logical Inversion of all functions 0-VRSN and VRSP not swapped 1-VRSN and VRSP swapped
0-Disable 2.5V CM	Disable 2.5 V reference 0-Internal 2.5 V Ref connected to VRSN and VSRP 1-Internal 2.5 V Ref disconnected from VRSN and VRSP

5.7.3.2 SPI control registers

Table 63. VRS engine cranking parameters register

Reg #	Hex			7	6	5	4	3	2	1	0
13	D	VRS Engine Cranking Parameters		Threshold 3	Threshold 2	Threshold 1	Threshold 0	Filter Time 3	Filter Time 2	Filter Time 1	Filter Time 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 64. VRS engine cranking parameters register field description

Field	Description
7-4 Threshold x	Input Comparator Threshold Value Selection, Table 56
3-0 Filter Time x	Blanking Time Selection, Table 57

5.7.3.3 SPI status registers

Table 65. VRS status register

Reg #	Hex			7	6	5	4	3	2	1	0
11	B	VRS Conditioner and ISO9141 Faults		Peak 8	Peak 4	Peak 2	Peak 1	x	Clamp-active VRSP	Clamp-active VRSN	ISO Overtemp OT
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 66. VRS status register description field

Field	Description
7-4 Peak x	Reflect the magnitude of the positive peak of the VRS input according to **Table 58**
2-Clamp Active VRSP	Positive Clamp Active status 0-Clamp Value not reached 1-Clamp Value reached
1-Clamp Active VRSN	Negative Clamp Active status 0-Clamp Value not reached 1-Clamp Value reached

5.8 ISO9141 bus

Three pins are used to provide an ISO9141 K-line communication link for the MCU to support system diagnostics.

5.8.1 MTX output pin

MTX is the 5.0 V logic level serial input to the IC from the MCU.

5.8.2 MRX input pin

MRX is the 5.0 V logic level serial output line to the MCU.

5.8.3 ISO9141 pin

The ISO9141 pin is a bi-directional line with an internal 32k pull-up to V_{PWR}. This allows to customer to save an external pull-up resistor.

5.8.4 Functions description

Three pins are used to provide an ISO9141 K-line communication link for the MCU to support system diagnostics. This system is consistent with the ISO9141 specification for signaling to and from the MCU.

K-Line has its own overtemperature protection and fault bit reporting.

5.8.5 SPI drivers registers

There is only one bit in the SPI Status register to indicate an overtemperature fault from the ISO9141 functional block. There are no Configuration or Control registers associated with this functional block.

Table 67. ISO status register

Reg #	Hex			7	6	5	4	3	2	1	0
11	B	VRS Conditioner and ISO9141 Faults		Peak 8	Peak 4	Peak 2	Peak 1	x	Clamp-active VRSP	Clamp-active VRSN	ISO Overtemp OT
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 68. ISO status register description field

Field	Description
0-ISO Overtemp OT	Overtemp condition fault 0-No overtemp condition reached 1-Overtemp condition reached

5.9 Mode code and revision number

One status register is reserved for reporting the model code and revision of the C circuits. The model code for the 33814 is 001. The revision code is the current version number for the circuit. This register is read-only.

Table 69. Model code/revision number register

Reg #	Hex			7	6	5	4	3	2	1	0
15	F	Model Code/ Revision Number* *Read Only except for POST Enable		Model Code 2	Model Code 1	**Model Code 0**	Rev #	Rev #	Rev #	Rev #	Rev #
			Reset	(0)	(0)	(1)	(x)	(x)	(x)	(x)	(x)

Table 70. Model code/revision number register field description

Field	Description
7-5 Model Code	Model Code #001 = 33814 device
4-0 Rev #	Rev #

5.10 SPI

5.10.1 Pin description

5.10.1.1 SCLK input

The serial clock (SCLK) pin clocks the internal SPI shift register of the 33814. The SI data is latched into the input shift register on the rising edge of SCLK signal. The SO pin shifts status bits out on the falling edge of SCLK. The SO data is available for the MCU to read on the rising edge of SCLK. With CSB in a logic high state, signals on the SCLK and SI pins are ignored and the SO pin is in a high-impedance state.The SCLK signal consists of a 50 % duty cycle with CMOS logic levels referenced to V_{CC}. All SPI transfers consist of exactly 16 SCLK pulses. If any more or less than 16 clock pulses are received within one frame of CSB going low and then high, a SPI error is reported in the SPI Status Register. The SPI error bit also sets whenever an invalid SPI message is received, even though it may contain 16 bits.

5.10.1.2 CSB input

The system MCU selects which slave is to receive SPI communication using separate chip select (CSB) pins. With the CSB in a logic low state, SPI words may be sent to the 33814 via the serial input (SI) pin and status information is received by the MCU via the serial output (SO) pin. The falling edge of CSB enables the SO output and transfers status information into the SO buffer.

The rising edge of the CSB initiates the following operation:

- Disables the SO driver (high-impedance)
- Activates the received command word, allowing the 33814 to activate/deactivate output drivers

To avoid spurious data, the high-to-low and low-to-high transitions of the CSB signal must occur only when SCLK is in a logic low state. Internal to the 33814 device is an active pull-up to V_{CC} on CSB. In cases where voltage exists on CSB without the application of V_{CC}, no current flows from CSB to the VCC pin.This input requires CMOS logic levels referenced to V_{CC} and has an internal active pull-up current source.

5.10.1.3 SI input

The SI pin is used for serial instruction data input. SI information is latched into the input register on the rising edge of SCLK and the input data transitions on the falling edge of SCLK. A logic high state present on SI programs a one in the command word on the rising edge of the CSB signal. To program a complete word, 16 bits of information must be entered into the device.This input requires CMOS logic levels referenced to V_{CC}.

5.10.1.4 SO output

The SO pin is the output from the SPI shift register. The SO pin remains high-impedance until the CSB pin transitions to a logic low state. All normal operating drivers are reported as zero, all faulted drivers are reported as one. The negative transition of CSB enables the SO driver. The SI/SO shifting of the data follows a first-in-first-out protocol with both input and output words transferring the most significant bit (MSB) first. The serial output data is available to be latched by the MCU on the rising edge of SCLK. The SO data transitions on the falling edge of the SCLK. This output provides CMOS logic levels referenced to $V_{CC.}$

5.10.2 MCU SPI interface description

The 33814 device directly interfaces to a 5.0 V microcontroller unit (MCU) using a16-bit serial peripheral interface (SPI) protocol. SPI serial clock frequencies up to 8.0 MHz can be used when programming and reading output status information (production tested at 1.0 MHz). Figure 19 illustrates the SPI configuration between an MCU and one 33814.

Data is sent to the 33814 device through the SI input pin. As data is being clocked into the SI pin, other data is being clocked out of the device by the SO output pin. The response data received by the MCU during SPI communication depends on the previous SPI message sent to the device. The SPI can be used to read or write data to the configuration and control registers and to read or write the data contained in the status registers.

The MCU is only allowed to read or clear bits (write zeros) in the status register unless the Power ON Self-test (POST) enable bit in the control register is set. When the POST enable bit is set, the MCU can read and write zeros or ones to the status register. Note that the MCU must clear the POST enable bit before operation is resumed or the status register does not update with fault indications.

5.10.2.1 SPI integrity check

One SPI word is reserved as a SPI check message. When bits 12 through15 are all zero, the SPI echoes the remaining 12-bit SPI word sent and flips bits 12 through14, bit 15 remains a 0. This allows the MCU to poll the SPI and compare the received message to confirm the integrity of the SPI communication channel to the 33814. There is a SPI error bit in the SPI status register indicating if an incorrect SPI message has been received. The SPI error bit in the SPI status register is set whenever any SPI message error is detected.

Important A SCLK pulse count strategy has been implemented to ensure integrity of SPI communications. Only SPI messages consisting of 16 SCLK pulses are acknowledged. SPI messages consisting of other than 16 SCLK pulses are ignored by the device and reported as a SPI error. Invalid SPI messages, containing invalid commands or addresses are also flagged as a SPI error.

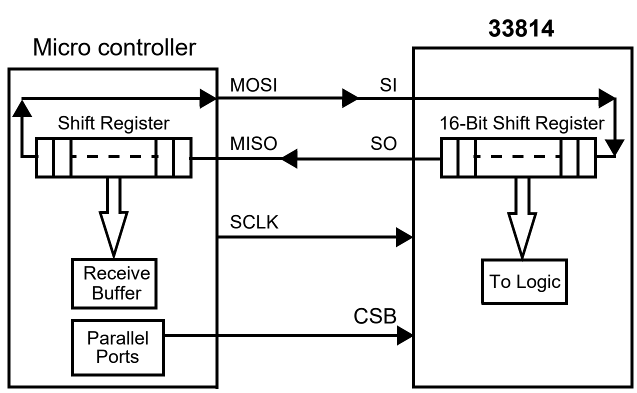


Figure 19. SPI interface with microprocessor

Two or more 33814 devices can be used in a module system. Multiple ICs can be SPI configured in parallel only**.** Figure 19 demonstrates the configuration.

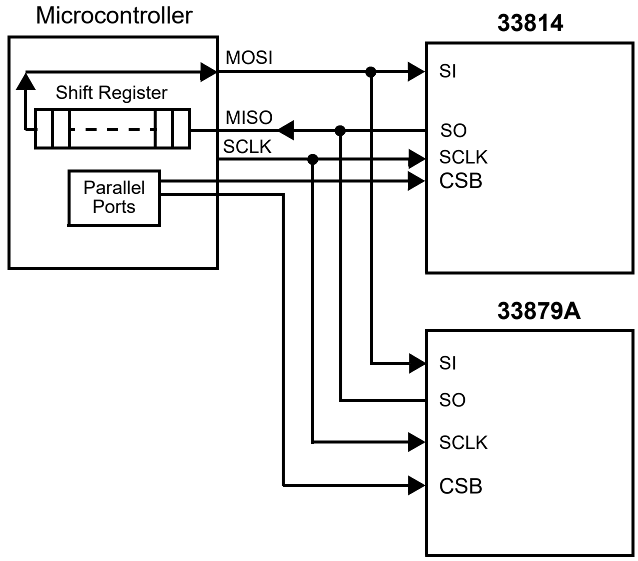


Figure 20. SPI parallel interface (only) with microprocessor

5.10.2.2 SPI register definitions

There are three basic SPI register types:

Configuration registers - used to set the operating modes and parameters for the 33814 functional blocks. Each output can be configured by setting the individual bits in the configuration register for output according to the descriptions in the previous functional descriptions for each particular output.

Control registers - used to turn outputs on and off and set the PWM duty cycle for outputs used as PWM outputs. Setting the temporary operating parameters for the watchdog timer and the VRS circuit is also used.

Status registers - used to annunciate faults and other values the MCU may need to act upon. Each output and functional block has a status register associated with it and the individual fault bits for each of the faults monitored are contained in these registers.

Non-fault bits in the status register can be set and cleared by the 33814 circuit. All status register bits not marked as ‘x’ can be cleared by the MCU only when the POST bit is zero (0). When the POST bit is one (1), the MCU can read or write any existing bit in the status register. Non-existing bits (marked with an ‘x’ in the table) cannot be changed from the default zero (0) value.

Entries in the following SPI Registers marked with an ‘x’ are non-existent bits. They are set to zero (0) by default and cannot be changed by reading or writing to them. They should be ignored when testing registers during POST.

5.10.2.3 SPI command summary

The SPI commands are defined as 16 bits with 4 address control bits and 12 command data bits. There are 7 separate commands used to set the operational parameters of device. The operational parameters are stored internally in 8-bit registers. Write commands write the data contained in the present SPI word whereas read commands must wait until the next SPI command is sent to read the data requested. Table 11 defines the commands and default state of the internal registers at POR. SPI commands may be sent to the device at any time while the device is in the Normal state. Messages sent are acted upon on the rising edge of the CSB input. The bit value returned equals bit value sent for this command.

Table 71. SPI command messages

Command		Control Address Bits				Data Bits											
	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI Check	0	0	0	0	0	X*	X*	X*	X*	X*	X*	X*	X*	X*	X*	X*	X*
Read Configuration Register	1	0	0	0	1	<0000> Internal Register Address				0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Write Configuration Register	2	0	0	1	0	<0000> Internal Register Address				0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Table 71. SPI command messages (continued)

Command		Control Address Bits				Data Bits											
	hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Status Register	3	0	0	1	1	<0000> Internal Register Address				0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Write Status Register	4	0	1	0	0	<0000> Internal Register Address				0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Read Control Register	5	0	1	0	1	<0000> Internal Register Address				0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Write Control Register	6	0	1	1	0	<0000> Internal Register Address				0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
SPI Check Response	7	0	1	1	1	X*	X*	X*	X*	X*	X*	X*	X*	X*	X*	X*	X*

There are seven SPI commands issued by the MCU to:

- Do a SPI Check verification
- Read the contents of the SPI configuration registers
- Write the contents of the SPI configuration registers
- Read the contents of the SPI status registers
- Write the contents of the SPI status registers
- Read the contents of the SPI control registers
- Write the contents of the SPI control registers

5.10.3 SPI drivers register

Table 72. Power supply and any system fault status register

Reg #	Hex			7	6	5	4	3	2	1	0
13	D	Power Supply and Any System Faults		Any System Faults	Keysw	Pwren	Batsw	SPI error	V_{PROT} Short to Battery	V_{PROT} Overtemp OT	V_{PROT} Short to Ground
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 73. Power supply and any system fault status register description field

Field	Description
3-SPI Error	SPI Error fault status 0-No fault reported 1-Fault reported

5.11 SPI registers mapping

The SPI interface consists of three blocks of four, 8-bit read/write registers. There are three types of SPI registers:

- **Configuration registers** - These registers allow the MCU to configure the various parameters and options for the various functional blocks.
- **Control registers** - These registers are used to command the outputs on and off and set the PWM duty cycle values.
- **Status registers** - These registers report back faults and other conditions of the various functional blocks.

The following conventions are used in the SPI register tables:

- All default selections are in **BOLD** fonts.
- Non-default selections are in normal font.
- The first selection listed is the default selection.
- The binary values shown, (0 or 1) are the default values after a reset has occurred.

Table 74. SPI configuration registers

Reg #	Hex			7	6	5	4	3	2	1	0
0	0	Injector 1 Driver		Retry Enable	x	x	**OL Current Sink Enable**	In-Rush Delay	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
1	1	Injector 2 Driver		Retry Enable	x	x	**OL Current Sink Enable**	In-Rush Delay	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
2	2	Relay 1 Driver		Retry Enable	x	x	**OL Current Sink Enable**	In-Rush Delay	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
3	3	Relay 2 Driver		Retry Enable	Shutdown DisableSD D	x	**OL Current Sink Enable**	In-Rush Delay	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
4	4	Tachometer Driver		Retry Enable	**Vrsout**/ LSD	**Vrsout**/ Osc. mode	N16/OL Current Sink Enable	N8/In-Rush Delay	N4/Osc 2	N2/Osc 1/ PWM Freq. 1	N1/Osc 0/ PWM Freq. 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(1)
5	5	Lamp Driver		Retry Enable	x	x	**OL Current Sink Enable**	**In-Rush Delay**	x	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(1)	(0)	(0)	(0)
6	6	Battery Switch Logic Output		HSD Mode	X	x	x	x	x	PWM Freq.1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
7	7	O2 Heater Pre-driver		**GPGD**/IGN Select	Retry Enable	x	**OL Current Sink**	x	***OR***/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(0)	(0)
8	8	Ignition 1 Pre-driver		GPGD/**IGN** Select	Retry Enable	x	OL Current Sink	x	***OR***/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
9	9	Ignition 2 Pre-driver		GPGD/**IGN** Select	Retry Enable	x	OL Current Sink	x	**OR**/AND	PWM Freq. 1	PWM Freq. 0
			Reset	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
10	A	Watchdog Parameters		Disable/ **Enable**	Load Time x1 sec	Load Time x100 ms	Load Time x10 ms	Load Time 8	Load Time 4	Load Time 2	Load Time 1
			Reset	(1)	(1)	(0)	(0)	(1)	(0)	(1)	(0)
11	B	VRS Engine Running Parameters		Threshold 3	Threshold 2	Threshold 1	Threshold 0	Filter Time 3	Filter Time 2	Filter Time 1	Filter Time 0
			Reset	(0)	(1)	(0)	(1)	(0)	(0)	(1)	(1)
12	C	VRS Automatic Parameters		mantiss 8	mantiss 4	mantiss 2	mantiss 1	exponent 8	exponent 4	exponent 2	exponent 1
			Reset	(0)	(0)	(1)	(0)	(0)	(0)	(0)	(1)
13	D	VRS Miscellaneous Parameters		**Man.**/Auto	Disable VRS	x	**High**/ Low Ref	De-glitch	Gnd VRSN	Inv Inputs	Disable 2.5 V CM
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 75. SPI control registers

Reg #	Hex			7	6	5	4	3	2	1	0
0	0	Main OFF/ON Control		INJ1	INJ2	REL1	REL2	LAMP	IGN1	IGN2	O2H
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
1	1	Other OFF/ON Control		Pwren **OFF**/ON	POST Enable **OFF**/ON	X	VProt OFF/ **ON**	X	Batsw **OFF**/ON	Tach OFF/**ON**	RESET internal only
			Reset	(0)	(0)	(0)	(1)	(0)	(0)	(1)	(0)
2	2	Injector 1 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
3	3	Injector 2 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
4	4	Relay 1 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
5	5	Relay 2 Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
6	6	Tachometer Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
7	7	Lamp Driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
8	8	Batsw		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
9	9	O2 Heater Pre-driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
10	A	Ignition 1 Pre-driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
11	B	Ignition 2 Pre-driver		X	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
12	C	Watchdog		WDRFSH	Load Time x1 sec	Load Time x100 ms	Load Time x10 ms	Load Time 8	Load Time 4	Load Time 2	Load Time 1
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
13	D	VRS Engine Cranking Parameters		Threshold 3	Threshold 2	Threshold 1	Threshold 0	Filter Time 3	Filter Time 2	Filter Time 1	Filter Time 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 76. SPI status registers

Reg #	Hex			7	6	5	4	3	2	1	0
0	0	Injector 1 Driver Faults		Faults	x	x	x	Open Load OL	Over - current OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
1	1	Injector 2 Driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
2	2	Relay 1 Driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Table 76. SPI status registers (continued)

3	3	Relay 2 Driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
4	4	Tachometer Driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	Overtemp OT	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
5	5	Lamp Driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	Overtemp OT	Short Gnd SG
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
7	7	O2 Heater Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
8	8	Ignition 1 Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
9	9	Ignition 2 Pre-driver Faults		Faults	x	x	x	Open Load OL	Overcurrent OC	x	x
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
10	A	Watchdog State		Enable/ Disable	WD timer bit 6	WD timer bit 5	WD timer bit 4	WD timer bit 3	WD timer bit 2	WD timer bit 1	WD timer bit 0
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
11	B	VRS Conditioner and ISO9141 Faults		Peak 8	Peak 4	Peak 2	Peak 1	x	Clamp-active VRSP	Clamp-active VRSN	ISO Overtemp OT
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
13	D	Power Supply and Any System Faults		Any System Faults	Keysw	Pwren	Batsw	SPI Error	V_{PROT} Short to Battery	V_{PROT} Overtemp OT	V_{PROT} Short to Ground
			Reset	(0)	(1)	(0)	(0)	(0)	(0)	(0)	(0)
14	E	System On/Off Indicators		INJ1 **Off**/On	INJ2 **Off**/On	REL1 **Off**/On	REL2 **Off**/On	LAMP **Off**/On	IGN1 **Off**/On	IGN2 **Off**/On	O2H **Off**/On
			Reset	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)
15	F	Model Code/ Revision Number* *Read Only except for POST Enable		Model Code 2	Model Code 1	**Model Code 0**	Rev #	Rev #	Rev #	Rev #	Rev #
			Reset	(0)	(0)	(1)	(0)	(0)	(0)	(0)	(0)

Table 77. SPI configuration bits R/W access

	Reg #	Hex	Description	7	7 access	6	6 access	5	5 access	4	4 access	3	3 access	2	2 access	1	1 access	0	0 access
Configuration registers	0	0	Injector 1 driver	Retry enable	R/W	x	R[28]	x	R[28]	OL current sink enable	R/W	In-rush delay	R/W	OR/AND	R/W	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	1	1	Injector 2 driver	Retry enable	R/W	x	R[28]	x	R[28]	OL current sink enable	R/W	In-rush delay	R/W	OR/AND	R/W	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	2	2	Relay 1 driver	Retry enable	R/W	x	R[28]	x	R[28]	OL current sink enable	R/W	In-rush delay	R/W	OR/AND	R/W	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	3	3	Relay 2 driver	Retry enable	R/W	Shut down disable SDD	R/W	x		OL current sink enable		In-rush delay	R/W	OR/AND	R/W	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	4	4	Tachometer driver	Retry enable	R/W	VRSout /LSD	R/W	Vrsout/ Osc mode	R/W	N16/OL current sink enable	R/W	N8/In-rush delay	R/W	N4/Osc 2	R/W	N2/OSC 1/ PWM Freq.1	R/W	PWM Freq. 0	R/W
	5	5	Lamp driver	Retry enable	R/W	x	R[28]	x	R[28]	OL current sink enable	R/W	In-rush delay	R/W	x	R[28]	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	6	6	Battery switch logic output	HSD mode	R/W	x	R[28]	x	R[28]	x	R[28]	x	R[28]	x	R[28]	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	7	7	O2 heater predriver	CPGD/ IGN select	R/W	Retry enable	R/W	x	R[28]	OL current sink enable	R/W	x	R[28]	OR/AND	R/W	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	8	8	Ignition 1 predriver	CPGD/ IGN select	R/W	Retry enable	R/W	x	R[28]	OL current sink enable	R/W	x	R[28]	OR/AND	R/W	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	9	9	Ignition 2 predriver	CPGD/ IGN select	R/W	Retry enable	R/W	x	R[28]	OL current sink enable	R/W	x	R[28]	OR/AND	R/W	PWM Freq. 1	R/W	PWM Freq. 0	R/W
	10	A	Watchdog parameters	Disable/ Enable	R/W	Load time x1 sec	R/W	Load time x100 ms	R/W	Load time x10 ms	R/W	Load time 8	R/W	Load time 4	R/W	Load time 2	R/W	Load time 1	R/W
	11	B	VRS engine running parameters	Threshold 3	R/W	Thresh old 2	R/W	Threshold 1	R/W	Threshold 0	R/W	Filter time 3	R/W	Filter time 2	R/W	Filter time 1	R/W	Filter time 0	R/W
	12	C	VRS automatic parameters	Mantiss 8	R/W	Mantiss 4	R/W	Mantiss 2	R/W	Mantiss 1	R/W	Exponent 8	R/W	Exponent 4	R/W	Exponent 2	R/W	Expone nt 1	R/W
	13	D	VRS miscellaneous parameters	Man/Auto	R/W	Disable VRS	R/W	x	R[28]	High/low ref	R/W	De-glitch	R/W	GND VRSN	R/W	Inv inputs	R/W	Disable 2.5 V CM	R/W

Notes
28. Only read as 0

Table 78. SPI control bits R/W access

	Reg #	Hex	Description	7		6		5		4		3		2		1		0	
Control registers	0	0	Main ON/OFF control	INJ1	R/W	INJ2	R/W	REL1	R/W	REL2	R/W	LAMP	R/W	IGN1	R/W	IGN2	R/W	O2H	R/W
	1	1	Other OFF/ ON control	Pwren OFF/ ON	R[29]	POST enable OFF/ ON	R/W	x	R[29]	Vprot OFF/ ON	R/W	x	R[29]	Batsw OFF/ON	R/W	Tach OFF/ON	R/W	RESET internal only	W
	2	2	Injector 1 driver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	3	3	Injector 2 driver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	4	4	Relay 1 driver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	5	5	Relay 2 driver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	6	6	Tachometer driver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	7	7	Lamp driver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	8	8	Batsw	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	9	9	O2 heater predriver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	10	A	Ignition 1 predriver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	11	B	Ignition 2 predriver	x	R[29]	PWM6	R/W	PWM5	R/W	PWM4	R/W	PWM3	R/W	PWM2	R/W	PWM1	R/W	PWM0	R/W
	12	C	Watchdog	WDRFSH	[30]	Load time x1 sec	R/W	Load time x100 ms	R/W	Load time x10 ms	R/W	Load time 8	R/W	Load time 4	R/W	Load time 2	R/W	Load time 1	R/W
	13	D	VRS engine cranking parameters	Threshold 3	R/W	Thresh old 2	R/W	Thres hold 1	R/W	Threshold 0	R/W	Filter time 3	R/W	Filter time 2	R/W	Filter time 1		Filter time 0	R/W

Notes
29. Only read as 0
30. Can only be written to 1. Write 0 has no effect. Only read as 0.

Table 79. SPI status bits R/W access

	Reg #	Hex	Description	7		6		5		4		3		2		1		0	
Status registers	0	0	Injector 1 driver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	Over temp OT	R[33]	Short to GND (SG)	R[33]
	1	1	Injector 2 driver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	Over temp OT	R[33]	Short to GND (SG)	R[33]
	2	2	Relay 1 driver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	Over temp OT	R[33]	Short to GND (SG)	R[33]
	3	3	Relay 2 driver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	Over temp OT	R[33]	Short to GND (SG)	R[33]
	4	4	Tachometer driver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	Over temp OT	R[33]	x	R[32]
	5	5	Lamp driver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	Over temp OT	R[33]	Short to GND (SG)	R[33]
	7	7	O2 heater predriver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	x	R[32]	x	R[32]
	8	8	Ignition 1 predriver faults	Faults	R[31]	x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	x	R[32]	x	R[32]
	9	9	Ignition 2 predriver faults	Faults		x	R[32]	x	R[32]	x	R[32]	Openload OL	R[33]	Over current OC	R[33]	x	R[32]	x	R[32]
	10	A	Watchdog state	Disable/ Enable	R	WD timer bit 6	R	WD timer bit 5	R	WD timer bit 4	R	WD timer bit 3	R	WD timer bit 2	R	WD timer bit 1	R	WD timer bit 0	R
	11	B	VRS conditioner and ISO 9141 faults	Peak 8	R	Peak 4	R	Peak 2	R	Peak 1	R	x	R[32]	Clamp active VRSP	R	Clamp active VRSN	R	ISO overtemp OT	R[33]
	13	D	Power supply and any system faults	Any system faults	R[31]	Keysw	R	PWREN	R	BATSW	R	SPI error	R[33]	Vprot short to battery	R[33]	Vprot overtemp	R[33]	Vprot short to ground	R[33]
	14	E	System On/ Off indicators	INJ1 OFF/ON	R	INJ12 OFF/ ON	R	REL1 OFF/ ON	R	REL2 OFF/ ON	R	LAMP OFF/ON	R	IGN1 OFF/ ON	R	IGN2 OFF/ON	R	O2H OFF/ON	R
	15	F	Model code/ revision number	Model code 2	R	Model code 1	R	Model code 0	R	REV#	R	Rev#	R	Rev#	R	Rev#	R	Rev#	R

Notes
31. Can only be written to 0 when faults have disappeared
32. Only read as 0
33. Can only be written to 0 when the fault has disappeared

6 Typical applications

6.1 Output OFF open load fault

An Output OFF Open Load Fault is the detection and reporting of an open load when the corresponding output is disabled (input bit programmed to a logic low state). The Output OFF Open Load Fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

Each output has an internal pull-down current source or resistor. The pull-down current sources are enabled on power-up and must be enabled for Open Load Detect to function. In cases were the Open Load Detect current is disabled, the status bit always responds with logic 0. The device only shuts down the pull-down current in Sleep mode or when disabled via the SPI.

During output switching, especially with capacitive loads, a false Output OFF Open Load Fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100 to 450 μs is incorporated. The duration for which a false fault may be reported is a function of the load impedance $R_{DS(ON)}$, C_{OUT} of the MOSFET as well as the supply voltage V_{PWR}. The rising edge of CSB triggers the built-in fault delay timer. The timer must time out before the fault comparator is enabled to detect a faulted threshold. Once the condition causing the Open Load Fault is removed, the device resumes normal operation. The Open Load Fault, however, is latched in the output SO Response register for the MCU to read.

6.2 Low voltage operation

Low voltage condition (6.5 V< V_{PWR} <9.0 V) operates per the command word, however parameter tables may be out of specification and status reported on SO pin is not guaranteed.

6.3 Low-side injector driver voltage clamp

Each Injector output of the 33814 incorporates an internal voltage clamp to provide fast turn-OFF and transient protection. Each clamp independently limits the drain-to-source voltage to V_{CL}. The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) (see Figure 21). Characterization of the output clamps indicates the maximum energy to be 100 mJ at 125 °C junction temperature per output.

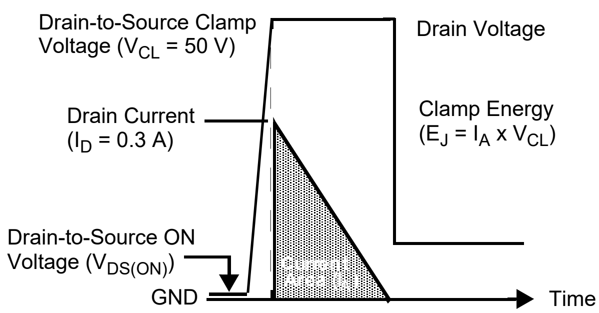


Figure 21. Output voltage clamping

6.4 Reverse battery protection

The 33814 device requires external reverse battery protection on the VPWR pin. All outputs consist of a power MOSFET with an integral substrate diode. During a reverse battery condition, current flows through the load via the substrate diode. Under this condition load, devices turn on. If load reverse battery protection is desired, a diode must be placed in series with the load.

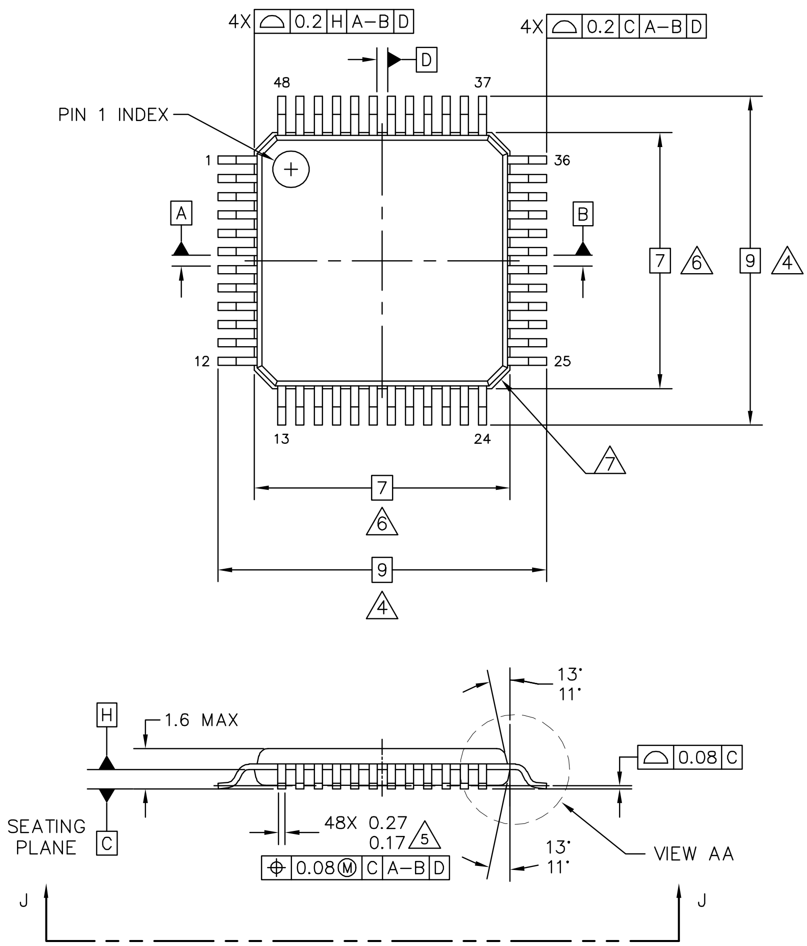
7 Packaging

7.1 Package mechanical dimensions

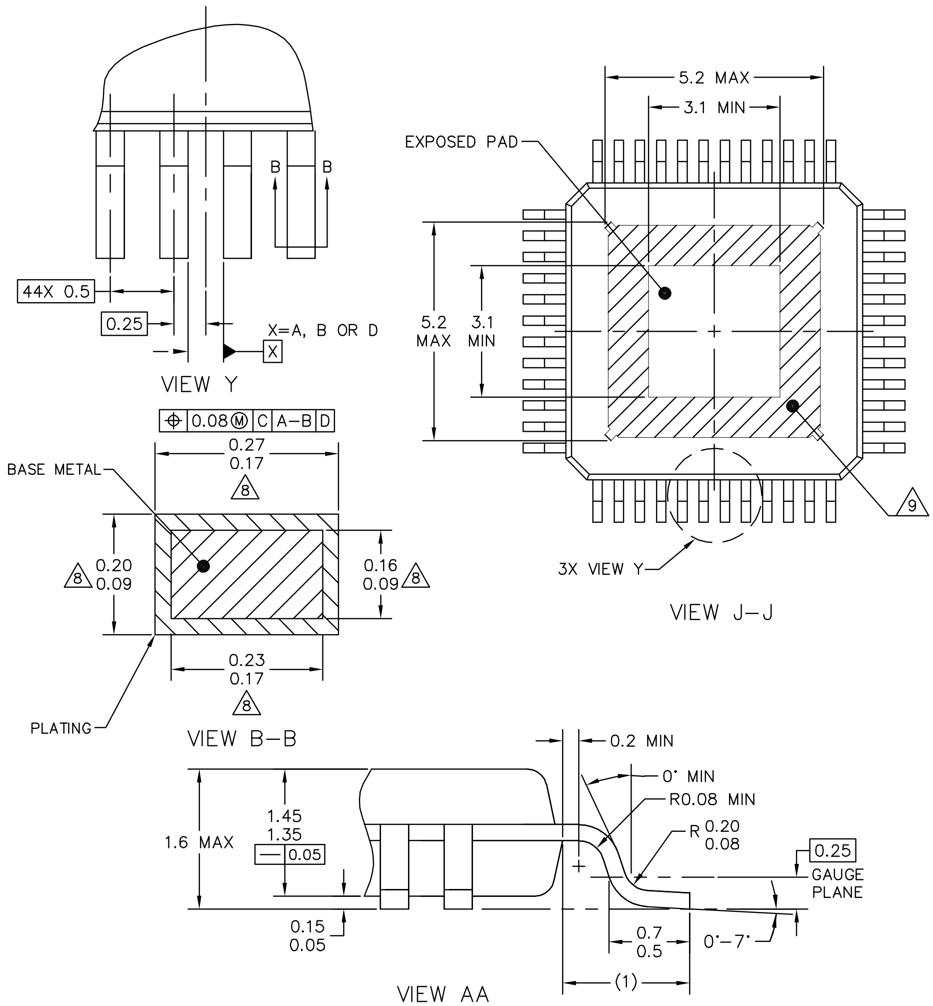
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 80. 98A reference documents

Package	Suffix	Package outline drawing number
48-pin LQFP-EP	AE	98ASA00737D



© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.15X4.15 EXPOSED PAD	DOCUMENT NO: 98ASA00737D	REV: A
	STANDARD: JEDEC MS-026 BBC	
	SOT1571-3	12 JAN 2016



	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.15X4.15 EXPOSED PAD	DOCUMENT NO: 98ASA00737D	REV: A
	STANDARD: JEDEC MS-026 BBC	
	SOT1571-3	12 JAN 2016

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.

6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.

9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 48 LEAD LQFP, 7X7X1.4 PKG, 0.5 PITCH, 4.15X4.15 EXPOSED PAD	DOCUMENT NO: 98ASA00737D	REV: A
	STANDARD: JEDEC MS−026 BBC	
	SOT1571−3	12 JAN 2016

8 Revision history

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	8/2012	• Initial release • Removed Freescale Confidential Proprietary on page 1
2.0	4/2013	• Confirmed that all known edits requested for version1.0 are present. • Changed "VRS Low-state Output Voltage" to "VRS High-state Output Voltage" and "IVRS-LOW" to"IVRS-HIGH" for V_{VRSOUT_HIGH} in Table 4. • Changed "Voltage to Current" for $I_{RESET_LEAKAGE_HIGH}$in Table 4 • Added units to the ROUT2 section of Table 4 • Corrected spelling of "ISO9141" in section 5.1.15 • Changed VPP Supply Voltage (If supplied externally and not using internal VPP regulator) to reflect two separate limits • Changed VPROT Output Voltage (tracks VCC) Max limit • Changed Typ and Max limit on Load Regulation (Both VCC and VPROT) measured from 10 % to 90 % of IVCC_C and IPROT_C, VPWR = 13 V • Changed Min. limit on VRS Negative Clamp Voltage at ICLAMP = 10 mA • Changed Note 12 • Updated Table 10 and Table 12 • Added lower limit note for VCC Output Current Limiting • Updated Output Clamp Energy (INJOUT1, INJOUT2, ROUT1, ROUT2), Output Clamp Energy (INJOUT1, INJOUT2)(Continuous operation) and added Output Clamp Energy (LAMPOUT) • Added ESD Voltage • Added clarification to 5.1.21, "LAMPOUT Driver Output" • Corrected RESET Pull-down Resistor min. and max
3.0	5/2013	• Added symbol to Output OFF Open Load Detection Current TachOut • Added Output load current at ISO I/O pin (MTX = 0, RLOAD = 1.0 kΩ, ±10 %)
4.0	5/2013	• Changed part number from PC33814AE to MC33814AE in Table 1, Orderable part variations
5.0	6/2013	• Corrected typo in Table 74, Reg. 13 • Corrected package from 98ASA00173D to 98ASA00430D
6.0	10/2015	• Corrected package from 98ASA00430D to 98ASA00737D and associated images as per PCN # 16956
7.0	3/2016	• Rewrite of section 4.4. Timing diagrams, page 18 • Updated the IC description and list of features • Updated Figure 1 with better representations • Updated description for pre-driver pins in 3.2. Pin definitions, page 5 • Removed Output clamp energy in continuous operation mode • Corrected VESD1 parameter • Updated the INJOUT1/2 Output Self Limiting Current low limit from 1.6A to 1.8A • Corrected the description in pre-driver section for VIGNFB/GPGD • ISO9141 section: Added Overtemperature threshold & Hysteresis parameter • Added KEYSW Filter time parameter • Updated 4.5.2. VCC and VPROT characteristics, page 20 • Rewrite of section 5. General IC functional description and application information, page 22 • Updated data sheet document format and style
	3/2016	• Corrected typo (100 KHz changed to 100 Hz) • Updated 5.7.2.6. GND VRSN bit, page 51
	4/2016	• Corrected Figure 16
8.0	8/2016	• Added VCC max. rating (7.0 V) • Clarified overcurrent and short to V_{BAT} fault bit reporting for drivers and pre-drivers • Corrected the effect of open load sink current disable bit • Clarified current sense feature of the pre-drivers • Added the 32 kΩ internal pull-up present on ISO Pin • Updated 98A
9.0	10/2016	• Removed VPWR_UV condition from Figure 13

REVISION	DATE	DESCRIPTION OF CHANGES
10.0	7/2017	• Design enhancement to fulfill ISO 16750 test, and modification of the state machine related to exit condition from Prepare to Shutdown mode as per CIN# 201706024I • Updated Figure 13 • Added note to 5.1.2.4. Prepare to shutdown state, page 24
11.0	5/2018	• Minor typo corrections • Added Table 20, Table 77, Table 78 and Table 79
11.1	5/2018	• Added text for clarification
12.0	8/2018	• Updated the description for $V_{OUT(FLT-TH)}$ parameter in Table 4 (deleted Short to GND)
13.0	12/2019	• Updated $I_{RESET\_LEAKAGE\_HIGH}$ minimum value in Table 4 as per CIN 201912008I

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Document Number: MC33814
Rev. 13.0
12/2019