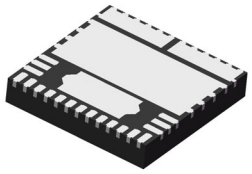
Document Number: MC20XS4200
Rev. 8.0, 11/2022

Dual 24 V, 20 mOhm high-side switch

20XS4200

HIGH-SIDE SWITCH



FK SUFFIX (PB-FREE)
98ASA00428D
23 PIN PQFN
(12 X 12 mm)

The 20XS4200 device is part of a 24 V dual high side switch product family with integrated control, and a high number of protective and diagnostic functions. It has been designed for truck, bus, and industrial applications. The low $R_{DS(on)}$ channels (<20 mΩ) can control different load types; bulbs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit serial peripheral interface (SPI), allowing easy integration into existing applications. This device is powered by SMARTMOS technology

Both channels can be controlled individually by external/internal clock signals, or by direct inputs. Using the internal clock allows fully autonomous device operation. Programmable output voltage slew-rates (individually programmable) helps improve electromagnetic compatibility (EMC) performance. To avoid shutting off the device upon inrush current, while still being able to closely track the load current, a dynamic overcurrent threshold profile is featured. Switching current of each channel can be sensed with a programmable sensing ratio. Whenever communication with the external microcontroller is lost, the device enters a Fail-safe operation mode, but remains operational, controllable, and protected.

Features

- Two fully-protected 20 mΩ (@ 25 °C) high-side switches
- Up to 4.4 A steady state current per channel
- Separate bulb and DC motor latched overcurrent handling
- Individually programmable internal/external PWM clock signals
- Overcurrent, short-circuit, and overtemperature protection with programmable autoretry functions
- Accurate temperature and current sensing
- Openload detection (channel in OFF and ON state), also for LED applications (7.0 mA typ.)
- Normal operating range: 8.0 to 36 V, extended range: 6.0 to 58 V
- 3.3 V and 5.0 V compatible 16-bit SPI port for device control, configuration and diagnostics at rates up to 8.0 MHz

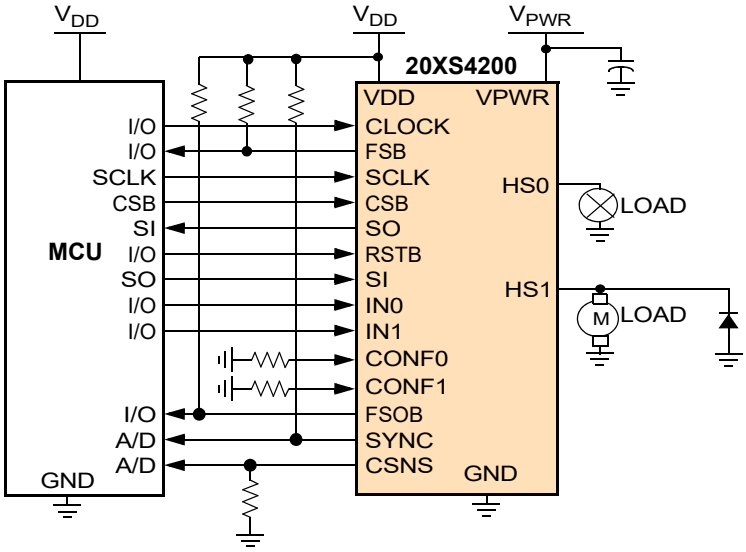


Figure 1. Simplified application diagram

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1 Orderable parts

Table 1. Simplified orderable part variations table [1]

Orderable part number	Version	Reverse battery voltage (V)	Negative clamp voltage (V)	Slew rate	Product ID bit	Overcurrent profile configuration
MC20XS4200FK	–	-28 V	-24 V	Standard	01	Hardware
MC20XS4200BFK	B [3]	-32 V	-32 V			Hardware + Software
MC20XS4200DFK[2]	D[3]					
MC20XS4200BAFK	BA [3], [4]			Accelerated	00	
MC20XS4200BDFK [2]	BD[3], [4]					

Notes

1. To order parts in tape and reel, add the R2 suffix to the part number.
2. Recommended for all new designs.
3. Version B and D, BA and BD devices can support negative voltage battery and ground loss down to -32V, the overcurrent profile can be selected by the SPI. It is no longer recommended to disable the OFF state openload for the HS1 output in parallel mode, errata sheet MC24XS4ER is no longer valid.
4. Version BA and BD devices have faster slew rates to reduce switching losses.

2 Internal block diagram

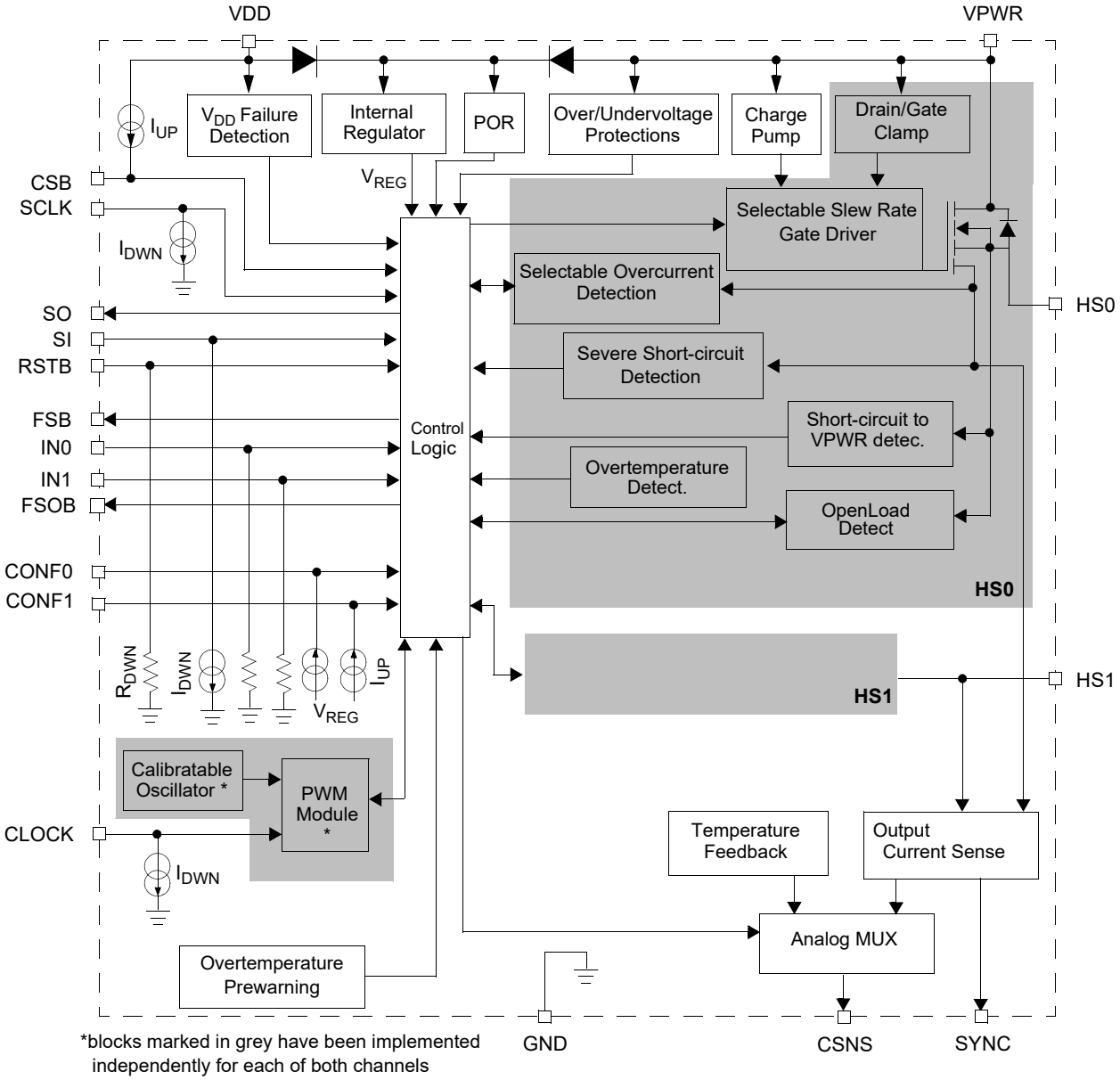
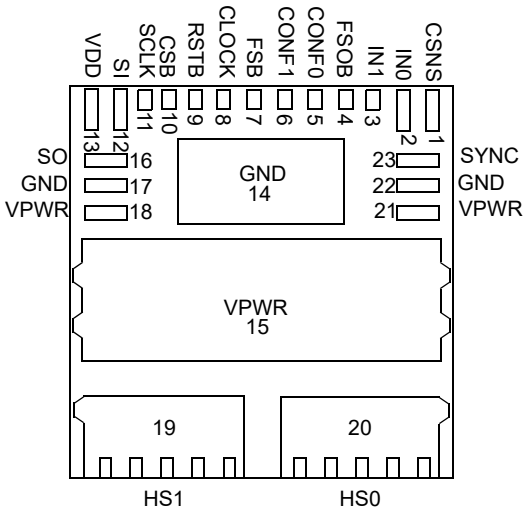


Figure 2. Internal block diagram

3 Pin assignment

Transparent top view



PQFN package

Figure 3. 20XS4200 device pin assignments

The function of each pin is described in the section Functional description

Table 2. 20XS4200 pin description

Pin number	Pin name	Function	Formal name	Definition
1	CSNS	Output	Output Current/ Temperature Monitoring	This pin either outputs a current proportional to the channel's output current or a voltage proportional to the temperature of the GND pin (pin 14). Selection between current and temperature sensing, as well as setting the current sensing sensitivity are performed through the SPI interface. An external pull-down resistor must be connected between CSNS and GND.
2 3	IN0 IN1	Input	Direct Inputs	The IN[0:1] input pins are used to directly control the switching state of both switches and consequently the voltage on the HS0:HS1 output pins. The pins are connected to GND by internal pull-down resistors.
4	FSOB	Output	Fail-safe Output (Active Low)	FSOB is asserted (active-low) upon entering Fail-safe mode (see Functional description) This open-drain output requires an external pull-up resistor to VPWR
5 6	CONF0 CONF1	Input	Configuration Input	The CONF[0:1] input pins are used to select the appropriate overcurrent detection profile (bulb/DC motor) for each of both channels. CONF requires a pull-down resistor to GND.
7	FSB	Output	Fault Status (Active Low)	This open-drain output pin (external pull-up resistor to VDD required) is set when the device enters Fault mode (see Fault mode).
8	CLOCK	Input	PWM Clock	The clock input gives the time-base when the device is operated in external clock/ internal PWM mode. This pin has an internal pull-down current source.
9	RSTB	Input	Reset	This input pin is used to initialize the device's configuration - and fault registers. Reset puts the device in Sleep mode (low current consumption) provided it is not stimulated by direct input signals.This pin is connected to GND by an internal pull-down resistor.
10	CSB	Input	Chip Select (Active Low)	This input pin is connected to the SPI chip-select output of an external micro-controller. CSB is internally pulled up to V_{DD} by a current source I_{UP}.
11	SCLK	Input	Serial Clock	This input pin is to be connected to an external SPI Clock signal. The SCLK pin is internally connected to a pull-down current source I_{DWN}.

Table 2. 20XS4200 pin description (continued)

Pin number	Pin name	Function	Formal name	Definition
12	SI	Input	Serial Input	This input pin receives the SPI input data from an external device (micro-controller or another extreme switch device in case of daisy-chaining). The SI pin is internally connected to a pull-down current source $I_{DWN.}$
13	VDD	Power	Digital Drain Voltage	This is the positive supply pin of the SPI interface.
16	SO	Output	Serial Output	This output pin transmits SPI data to an external device (external micro-controller or the SI pin of the next SPI device in case of daisy-chaining). The pin doesn't require external pull-up or pull-down resistors, but a series resistor is recommended to limit current consumption in case of GND disconnection.
14, 17, 22	GND	Ground	Ground	These pins, internally connected, are the ground pins for the logic and analog circuitry. It is recommended to also connect these pins on the PCB.
15,18,21	VPWR	Power	Positive Power Supply	These pins, internally connected, supply both the device's power and control circuitry (except the SPI port). The drain of both internal MOSFET switches is connected to them. Pin 15 is the device's primary thermal pad.
19 20	HS1 HS0	Output	Power Switch Outputs	Output pins of the switches, to be connected to the load.
23	SYNC	Output	Output Current Monitoring Synchronization	This output pin is asserted (active low) when the Current Sense (CS) output signal is within the specified accuracy range. Reading the SYNC pin allows the external micro-processor to synchronize to the device when operating in autonomous operating mode. SYNC is open-drain and requires a pull-up resistor to VDD.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Parameter	Symbol	Maximum ratings	Unit
Electrical ratings			
VPWR supply voltage range • Load dump at 25 °C (350 ms) • Reverse battery at 25 °C 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK • Fast negative transient pulses (ISO 7637-2 pulse #1, V_{PWR}=28 V & Ri=10 Ω)	V_{PWR}	 58 -28 -32 -60	V
VDD supply voltage range	V_{DD}	-0.3 to 5.5	V
Voltage on input pins [(5)] (except IN[0:1]) and Output pins [(6)]) (except HS[0:1])	$V_{MAX,LOGIC}$[(5)]	-0.3 to 5.5	V
Voltage on Fail-safe output (FSOB)	V_{FSO}	-0.3 to 58	V
Voltage on SO pin	V_{SO}	-0.3 to V_{DD}+0.3	V
Voltage (continuous, max. allowable) on IN[0:1] inputs	$V_{IN,MAX}$	58	V
Voltage (continuous, max. allowable) on output pins (HS [0:1]) 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK	$V_{HS[0:1]}$	 -28 to 58 -32 to 58	V
Rated continuous output current per channel [(7)]	$I_{HS[0:1]}$	4.4	A
Maximum allowable energy dissipation per channel and two parallel channels, single-pulse method [(8)]	$E_{CL[0:1]\_SING}$	70	mJ

Notes:

5. Concerned Input pins are: CONF[0:1], RSTB, SI, SCLK, Clock, and CSB.
6. Concerned Output pins are: CSNS, SYNC, and FSB.
7. Output current rating valid as long as maximum junction temperature is not exceeded. For computation of the maximum allowable output current, the thermal resistance of the package & the underlying heatsink must be taken into account
8. Single pulse Energy dissipation, Single-pulse short-circuit method (L_L = 0.5 mH, R = 48 mΩ V_{PWR} = 28 V, T_J = 150 °C initial).

Table 3. Maximum ratings ***(continued)***

All voltages are relative to ground unless mentioned otherwise. Exceeding these ratings may cause permanent damage.

Parameter	Symbol	Maximum ratings	Unit
Electrical ratings (continued)			
ESD Voltage[9] • Human Body Model (HBM) for HS[0:1], VPWR and GND • Human Body Model (HBM) for other pins • Charge Device Model (CDM) Package corner pins All other pins	 V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	 ±8000 ±2000 ±750 ±500	V
Thermal ratings			
Operating temperature • Ambient • Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage temperature	T_{STG}	-55 to 150	°C
Thermal Resistance Junction to Case Bottom / VPWR Flag Surface	$R_{\theta JC}$	0.32	°C/W
Peak package reflow temperature during reflow[10],[11]	T_{PPRT}	Note 11	°C

Notes:

9. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
10. Pin soldering temperature limit is for 40 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
11. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes), and the core ID to view all orderable parts, and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply electrical characteristics					
Supply voltage range: • Full specification compliant • Extended mode[12]	V_{PWR}	 8.0 6.0	 24 –	 36 58	V
V_{PWR} supply current, device in wake-up mode, channel on, openload • Outputs in ON state, HS[0:1] open, IN[0:1] > V_{IH}	$I_{PWR(ON)}$	–	6.5	8.0	mA
V_{PWR} supply current, device in wake-up mode (Standby), channel Off openload in OFF state detection disabled, HS[0:1] shorted to ground with V_{DD} = 5.5 V and RSTB > V_{WAKE} 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK	$I_{PWR(SBY)}$	 – –	 6.5 6.5	 8.0 8.5	mA
Sleep state supply current V_{PWR} = 24 V, RSTB = IN[0:1] < V_{WAKE}, HS[0:1] connected to ground • T_A = 25 °C • T_A = 125 °C	$I_{PWR(SLEEP)}$	 – –	 3.0 –	 10.0 60.0	µA
V_{DD} supply voltage	$V_{DD(ON)}$	3.0	–	5.5	V
V_{DD} supply current at V_{DD} = 5.5 V • No SPI communication • 8.0 MHz SPI communication[13]	$I_{DD(ON)}$	 – –	 – 5.0	 2.2 –	mA
V_{DD} sleep state current at V_{DD} = 5.5 V with or without V_{PWR}	$I_{DD(SLEEP)}$	–	–	5.0	µA
Overvoltage shutdown threshold	$V_{PWR(OV)}$	39	42	45.5	V
Overvoltage shutdown hysteresis	$V_{PWR(OVHYS)}$	0.2	0.8	1.5	V
Undervoltage shutdown threshold[14]	$V_{PWR(UV)}$	5.0	–	6.0	V
V_{PWR} power-on reset (POR) voltage threshold[14]	$V_{PWR(POR)}$	2.2	2.6	4.0	V
V_{DD} power-on reset (POR) voltage threshold[14]	$V_{DD(POR)}$	1.5	2.0	2.5	V
V_{DD} supply failure voltage threshold (assumed V_{PWR} > $V_{PWR(UV)}$)	$V_{DD(FAIL)}$	2.2	2.5	2.8	V

Notes

12. In extended mode, availability of several device functions (channel control, value of $R_{DS(ON)}$, overtemperature protection) is guaranteed, but compliance with the specified values in this document is not. Below 6.0 V, the device is only protected from overheating (thermal shutdown). Above $V_{PWR(OV)}$, the channels can only be turned ON when the overvoltage detection function has been disabled.
13. Typical value guaranteed per design.
14. When the device recovers from undervoltage and returns to normal mode (6.0 V < V_{PWR} < 58 V) before the end of the auto-retry period (see Auto-retry), the device performs normally. When V_{PWR} drops below $V_{PWR(UV)}$, undervoltage is detected (see Undervoltage fault (Latchable fault) and EMC Performances).

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Electrical characteristics of the output stage (HS0 and HS1)					
ON-Resistance, Drain-to-Source (I_{HS} = 3.0 A, T_J = 25 °C) CSNS_ratio = 0 • V_{PWR} = 8.0 V • V_{PWR} = 28 V • V_{PWR} = 36 V	$R_{DS(ON)25}$	– – –	– – –	20 20 20	mΩ
ON-Resistance, Drain-to-Source (I_{HS} = 3.0 A,T_J = 150 °C) CSNS_ratio = 0 • V_{PWR} = 8.0 V • V_{PWR} = 28 V • V_{PWR} = 36 V	$R_{DS(ON)150}$	– – –	– – –	36 36 36	mΩ
ON-Resistance, Drain-to-Source difference from one channel to the other in parallel mode (I_{HS} = 1.0 A,T_J = 150 °C) CSNS_ratio = X	$\Delta R_{DS(ON)150}$	-0.9	–	+0.9	mΩ
ON-Resistance, Source-Drain (I_{HS} = -3.0 A, T_J = 150 °C, V_{PWR} = -24 V)	$R_{SD(ON)150}$	–	–	36	mΩ
Max. detectable wiring length (2.5 mm²) for severe short-circuit detection (see Severe short-circuit fault (Latchable fault)): 20XS4200FK, 20XS4200BFK and 20XS4200DFK • High slew rate selected • Medium slew rate selected • Low slew rate selected 20XS4200BAFK and 20XS4200BDFK • High slew rate selected • Medium slew rate selected • Low slew rate selected	L_{SHORT}	 50 100 200 30 55 110	 130 260 500 100 175 365	 300 600 1200 180 300 620	cm
Overcurrent detection thresholds with CSNS_ratio bit = 0 (CSR0)	$I_{\_OCH1\_0}$ $I_{\_OCH2\_0}$ $I_{\_OCM1\_0}$ $I_{\_OCM2\_0}$ $I_{\_OCL1\_0}$ $I_{\_OCL2\_0}$ $I_{\_OCL3\_0}$	27.5 17.5 10.8 6.7 4.5 3.0 1.5	33.0 21.0 13.0 8.0 5.4 3.6 1.8	38.5 24.5 15.2 9.3 6.3 4.2 2.1	A
Overcurrent detection thresholds with CSNS_ratio bit = 1(CSR1)	$I_{\_OCH1\_1}$ $I_{\_OCH2\_1}$ $I_{\_OCM1\_1}$ $I_{\_OCM2\_1}$ $I_{\_OCL1\_1}$ $I_{\_OCL2\_1}$ $I_{\_OCL3\_1}$	9.2 5.8 3.6 2.2 1.5 1.0 0.48	11.0 7.0 4.3 2.7 1.8 1.2 0.6	12.8 8.2 5.1 3.1 2.1 1.4 0.72	A

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Electrical characteristics of the output stage (HS0 and HS1) (continued)					
Output (HS[x]) leakage current in sleep state (positive value = outgoing) 20XS4200FK • $V_{HS,OFF}$ = 0 V ($V_{HS,OFF}$ = output voltage in OFF state) • $V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 24 V) 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK • $V_{HS,OFF}$ = 0 V ($V_{HS,OFF}$ = output voltage in OFF state) • $V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 24 V) • $V_{HS,OFF}$ = V_{PWR}, device in sleep state (V_{PWR} = 36 V)	I_{OUT_LEAK}	 – -40.0 – -120 -1400	 – – – – –	 +16 +5.0 +16 +5.0 +5.0	µA
Output biasing current in OFF state (positive value = outgoing) 20XS4200FK, 20XS4200BFK, and 20XS4200DFK with OL_OFF disabled (worst case for V_{PWR} = 36 V, $V_{HS,OFF}$ = 34 V) • Fast slew rate selected • Medium slew rate selected • Slow slew rate selected • With OL_OFF disabled and ECU ground disconnected (V_{PWR} = 32 V) 20XS4200BAFK and 20XS4200BDFK with OL_OFF disabled (worst case for V_{PWR} = 36 V, $V_{HS,OFF}$ = 34 V) • Fast slew rate selected • Medium slew rate selected • Slow slew rate selected	I_{OUT_OFF}	 -500 -370 -300 0 -620 -440 -330	 -400 -300 -250 - -495 -360 -280	 -300 -230 -200 1000 -380 -280 -230	µA
Switch turn-on threshold for supply overvoltage (V_{PWR} -GND)	$V_{D\_GND(CLAMP)}$	58	–	66	V
Switch turn-on threshold for Drain-Source overvoltage (measured at I_{OUT} = 500 mA	$V_{DS(CLAMP)}$	58	–	66	V
Switch turn-on threshold for Drain-Source overvoltage difference from one channel to the other in parallel mode (@ I_{HS} = 500 mA)	$\Delta V_{DS(CLAMP)}$	-2.0	–	+2.0	V
Current sensing ratio[15] • CSNS_ratio bit = 0 (high current mode) • CSNS_ratio bit = 1 (low current mode)	 C_{SR0} C_{SR1}	 – –	 1/1500 1/500	 – –	–
Minimum measurable load current with compensated error[16]	$I_{\_LOAD\_MIN}$	–	–	50	mA
CSNS leakage current in OFF state (CSNSx_en = 0, CSNS_ratio bit_x = 0)	I_{CSR_LEAK}	-4.0	–	+4.0	µA
Systematic offset error (see Current sense errors) • 20XS4200FK • 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK	$I_{\_LOAD\_ERR\_SYS}$	 – –	 5.5 -5	 – –	mA
Random offset error	$I_{\_LOAD\_ERR\_RAND}$	-125	–	125	mA

Notes:

15. Current Sense Ratio C_{SRx} = I_{CSNS} / ($I_{HS[x]}$ + $I_{\_LOAD\_ERR\_SYS}$)
16. See note [15], but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and use of offset compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration.

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Electrical characteristics of the output stage (HS0 and HS1) (continued)					
E_{SR0} output current sensing error (%, uncompensated[17] at output current level (sense ratio C_{SR0} selected):					
T_J=-40 °C					
• 3.0 A		-13	–	13	
• 1.5 A		-12	–	12	
• 0.75 A		-17	–	17	
• 0.375 A		-31	–	31	
T_J=125 °C					
• 3.0 A	E_{SR0_ERR}	-10	–	10	%
• 1.5 A		-9.0	–	9.0	
• 0.75 A		-12	–	12	
• 0.375 A		-19	–	19	
T_J=25 to 125 °C					
• 3.0 A		-10	–	10	
• 1.5 A		-9.0	–	9.0	
• 0.75 A		-12	–	12	
• 0.375 A		-22	–	22	
E_{SR0} output current sensing error (% after offset compensation[17] at output current level (sense ratio C_{SR0} selected):					
T_J=-40 °C					
• 3.0 A		-10	–	10	
• 1.5 A		-10	–	10	
• 0.75 A		-10	–	10	
• 0.375 A		-10	–	10	
T_J=125 °C					
• 3.0 A	E_{SR0_ERR}(Comp)	-9.0	–	9.0	%
• 1.5 A		-8.0	–	8.0	
• 0.75 A		-8.0	–	8.0	
• 0.375 A		-9.0	–	9.0	
T_J=25 to 125 °C					
• 3.0 A		-9.0	–	9.0	
• 1.5 A		-8.0	–	8.0	
• 0.75 A		-8.0	–	8.0	
• 0.375 A		-9.0	–	9.0	

Notes:

17. E_{SRx_ERR}=(I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRx} , ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current sense error model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRx} - $I_{\_LOAD\_ERR\_SYS}$

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Electrical characteristics of the output stage (HS0 and HS1) (continued)					
E_{SR1} output current sensing error (%, uncompensated [18] at output current level (sense ratio C_{SR1} selected): T_J=-40 °C • 0.75 A T_J=125 °C • 0.75 A T_J=25 to 125 °C • 0.75 A	E_{SR1_ERR}	 -15 -12 -12	 – – –	 15 12 12	%
E_{SR1} output current sensing error (% after offset compensation[19] at output current level (sense ratio C_{SR1} selected): T_J=-40 °C • 0.75 A • 0.25 A • 0.125 A • 0.075 A T_J=125 °C • 0.75 A • 0.25 A • 0.125 A • 0.075 A T_J=25 to 125 °C • 0.75 A • 0.25 A • 0.125 A • 0.075 A	E_{SR1_ERR}(Comp)	 -10 -11 -18 -29 -8.0 -10 -12 -16 -8.0 -10 -13 -21	 – – – – – – – – – – – –	 10 11 18 29 8.0 10 12 16 8.0 10 13 21	%
E_{SR0} output current sensing error in parallel mode (%, uncompensated[20]) at outputs current level (Sense ratio C_{SR0} selected): T_J=-40 °C • 6.0 A • 3.0 A T_J=125 °C • 6.0 A • 3.0 A T_J=25 to 125 °C • 6.0 A • 3.0 A	$E_{SR0\_ERR\_PAR}$	 -10 -11 -8.0 -8.0 -8.0 -8.0	 – – – – – –	 10 11 8.0 8.0 8.0 8.0	%

Notes:

18. E_{SRx_ERR}=(I_{CSNS_MEAS} / I_{CSNS_MODEL}) -1, with I_{CSNS_MODEL} = (I(HS[x])+ $I_{\_LOAD\_ERR\_SYS}$) * C_{SRx} , ($I_{\_LOAD\_ERR\_SYS}$ defined above, see section Current sense error model). With this model, load current becomes: I(HS[x]) = I_{CSNS} / C_{SRx} - $I_{\_LOAD\_ERR\_SYS}$
19. See note [21], but with I_{CSNS_MEAS} obtained after compensation of $I_{\_LOAD\_ERR\_RAND}$ (see Activation and use of offset compensation). Further accuracy improvements can be obtained by performing a 1 or 2 point calibration
20. Minimum required value of openload impedance for detection of openload in OFF state: 200 kΩ.($V_{OLD(THRES)}$ = V_{HS} @ $I_{OLD(OFF)}$)

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Electrical characteristics of the output stage (HS0 and HS1) (continued)					
Current sense clamping voltage (condition: R(CSNS) > 10 kOhm)	$V_{CL(CSNS)}$	5.5	–	7.5	V
Openload detection current threshold in OFF state [21]	$I_{OLD(OFF)}$	30	–	100	µA
Openload fault detection voltage threshold [21]	$V_{OLD(THRES)}$	4.0	–	5.5	V
Openload detection current threshold in ON state (see Openload detection in ON state (OL_ON)): • CSNS_ratio bit = 0 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK • CSNS_ratio bit = 1 (fast slew rate SR[1:0] = 10 mandatory for this function)	$I_{OLD(ON)}$	 60 40 5.0	 150 150 7.0	 300 300 10	mA
Time period of the periodically activated openload in ON state detection for CSNS_ratio bit = 1	t_{OLLED}	105	150	195	ms
Output shorted-to-V_{PWR} detection voltage threshold (channel in OFF state)	$V_{OSD(THRES)}$	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V
Switch turn-on threshold for negative output voltages (protects against negative transients) - (measured at I_{OUT} = 100 mA, Channel in OFF state) 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK	V_{CL}	 -35 -38	 – –	 -24 -32	V
Switch turn-on threshold for Negative Output Voltages difference from one channel to the other in parallel mode - (measured at I_{OUT} = 100 mA, channel in OFF state)	ΔV_{CL}	-2.0	–	+2.0	V
Switching state (ON/OFF) discrimination thresholds	V_{HS_TH}	0.45*V_{PWR}	0.5*V_{PWR}	0.55*V_{PWR}	V
Shutdown temperature (Power MOSFET junction; 6.0 V < V_{PWR} < 58 V)	T_{SD}	160	175	190	°C

Notes:

21. Minimum required value of openload impedance for detection of openload in OFF state: 200 kΩ.($V_{OLD(THRES)}$ = V_{HS} @ $I_{OLD(OFF)}$)

Table 4. Static electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C, V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Electrical characteristics of the control interface pins					
Logic input voltage, High[22]	V_{IH}	2.0	–	5.5	V
Logic input voltage, Low[22]	V_{IL}	-0.3	–	0.8	V
Wake-up threshold voltage (IN[0:1] and RSTB)[23]	V_{WAKE}	1.0	–	2.2	V
Internal pull-down current source (on Inputs: CLOCK, SCLK and SI)[24]	I_{DWN}	5.0	–	20	µA
Internal pull-up current source (input CSB)[25]	I_{UP_CSB}	5.0	–	20	µA
Internal pull-up current source (input CONF[0:1])[26]	I_{UP_CONF}	25	–	100	µA
Capacitance of SO, FSB and FSOB pins in Tri-state	C_{SO}	–	–	20	pF
Internal pull-down resistance (RSTB and IN[0:1])	R_{DWN}	125	250	500	kΩ
Input capacitance[27]	C_{IN}	–	4.0	12	pF
SO high state output voltage • (I_{OH} = 1.0 mA)	V_{SOH}	V_{DD}-0.4	–	–	V
SYNC, SO, FSOB and FSB low state output voltage • (I_{OL} = -1.0 mA)	V_{SOL}	–	–	0.4	V
SYNC, SO, CSNS, FSOB and FSB tri-state leakage current: • (0.0 V < V(SO) < V_{DD}, or V(FS) or V(SYNC) = 5.5 V, or V(FSO) = 36 V or V(CSNS) = 0.0 V	$I_{SO(LEAK)}$	-2.0	0.0	2.0	µA
CONF[0:1]: required values of the external pull-down resistor • Lighting applications • DC motor applications	R_{CONF}	1.0 50	– –	10 Infinite	kΩ

Notes

22. High and low voltage ranges apply to SI, CSB, SCLK, RSTB, IN[0:1] and CLOCK input signals. The IN[0:1] signals may be derived from V_{PWR} and can tolerate voltages up to 58 V.
23. Voltage above which the device wakes up
24. Valid for V_{SI} ≥ 0.8 V and V_{SCLK} ≥ 0.8 V and V_{CLOCK} ≥ 0.8 V.
25. Valid for V_{CSB} ≤ 2.0 V. CSB has an internal pull-up current source derived from V_{DD}
26. Pins CONF[0:1] are connected to an internal current source, derived from an internal voltage regulator (V_{REG} ~ 3.0 V).
27. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:1], CONF[0:1], and CLOCK pins. This parameter is guaranteed by the manufacturing process but is not tested in production.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output voltage switching characteristics					
Rising and falling edges medium slew rate (SR[1:0] = 00)[28] 20XS4200FK, 20XS4200BFK and 20XS4200DFK					
• V_{PWR} = 16 V	SR_{R_00} SR_{F_00}	0.164	–	0.65	V/µs
• V_{PWR} = 28 V		0.28	–	0.79	
• V_{PWR} = 36 V		0.34	–	0.90	
20XS4200BAFK and 20XS4200BDFK					
• V_{PWR} = 16 V		0.25	–	1.1	
• V_{PWR} = 28 V		0.45	–	1.4	
• V_{PWR} = 36 V		0.5	–	1.5	
Rising and falling edges low slew rate (SR[1:0] = 01)[28] 20XS4200FK, 20XS4200BFK and 20XS4200DFK					
• V_{PWR} = 16 V	SR_{R_01} SR_{F_01}	0.081	–	0.32	V/µs
• V_{PWR} = 28 V		0.14	–	0.395	
• V_{PWR} = 36 V		0.17	–	0.45	
20XS4200BAFK and 20XS4200BDFK					
• V_{PWR} = 16 V		0.125	–	0.55	
• V_{PWR} = 28 V		0.225	–	0.7	
• V_{PWR} = 36 V		0.25	–	0.75	
Rising and falling edges high slew rate / SR[1:0] = 10)[28] 20XS4200FK, 20XS4200BFK and 20XS4200DFK					
• V_{PWR} = 16 V	SR_{R_10} SR_{F_10}	0.29	–	1.30	V/µs
• V_{PWR} = 28 V		0.55	–	1.58	
• V_{PWR} = 36 V		0.68	–	1.80	
20XS4200BAFK and 20XS4200BDFK					
• V_{PWR} = 16 V		0.5	–	2.2	
• V_{PWR} = 28 V		0.9	–	2.8	
• V_{PWR} = 36 V		1.0	–	3.0	

Notes

28. Rising and Falling edge slew rates specified for a 20 % to 80 % voltage variation on a 10.0 Ω resistive load (see Output voltage slew rate and delay).

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output voltage switching characteristics (continued)					
Rising/falling edge slew rate matching (SR_R /SR_F) • 16 V < V_{PWR} < 36 V 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK	ΔSR	 0.75 0.75	 1.0 1.0	 1.2 1.25	
Edge slew rate difference from one channel to the other in parallel mode[29] 20XS4200FK, 20XS4200BFK and 20XS4200DFK 16 V < V_{PWR} < 36 V SR[1:0] = 00 SR[1:0] = 01 SR[1:0] = 10 20XS4200BAFK and 20XS4200BDFK 16 V < V_{PWR} < 36 V SR[1:0] = 10	ΔSR	 -0.1 -0.06 -0.14 -0.2	 0.0 0.0 0.0 0.0	 +0.1 +0.06 +0.14 +0.2	V/µs
Output turn-on and turn-off delays (medium slew rate: SR[1:0] = 00)[30] • 16 V < V_{PWR} < 36 V 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	t_{DLY_00}	 32 20	 – –	 128 120	µs
Output turn-on and turn-off delays (low slew rate / SR[1:0] = 01)[30] • 16 V < V_{PWR} < 36 V 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	t_{DLY_01}	 59 40	 – –	 245 240	µs
Output turn-on and turn-off delays (high slew rate / SR[1:0] = 10)[30] • 16 V < V_{PWR} < 36 V 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	t_{DLY_10}	 18 10	 – –	 68 60	µs
Turn-on and turn-off delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) • f_{PWM} = 400 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 00	Δt_{RF_00}	-25	0.0	25	µs
Turn-on and turn-off delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) • f_{PWM} = 200 Hz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 01 20XS4200FK, 20XS4200BAFK and 20XS4200BDFK 20XS4200BFK and 20XS4200DFK	Δt_{RF_01}	 -50 -90	 0.0 –	 50 90	µs

Notes

29. Rising and falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 Ω resistive load (see Output voltage slew rate and delay).
30. Turn-on delay time measured as delay between a rising edge of the channel control signal (IN[0:1] = 1) and the associated rising edge of the output voltage up to: $V_{HS[0:1]} = V_{PWR}$ / 2 (where R_L = 10.0 Ω). Turn-OFF delay time is measured as time between a falling edge of the channel control signal (IN[0:1] = 0) and the associated falling edge of the output voltage up to the instant at which: $V_{HS[0:1]} = V_{PWR}$ / 2 (R_L = 10.0 Ω)

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output voltage switching characteristics (continued)					
Turn-on and turn-off delay time matching ($t_{DLY(ON)}$ - $t_{DLY(OFF)}$) • f_{PWM} = 1.0 kHz, 16 V < V_{PWR} < 36 V, duty cycle on IN[x] = 50 %, SR[1:0] = 10	Δt_{RF_10}	-13	0.0	13	µs
Delay time difference from one channel to the other in parallel mode(31) 16 V < V_{PWR} < 36 V SR[1:0] = 00 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK SR[1:0] = 01 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK SR[1:0] = 10 20XS4200FK 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK	$\Delta t_{(DLY)}$	 -21 -25 -40 -50 -11 -12	 0.0 0.0 0.0 0.0 0.0 0.0	 21 25 40 50 11 12	µs
Fault detection delay time(32)	t_{FAULT}	–	5.0	8.0	µs
Output shutdown delay time(33)	t_{DETECT}	–	10.0	15.0	µs
Current sense output settling Time for SR[1:0] = 00 (medium slew rate) (34) 16 V < V_{PWR} < 36 V 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{CSNSVAL\_00}$	 0.0 0.0	 118 –	 235 200	µs
Current sense output settling Time for SR[1:0] = 01(low slew rate) (34) 16 V < V_{PWR} < 36 V 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{CSNSVAL\_01}$	 0.0 0.0	 185 –	 355 315	µs
Current sense output settling Time for SR[1:0] = 10 (high slew rate) (34) 16 V < V_{PWR} < 36 V 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{CSNSVAL\_10}$	 0.0 0.0	 108 –	 205 165	µs
SYNC output signal delay for SR[1:0] = 00 (medium SR) (34) 20XS4200FK 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{SYNCVAL\_00}$	 50 50 25	 – – –	 150 160 130	µs

Notes

31. Rising and Falling edge slew rates specified for a 20% to 80% voltage variation on a 10.0 Ω resistive load (see Output voltage slew rate and delay).
32. Time required to detect and report the fault to the FSB pin.
33. Time required to switch off the channel after detection of overtemperature (OT), overcurrent (OC), SC or UV error (time measured between start of the negative edge on the FSB pin and the falling edge on the output voltage until V(HS[0:1)) = 50% of V_{PWR}
34. Settling time (= $t_{CSNSVAL\_XX}$), SYNC output signal delay (= $t_{SYNCVAL\_XX}$) and Read-out delay (= $t_{SYNREAD\_XX}$) are defined for a stepped load current (100 mA< I(LOAD)<IOCLx A FOR CSNS_RATIO_S = 1, AND 300 mA< I(LOAD)<IOCLx A_0 FOR CSNS_RATIO_S = 0). See Figure 9 and Output current monitoring (CSNS).

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output voltage switching characteristics (continued)					
SYNC output signal delay for SR[1:0] = 01 (low SR) (35) 20XS4200FK 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{SYNCVAL\_01}$	 80 80 50	 – – –	 290 320 250	µs
SYNC output signal delay for SR[1:0] = 10 (high SR) (35) 20XS4200FK 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{SYNCVAL\_10}$	 24 22 10	 – – –	 80 80 65	µs
Recommended sync_to_read delay SR[1:0] = 00 (medium slew rate) (35) 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{SYNREAD\_00}$	 0.0 0.0	 – –	 200 150	µs
Recommended sync_to_read delay SR[1:0] = 01 (low slew rate) (35) 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{SYNREAD\_01}$	 0.0 0.0	 – –	 200 150	µs
Recommended sync_to_read delay SR[1:0] = 10 (high slew rate) (35) 20XS4200FK, 20XS4200BFK and 20XS4200DFK 20XS4200BAFK and 20XS4200BDFK	$t_{SYNREAD\_10}$	 0.0 0.0	 – –	 200 150	µs
Upper overcurrent threshold duration	t_{OCH1} t_{OCH2}	6.0 12.0	8.6 17.2	11.2 22.4	ms
Medium overcurrent threshold duration (CONF = 0; Lighting Profile)	t_{OCM1_L} t_{OCM2_L}	48 96	67 137	87 178	ms
Medium overcurrent threshold duration (CONF = 1; DC motor Profile)	t_{OCM1_M} t_{OCM2_M}	48 96	67 137	87 178	ms
Frequency and PWM duty cycle ranges (36)(protections fully operational, see Protective functions)					
Switching frequency range - direct Inputs	$f_{CONTROL}$	0.0	–	1000	Hz
Switching frequency range - external clock with internal PWM (recommended)	f_{PWM_EXT}	20	–	1000	Hz
Switching frequency range - internal clock with internal PWM (recommended)	f_{PWM_INT}	60	–	1000	Hz
Duty cycle range	$R_{CONTROL}$	0.0	–	100	%

Notes

35. Settling time (= $t_{CSNSVAL\_XX}$), SYNC output signal delay (= $t_{SYNCVAL\_XX}$) and Read-out delay (= $t_{SYNREAD\_XX}$) are defined for a stepped load current (100 mA< I(LOAD)<IOCLX A FOR CSNS_RATIO_S = 1, AND 300 mA< I(LOAD)<IOCLX A_0 FOR CSNS_RATIO_S = 0) See Figure 9 and Output current monitoring (CSNS).
36. In Direct Input mode, the lower frequency limit is 0 Hz with RSTB=5.0 V and 4.0 Hz with RSTB=0.0 V. Duty-cycle applies to instants at which V_{HS} = 50 % V_{PWR}. For low duty-cycle values, the effective value also depends on the value of the selected slew rate.

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Availability diagnostic functions for CSR0 over duty cycle and switching frequency (protections & diagnostics both fully operational, see Diagnostic features for the exact boundary values)					
Available duty cycle range, f_{PWM} = 1.0 kHz high slew rate, PWM mode[37] • OL_OFF • OL_ON • OS	$R_{PWM\_1K\_H}$	0.0 35 0.0	– – –	62 100 90	%
Available duty cycle range, f_{PWM} = 400 Hz, medium slew rate, PWM mode[37] • OL_OFF • OL_ON • OS	$R_{PWM\_400\_M}$	0.0 21 0.0	– – –	81 100 88	%
Available duty cycle range, f_{PWM} = 400 Hz, high slew rate, PWM mode[37] • OL_OFF • OL_ON • OS	$R_{PWM\_400\_H}$	0.0 14 0.0	– – –	84 100 95	%
Available duty cycle range, f_{PWM} = 200 Hz, low slew rate mode, PWM mode[37] • OL_OFF • OL_ON • OS	$R_{PWM\_200\_L}$	0.0 15 0.0	– – –	86 100 93	%
Available duty cycle range, f_{PWM} = 200 Hz, medium slew rate, PWM mode[37] • OL_OFF • OL_ON • OS	$R_{PWM\_200\_M}$	0.0 11 0.0	– – –	90 100 94	%
Available duty cycle range, f_{PWM} = 100 Hz in low slew rate, PWM mode[37] • OL_OFF • OL_ON • OS	$R_{PWM\_100\_L}$	0.0 8.0 0.0	– – –	93 100 96	%
Deviation of the internal clock PWM frequency after calibration[38]	$A_{FPWM(CAL)}$	-10	–	+10	%
Default output frequency when using an uncalibrated oscillator	$f_{PWM(0)}$	280	400	520	Hz
Minimal required low time during calibration of the internal clock through CSB	$t_{CSB(MIN)}$	1.0	1.5	2.0	µs
Maximal allowed low time during calibration of the internal clock through CSB	$t_{CSB(MAX)}$	70	100	130	µs
Recommended external clock frequency range (external clock/PWM module)	f_{CLOCK}	15	–	512	kHz
Upper detection threshold for external clock frequency monitoring	$f_{CLOCK(MAX)}$	512	730	930	kHz
Lower detection threshold for external clock frequency monitoring	$f_{CLOCK(MIN)}$	5.0	7.0	10	kHz

Notes

37. The device can be operated outside the specified duty cycle and frequency ranges (basic protective functions OC, SC, UV, OV, OT remain active) but the availability of the diagnostic functions OL_ON, OL_OFF, OS is affected.
38. Values guaranteed from 60 Hz to 1.0 kHz (recommended switching frequency range for internal clock operation).

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Timing: SPI Port, IN[0]/ IN[1] Signals and Autoretry					
Required low time allowing delatching or triggering sleep mode (direct input mode)	t_{IN}	175	250	325	ms
Watchdog timeout for entering Fail-safe mode due to loss of SPI contact(39)	t_{WDTO}	217	310	400	ms
Auto-retry repetition period (when activated): • Auto_period bits = 00 • Auto_period bits = 01 • Auto_period bits = 10 • Auto_period bits = 11	 t_{AUTO_00} t_{AUTO_01} t_{AUTO_10} t_{AUTO_11}	 105 52.5 26.2 13.1	 150 75 37.5 17.7	 195 97.5 47.8 24.4	ms
GND pin temperature sensing function					
Thermal prewarning detection threshold(40)	T_{OTWAR}	110	125	140	°C
Temperature sensing output voltage @ T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)	T_{FEED}	918	1078	1238	mV
Gain temperature sensing output @ T_A = 25 °C (470 Ω < R_{CSNS} < 10 kΩ)(40)	DT_{FEED}	10.7	11.1	11.5	mV/°C
Temperature sensing error, range [-40 °C, 150 °C], default(40)	T_{FEED_ERROR}	-15	–	+15	°C
Temperature sensing error, [-40 °C, 150 °C] after 1 point calibration @ 25 °C(40)	$T_{FEED\_ERROR\_CAL}$	-5.0	–	+5.0	°C

Notes

39. Only when the WD_dis bit set to logic [0] (default). Watchdog timeout defined from the rising edge on RST to rising edge HS[0,1]
40. Values were obtained by lab. characterization

Table 5. Dynamic electrical characteristics (continued)

Unless specified otherwise: 8.0 V ≤ V_{PWR} ≤ 36 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V. Typical values are average values evaluated under nominal conditions T_A = 25 °C,V_{PWR} = 28 V & V_{DD} = 5.0 V, unless specified otherwise.

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPI Interface Electrical Characteristics(41)					
Maximum operating frequency of the Serial Peripheral interface (SPI)(42)	f_{SPI}	–	–	8.0	MHz
Required low state duration for reset RSTB (43)	t_{WRSTB}	10	–	–	µs
Required duration from the rising to the falling edge of CSB (required setup time)(44)	t_{CSB}	1.0	–	–	µs
Rising edge of RSTB to falling edge of CSB (required setup time)(44)	t_{ENBL}	5.0	–	–	µs
Falling edge of CSB to rising edge of SCLK (required setup time)(44)	t_{LEAD}	500	–	–	ns
Falling edge of SCLK to rising edge of CSB (required setup lag time)(44)	t_{LAG}	60	–	–	ns
Required high state duration of SCLK (required setup time)(44)	t_{WSCLKh}	50	–	–	ns
Required low state duration of SCLK (required setup time)(44)	t_{WSCLKl}	50	–	–	ns
SI to falling edge of SCLK (required setup time)(45)	$t_{SI(SU)}$	15	–	–	ns
Falling edge of SCLK to SI (required hold time of the SI signal)(45)	$t_{SI(H)}$	30	–	–	ns
SO rise time • C_L = 80 pF	t_{RSO}	–	–	20	ns
SO fall time • C_L = 80 pF	t_{FSO}	–	–	20	ns
SI, CSB, SCLK, max. rise time allowing operation at f_{SPI} = 8.0 MHz(45)	t_{RSI}	–	–	11	ns
SI, CSB, SCLK, max. fall time allowing operation at f_{SPI} = 8.0 MHz(45)	t_{FSI}	–	–	11	ns
Time from rising edge of SCLK to reach a valid level at the SO pin(46)	t_{VALID}	–	–	44	ns
Time from falling edge of CSB to reach low-impedance on SO (access time)(47)	t_{SOEN}	–	–	30	ns

Notes:

41. Parameters guaranteed by design. It is recommended to tie unused SPI-pins to GND by resistors 1.0 k <R <10 k
42. For clock frequencies > 4.0 MHz, series resistors on the SPI pins should preferably be removed. Otherwise, 470 pF ($V_{MAX.}$ > 40 V) ceramic speed-up capacitors in parallel with the >8.0 kΩ input resistors are required on pins SCLK, SI, SO, CS
43. RSTB low duration is defined as the minimum time required to switch off the channel when previously put ON in SPI mode (direct inputs inactive).
44. Minimum setup time required for the device is the minimum required time that the microcontroller must wait or remain in a given state.
45. Rise and Fall time of incoming SI, CSB, and SCLK signals.
46. Time required for output data to be available for use at SO, measured with a 1.0 kΩ series resistor connected CSB.
47. Time required for output data to be terminated at SO measured with a 1.0 kΩ series resistor connected CSB.

4.4 Timing diagrams

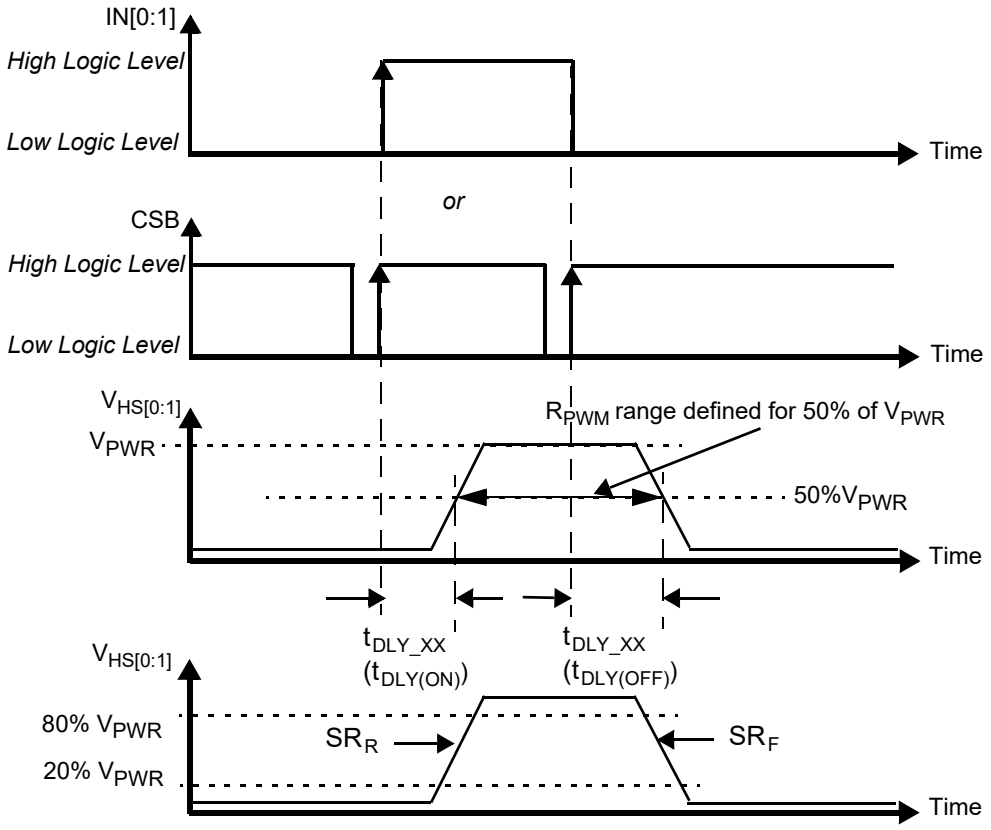


Figure 4. Output voltage slew rate and delay

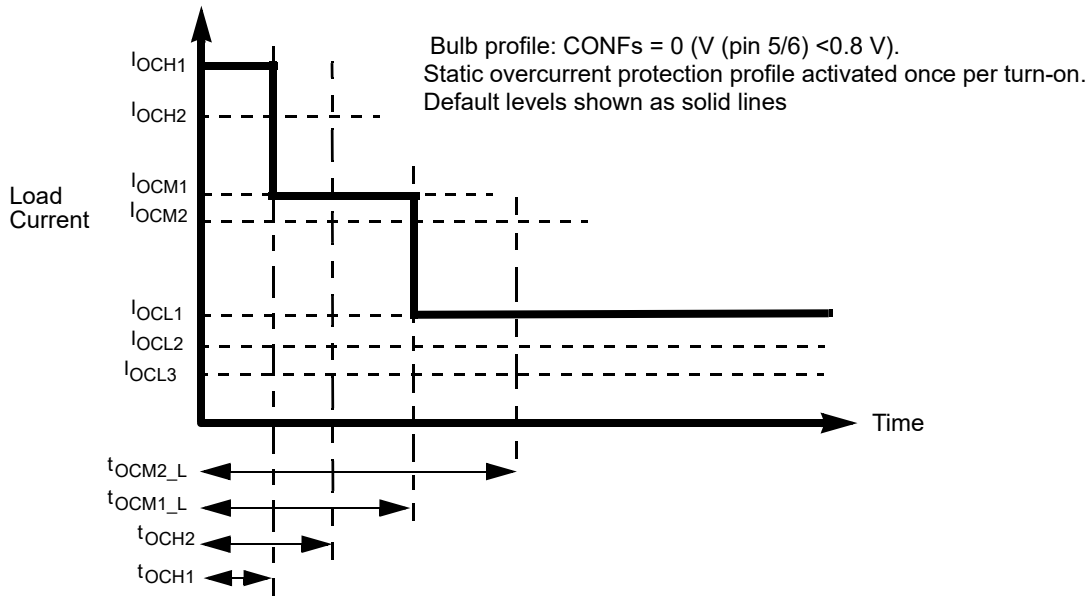


Figure 5. Overcurrent protection profile for bulb applications

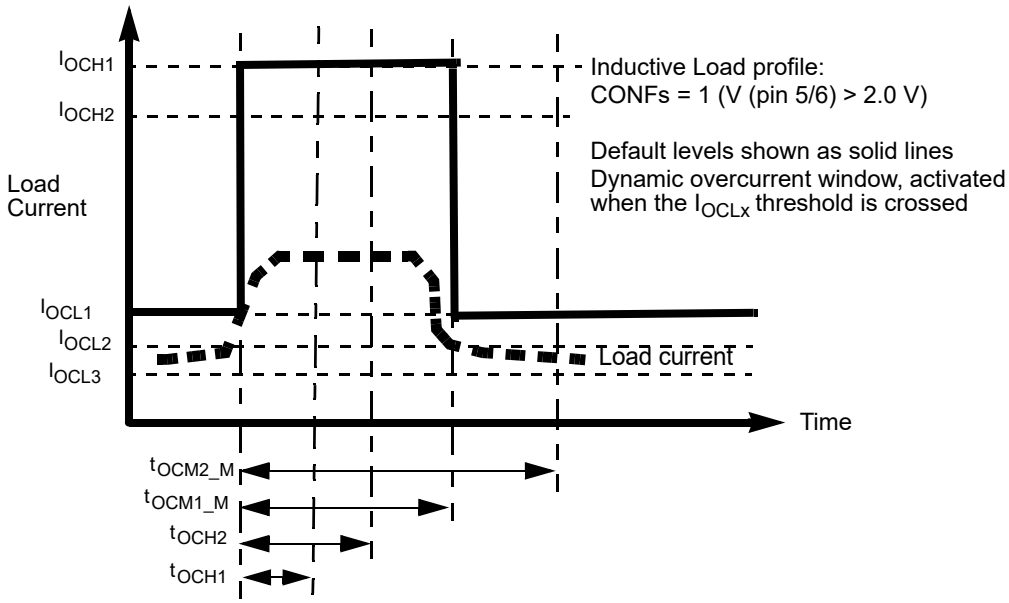


Figure 6. Overcurrent protection profile for applications with Inductive loads (DC motors, solenoids)

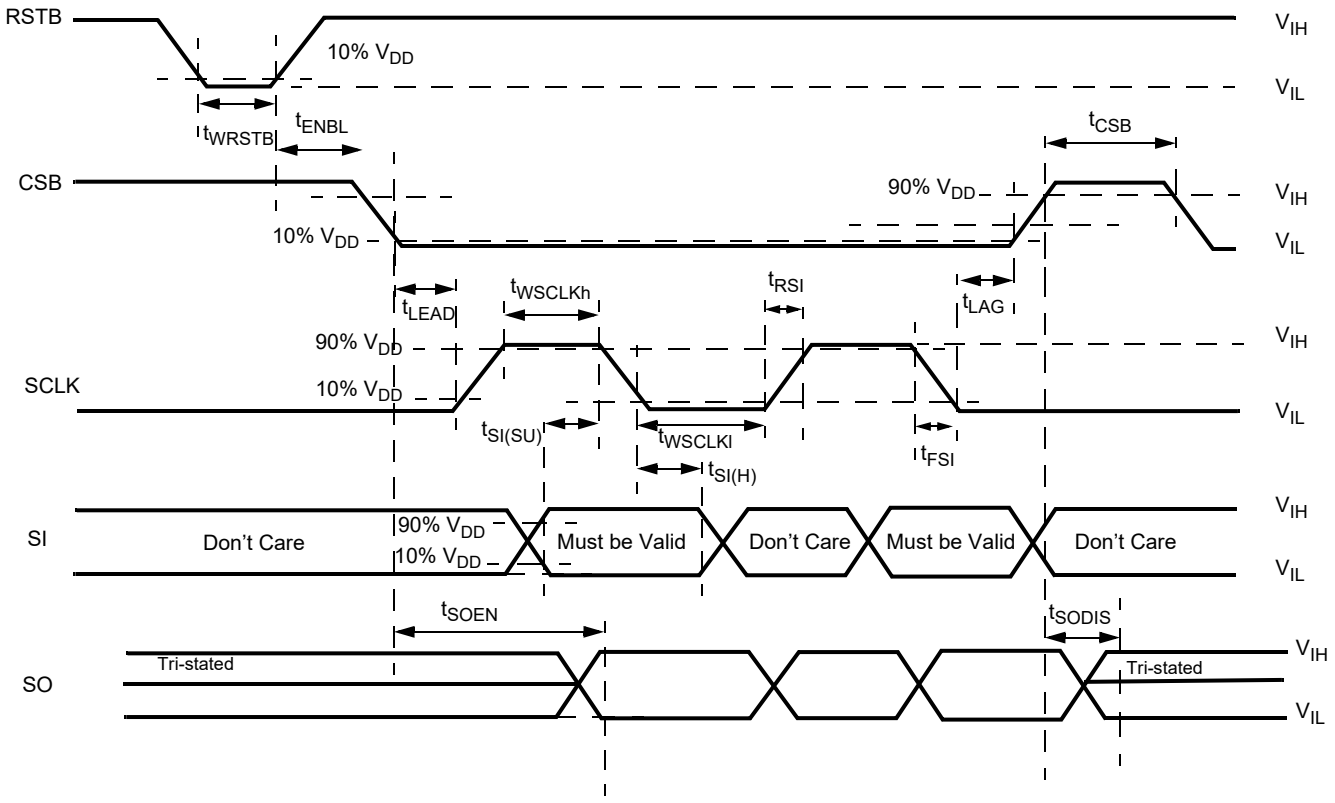


Figure 7. Timing requirements during SPI communication

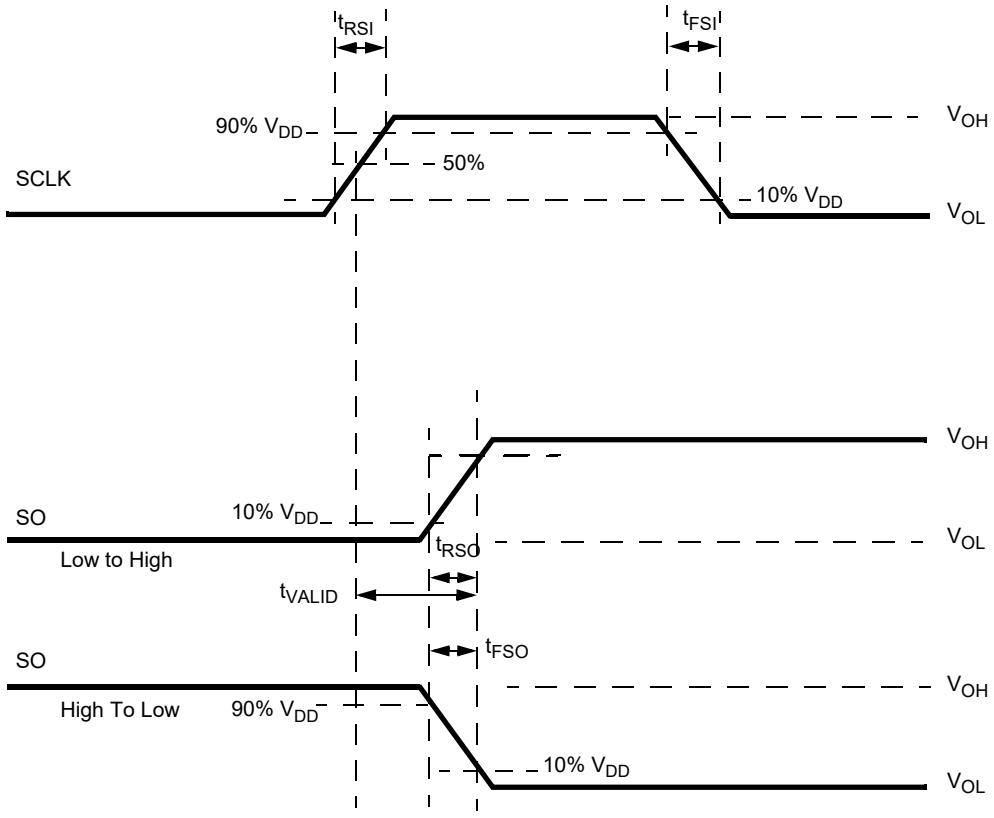


Figure 8. Timing diagram for Serial Output (SO) data communication

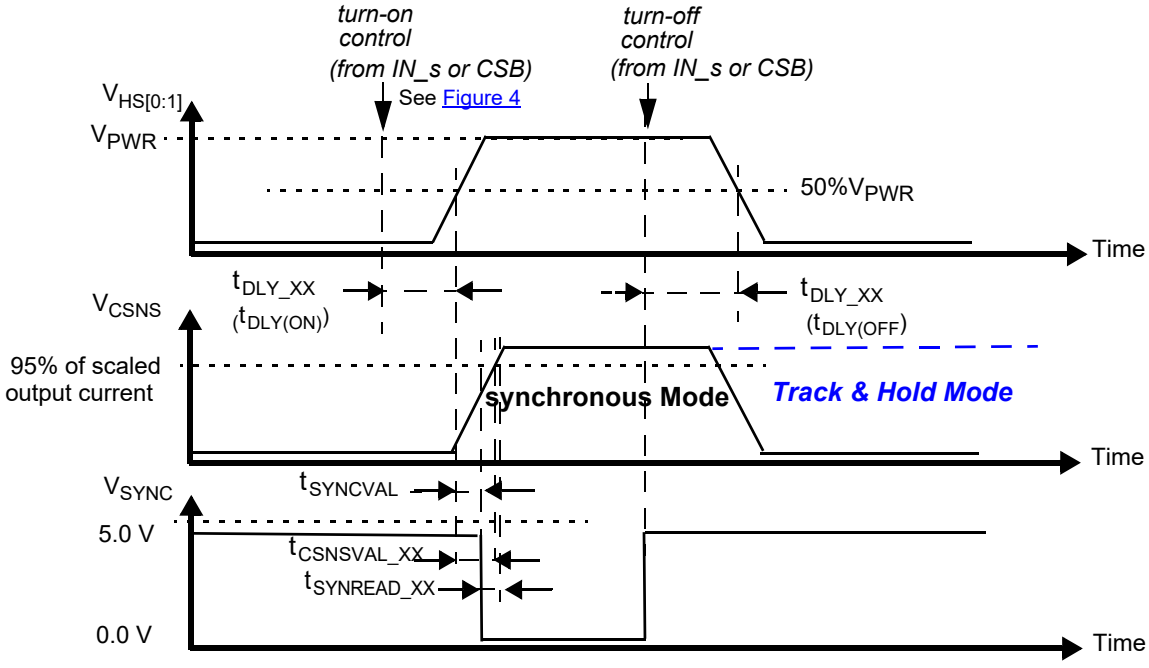


Figure 9. Synchronous and Track & Hold current sensing modes: associated delay and settling times

5 Functional description

5.1 Introduction

The 20XS4200 is a two-channel, 24 V high side switch with integrated control and diagnostics designed for truck, bus, and industrial applications. The device provides a high number of protective functions. Both low $R_{DS(on)}$ channels (<20 mΩ) can independently drive various load types like light bulbs, solenoid actuators, or DC motors. Device control and diagnostics are configured through a 16-bit SPI port with daisy chain capability.

Independently programmable output voltage slew rates allow satisfying electromagnetic compatibility (EMC) requirements.

Both channels can independently be operated in three different switching modes: internal clock and internal PWM mode (fully autonomous operation), external clock and internal PWM mode, and direct control switching mode.

Current sensing with an adjustable ratio is available on both channels, allowing both high current (bulbs) and low current (LED) monitoring. By activating the Track & Hold Mode, current monitoring can be performed during the switch-Off phase. This allows random access to the current sense functionality. A patented offset compensation technique further enhances current sense accuracy.

To avoid turning off upon inrush current, while being able to monitor it, the device features a dynamic overcurrent threshold profile. For bulbs, this profile is a stair function with stages of which the height and width are programmable through the SPI port. DC motors can be protected from overheating by activating a specific window-shaped overcurrent profile that allow stall currents of limited duration.

Whenever communication with the external micro-controller is lost, the device enters Fail-safe operation mode, but remains operational, controllable, and protected.

5.2 Pin assignment and functions

Functions and register bits that are implemented independently for both channels have extension "_s". Max. ratings of the pins are given in Table 3.

5.2.1 Output current monitoring (CSNS)

The CS pin allows independent current monitoring of channel 0 or channel 1 up to the steady state overcurrent threshold. It can also be used to sense the device temperature. The different functions are selected by setting bits CSNS1_en and CSNS0_en to the appropriate value (Table 23). When the CSNS pin is sensed during switch-off in the (optional) track & hold mode (see Figure 9), it outputs the scaled value of the load current as it was just before turn-Off. When several devices share the same pull-down resistor, the CSNS pins of devices the current of which is not monitored must be tri-stated. This is accomplished by setting CSNS0_en = 0 and CSNS1_en = 0 in the GCR register (Table 10). Settling time ($t_{CSNSVAL\_XX}$) is defined as the time between the instant at the middle of the output voltage's rising edge (HS[0:1] = 50% of V_{PWR}), and the instant at which the voltage on the CSNS-pin has settled to ±5.0% of its final value. Anytime an overcurrent window is active, the CSNS pin is disabled (see Overcurrent detection on resistive and inductive loads). The current and temperature sensing functions are unavailable in Fail-safe mode and in Normal mode when operating without the V_{DD} supply voltage. In order to generate a voltage output, a pull-down resistor is required (R(CSNS)=1.0 kΩ typ. and 470 < R(CSNS) < 10 k). When the current sense resistor connected to the CSNS pin is disconnected, the CSNS voltage is clamped to $V_{CL(CSNS)}$. The CSNS pin can source currents up to about 5.6 mA.

5.2.2 Current sense synchronization (SYNC)

To synchronize current sensing with an external process, the SYNC signal can be connected to a digital input of an external MCU. SYNC is asserted logic low when the current sense signal is accurate and ready to be read. The current sense signal on the CSNS pin has the specified accuracy $t_{SYNREAD\_XX}$ seconds after the falling edge on the SYNC pin (Figure 9) and remains valid until a rising edge is generated. The rising edge that is generated by the SYNC pin at the turn-OFF instant (internal or external) may also be used to implement synchronization with the external MCU. Parameter $t_{SYNCVAL\_XX}$ is defined as the time between the instant at the middle of the output-voltage rising edge (HS[0:1] = 50% of VPWR), and the instant at which the voltage on the SYNC-pin drops below 0.4 V (V_{SOL}). The SYNC pins of different devices can be connected together to save µ-controller input channels. However, in this configuration, the CSNS function of only one device should be active at a time. Otherwise, the MCU does not determine the origin of the SYNC signal. The SYNC pin is open drain and requires an external pull-up resistor to VDD.

5.2.3 Direct control inputs (IN0 and IN1)

The IN[0:1] pins allow direct control of both channels. A logic [0] level turns off the channel and a logic[1] level turns it on (Channel control in Normal mode). When the device is in Sleep mode, a transition from logic 0 to logic 1 on any of these pins wake it up (Sleep mode). If it is desired to automatically turn on the channels after a transition to Fail-safe mode, inputs IN[0] and IN[1] must be externally connected to the VPWR pin by a pull-up resistor (e.g. 10 kΩ typ.). However, this prevents the device from going into Sleep mode. Both IN pins are internally connected to a pull-down resistor.

5.2.4 Configuration inputs (CONF0 and CONF1)

The CONF[0:1] input pins allow configuring both channels for the appropriate load type. CONF = 0 activates the bulb overcurrent protection profile, and CONF = 1 the DC motor profile. These inputs are connected to an internal voltage regulator of 3.3 V by an internal pull-up current source I_{UP}. Therefore, CONF = 1 is the default value when these pins are disconnected. Details on how to configure the channels are given in Table 9.

5.2.5 Fault status (FSB)

This open-drain output is asserted low when any of the following faults occurs (see Fault mode): overcurrent (OC), overtemperature (OT), Output connected to V_{PWR}, Severe short-circuit (SC), openload in ON state (OL_ON), openload in OFF state (OL_OFF), External Clock-fail (CLOCK_fail), overvoltage (OV), undervoltage (UV). Each fault type has its own assigned bit inside the STATR, FAULTR_s, or DIAGR_s register. Fault type identification and fault bit reset are accomplished by reading out these registers. They are part of the SO register (Fault mode) and are accessed through the SPI port.

5.2.6 PWM clock (CLOCK)

This pin is the input for an external clock signal that controls the internal PWM module.The clock signal is monitored by the device. The PWM module controls ON-time and turn-ON delay of the selected channels. The CLOCK pin should not be confused with the SCLK pin, which is the clock pin of the SPI interface. CLOCK has an internal pull-down current source (I_{DWN}) to GND.

5.2.7 Reset (RSTB)

All SPI register contents are reset when RSTB = 0. When RSTB = 0, the device returns to Sleep mode t_{IN} sec. after the last falling edge of the last active IN[0:1] signal. As long as the Reset input (RSTB pin) is at logic 0 and both direct input states are low, the device remains in Sleep mode (Channel configuration through the SPI). A 0-to-1 transition on RSTB wakes up the device and starts a watchdog timer to check the continuous presence of the SPI signals. To do this, the device monitors the contents of the first bit (WDIN bit) of all SPI words following that transition (regardless the register it is contained in). When this contents is not alternated within a duration t_{WDTO}, SPI communication is considered lost, and Fail-safe mode is entered (Entering Fail-safe mode). RSTB is internally pulled-down to GND by resistor R_{DWN}.

5.2.8 Chip Select (CSB)

Data communication over the SPI port is enabled when the CSB pin is in the logic [0] state. Data from the Input Shift registers are locked in the addressed SI registers on the rising edge of CSB. The device transfers the contents of one of the eight internal registers to the SO register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is at logic [0] (Figure 7 and Figure 8). CSB is internally pulled up to V_{DD} through I_{UP}.

5.2.9 SPI serial clock (SCLK)

The SCLK pin clocks the SPI data communication of the device. The serial input pin (SI) transfers data to the SI shift registers on the falling edge of the SCLK signal while data in the SO registers are transferred to the SO pin on the rising edge of the SCLK signal. The SCLK pin must be in low state when CSB makes any transition. For this reason, it is recommended to have the SCLK pin in the logic [0] state when the device is not accessed (CSB is at logic [1]). When CSB is set to logic [1], the signals at the SCLK and SI pins are ignored and the SO output is tri-stated (high-impedance). The SCLK pin is connected to an internal pull-down current source I_{DWN}.

5.2.10 Serial input (SI)

Serial input (SI) data bits are shifted in at this pin. SI data is read on the falling edge of SCLK. 16-bit data packages are required on the SI pin (see Figure 7), starting with bit D15 (MSB) and ending with D0 (LSB). All the internal device registers are addressed and controlled by a 4-bit address (D9-D12) described in Table 14. Register addresses and function attribution are described in Table 15. The SI pin is internally connected to a pull-down current source, I_{DWN}.

5.2.11 Supply of the digital circuitry (VDD)

This pin supplies the SPI circuit (3.3 V or 5.0 V). When lost, all circuitry becomes supplied by a V_{PWR} derived voltage, except the SPI's SO shift-register that can no longer be read.

5.2.12 Ground (GND)

This is the GND pin common for both the SPI and the other circuitry.

5.2.13 Positive supply pin (VPWR)

This pin is the positive supply and the common input pin of both switches. A 100 nF ceramic capacitor must be connected between VPWR and GND, close to the device. In addition, it is recommended to put a ceramic capacitor of at least 1.0 µF in parallel with this 100 nF capacitor.

5.2.14 Serial output (SO)

The SO pin is a tri-stateable output pin that conveys data from one of the 13 internal SO registers or from the previous SI register to the outside world. The SO pin remains in a high-impedance state (tri-state) until the CSB pin becomes logic [0]. It then transfers the SPI data (device state, configuration, fault information). The SO pin changes state at the rising edge of the SCLK signal. For daisy-chaining, it can be read out on the falling edge of SCLK. V_{DD} must be present before the SO registers can be read. The SO register assignment is described in Table 13.

5.2.15 Power switch output pins (HS0 and HS1)

HS0 and HS1 are the output pins of the power switches, to be connected to the loads. A ceramic capacitor (<= 22 nF (+/- 20%) is recommended between these pins and GND for optimal EMC performances.

5.2.16 Fail-safe output (FSOB)

This pin (active low) is used to indicate loss of SPI communication or loss of SPI supply voltage, V_{DD}. This open-drain output requires an external pull-up resistor to VPWR.

5.3 Functional internal block description

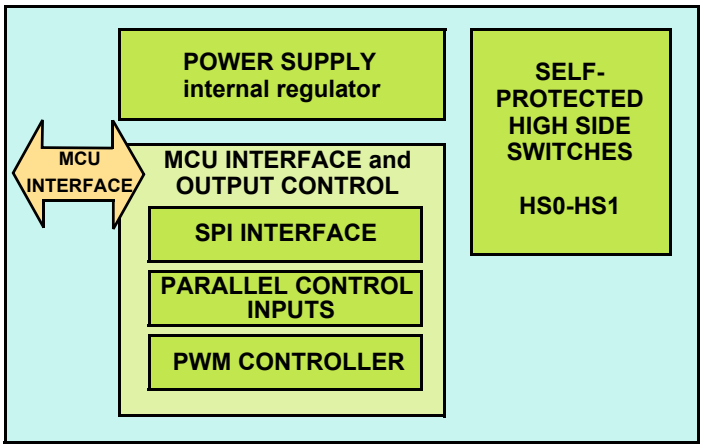


Figure 10. Internal block description

5.3.1 Power supply

The device operates with supply voltages from 6.0 to 58 V (V_{PWR}), but is full spec. compliant between 8.0 and 36 V. The VPWR pin supplies power to the internal regulator, analog, and logic circuit blocks. The VDD pin (5.0 V typ.) supplies the output register of the Serial Peripheral Interface (SPI). Consequently, the SPI registers cannot be read without presence of V_{DD}. The employed IC architecture guarantees a low quiescent current in Sleep mode.

5.3.2 Switch output pins HS0 and HS1

HS0 and HS1 are the output pins of the power switches. Both channels are protected against various kinds of short-circuits and have active clamp circuitry that may be activated when switching off inductive loads. Many protective and diagnostic functions are available. For large inductive loads, it is recommended to use a freewheeling diode. The device can be configured to control the output switches in parallel, which guarantees good switching synchronization.

5.3.3 Communication interface and device control

In Normal mode the output channels can either be controlled by the direct inputs or by the internal PWM module, which is configured by the SPI register settings. For bidirectional SPI communication, V_{DD} has to be in the authorized range. Failure diagnostics and configuration are also performed through the SPI port. The reported failure types are: OpenLoad, short-circuit to battery, severe short-circuit to ground, overcurrent, overtemperature, clock-fail, undervoltage, and overvoltage. The SPI port can be supplied either by a 5.0 V or by a 3.3 V voltage supply. For direct input control, V_{DD} is not required.

A Pulse Width Modulation (PWM) circuit allows driving loads at frequencies up to 1.0 kHz from an external or an internal clock. SPI communication is required to set these options.

6 Functional device operation

6.1 Operation and operating modes

The device possesses two high side switches (channels) each of which can be controlled independently. The device has four fundamental operating modes: Sleep, Normal, Fail-safe, and Fault mode, as shown in Table 6.

Each channel can be controlled in three different ways in Normal mode: by a signal on the Direct Input pin, by an internal clock signal (autonomous operation) or by an external clock signal. For bidirectional SPI communication, a second supply voltage is required (V_{DD} = 5.0 V or 3.3 V). When only the direct inputs IN[x] are used, V_{DD} isn't required.

6.1.1 Device start-up sequence

To put the device in a known configuration and guarantee predictable behavior, the device must undergo a wake-up sequence. However, it should not be woken up earlier than the moment at which V_{PWR} has exceeded its undervoltage threshold, V_{PWR}(UV), and V_{DD} has exceeded its supply failure threshold, V_{DD}(FAIL). In applications using the SPI port, the device is typically put in wake mode by setting RSTB=1. Wake-up of applications with direct input control can be achieved by having signals IN_ON[0] = 1 or IN_ON[1]= 1 (see Figure 11). After wake-up, all SPI register contents are reset (as defined in Table 12 and Table 13) and Normal mode is entered. All the device functions are available 50 µs later (typically).

If the start-up sequence is not performed at device start-up, its configuration may be undetermined and correct operation is not guaranteed. In situations where the above described start-up sequence can not be performed, it is recommended to generate a wake-up event after the moment V_{PWR} has reached the undervoltage threshold.

6.1.2 Channel configuration through the SPI

6.1.2.1 Setting the channel configuration

The channel configuration is determined by the contents of the pulse-width (PWMR_s), the configuration (CONFR_s) and the overcurrent (OCR_s) registers. They allow setting, among others, the following parameters: duty-cycle, delay, Slew Rate, PWM enable (PWM_en), clock selection (CLOCK_sel), prescaler (PR), and direct_input disable (DIR_dis). Extension "_s" means that these registers exist for each of both channels. Function assignment is described in detail in the section SI register addressing.

6.1.2.2 Reading back the channel's status and settings

The channel's global switching and operating states (ON/OFF, normal/fault) are all contained in the SO-STATR register (see Table 16). The precise fault type can be found by reading out the FAULTR_s and STATR registers. The current channel settings (channel configuration) can be known by reading the PWMR, CONF, OCR, RETRYR, GCR, and DIAG registers (see section Serial output register assignment and beyond).

6.1.3 Normal mode

Normal mode (bit NM = 1) can be entered in two ways: either by driving the device through the direct inputs (IN[x]) or by establishing SPI communication (requires RSTB =high). Bidirectional SPI communication additionally requires the presence of V_{DD}. To maintain the device in Normal mode, communication must take place regularly (see Entering and maintaining Normal mode). The device is in Normal mode (NM) when:

- V_{PWR} (and V_{DD}) are within the normal range and
- wake-up = 1, and
- fail-safe = 0, and
- fault = 0.

6.1.3.1 Channel control in Normal mode

In direct input mode, the channel's switching state (ON/OFF) is controlled by the logic state of the direct input signal with the default values (00) of turn-on delay and slew rate, specified in Table 5.

In internal clock mode, the switching state is controlled by an internal clock signal (Internal clock and internal PWM (Clock_int_s bit = 1)). Frequency, slew rate, duty-cycle, and turn-on delay are programmable independently for both channels.

In external clock mode, the frequency of the external clock controls the output's PWM frequency, but slew rate, duty-cycle, and turn-on delay are still programmable.

6.1.3.2 Factors determining the channel's switching state

The switching state of a channel is defined by the instantaneous value of the output voltage. It is defined as "On" when the output voltage V(HS[x]) > V_{PWR} /2 and "Off" when V(HS[x]) < V_{PWR} /2. The channel's switching state should not be confused with the device's internal channel control state hson[x] (= High Side On). Signal hson[x] defines the targeted switching state of the channel (On/Off). It is either controlled by the value of the direct input signal or by that of the internal/external clock signals combined with the SPI register settings. The value of hson[x] is given by the following boolean expression:

hson[x] = [(IN[x] and $\overline{\text{DIR\_dis[x]}}$) or (On bit [x] and Duty_cycle[x] and PWM_en[x] = 1) or (On bit [x] and PWM_en[x] = 0)].

In this expression Duty_cycle[x] represents the value of the duty cycle, set by bits D7…D0 of the PWMR register (Table 7). The channel's actual switching state may differ from the control signal's state in the following cases:

- short-circuits to GND, before automatic turn-Off (t < t_{FAULT})
- short-circuits to V_{PWR} when the channel is set to Off
- V_{PWR} < 13 V when openload in OFF state detection is selected and the load is actually lost
- during the turn-on transition as long as V(HS[x])< V_{PWR}/2
- during the turn-off transition as long as V(HS[x]) > V_{PWR}/2

6.1.3.3 Entering and maintaining Normal mode

A 0-to-1 transition on RSTB, (when both V_{PWR} and V_{DD} are present) or on any of both direct inputs IN[x] (when only supplied by V_{PWR}) puts the device in Normal mode. If desired, the device can be operated in Normal mode without V_{DD}, but this requires that at least one of both direct inputs be regularly turned on (Operation and operating modes). To maintain the device in Normal mode (NM), communication must take place on a regular basis.

For SPI communication, the state of the WDIN bit must be alternated at least every 310 ms (typ.) (t_{WDTO}), unless the WD_disable bit is set to 1.

For direct input control, the timing requirements are shown in Figure 11. A signal called IN_ON[x] is not directly accessible to the user but is used by the internal logic circuitry to determine the device state. When no activity is detected on a direct input pin (IN[x]) for a time longer than t_{IN} = 250 ms (typ.), timeout is detected and IN_ON[x] goes low. When this occurs on both channels, Sleep mode is entered (Sleep mode), provided reset = RSTB = 0.

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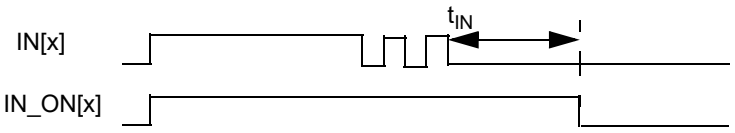

Figure 11. Relation between signals IN(x) and IN_ON[x]

6.1.3.4 Direct control mode

When RSTB = 0 (and also in Fail-safe mode), the channels are merely controlled by the direct input pins IN[x]. All protective functions (OC, OT, SC, OV, and UV) are operational including auto-retry. To avoid entering Sleep mode at frequencies < 4.0 Hz, reset should be set to RSTB = 1.

6.1.3.5 Going from Normal to Fail-safe, Fault or Sleep mode

The device changes from Normal to Fail-safe (Fail-safe mode), Sleep mode (Sleep mode), or Fault mode (Fault mode), according to the value of the following signals (see Table 6).

- wake-up = RSTB or IN_ON[0] or IN_ON[1]
- fail-safe = (V_{DD} Failure and V_{DD}_FAIL_en) or (SPI watchdog timeout (t_{WDTO}) and WD_dis = 0)
- fault = OC[0:1] or OT[0:1] or SC[0:1] or UV or (OV and $\overline{OV\_dis}$)

Table 6. Device operating modes

Mode	Wake-up	Fail-safe	Fault	Comments
Sleep	0	x	x	All channels are OFF.
Normal	1	0	0	The SPI Watchdog is active when: VDD = 5.0 V, WD_dis = 0, RSTB = 1
Fail-safe	1	1	0	The channels are controlled by the IN inputs. (see Fail-safe mode)
Fault	1	X	1	The channels are OFF, see Fault mode.

x = Don't care.

It enters Fail-safe mode in case of a timeout on SPI communication or when V_{DD} is lost after having been initially present (if this function was previously enabled by setting: $V_{DD\_FAIL\_EN}$ bit = [1]). Setting watchdog disabled (WD_dis = 1, D4 of the GCR register) avoids entering Fail-safe mode after watchdog timeout. Device behavior upon fault occurrence is explained in the paragraph on Faults (Fault mode).

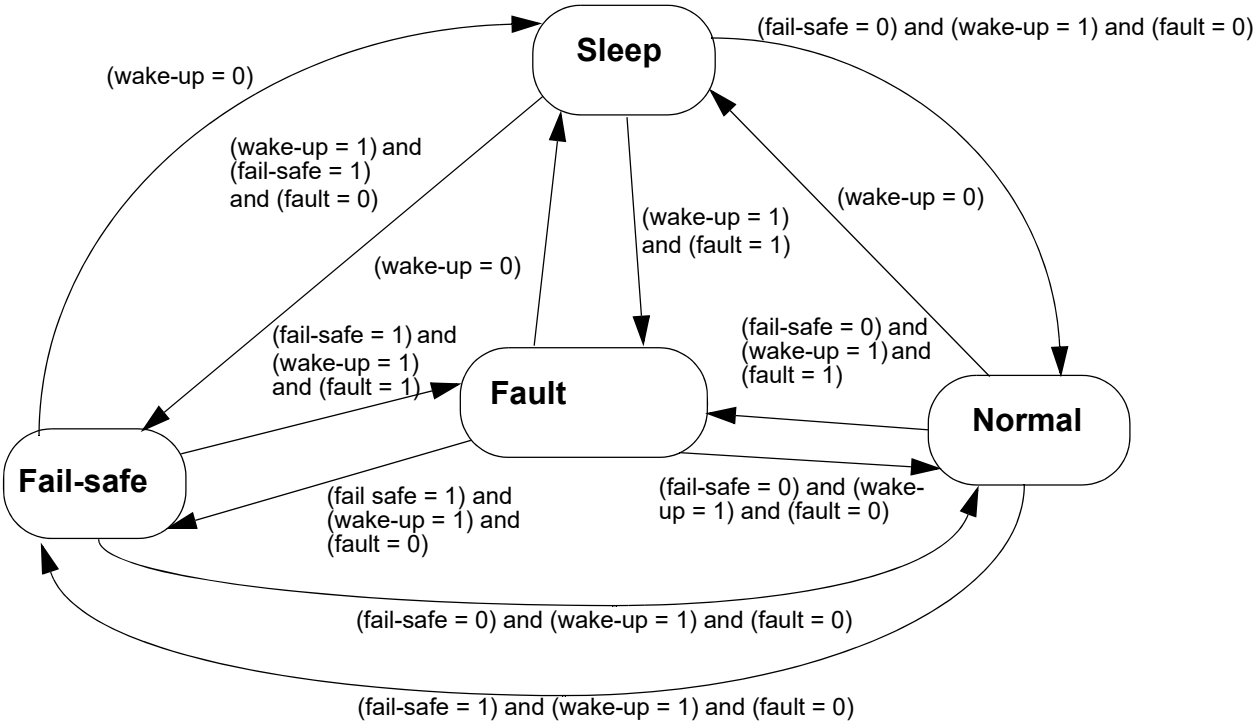

Figure 12. Device operating modes

6.1.4 Sleep mode

In Sleep mode, the channels and the SPI interface are turned off to minimize current consumption.

The device enters Sleep mode (wake-up = 0) when both Direct Input pins IN(x) remain Off longer than t_{IN} sec. (when reset is active; RSTB = 0). This is expressed as follows:

- V_{PWR} (and V_{DD}) are within the normal range, and
- wake-up = 0 (wake-up = RSTB or IN_ON[0] or IN_ON[1])
- and
- fail-safe = X and
- fault = X

When employed, V_{DD} must be kept in the normal range. Sleep mode is the default mode after the first application of the supply voltage (V_{PWR}), prior to any I/O communication (RSTB and the internal states IN_ON[0:1] are still at logic [0]). All SPI register contents remain in their default state during sleep mode.

6.1.5 Fail-safe mode

6.1.5.1 Entering Fail-safe mode

Fail-safe mode is entered either upon loss of SPI communication or after loss of optional SPI supply voltage V_{DD} (VDD out of range). The FSOB pin goes low and the channels are only controlled by the direct inputs (IN[0:1]). All protective functions remain fully operational. Previously latched faults are delatched and SPI register contents is reset (except bits POR & PARALLEL). The SPI registers can not be accessed. These conditions are also described by the following expressions:

- V_{PWR} is within the normal voltage range, and
- wake-up = 1, fault = 0, and
- fail-safe = 1 ((V_{DD} Failure and V_{DD}_FAIL_en=1 before) or (t(SPI)> t_{WDTO} and WD_dis = 0).

The last condition describes the loss of SPI communication which is detailed in the next section.

6.1.5.2 Watchdog on SPI communication and Fail-safe mode

When V_{DD} is present, the SPI watchdog timer is started upon a rising edge on the RSTB pin. Thereafter the device monitors the state of the first bit (WDIN) of all received SPI words. When the state of this bit is not alternated at least once within a data stream of duration t_{WDTO} = 310 ms typ., the device considers that SPI communication has been lost and enters Fail-safe mode. This behavior can be disabled by setting the bit WD_DIS = 1. The value of watchdog timeout is derived from an internal oscillator.

6.1.5.3 Returning from Fail-safe to Normal mode

To exit Fail-safe mode and return to normal mode again, first a SPI data word with its WDIN bit = 1 (D15) must be received by the device (regardless the register it is contained in and regardless the values of the other bits in this register). Next, a second data word must be received within the timeout period (t_{WDTO} = 310 ms typ.) to be able to change any SPI register contents. Upon entering Normal mode, the FSOB pin returns to logic high and previously set faults and SPI registers are reset, except bits POR, PARALLEL and fault bits of latchable faults that had actually been latched.

6.1.6 Fault mode

The device enters Fault mode when any of the following faults occurs in Normal or Fail-safe mode:

- Overtemperature fault, (latchable fault)
- Overcurrent fault, (latchable fault)
- Severe short-circuit fault, (latchable fault)
- Output shorted to V_{PWR} in OFF state (default: disabled)
- OpenLoad fault in OFF state (default: disabled)
- OpenLoad fault in ON state (default: disabled)
- External Clock Failure (default: enabled)
- Overvoltage fault (enabled by default)
- Undervoltage fault, (latchable fault)

The Fault Status pin asserts a fault occurrence on any channel in real time (active low). Additionally, the assigned fault bit in the STATR_s or FAULTR_s register is set to one. Conversely to the FSB pin, a fault bit remains set until the corresponding register is read, even if the fault has disappeared. These bits can be read via the SO pin. Fault occurrence results in a turn-off of the incurred channel, except for the following faults: openload (ON and OFF state), External Clock Failure and Output(s) shorted to V_{PWR}. Under and overvoltage occurrences cause simultaneous turn-off of both channels. Details on the device's behavior after the occurrence of one of the above faults can be found in Protection and diagnostic features.

Fault mode (Operation and operating modes) is entered when:

- V_{PWR} ($+V_{DD}$) were within the normal voltage range, and
- wake-up = 1, and
- fail-safe = X, and
- fault = 1 (see Going from Normal to Fail-safe, Fault or Sleep mode)

6.1.6.1 Resetting FAULT bits

Registers STATR_s and FAULTR_s contain global and channel-specific fault information. Reading the register the fault bit is contained in clears it, provided failure cause disappearance was detected and the fault wasn't latched.

6.1.6.2 Entering Fault mode from Fail-safe mode

When a Fault occurs in Fail-safe mode, the device is in Fault/Fail-safe mode and behaves according to the description of fault mode. However, SPI registers remain reset and can not be accessed. Only the Direct inputs control the channels.

6.1.6.3 Returning from Fault mode to Fail-safe mode

When disappearance of the fault previously produced in Fail-safe mode has been detected, the device returns to Fail-safe mode and behaves accordingly. FSB goes high, but the auto-retry counter is not reset. Latched faults are not delatched. SPI registers remain reset.

6.1.7 Latchable faults

An auto-retry function (see Auto-retry) controls how the device responds to the so-called latchable faults. Latchable faults are: overcurrent (OC), severe short-circuit (SC), overtemperature (OT), and undervoltage (UV). If a latchable fault occurs, the channel is turned off, the FSB terminal goes low, and the assigned fault bit is set. These bits can not be reset before the next turn-on event is generated by auto-retry. Next, the channel automatically turns on at a programmable interval (provided auto-retry was enabled and the channel wasn't latched).

If the failure disappears prior to the expiration of the available amount of auto-retries, the FSB pin automatically returns to logic [1], but the fault bit remains set. It can then still be reset by reading the SPI register it is contained in.

However, the fault actually gets latched if the failure cause has not disappeared at the first turn-on event following expiration of the available amount of auto-retries (see Auto-retry). In that case, the channel gets latched and the FSB terminal remains low. The fault bit can not be reset by reading out the associated SPI register prior to performing a delatch sequence (Fault delatching).

6.1.7.1 Fault delatching

To delatch a latched channel and be able to turn it on again, a delatch sequence must be executed after disappearance of the failure cause. Delatching resets the fault bit of latched faults (see Resetting FAULT bits). To reset the FSB pin, both channels must be delatched.

Delatching is achieved either by alternating the state of the channels' fault control signal fc[x] (generating a 1_0_1 sequence), or by resetting the auto-retry counter (provided retry is enabled). See Reset of the auto-retry counter. Delatching then actually occurs at the rising edge of the turn-on event.

Signal fc[x] is an internal signal used by the device's internal logic circuitry to control the diagnostic functions. The value of fc[x] depends on the state of the variables IN_ON[x], DIR_dis[x] and ON[x] and is expressed as follows:

fc[x] = ((IN_ON[x] and DIR_dis[x] = 0) or ON[x] = 1)

Alternating the fc[x] signal is achieved differently according to the way the user controls the device.

- In direct-input controlled mode (DIR_dis_s = 0), the IN[x] pin must be set low, remain low for at least t_{IN} seconds, and set high again (be switched On). This might happen automatically when operating at frequencies f<4.0 Hz.
- In SPI-controlled mode, the ON_bit state (D8 of the PWMR_s reg.) must be alternated ('toggled'). No minimum OFF state duration is required in this case.

Performing a delatch sequence anytime during an ongoing auto-retry sequence (before latching) allows turning the channel on unconditionally.

When a power-on event occurs (see Loss of VPWR, loss of VDD, and power-on reset (POR)), latched channels are also delatched and faults are reset.

When Fail-safe mode is entered (fault=1, fail-safe becomes 1) during operating in Fault mode (fault=1, fail-safe=0), previously latched faults are delatched and SPI register content is reset (except bits POR & PARALLEL). The device is then in a combined Fail-safe/Fault mode.

When the device was already in Fail-safe mode (fault=1, failsafe=1) and (new) faults occurs, the internal auto-retry counter does not reset and latched channels are not delatched until a delatching sequence has been performed (see Protection and diagnostic features).

6.1.8 Programmable PWM module

Each channel has a fully independent PWM module activated by setting PWM_en_s. It modulates an internal or external clock signal. Setting Clock_int_s = 1 (bit D6 of the OCR_s register) activates the internal clock, and setting Clock_int_s = 0 activates the external clock. The duty cycle can be set in a range from 0% to 100% with 8 bit-resolution (Table 7) by setting bits D8…D0 of the PWMR_s register (Table 12). The channel's switching frequency equals the clock frequency divided by 256 in internal clock mode, and by 256 or 512 in external clock mode.

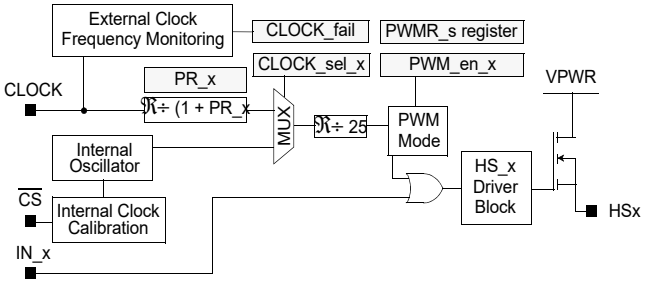

Figure 13. Internal and external clock operation

Table 7. PWM duty cycle value assignment

ON-bit	Duty cycle	Channel configuration
0	**X**	**OFF**
1	00000000	PWM (duty-cycle=1/256)
1	00000001	PWM (duty-cycle=2/256)
1	00000010	PWM (duty-cycle=3/256)
1	n	PWM (duty-cycle=(n+1)/256)
1	11111111	fully ON

By delaying the activation of one channel relative to the other (Table 8), switch-on surges can be delayed, which may improve EMC performance. Switch-On delay can be selected among seven different values (default=0) by setting bits D2…D0 of the CONFR_s register (expressed as a number of ext./int. PWM clock periods). To start the PWM function at a known point in time, the PWM_en_s bit (D8 /D7 of the GCR reg.) must be set to 1 after having set the PWMR_s (duty cycle) and CONFR_s (delay) registers. The best way to improve EMC is to use an external clock with a staggered switch on delay.

Table 8. Switch-on delay in PWM mode

Delay bits	Switch-on delay
000	no delay
001	32 PWM clock periods
010	64 PWM clock periods
011	96 PWM clock periods
100	128 PWM clock periods
101	160 PWM clock periods
110	192 PWM clock periods
111	224 PWM clock periods

6.1.8.1 External clock and internal PWM (CLOCK_int_s = 0)

The channels can be controlled by an external clock signal by setting bit D6 =0 of the OCR_s register (Clock_int_s). Duty cycle values specified in Table 7 apply. When an external clock is used, the value of frequency division (256 when PR[x] = 0) may be doubled by setting the prescaler bit PR[x]) = 1(bit D7 of the OCR_s reg.). This allows driving the channels at different switching frequencies from a single clock signal. Simultaneously setting PWM_en_1=1 and PWM_en_0=1 synchronizes the channels.

The clock frequency on the CLOCK pin is monitored when external clock (CLOCK_int_s = 0) and pulse width modulation (PWM_en_s = 1) are both selected. If a clock failure occurs under these conditions (f< $f_{CLOCK(LOW)}$ or f> $f_{CLOCK(HIGH)}$), the external clock signal is ignored and a fault is detected (FSB =0), CLOCK_fail bit is set (OD2 in the DIAGR register). The state of the ON_s bit in the SPI register then determines the channel's switching state. To return to external clock mode (and reset FSB), the clock-fail bit must be read and the external clock has to be within the authorized range again.

6.1.8.2 Internal clock and internal PWM (Clock_int_s bit = 1)

By using a reference time slot (usually available from an external microcontroller), the period of each of the internal PWM clocks can be changed or calibrated (see Programmable PWM module). Calibration of the default period = $1/f_{PWM(0)}$ reduces it maximum variation from about +/-30% to +/-10%. The programming procedure is initialized by sending a dedicated word to the SI-CALR register (see Table 7). Next, the device sets the new value of the switching period in 2 steps. First it measures the time elapsed between the first falling edge on the CSB pin and the next rising edge on the CSB pin (t_{CSB}). Then it changes the value of the internal clock period accordingly. The actual value of the channel's switching period is obtained by multiplying the internal clock period by 256.

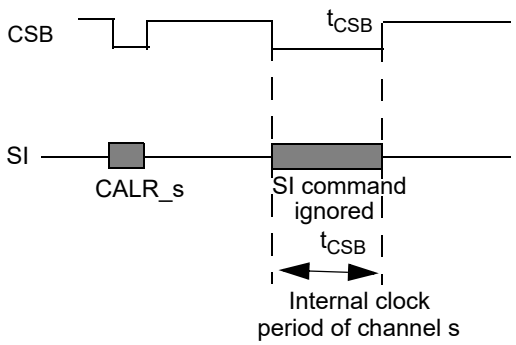

Figure 14. Internal clock calibration

When the duration of the negative CSB pulse is outside a predefined time slot (from $t_{CSB(MIN)}$ to $t_{CSB(MAX)}$), the calibration event is ignored and the internal clock frequency remains unchanged. If the value ($f_{PWM(0)}$) has not been previously calibrated, it remains at its default level.

6.1.8.3 Synchronization of both channels

When internal clock signals are used to drive the PWM modules, perfect synchronization over a long time can not be achieved since both clock signals are independent. However, when the channels are driven by an external clock, perfect synchronization can be achieved by simultaneously setting PWM_en_1=1 and PWM_en_0=1. The best way to optimize EMC is to use an external clock with a staggered switch on delay (see Table 8).

6.1.9 Parallel operation

The channels can be paralleled to drive higher currents. Setting the PARALLEL bit in the GCR register to logic [1] is mandatory in this case. The improved synchronization of both transistors allows an equal current distribution between both channels. In parallel mode, both output pins (HS[x]) must be connected (as well as both IN[x] pins in case of external control). CONF0 and CONF1 must be set to equal values.

1- Device configuration in Parallel mode:

There are two ways to configure the On/Off control: SPI-configured PWM control and Direct Input Control.

- *SPI configured Parallel mode*:

The switching configuration is solely defined by the (SI) PWMR_0, CONFR_0, OCR_0, and RETRY_0 registers. As soon as PARALLEL=1, the contents of the corresponding registers in bank 1 are replaced by that of bank 0, except bits D6-D8 of the CONFR_1

register (configuration of the openload/output short-circuited diagnostics). It is recommended to disable the OFF state openload for the HS1 output (not necessary for 20XS4200B). After setting PARALLEL=1, contents of SO registers in bank 0 are copied to registers of bank 1 only when new information is written in them. Bits OD3, OD4 and OD5 of both FAULTR_s registers (OLON, OLOFF, OS) are always reported independently.

- *Direct Input controlled Parallel mode:*

The IN0 and IN1 pins must be connected externally.

2- Diagnostics in Parallel mode:

The diagnostics in Parallel mode operate as follows:

- Openload in OFF state and - openload in ON state:

The OL_ON and OL_OFF bits of both FAULTR registers independently report failures of the channels according to the settings of bits D7 and D6 of the CONFR_s register.

- Current sensing:

See Table 23 for a description of the various current sensing modes.

Only the Current sense ratio of bank 0 (D5 of the OCR_0 register) is considered. The corresponding bit in the OCR_1 register is copied from that of the OCR_0 register.

- output shorted to battery:

The OS-bit (OD3) of each of both FAULT registers independently report this fault, according to the settings of bit D8 of the CONFR_s reg.

3- Protections in Parallel mode:

- Overcurrent:

-Only the configuration of overcurrent thresholds & blanking windows of channel 0 are considered.

-In case overcurrent (OC) occurs on any channel, both channels are turned-off. Regardless the order of occurrence of OC, both OC-bits (OD0) in the FAULT registers are simultaneously set to logic 1.

- severe short-circuit:

In case of SC detection on any channel, both channels are turned-off and the SC bits (OD1) in both FAULT registers are simultaneously set to logic 1.

- overtemperature:

In case of OT detection on any channel, both channels are turned-off and both OT bits in the FAULT registers (OD2) are simultaneously set to logic 1.

- auto-retry:

Only one 4-bit auto-retry counter specifies the number of successive turn-on events on paralleled channels (RETRYR_0). The counter value in register RETRYR_1 (OD4…OD7) is copied from that in RETRYR_0.

To delatch the channels, only channel 0 needs to be delatched.

6.2 Protection and diagnostic features

6.2.1 Protective functions

6.2.1.1 Overtemperature fault (Latchable fault)

The channels have individual overtemperature detection. As soon as a channel's junction temperature rises above T_{SD} (175 °C typ.), it is turned OFF, the overtemperature bit (OT = OD2) is set, and FSB = 0. FSB can only be reset by turning ON the channel when the junction temperature of both channels has dropped below the threshold: $T_J<T_{SD}$. Overtemperature is detected in ON and in OFF state:

- If the channel is ON, the associated output is switched OFF, the OT bit is set, and FSB = 0.
- If the channel is OFF: FSB goes to logic [0] and remain low until the temperature of both channels is below T_{SD} and any of the channels is turned on again.

The auto-retry function (if activated) automatically turns the channel on when the junction temperature has dropped below T_{SD}. The OT fault bit can only be reset by reading out the FAULTR register, provided that $T_J<T_{SD}$ and FSB = 1 again.

6.2.1.2 Overcurrent fault (Latchable fault)

When overcurrent (OC) is detected, the channel is immediately turned Off (after t_{FAULT} seconds). The OC-bit is set to 1 and FSB becomes low [0]. Overcurrent is detected anytime the load current crosses an overcurrent threshold or exceeds the window width of the selected overcurrent protection profile. This profile is a stair function with windows the height and width of which are preselected through the SPI port. The maximum allowable value of the load current at a particular moment in time is defined by levels $I_{\_OCH}$ and $I_{\_OCM}$ and windows t_{OCM_x} and t_{OCH} (programmable by SPI bits). The steady-state overcurrent protection level $I_{\_OCL}$ is defined by the settings of the OCL and HOCR bits. Anytime an overcurrent window is active, current sensing is blanked and SYNC becomes 1.

6.2.1.3 Overcurrent duration counter

The load current can spend only a defined amount of time in a particular window of the overcurrent profile. If the time in the window exceeds the selected window width (t_{OCx}) or the overcurrent threshold is crossed, the channel is turned off (OC fault), followed by auto-retry (if enabled). An internal overcurrent duration counter is employed for this function.

6.2.1.4 Overcurrent detection on resistive and inductive loads

According to the load type (resistive or inductive), one of two different overcurrent profiles should be selected. This is done by connecting a resistor with the appropriate value between the CONF[0:1] pins and GND (Table 9).

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Table 9. Overcurrent profile selection

CONF[0:1] resistor/voltage	Type of load
1.0 kOhm < R(CONF[x]) < 10 kOhm or 0 < V(CONF[X) < VIL (0.8 V)	resistive: CONF = 0, Lighting-Mode
R(CONF[x]) > 50 kOhm or VIH (2.0 V)< V(CONF) < 5.0 V	inductive: CONF = 1, DC motor mode

When overcurrent windows are active, current sensing is disabled and the SYNCB pin remains high. This is illustrated by Figure 15. After turn on, the output voltage (second waveform (20 V/div.) and the output current (first waveform, 12 A/div.) rise immediately, but the current sense voltage (third waveform, 2.0 V/div, 1.0 V = 3.0 A) and its synchronization signal SYNC (fourth waveform, 5.0 V/div.) only become active at the end of the selected overcurrent window (duration t_{OCM2_L}).

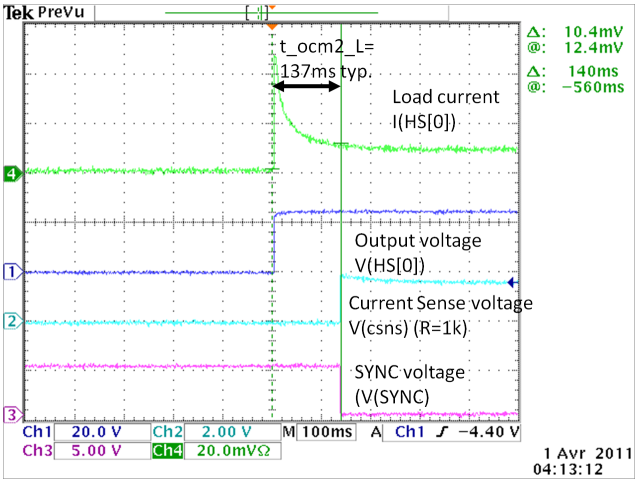

Figure 15. Current sense blanking during overcurrent window activity

Activation of the lighting profile is time driven and activation of the DC motor profile is event driven, as explained below.

In lighting mode, the height of the overcurrent profile is defined by three different thresholds ($I_{\_OCH}$, $I_{\_OCM}$ and $I_{\_OCL}$, which stand for the higher, the middle, and the lower overcurrent threshold), as illustrated by Figure 5. This profile has two adjacent windows the width of which is compatible with typical bulb inrush current profiles. The width of the first of these windows is either t_{OCH1} or t_{OCH2}. The width of the second window is either t_{OCM1_L} or t_{OCM2_L} (see Table 18). The lighting profile is activated at each turn-on event including auto-retry, except in switch mode. In switch mode, the profile is activated only at the first turn-on event, but is not renewed. During the on-period, the load current is continuously compared to the programmed overcurrent profile. The channel is switched Off when a threshold is crossed or a window width is exceeded.

In DC motor mode, only one overcurrent window exists, defined by only two different thresholds ($I_{\_OCH}$ and $I_{\_OCL}$) as illustrated by Figure 6. This window is opened anytime the output current exceeds the selected lower overcurrent threshold (I_{OCLx}). In this case, the allowed overcurrent duration is defined by parameters t_{OCM1_M}, t_{OCM2_M}, t_{OCH1} and t_{OCH2}.

The selection of the different profiles and values is explained in the section Address A0100— Overcurrent protection configuration register (OCR_s).

6.2.1.5 Auto-retry after overcurrent shut off

When auto-retry is activated, OC-latching (Overcurrent fault (Latchable fault)) only occurs after expiration of the available amount of auto-retries (described in section Auto-retry).

6.2.1.6 Switch mode operation and overcurrent duration

Switch mode is defined as any device operation with a duty cycle lower than 100% at a frequency above f_{PWM_EXT} (min.) or f_{PWM_INT} (min.). The device may operate in Switch mode in internal/external PWM or in direct input mode. In switch mode, the accumulated time spent by the load current in a particular window segment during On times of successive switching periods is identified by the aforementioned duration counter, and compared to the active segment width. The associated off-times are excluded by the duration counter. The channel is turned-off when the value of the counter exceeds the window width. In Figure 16, overcurrent detection shutdown

is shown in case of switch mode operation with a duty cycle of 50% (solid line) and 100% (fully-on, dashed line). The device is turned off much later in switch mode than in fully-on mode, since the duration counter only counts overcurrent during on-times.

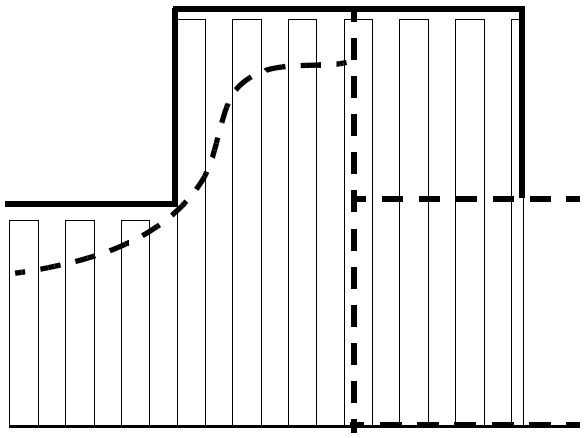

Figure 16. Overcurrent shutdown in PWM mode (solid line) and Fully-on mode (dashed line)

6.2.1.7 Reset of the duration counter

Reset of the duration counter is achieved by performing a delatch sequence (Fault delatching). In lighting mode (CONFs = 0), this counter is also reset automatically at each auto-retry (but not in DC motor mode).

In DC motor mode, the duration counter is reset by a performing a delatch sequence and automatically after a full on-period without overcurrent ([hson[x]=1 for any duration). Reset then actually occurs at the first turn-off instant following that on-period.

In switch mode, the duration counter is not reset by normal PWM activity unless delatching is performed.

6.2.1.8 Severe short-circuit fault (Latchable fault)

When a severe short-circuit (SC) is detected at turn-ON (wiring length $L_{LOAD} < L_{SHORT}$, see Table 4), the channel is shut off immediately. For wiring lengths above L_{SHORT}, the device is protected from short-circuits by the normal overcurrent protection functions (Overtemperature fault (Latchable fault)). When an SC occurs, FSB goes low (logic [0]), and the SC bit is set, eventually followed by an auto-retry. SC is of the latchable fault type (see Protection and diagnostic features and Fault delatching).

6.2.1.9 Overvoltage detection (enabled by default)

By default, the supply overvoltage protection (V_{PWR}) is enabled. When overvoltage occurs ($V_{PWR} \geq V_{PWR(OV)}$), the device turns OFF both channels simultaneously, the FSB pin is asserted low, and the OV fault bit is set to logic [1]. The channels remain OFF until the supply voltage drops below a threshold voltage $V_{PWR} \leq V_{PWR(OV)} - V_{PWR(OVHYS)}$. The OV bit can then be reset by reading out the STATR register.

The overvoltage protection can be disabled by setting the OV_dis = 1 in the general configuration (GCR) register. In this case, the FSB pin neither asserts a fault occurrence, nor turns off the channels. However, the fault register (OV bit) still reports an overvoltage occurrence (when $V_{PWR} \geq V_{PWR(OV)}$) as a warning. When $V_{PWR} \geq V_{PWR(OV)}$, the value of the on-resistance on both channels ($R_{DS(ON)}$) still lays within the ranges specified in Table 4.

6.2.1.10 Undervoltage fault (Latchable fault)

The channels are always turned off when the supply voltage (V_{PWR}) drops below $V_{PWR(UV)}$. FSB drops to logic [0], and the fault register's (common) UV bit is set to [1].

When the undervoltage condition then disappears, two different cases exist:

- If the channel's internal control signal hson[x] is off, FSB returns to logic [1], but the UV bit remains set until at least one output is turned on (warning).
- If the channel's control signal is on, the channel is turned on if a delatch or POR sequence is performed prior to the turn on request. The UV bit can then only be reset by reading out the STATR register.

Auto-retry (if enabled) starts as soon as the UV condition disappears.

6.2.1.11 Extended mode protection

In extended mode (6.0 V < V_{PWR} < 8.0 V or 36 V < V_{PWR} < 58 V), the channels are still fault protected, but compliance with the specified protection levels is not guaranteed. The register settings however (including previously detected faults) remain unaltered, provided V_{DD} is within the authorized range. Below 6.0 V, the channels are only protected from overtemperature, and this fault is only reported in the SPI register the moment V_{PWR} has again risen above $VPWR_{(UV)}$. To allow the outputs to remain ON between 36 V and 58 V, overvoltage detection should be disabled (by setting OV_dis = 1 in the GCR register).

Faults (overtemperature, overcurrent, severe short-circuit, over and undervoltage) are reset if:

- $V_{DD} \leq V_{DD(FAIL)}$ with V_{PWR} in the normal voltage range
- V_{DD} and V_{PWR} are below the $V_{SUPPLY(POR)}$ voltage threshold
- The corresponding SPI register is read after the disappearance of the failure cause (and delatching)

6.2.1.12 Drain/source overvoltage protection

The device tries to limit the Drain-to-Source voltage by turning on the channel whenever V_{DS} exceeds $V_{DS(CLAMP)}$. When a fault occurs (SC, OC, OT, UV), the device is rapidly switched Off (in t < t_{FAULT} seconds), regardless the value of the selected slew rate. This may induce voltage surges on V_{PWR} and/or the output pin (HS[x]) when connected to an inductive line/load. Turning on the device also dissipates the energy stored in the inductive supply line. This function monitors overvoltage for V_{PWR} > 30 V. For supply voltages V_{PWR} < 30 V, the device is protected from negative output voltages by automatically turning on the channel. The feature remains functional after device ground loss.

6.2.1.13 Supply overvoltage protection

In order to protect the device from excessive voltages on the supply lines, the voltage between the device's supply pins (VPWR and the GND) is monitored. When the V_{PWR}-to-GND voltage exceeds the threshold $V_{D\_GND(CLAMP)}$, the channel is automatically turned on. The feature is not operational in cases of ground loss.

6.2.1.14 Negative output voltage protection

The device tries to limit the undervoltage on the output pins HS[x] when turning off inductive loads. When the output voltage drops below V_{CL}, the channel is switched on automatically. This feature is not guaranteed after a device ground loss.

The energy dissipation capabilities of the circuit are defined by the $E_{CL[0:1]}$ parameters. For inductive loads larger than 20 µH, it is recommended to employ a freewheeling diode. The three different overvoltage protection circuits are symbolically represented in Figure 17. The values of the clamping diodes are those specified in Table 4. Coupling factor k represents the current ratio between the current in the supply-voltage measurement-diode (zener) and the current injected into the MOSFET's gate to turn it on.

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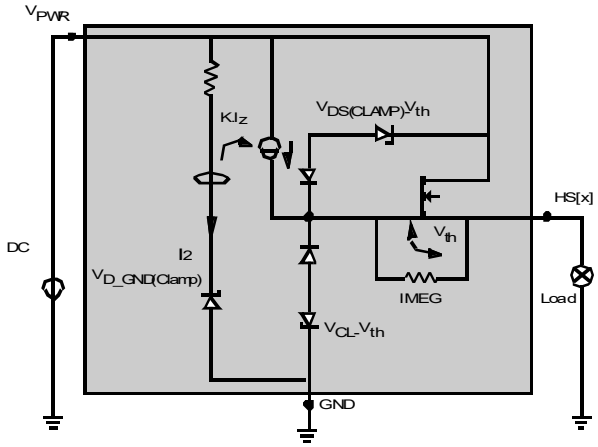

Figure 17. Supply and output voltage protections

6.2.1.15 Reverse voltage protection on V_{PWR}

The device can withstand reverse supply voltages on VPWR down to -28 V. Under these conditions, the outputs are automatically turned On and the channel's on-resistance ($R_{DS(on)}$) is similar to that during positive supply voltages. No additional components are required to protect the V_{PWR} circuit except series resistors (>8.0 k) between the direct inputs IN[0:1] and V_{PWR}, in case they are connected to VPWR. The VDD pin needs reverse voltage protection from an externally connected diode (Figure 23).

6.2.1.16 Load and system ground loss

In case of load ground loss, the channel's state does not change, but the device detects an openload fault. In case of a system GND loss, the channels are turned off.

6.2.1.17 Device ground loss

In the (improbable) case the device loses all of its three ground connections (pins 14, 17, and 22), the channels' state (ON/ OFF), depends on several factors: the values of the series resistors connected to the device pins, the voltage of the direct input signals, the device's momentary current consumption (influenced by the SPI settings) and the state of other high side switches on the board when there are pins in common like FSB, FSOB, and SYNC. In the following description, all voltages are referenced to the system (module) GND.

When series resistors are used, the channel state can be controlled by entering Fail-safe mode. The channels are turned off automatically when the voltage applied to the IN[x] input(s) through the series resistor(s) is not higher than V_{DD} and be turned on when the IN[x] input(s) are tied to V_{PWR}. Fail-safe is entered under the following conditions:

- all unused pins are tied to the overall system's GND connection by resistors > 8.0 k
- any device pin connected to external system components has a series resistors > 8.0 k (except pins Vpwr, VDD, HS[0], HS[1], and R(CSNS)>2.0 k)
- the FSB, FSOB, and SYNC pins are in the logic high state when they are shared with other devices. This means that none of the other devices is in Fault or Fail-safe mode, nor should current sensing be performed on any one of them when GND is lost

When no series resistors are employed, the channel state after GND loss is determined by the voltage on pins IN[0:1] and the voltage shift of the device GND. Device GND shift is determined by the lowest value of the external voltage applied to either pin of the following list: CLOCK, FSB, IN[0:1], FSOB, SCLK, CS,SI, SO, RSTB, CONF[0:1], SYNC, and CSNS. When the device GND voltage becomes logic low (V(GND)< V_{IL}), the SPI port continues to operate and the device operates normally. When the GND voltage becomes logic high (V(GND)> V_{IH}), SPI communication is lost and Fail-safe mode is entered. When the voltage applied to the IN[0:1] input is V_{PWR}, the channel is turned on when it is V_{DD}, the channel is turned off if (V_{DD} - V(GND)) < V_{IH}.

6.2.2 Supply voltages out of range

6.2.2.1 V_{DD} out of range

If the external V_{DD} supply voltage is lost (or falls outside the authorized range: V_{DD}<$V_{DD(FAIL)}$), the device enters Fail-safe mode, provided the VDD_FAIL_en bit had been set. Consequently, the contents of all SPI registers are reset. The channels are controlled by the direct inputs IN[0:1] (if V_{PWR} is within the normal range). Since the VPWR pin supplies the circuitry of the SPI, current sense and most of the protective functions (overtemperature, overcurrent, severe short-circuit, short to V_{PWR}, and OpenLoad detection circuitry), these faults are still detected and reported at the FSB pin. However, without V_{DD}, the SO pin is no longer functional. The SPI registers can no longer be read and detailed fault information is unavailable. Current sensing also becomes unavailable. If $V_{DD\_FAIL\_EN}$ wasn't set before V_{DD} was lost, the device remains SPI-controlled, even though the SPI registers can't be read. No current flows from the VPWR to the VDD pin.

6.2.2.2 V_{PWR} supply voltage out of range

In case V_{PWR} is below the undervoltage threshold $V_{PWR(UV)}$, it is still possible to address the device by the SPI port, provided V_{DD} is within the normal range. It does not prevent other devices from operating when a device is part of a daisy-chain. To accomplish this, RSTB must be kept at logic [1]. When the device operates at supply voltages above the maximum supply voltage (V_{PWR}=36 V), SPI communication is not affected (see Overvoltage detection (enabled by default)). The internal pull-up and pull-down current sources on the SPI pins are not operational. Executing a Power-on-Reset (POR) sequence is recommended when V_{PWR} re-enters its authorized range. No current flows from the VDD to the VPWR pin.

6.2.2.3 Loss of V_{PWR}, loss of V_{DD}, and power-on reset (POR)

In typical applications (Figure 23 and Figure 24), an external voltage regulator may be used to derive V_{DD} from V_{PWR}. In wake mode, a Power-on-Reset (POR) sequence is executed and the POR bit (OD6 of the STATR register) is set when:

- $V_{PWR} > V_{PWR\ (POR)}$, after a period $V_{PWR} < V_{PWR\ (POR)}$ (and $V_{DD} < V_{DD\ (POR)}$ before and after)
- $V_{DD} > V_{DD\ (POR)}$ after a period with $V_{DD} < V_{DD\ (POR)}$ ($V_{PWR} < V_{PWR\ (POR)}$ before and after)

POR is also set at the transition to wake-up (by setting RSTB =1 or IN[x]=1) when $V_{PWR} > V_{PWR\ (POR)}$ (before and after) or $V_{DD} > V_{DD(POR)}$ (before and after). POR is not performed when $V_{PWR} > V_{PWR\ (POR)}$ after a period $V_{PWR} < V_{PWR\ (POR)}$ (and $V_{DD} > V_{DD\ (POR)}$ permanently).

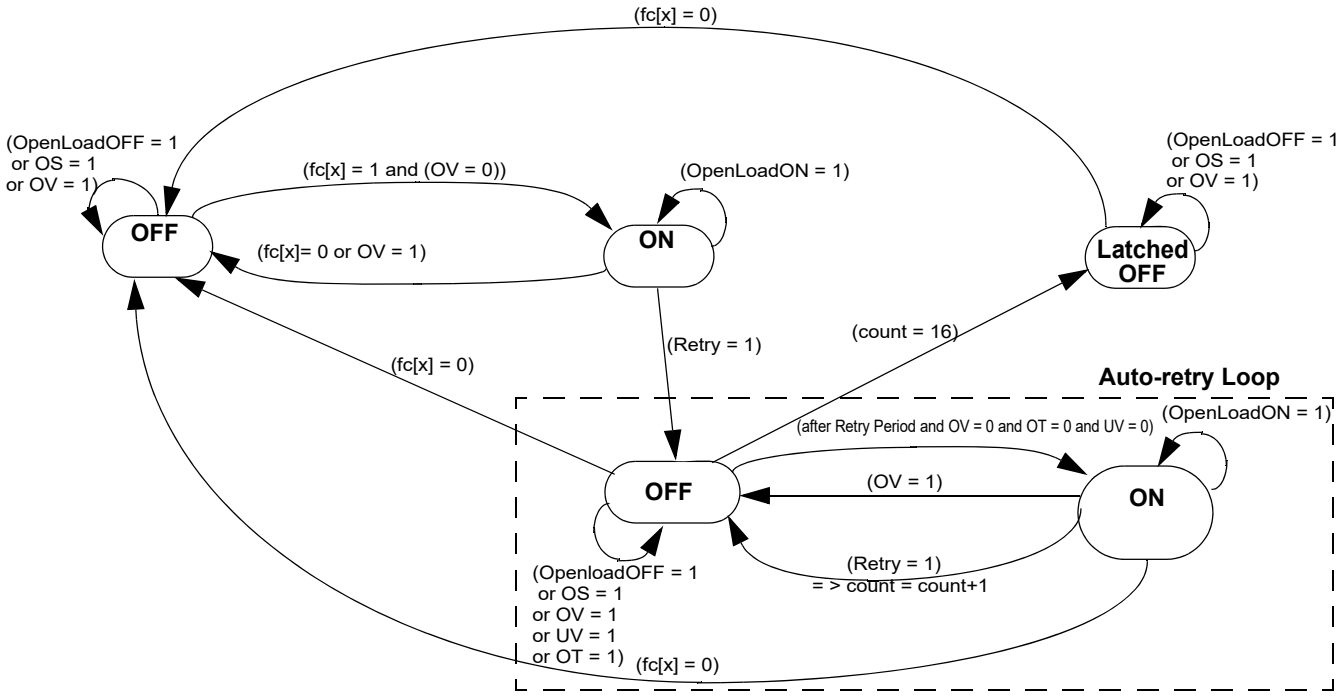

Figure 18. State machine: fault occurrence and auto-retry

6.2.3 Auto-retry

The auto-retry circuitry automatically tries to turn on the channel on a cyclic basis. Only faults of the latchable type (overcurrent, severe short-circuit, overtemperature (OT), and undervoltage (UV)) may activate auto-retry. For UV and OT faults, auto-retry only starts after disappearance of the failure cause (when auto-retry is enabled). The retry condition is expressed by:

Retry[x] = OC[x] or SC[x] or OT[x] or UV.

If Auto-retry has been enabled, its mode of operation depends on the settings of the auto-retry related bits (bits D0...D3 of the SI-RETRY_s register, see Table 12) and the available amount of auto-retries (bits OD7...OD4 of the SO-RETRY_s reg.). More details can be found in Amount of auto-retries.

If Auto-retry is disabled, latchable faults are immediately latched upon their occurrence (see Protection and diagnostic features).

6.2.3.1 Auto-retry configuration

To enable the auto-retry function, bit retry_s (D0 of the SI RETRY_s register) has to be set to the appropriate value. Auto-retry is enabled for retry_s = 0 when the channel is configured for lighting applications (CONF=0). It is enabled for retry_s=1 for DC motor applications (CONF[x] =1).

Table 10. Auto-retry activation for lamps (CONF=0) and DC motors (CONF=1)

CONF[x]	Retry_s bit	auto-retry
0	0	enabled
0	1	disabled
1	0	disabled
1	1	enabled

If auto-retry is enabled, an auto-retry sequence starts when the channel's fault control signal is set to 1 (fc[x] = 1, see Fault delatching) and the retry condition applies (Retry[x]=1, see Auto-retry).

When a failure occurs (fault = 1), the channel automatically switches on again after the auto-retry period. The value of this period (t_{AUTO}) is set through the SPI port (bits D2 and D3 of the RETRY_s register, see Table 22). When the failure cause disappears before expiration of the available amount of auto-retries, the device behaves normally (FSB = 1), but the retry counter keeps its current value and the fault bit remains set until it is cleared. This guarantees a maximum device availability without preventing fault detection.

6.2.3.2 Amount of auto-retries

In case the device is configured for an unlimited amount of auto-retries (Retry_unlimited_s = 1), auto-retry continues as long as the device remains powered. The channel never latches off.

In case a limited amount of retries was selected (Retry-unlimited_s = 0), auto-retry continues as long as the value of the 4-bit auto-retry counter does not exceed 15 (bits OD4...OD7 of the RETRY_s register). After 15 retries, the Rfull bit of the STATR (OD4 for channel 0, OD5 for channel 1) register is set to a logic high. The amount of available auto-retries is then reduced to one. If the fault still hasn't disappeared at the next retry, the corresponding channel is switched off definitively and the fault is latched (FSB = 0, see Protection and diagnostic features and Fault delatching).

Any channel can be turned on at any moment during the auto-retry cycle by performing a delatch sequence. However, this does not reset the retry counter.

The value of the auto-retry counter can be read back in Normal mode only (SO-RETRYR register bits OD7-OD4).

6.2.3.3 Reset of the auto-retry counter

Any one of the below events reset the retry counter:

- Fail-safe is entered (Fail-safe mode)
- Sleep mode is left (Sleep mode)
- POR occurs (Supply voltages out of range)
- the retry function is set to unlimited (bit Retry-unlimited_s = 1 (D1 = 1))
- the retry function is disabled (retry_s bit= D0 of the RETRY_s register under goes a 1-0 transition for CONF = 1 and a 0-1 transition for CONF = 0).

If the channel is latched at the moment the auto-retry counter was reset (case 4), the channel is delatched, and turned on after one retry period (if retry was enabled).

6.2.3.4 Auto-retry and overcurrent duration

During the on-period following an auto-retry, the load current profile is compared to the length and height of the selected overcurrent threshold profile, as described in the section on overcurrent protection (See Overcurrent fault (Latchable fault)).

When the lighting profile is activated, the overcurrent duration counter is reset at each auto-retry (to allow sustaining new inrush currents).

For DC motor mode however, it is only reset at the turn-off event of the first PWM period without any overcurrent (see Reset of the duration counter). Figure 18 gives a description of the retry state machine with the various transitions between operating modes.

6.2.4 Diagnostic features

Diagnostic functions openload-in-ON state (OLON), openload-in-OFF state (OLOFF) and output short-circuited to V_{PWR} (OS) are operational over the frequency and duty cycle ranges specified in Table 5 for PWM mode, but the precise values also depend on the way the device is controlled (direct/internal PWM), on the current sense ratio and on the optional activation of the openload-in-ON state detection. As an example, in direct input (DIR_dis_s = 0), Low-Current mode (CSR1), OLON, OLOFF and OS detection are performed for duty cycle values up to: RPWM_400_h = 85% (instead of 90%) when openload in ON state detection is enabled (OLON_dis=0).

Occurrence of an OLON, OLOFF or OS fault sets the associated bit in the FAULTR_s register but does not trigger automatic turn-off. Any of these diagnostic functions can be disabled by setting OLON_dis_s=1, OLOFF_dis_s=1, or OS_dis_s=1 (bits D8...D6 of the CONFR reg.).

The functions are guaranteed over the specified ranges for output capacitor values up to 22 nF (+/-20%).

6.2.4.1 Output shorted-to-V_{PWR} fault

The device detects short-circuits between the output and VPWR. The detection is performed during the OFF state. The output-shorted-to-VPWR fault-bit (OS_s) is set whenever the output voltage rises above $V_{OSD(THRES)}$. The fault is reported in real time on the FSB pin and saved by the OS_s bit. Occurrence of this fault does not trigger automatic turn-off.

Even if the short-circuit disappears, the OS_s bit is not cleared until the FAULTR register is read. The function may be disabled by setting OS_dis_s=1. The function operates over the duty cycle ranges specified in Diagnostic features.

This type of event shall be limited to 1000 min. during the vehicle lifetime. In case of permanent output shorted to the battery condition, it is needed to turn-on the corresponding channel.

6.2.4.2 Openload detection in OFF state

Openload-in-OFF state detection (OL_OFF) is performed continuously during each OFF state (both for CSR0 and CSR1). This function is implemented by injecting a small current into the load ($I_{OLD(OFF)}$). When the load is disconnected, the output voltage rises above $V_{OLD(THRES)}$. OL_OFF is then detected and the OL_OFF bit in the FAULTR register is set. If disappearance of the openload fault is detected, the FSB output pin returns to a high immediately, but the OL_OFF bit in the fault register remains set until it is cleared by a read out of the FAULTR register. The function may be disabled by setting OLOFF_dis_s=1. The function operates over the duty cycle ranges specified in Diagnostic features.

6.2.4.3 Openload detection in ON state (OL_ON)

Openload-in-ON state detection (OLON) is performed continuously during the ON state for CSR0 over the ranges specified in section Diagnostic features. An openload-in-ON state fault is detected when the load current is lower than the openload current threshold $I_{OLD(ON)}$. This happens at $I_{OLD(ON)}$ = 150 mA (typ.) for high current sense mode (CSR0), and at 7.0 mA (typ.) for low current mode. FSB is asserted low and the OLON bit in the fault register is set to 1 but the channel remains On. FSB goes high as soon as disappearance of the failure cause is detected, but the OL_ON bit remains set.

In high current mode (CSR0), openload-in-ON state detection is done continuously during the On state and the OLON-bit remains set even if the fault disappears.

In high current mode, the OLON-bit is cleared when the FAULTR register is read during the OFF state, even if the fault hasn't disappeared. The OLON-bit is also cleared when the FAULTR register is read during the ON state, provided the failure cause (load disconnected) has disappeared.

In low current mode (CSR1), OL_ON is done periodically instead of continuously and only operates when fast slew rate is selected. When the internal PWM module is used with an internal or external clock (case 1), the period is 150 ms (typ.). When the direct inputs are used (case 2), the period is that of the input signal. The detection instants in both cases are given by the following:

1. In ***internal PWM (int./ext. clock)****, low current mode (CSR1)*, OpenLoad in ON state detection is not performed each switching period, but at a fixed frequency of about 7.0 Hz (each t_{OLLED} =150 ms typ.). The function is available for a duty cycle of 100%.
   OLON detection is also performed at 7.0 Hz, at the first turn-off event occurring 150 ms after the previous OL_ON detection event (before OS and OL_OFF).
2. In ***direct input****, low current mode (CSR1)*, OL_ON is performed each switching period (at the turn-off instant) but the duty cycle is restricted to the values. Consequently, when the signal on the IN[x] pin has a duty cycle of 100%, OL_ON is not performed. To solve this problem, either the internal PWM function must be activated with a duty cycle of 100%, or the channel's direct input must be disabled by setting Dir_dis_s=1 (bit D5 of the CONFR-s register). The OLON-bit is only reset when the FAULTR register is read after occurrence of an OL_ON detection event without fault presence.

6.2.4.4 Openload detection in discontinuous conduction mode

If small inductive loads (solenoids/DC motors) are driven at low frequencies, discontinuous conduction mode may occur. Undesired openload in ON state errors may then be detected, as the inductor current needs some time to rise above the openload detection threshold after turn-on. This problem can be solved by increasing the switching frequency or by disabling the function and activating openload in OFF state detection instead.

When small DC motors are driven in discontinuous conduction mode, undesired openload in OFF state detection may also occur when the load current reaches 0.0 A during the OFF state. This problem can be solved by increasing the switching frequency or by enabling openload in OFF state detection only during a limited time, preferably directly after turn-off (see Diagnostic features). The signal on the SYNC pin can be used to identify the turn-off instant.

6.2.5 Current and temperature sensing

The scaled values of either of the output currents or the temperature of the device's GND pin (#14) can be made available at the CSNS pin. To monitor the current of a particular channel or the general device temperature, the CSNS0_en and CSNS1_en bits (see Table 23) in the General Configuration Register (GCR) must be set to the appropriate values. When overcurrent windows are active, current sensing is disabled and the SYNCB pin remains high.

6.2.5.1 Instantaneous and sampled current sensing

The device offers two possibilities for load current sensing: instantaneous (synchronous) sensing mode and track & hold mode (see Figure 9). In synchronous mode, the load current is mirrored through the current sense pin (Output current monitoring (CSNS)) and is therefore synchronous with it. After turn-off, the current sense pin does not output the channel current. In track & hold mode however, the current sense pin continues to mirror the load current as it was just before turn-off. Synchronous mode is activated by setting the T_H_en bit to 0, and Track & Hold mode by setting the T_H_en bit to 1.

6.2.5.2 Current sense ratio selection

The load current is mirrored through the CSNS pin with a sense ratio (Figure 19) selected by the CSNS_ratio bit in the OCR register. To achieve optimal accuracy at low current levels, the lower current sensing ratio, called CSR1, must be selected. In that case, the overcurrent threshold levels are decreased. The best accuracy that can be obtained for either ratio is shown in Figure 20. The amount of current the CSNS pin can sink is limited to $I_{CSNS,MAX}$. The CSNS pin must be connected to a pull-down resistor (470 Ω < R(CSNS) <10 kΩ, 1.0 kΩ typical), in order to generate a voltage output. A small low-pass filter can be used for filtering out switching transients (Figure 23). Current sensing operates for load currents up to the lower overcurrent threshold (OCLx A).

6.2.5.3 Synchronous current sensing mode

For activation of synchronous mode, T_H_en must be set to 0 (default). After turn-on, the CSNS output current accurately reflects the value of the channel's load current after the required settling time. From this moment on (CSNS valid), the SYNC pin goes low and remains low until a switch off signal (internal/external) is received. This allows synchronization of the device's current sensing feature with an external process running on a separate device (see Current sense synchronization (SYNC)). After turn-off, the load current does not flow through the switch, and the load current cannot be monitored.

6.2.5.4 Track & Hold current sensing mode

In Track & Hold mode (T&H) (T_H_en = 1), conversely from synchronous mode, the CSNS output current is available even after having switched off the load. This feature is useful when the device operates autonomously (internal clock/PWM), since it allows current monitoring without any synchronization of the device. An external sample and hold (S/H) capacitor is not required. After turn on, the CSNS output current reflects the channel's load current with the specified accuracy after occurrence of the negative edge on the SYNC pin, as in synchronous mode (see Current sense synchronization (SYNC)). However, at the switch-off instant, the last observed CSNS current is sampled and its value saved, thanks to an internal S/H capacitor. The SYNC pin goes high (SYNC = 1). If the channel on which Track & Hold current sensing is performed is changed to another, the internal S/H hold capacitor is first emptied and then charged again to allow current monitoring of the other channel. Consequently, T&H current monitoring of a channel is lost when this channel is in the OFF state at the moment the current is monitored on the other channel. Track & Hold mode should not be used for frequencies below 60 Hz.

When Track and Hold is used to sense the temperature and then to sense a current, the Track & Hold mode has to be reset by a turn off, then turn on before sensing a new current.

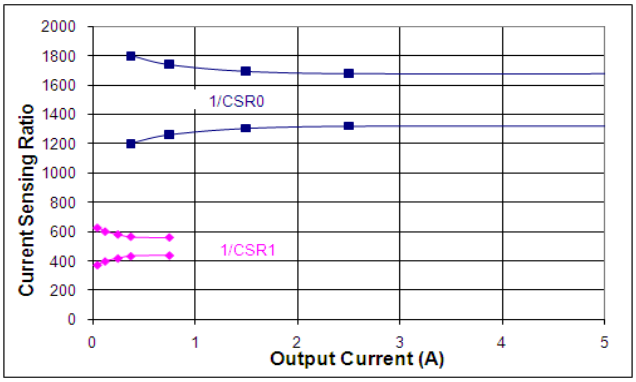

Figure 19. Current sensing ratio versus output current

6.2.5.5 Current sense errors

Current sense accuracy is adversely affected by errors of the internal circuitry's current sense ratio and offset. The value of the current sensing output current can be expressed with sufficient accuracy by the following equation:

$$I_{CSNS} = (I(HS[x]) + I_{\_LOAD\_ERR\_SYS} + I_{\_LOAD\_Err\_RAND}) * C_{SRx} \quad (1)$$

with $C_{SR0} = (1/1500+\varepsilon_{GAIN0})$ and $C_{SR1} = (1/500+\varepsilon_{GAIN1})$.

The device's offset error has a "systematic" and a "random" component ($I_{\_LOAD\_ERR\_SYS}$, $I_{\_LOAD\_ERR\_RAND}$). At low current levels, the random offset error may become dominant. The systematic offset error is caused by predictable variations with supply voltage and temperature, and has a small but positive value with small spread. The random offset error is a randomly distributed parameter with an average value of zero, but with high spread. The random offset error is subject to part-to-part variations and also depends on the values of supply voltage and device temperature. The device has a special feature called offset compensation, allowing an almost complete compensation of the random offset error (see E_{SR0_ERR}). This offset compensation technique greatly minimizes this error. Computing the compensated current sensing value is illustrated in the next sections.

6.2.5.6 Activation and use of offset compensation

According to the settings of the OFP_s bit (in the RETRYR_s register), opposite values of the random offset error are generated. To compensate the random offset error, two separate measurements with opposite values of the random offset error are required. The measured values must be saved by an external µ-processor. Compensation of the random offset error is achieved by computing the average of both. When a dedicated bit called Offset Positive (OFP = bit D8 of the RETRYR_s register) is set to 1, the current sunk through the CSNS pin (I_{CSNS}) can be described by:

$$I_{CSNS1} = CSR_x * (I_{LOAD} + I_{\_LOAD\_ERR\_SYS} + I_{\_LOAD\_ERR\_RAND}) \quad (2)$$

When bit OFP is set to 0, I_{CSNS} can be described by:

$$I_{CSNS2} = CSR_x * (I_{LOAD} + I_{\_LOAD\_ERR\_SYS} - I_{\_LOAD\_ERR\_RAND}) \quad (3)$$

The random offset term $I_{\_LOAD\_ERR\_RAND}$ can be computed from equations (2) and (3) as follows:

$$I_{\_LOAD\_ERR\_RAND} = (I_{CSNS1} - I_{CSNS2}) / (2*CSR_x) \quad (4)$$

The compensated current sense value $I_{CSNS,COMP}$ can be obtained by computing the average value of measurements I_{CSNS1} and I_{CSNS2} as follows:

$$I_{CSNS,COMP} = (I_{CSNS1} + I_{CSNS2}) / 2 \quad (5)$$

When equations 2 and 3 are substituted in equation 5, the random offset error cancels out, as shows eq. 6:

$$I_{CSNS,COMP} = (I_{\_LOAD\_ERR\_SYS} + I_{LOAD}) * CSR_x \quad (6)$$

The systematic offset error $I_{\_LOAD\_ERR\_SYS}$ is referenced at the operating point 28 V and 25 °C. It can eventually be fine tuned by performing a calibration. Gain errors at 25 °C (=current sense ratio errors, represented by ε_{GAIN0} and ε_{Gain1}) can also be reduced by performing a calibration at a point in the range of interest. If calibration can not be done, it is recommended to use the typical value of $I_{\_LOAD\_ERR\_SYS}$ (see E_{SR0_ERR}).

6.2.5.7 Current sense error model

The figures of uncompensated and compensated current sense accuracy mentioned in Table 4 have been obtained applying the error model of eq. 7 to the data:

$$I_{CSNS\_MODEL} = (I(HS[x]) + I_{\_LOAD\_ERR\_SYS}) * C_{SRx} \quad (7)$$

$$E_{SRx\_ERR} = (I_{CSNS1} - I_{CSNS\_MODEL})/I_{CSNS\_MODEL} \quad (8)$$

$$E_{SRx\_ERR(COMP)} = (I_{CSNS,COMP} - I_{CSNS\_MODEL})/I_{CSNS\_MODEL} \quad (9)$$

The computation has been applied to each of the specified measurement points. Model parameters $I_{\_LOAD\_ERR\_SYS}$ and C_{SRx} have the nominal values, specified in E_{SR0_ERR}.

The load current can be computed from this model as:

$$I(HS[x]) = I_{CSNS} / CSR_x - I_{\_LOAD\_ERR\_SYS} \quad (10)$$

$$I(HS[x]) = I_{CSNS,COMP} / CSR_x - I_{\_LOAD\_ERR\_SYS} \quad (11)$$

Using expression (11) generally gives more accurate values than expression (10), since in expression (11), random offset errors have been compensated.

6.2.5.8 Offset compensation in Track & Hold mode

In Track & Hold mode, the last observed sense current (I_{CSNS}) is sampled at the switch off instant. This takes into account the currently active settings of the OFP_s offset compensation bit. Changing the value of the OFP bit during the switch's off time produces an identical value of the current sense output. Consequently, to implement the before mentioned offset compensation technique, the channel must have been turned on at least once prior to sensing the output current with an opposite value of the OFP bit.

6.2.5.9 System requirements for current monitoring

Current monitoring is usually implemented by reading the (RC-filtered) voltage across the pull-down resistor connected between the CSNS pin and GND (Figure 23). Therefore, measurements (1) and (2) must be spaced sufficiently wide apart (e.g. 5 time constants) to get stabilized values, but close enough to be sure that the offset value wasn't changed. The A/D converter of the external micro controller that is used to read the current sense voltage V(csns) must have sufficient resolution to avoid introducing additional errors.

6.2.5.10 Accuracy with and without offset compensation

The sensing accuracy for CSR0 and CSR1, obtained before and after offset compensation, is shown in Figure 20 (solid lines = full scale accuracy with offset compensation and dotted lines without offset compensation).

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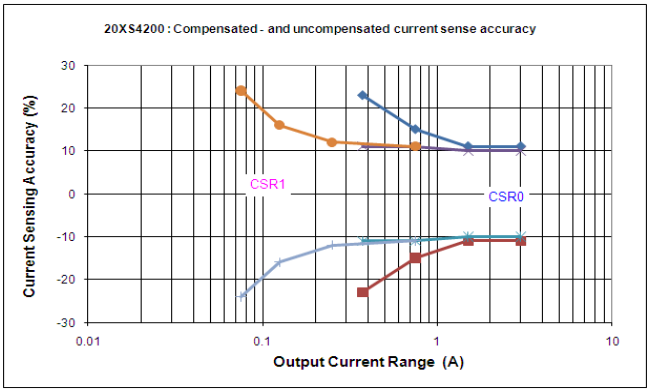


Figure 20. Current sense accuracy versus output current

In Track & Hold mode, the accuracy of the current sense function is lowered according to the values shown in Figure 21 (error percentage as a function of the switch-off time is displayed, for CSR0 and CSR1). Track & Hold mode shouldn't be used below f= 60 Hz.

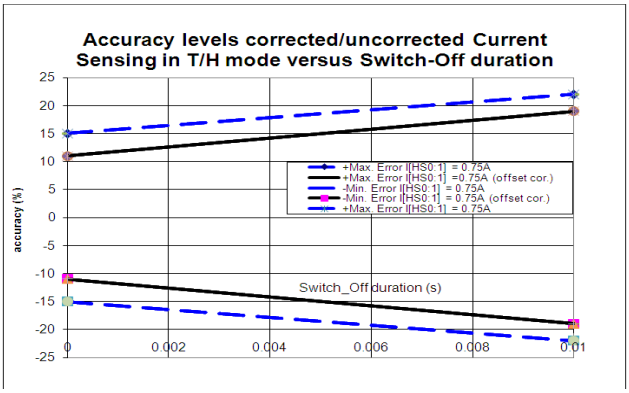


Figure 21. Track and Hold current sense accuracy

6.2.5.11 Temperature prewarning detection

In Normal mode, the temperature prewarning (OTW) bit is set (bit OD8 of the FAULTR register) when the observed temperature of the GND pin is higher than T_{OTWAR} (pin #14, see Figure 3). The feature is useful when the temperature of the direct surroundings of the device must be monitored. However, the channel isn't switched off. To be able to reset the OTW-bit, the FAULTR register must be read after the moment that temperature T °C < T_{OTWAR}.

6.2.5.12 Switching state monitoring

The switching state (ON/OFF) of the channels is reported in real time by bits OUT[x] in the STATR register (bit OD0/OD1). The Out[x] bit is asserted logic high when the channel is on (output voltage V(HS[x]) higher than V_{PWR} /2). When supply voltage V_{PWR} drops below 13 V, the reported channel state may not correspond to the state of the channel's control signal hson[x] in case of an openload fault (see Factors determining the channel's switching state).

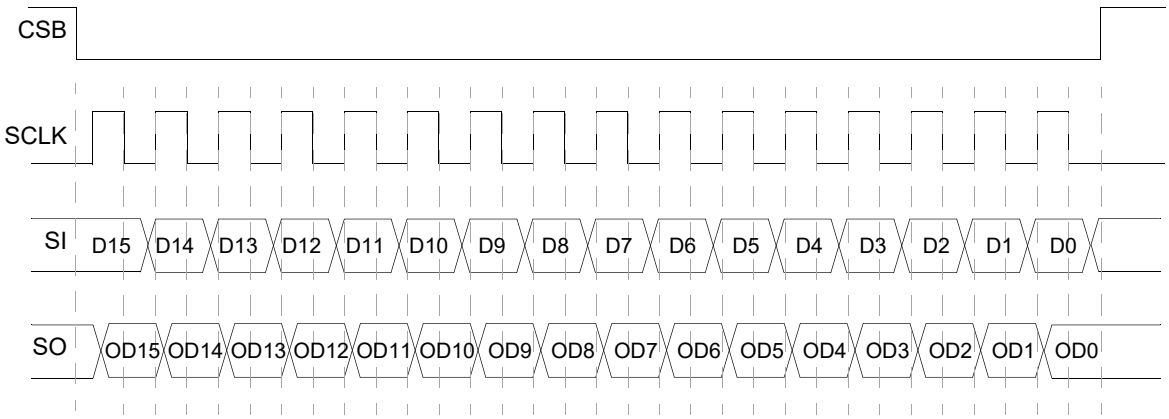
6.2.6 EMC Performances

Specified EMC performance is board and module dependent and applies to a typical application (Figure 23). The device withstands transients per ISO 7637-2 /24 V. An external freewheeling diode connected to at least one output is required for sustaining ISO 7637 Pulse 1 (-600 V). To withstand Pulse 2, at least one of the two channels must be connected to a typical load (bulb). It withstands electric fields up to 200 V/m and Bulk Current Injection (BCI) up to 200 mA per ISO11452.

6.3 Logic commands and SPI registers

6.3.1 SPI protocol description

The SPI interface offers full duplex, synchronous data transfer over four I/O lines: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select (CSB).The SI/SO pins of the device follow a first-in first-out (D15 to D0) protocol. Transfer of input and output words starts with the most significant bit (MSB). All inputs are compatible with 5.0 or 3.3 V CMOS logic levels. Parity check is performed after transfer of each 16-bit SPI data word.The SPI interface can be driven without series resistors provided that voltage ratings on VDD and SPI pins (Table 3) aren't exceeded. Unused SPI pins must be tied to GND, eventually by resistors (see Device ground loss).



Notes 1. $\overline{\text{RSTB}}$ must be in a logic [1] state during data transfer.
2. Data enter the SI pin starting with D15 (MSB) and ending with bit D0.
3. Data are available on the SO pin starting with bit 0D15 (MSB) and ending with bit 0(OD0).

Figure 22. 16-bit SPI interface timing diagram

6.3.2 Serial input communication protocol

SPI communication requires that RSTB = high. SPI communication is accomplished with 16-bit messages. A valid message must start with the MSB (D15) and end with the LSB (D0) (Table 11). Incoming messages are interpreted according to Table 12. The MSB, D15, is the watchdog bit (WDIN). Bit D14, Parity check (P), must be set such that the total number of 1-bits in the SPI word is even (P=0 for an even number of 1-bits and P=1 for an odd number). Bank selection is done by setting bit D13. Bits D12:D10 are used for register addressing. The remaining ten bits, D9:D0, are used to configure the device and activate diagnostic and protective functions. Multiple messages can be transmitted for applications with daisy chaining (or to validate already transmitted data) by keeping the CSB pin at logic 0. Messages with a length different from a multiple of 16 or with a parity error is ignored. The device has thirteen input registers for device configuration and thirteen output registers containing the fault/device status and settings. Table 12 gives the SI register function assignment. Bit names with extension "_s" refer to functions that have been implemented independently for each of both channels.

6.3.3 Serial port operation

When Chip Select occurs (1-to-0 transition on the CSB pin), the output register data is clocked out of the SO pin (MSB-first) at the serial clock frequency (SLCK). Bits at the SI pin are clocked in at the same time. The first sixteen SO register bits are those addressed by the previous SI word (bit D13, D2…D0 of the STATR_s input register). At the end of the chip select event (0-to-1 transition), the SI register contents are latched. The second SPI word clocked out of the Serial Output (SO) after the first CSB event represents the initial SO register contents. This allows daisy chaining and data integrity verification.

The message length is validated at the end of the CSB event (0-to-1 transition). If it is valid (multiples of 16, no parity error), the data is latched into the selected register. After latch-in, the SO pin is tri-stated and the status register is updated with the latest fault status information.

6.3.3.1 Daisy chain operation

Daisy-chaining propagates commands through devices connected in series. The commands enter the device at the SI pin and leave it by the SO pin, delayed by one command cycle of 16 bits. To address a particular device in a daisy chain, the CSB pin of all the devices in that chain has to be kept low until the SPI message has arrived at its destination. Once the command has been clocked in by the addressed device, it can be executed by setting CSB=1.

Table 11. SI message bit assignment

Bit n°	SI Reg. Bit	Bit functional description
MSB . . . LSB	D15	Watchdog in (WDIN): state must be alternated at least once within the timeout period
	D14	Parity (P) check. P-bit must be set to 0 for an even number of 1-bits and to 1 for an odd number
	D13	Selection between SI registers from bank 0 (0= channel 0) and bank 1 (Table 14)
	D12:D10	Register address bits
	D9:D0	Used to configure the device and the protective functions and to address the SO registers

Table 12. Serial input register addresses and function assignment

SI Register	SI Data														
	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STATR_s	WDIN	P	A_0	0	0	0	0	0	0	0	0	0	0	SOA2	SOA1	SOA0
PWMR_s	WDIN	P	A_0	0	0	1	0	ON_s	PWM7_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR_s	WDIN	P	A_0	0	1	0	0	OS_dis_s	OLON_dis_s	OLOFF_dis_s	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
OCR_s	WDIN	P	A_0	1	0	0	0	HOCR_s	PR_s	Clock_int_s	CSNS_ratio_s	t_{OCH_s}	tOCM_s	OCH_s	OCM_s	OCL_s
RETRY_s	WDIN	P	A_0	1	0	1	0	OFP_s	0	0	0	(48)	Auto_period1_s	Auto_period0_s	Retry_unlimited_s	retry_s
GCR	WDIN	P	0	1	1	0	0	PWM_en_1	PWM_en_0	PARALLEL	T_H_en	WD_dis	$V_{DD\_FAIL\_en}$	CSNS1_en	CSNS0_en	OV_dis
CALR_s	WDIN	P	A_0	1	1	1	0	1	0	1	0	1	1	0	1	1
contents after reset*	0	X	0	X	X	X	0	0	0	0**	0	0	0	0	0	0

* = RSTB = 0 or V_{DD}(FAIL) after V_{DD} = 5.0 V or POR
** = except bit D6 (PARALLEL) of the GCR register that is saved when V_{DD}(FAIL) occurs, provided V_{DD} = 5.0 V and $V_{DD\_FAIL\_EN}$ = 1 before
X = register address, P = parity bit

Notes

48. Bit D4 of RETRY_s Serial Input register
MC20XS4200FK = 0
MC20XS4200BFK and MC20XS4200DFK,MC20XS4200BAFK and MC20XS4200BDFK=CONF_SPI_s
Setting bit D4 to 0 (CONF_SPI_s=0) will configure the overcurrent profile as the CONF pin.
Setting bit D4 to 1 (CONF_SPI_s=1) will configure the overcurrent profile as the opposite of CONF pin.
After device reset, the overcurrent profile is defined by the CONF input pin. The SPI-SO CONF bit reporting shall combine external hardware configuration and SPI setting.

Table 13. Serial output register bit assignment

	bits D13, D2, D1, D0 of the Previous STATR				SO Returned Data														
	SOA3	**SOA2**	**SOA1**	**SOA0**	**OD15**	**OD14**	**OD13**	**OD12**	**OD11**	**OD10**	**OD9**	**OD8**	**OD7**	**OD6**	**OD5**	**OD4**	**OD3**	**OD2**	**OD1**	**OD0**
STATR	0	0	0	0	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	OV	UV	POR	R_FULL1	R_FULL0	FAULT1	FAULT0	OUT1	OUT0
FAULTR_s	A_0	0	0	1	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	OTW	0	0	OLON_s	OLOFF_s	OS_s	OT_s	SC_s	OC_s
PWMR_s	A_0	0	1	0	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	ON_s	PWM7_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR_s	A_0	0	1	1	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	OS_dis_s	OLON_dis_s	OLOFF_dis_s	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
OCR_s	A_0	1	0	0	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	HOCR_s	PR_s	Clock_int_s	CSNS_ratio_s	tOCH_s	tOCM_s	OCH_s	OCM_s	OCL_s
RETRYR_s	A_0	1	0	1	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	OFP	R3	R2	R1	R0	Auto_period1_s	Auto_period0_s	Retry_unlimited_s	retry_s
GCR	0	1	1	0	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	PWM_en_1	PWM_en_0	PARALLEL	T_H_en	WD_dis	VDD_Fail_en	CSNS1_en	CSNS0_en	OV_dis
DIAGR (49)	0	1	1	1	WDIN	PF	SOA3	SOA2	SOA1	SOA0	NM	CONF1	CONF0	ID1	ID0	IN1	IN0	CLOCK_fail	CAL_fail1	CAL_fail0
contents after reset or failure*	N/A	N/A	N/A	N/A	0	0	0	0	0	0	0	0	0	0**	0***	0	0	0	0	0

* = RSTB = 0 or V_{DD}(FAIL) after V_{DD} = 5.0 V, or POR
** = except bit D6 (PARALLEL) of the GCR register that is saved when V_{DD}(FAIL) occurs provided V_{DD} = 5.0 V and VDD_Fail_en = 1 before
*** = except bit D7 (POR) of the STATR register that is saved when V_{DD}(FAIL) occurs after V_{DD} = 5.0 V and VDD_Fail_en = 1 (fail-safe mode)
x = register address, PF = parity Fault

Notes
49. DIAGR Serial Output register bits D5 and D6 for product identification will report: MC20XS4200FK and MC20XS4200BFK and MC20XS4200DFK:01, MC20XS4200BAFK and MC20XS4200BDFK:00

6.3.4 SI register addressing

The address in the title of the following sections (A_0xxx) refer to bits D[13:10] of the SPI word required to address the associated SI register. Bit A_0 = D13 selects between registers of bank 0 and bank 1 (Table 14). The function assignment of register bits D[8:0] is described in the associated section. The "_s" behind a register name indicates that the variable applies to the register contents of both banks.

Table 14. Value of bit A_0 required for addressing register Banks 0 or 1

Value A_0 (D13)	Bank
0	0 = channel 0 (default)
1	1 = channel 1

6.3.5 Address $A_0$000—Status register (STATR_s)

To read back the contents of any of the 13 SO registers, bits D[13:10] of the channel's SI STATR register must be set to $A_0$000 and bits D[2:0] in the same SPI word to the address of the desired SO register. The SO registers thus addressed are: STATR, FAULTR_s, PWMR_s, CONFR_s, OCR_s, RETRY_s, GCR, and DIAGR (Table 13).

6.3.6 Address $A_0$001— PWM control register (PWMR_s)

The PWMR_s register contents determines the value of the PWM duty cycle at the output (Table 12), both for internal and external clock signals.

Bit D8 must be set to 1 to activate this function. The desired value of duty cycle is obtained by setting Bits D7:D0 to one of the 256 levels as shown in Table 7.To start the PWM function at a known point in time, the PWM_en_s bit (both in the GCR register) must be set to 1.

6.3.7 Address $A_0$010—Channel configuration register (CONFR_s)

The CONFR_s is used to select the appropriate value of slew rate and turn-ON delay. The settings of Bits D[8:6] determine the activation of openload and short-circuit (to V_{PWR}) detection. Bit D13 (= A_0) of the incoming SPI word determines which of both CONFR registers is addressed (Table 14).

Setting bit D8 (OS_dis_s) to logic [1] disables detection of short-circuits between the channel's output pin and the VPWR pin. The default value [0] enables the feature.

Setting bit D7 (OLON_dis_s) to logic [1] disables detection of openload in the ON state for the selected channel. The default value [0] enables this feature (Table 15).

Setting bit D6 (OLOFF_dis_s) to logic [1] disables detection of openload in the OFF state. The default value [0] enables the feature, see Table 15.

Table 15. Selection of openload detection features

OLON_dis_s (D7: On state)	OLOFF_dis_s (D6: Off state)	Selected openload detection function
0	0	both enabled (default)
0	1	OFF state detection disabled
1	0	ON state detection disabled
1	1	Both disabled

Setting bit D5 (DIR_DIS_s) to logic [0] enables direct control of the selected channel. Setting bit D5 to logic [1] disables direct control. In that case, the channel state is determined by the settings of the internal PWM functions.

D4:D3 bits (SR1_s and SR0_s) control the slew rate at turn on and turn off (Table 16). The default value ([00]) corresponds to the medium slew rate. Rising and falling edge slew rates are identical.

Table 16. Slew rate selection

SR1_s (D4)	SR0_s (D3)	Slew rate
0	0	medium (default)
0	1	low
1	0	high
1	1	medium SR <SR< high SR

Delaying a channel's turn-on instant with respect to the other is accomplished by setting bits D2:D0 of the PWMR_s register to the appropriate values. Switch On is delayed by the number of (internal/external) clock periods shown in Table 8. Refer to the section Programmable PWM module.

6.3.8 Address $A_0$100— Overcurrent protection configuration register (OCR_s)

The contents of the OCR_s registers determines operation of overcurrent, current sensing, and PWM related functions. For each load type (bulb or DC motor), a different kind of overcurrent profile exists (see Overcurrent protection profile for bulb applications). For lighting mode, the overcurrent profile is defined by three different thresholds each of which is active over a dedicated time slot. These thresholds

are called the higher (=$I_{\_OCH}$), the middle (=$I_{\_OCM}$) and the lower (=$I_{\_OCL}$) threshold. The DC motor profile only has two thresholds ($I_{\_OCH}$ and $I_{\_OCL}$).

Each threshold can be set to two different values, except $I_{\_OCL}$ that can be set to three different values ($I_{\_OCL1}$, $I_{\_OCL2}$, $I_{\_OCL3}$). Setting the low-current sense ratio (CSR1) reduces the values of all the overcurrent thresholds by a factor of three. The terminology is defined as follows: $I_{\_OCxy\_z}$ stands for overcurrent threshold x (x=$I_{\_OCH}$, $I_{\_OCM}$ or $I_{\_OCL}$) that can be set to two or three different values, selected by y (y=1, 2, (or 3)). The previously selected current sense ratio (z=0 for CSR0 and z=1 for CSR1) further determines the shape of the applicable overcurrent protection profile (see I_OCH1_0).

Setting bit D8 (HOCR_s) to 0 activates overcurrent level $I_{\_OCL1}$, the highest of the 3 levels, regardless the value of the D0 bit. Setting HOCR to 1 activates the medium level $I_{\_OCL2}$ when D0 = 0, and the lowest level $I_{\_OCL3}$ when D0 = 1 (Table 21). When overcurrent windows are active, current sensing is not available.

Bit D7 (PR_s) controls which of two divider values are used to create the PWM frequency from the external clock. Setting bit D7 to 1 causes the external clock to be divided by 512. When PR_s = 0, the divider is 256.

Setting bit D6 (Clock_int_s) activates the internal clock of the selected channel. The default value [0] configures the PWM module to use an external clock signal.

Setting bit D5 (CSNS_ratio_s) to 1 activates the “low- current” current sense ratio CSR1, optimal for measuring currents in the lowest range. The default value [0] activates the “high-current” sensing ratio CSR0 (Table 17).

Table 17. Current sense ratio selection

CSNS_ratio_s (D5)	Current sense ratio
0	CRS0 (default)
1	CRS1

The width of the overcurrent protection window(s) is controlled by bits D4 and D3 (t_{OCH_s} and t_{OCM_s}), and also depends on the load type configuration as shown in Table 18. (CONF[x]=0: bulb, CONF[x]=1: DC motor).

The lighting profile has two adjacent windows the width of which is compatible with typical bulb inrush current profiles. The width of the first of these windows is either t_{OCH1} or t_{OCH2}. The width of the second window is either t_{OCM1_L} or t_{OCM2_L} (see Table 18).

The DC motor profile has one overcurrent window defined by two different thresholds ($I_{\_OCH}$ and $I_{\_OCL}$), as illustrated by Figure 6. In this case, the maximum overcurrent duration is selected among four values: t_{OCM1_M}, t_{OCM2_M}, t_{OCH1} and t_{OCH2}.

Table 18. Dynamic overcurrent threshold activation times for bulb and DC motor profiles

CONF[x]	t_{OCH_s} (D4)	t_{OCM_s} (D3)	Selected threshold activation times
0	0	0	t_{OCH1} and t_{OCM1_L}
0	0	1	t_{OCH1} and t_{OCM2_L}
0	1	0	t_{OCH2} and t_{OCM1_L}
0	1	1	t_{OCH2} and t_{OCM2_L}
1	0	0	t_{OCM1_M}
1	0	1	t_{OCM2_M}
1	1	0	t_{OCH1}
1	1	1	t_{OCH2}

Bit D2 (OCH_s) selects the value of the higher (upper) overcurrent threshold among two values. The default value [0] corresponds to the highest value, and [1] to the lowest value (Table 19).

Table 19. OCH upper current threshold selection

OCH_s (D2)	$I_{\_OCH}$ current threshold
0	$I_{\_OCH1\_s}$ (default)
1	$I_{\_OCH2\_s}$

Bit D1 (OCM_s) sets the value of the middle overcurrent threshold. The default value [0] corresponds to the highest value, and [1] to the lowest value (Table 20). In DC motor mode, there is no middle overcurrent threshold and the value of this bit has no influence.

Table 20. OCM current threshold selection

OCM_s (D1)	OCM current threshold
0	$I_{\_OCM1\_s}$ (default)
1	$I_{\_OCM2\_s}$

Bit D0 (OCL_s) and D8 (HOCR) set the value of the lowest overcurrent threshold, as shown in Table 21.

Table 21. OCL current threshold selection

HOCR (D8)	OCL_s (bit D0)	Selected OCL current level
0	0	$I_{\_OCL1\_x}$(default)
0	1	$I_{\_OCL1\_x}$
1	0	$I_{\_OCL2\_x}$
1	1	$I_{\_OCL3\_x}$

6.3.9 Address $A_0$101— Auto-retry register (RETRYR_s)

The RETRYR_s register contents are used to set the different auto-retry options (Auto-retry) and the offset compensation feature of the current sense function.

Setting bit D8 to 1(OFP = 1) causes the random offset current (and the overcurrent profile on the 20XS4200B) to be added to the sensed current (pin CSNS). Setting bit D8 to 0 results in the offset current being subtracted from the sensed current.

Setting D3 and D2 (Table 22) to the appropriate values allows selection of the value of the auto-retry period among four predefined values.

Table 22. Auto-retry period

Auto_period1_s (D3)	Auto_period0_s (D2)	Retry period
0	0	t_{AUTO_00} (default)
0	1	t_{AUTO_01}
1	0	t_{AUTO_10}
1	1	t_{AUTO_11}

Setting bit D1 to 1 (RETRY_unlimited_s = 1) results in an unlimited number of auto retries, provided the auto-retry function wasn't disabled.

Setting bit D1 to 0 (RETRY_unlimited_s = 0) limits the amount of auto retries to 16 (see Amount of auto-retries). The value of the counter neither resets after delatching, nor when the fault disappears.

Setting bit D0 (retry_s) enables or disable auto-retry, accordingly to setting of the CONF pin.

For CONF[x] = 0 (Lighting profile configured), setting retry_s = 1 disables auto-retry. The default value [0] enables it.

For CONF[x] = 1 (DC motor), setting retry_s = 1 enables auto-retry. The default value [0] disables it.

For details, see Table 12.

6.3.10 Address 0110—global configuration register (GCR)

The GCR register is used to activate various functions and diagnostic functions.

Setting bits D8 = 1 and D7 = 1 of the GCR register (PWM_en_1 and PWM_en_0) activates the internal PWM function of both channels simultaneously according to the values of duty cycle and turn-on delays in the PWMR_s and CONFR_s registers (Table 7). However, this option should never be used to drive channels in parallel. To increase the load current capability, the instructions in the section Parallel operation should be followed.

Setting bit D6 sets parallel mode (improved switching synchronization between both channels). Only configuration and diagnostic information of bank 0 (A_0 = 0) is available in this setting (see Parallel operation).

Setting Bit D5 (T_H_en = 1) activates Track & Hold current sensing mode. When T&H is activated, the value of the channel's load current is kept available after turn-off.

Setting bit D4 (WD_dis = 1) disables the SPI watchdog function. A logic [0] enables the SPI watchdog.

Setting bit D3 ($V_{DD\_FAIL\_EN}$ = 1) enables or disable the V_{DD} failure detection. When enabled, the device enters Fail-safe mode after V_{DD} < $V_{DD(FAIL)}$.

Bits D6 (parallel bit), D2 and D1 set the different (current) sensing options. The CSNS pin outputs a scaled value of the selected channel's load current, the sum of both currents or the die temperature, according to the values in Table 23. When the highest overcurrent range is selected (bit D8 of the OCR register, HOCR = 0), the device's CSNS pin only outputs scaled values of a single channel's load current.

Table 23. Current sense pin functionality selection

D8	D6	D2	D1	Activated function at CSNS pin
x	x	0	0	disabled
0	x	0	1	current sensing on channel 0
0	x	1	0	current sensing on channel 1
0	x	1	1	temperature sensing
1	0	0	1	current sensing on channel 0
1	x	1	0	current sensing on channel 1
1	x	1	1	temperature
1	1	0	1	current sensing summed currents of channels 0 and 1

Setting bit D0 (OV_dis = 1 of the GCR reg.) disables overvoltage protection. Setting this bit to [0] (default), enables it.

6.3.11 Address $A_0$111—Calibration register (CALR_s)

The internal clock frequency of both channels can be calibrated independently. Setting the appropriate calibration word in the CALR_s register (Table 12) puts the device in calibration mode. The default switching frequency is 400 Hz, but can be changed by applying a specific calibration procedure. See Internal clock and internal PWM (Clock_int_s bit = 1).

6.3.12 SO register addressing

The device has two register banks, each of which has five channel-specific SO registers containing the channel's configuration and diagnostics status (Table 13). These registers are FAULTR_s, PWMR_s, CONFR_s, OCR_s, and RETRYR_s.

Global fault and diagnostic information are contained in the following common SO-registers: STATR, GCR, and DIAGR. All the SO registers can be addressed by setting the appropriate bits in the SI-STATR_s register (bits D13, D2, D1, D0). The value of the bit D13 determines which register bank is addressed (bank 0 or 1). Data is made available the next cycle after register addressing.

The output status register correctly reflects the contents of the addressed SO register as long as CSB is low, except when the data from the previous SPI cycle was invalid. In this case, the device outputs the contents of the last successfully addressed SO register.

6.3.13 Serial output register assignment

The output register shifted out through the SO pin is previously addressed by bits D13, D2, D1, and D0 of the STATR_s SI register. Table 13 gives the functional assignment (OD15:OD0) of each of the thirteen SO register bits, preceded by the address of the SI STATR_s required to address it.

- Bit OD15 (MSB) reports the state of the watchdog bit from the previously clocked-in SPI message.
- Bit OD14 (PF, active 1) reports an eventual parity error on the previously transferred SI register contents.
- Bits OD13:OD10 echo the state of bits D13, D2, D1, and D0 (SOA3:SOA0) of the previously received SI word.
- Bit OD9: Normal mode (NM) reports the device state. In Normal mode, NM = 1.
- Bits OD8:OD0 are the contents of the selected SO register (addressed by bit D13 and bits D2:D0 of the previous SI STATR register).

6.3.14 Previous address SOA_3:SOA_0 = 0000 (STATR)

When bits SOA3…SOA0 of the previously received SI STATR_s register = 0000, the SO STATR register is addressed. Bits OD8:OD0 contain the relevant channel information: Faults, channel state, and supply voltage errors.

- Bits OD8:OD6 report failures common to both channels
- Bit OD8 = OV = 1: overvoltage fault
- Bit OD7 = UV = 1: undervoltage fault
- Bit OD6 = POR = 1: power-on reset (POR) has occurred

Power-ON-Reset occurs when V_{PWR}<$V_{SUPPLY(POR)}$. The OV, UV, and POR bits can be reset by a reading the STATR register.

Bits OD5:OD4 (R_{FULL}) of the STATR register are set to logic [1] when the auto-retry counter of the corresponding channel is full. These bits are automatically cleared by resetting the corresponding auto-retry counter (see Reset of the auto-retry counter)

Bits OD3 (FAULT1) and OD2 (FAULT0) are set to logic [1] when channel-specific (non-generic) faults are detected:

FAULTs = OC_s + SC_s + OT_s + OS_s + OLOFF_s + OLON_s.

The FAULTs bit can be reset by reading out the common STATR register or the individual FAULTR_s register (provided the fault has disappeared).

Bits OD1:OD0 (OUT1 and OUT0) report the channel's switching state (ON/OFF) in real time.

6.3.14.1 Previous address SOA_3:SOA_0 = $A_0$001 (FAULTR_s)

Bit OD8 of both Fault registers (FAULTR_s) is set simultaneously when the overtemperature prewarning (OTW) condition occurs, but the channels are not switched off (temperature of the common GND pin (#14)> T_{OTWAR}).

Reading either FAULT register clears both OTW bits.

Bits OD5:OD0 of the Fault register (FAULTR_s) report the faults that occurred on the channel previously selected by bit SOA3 = A_0 (Table 14).

- bit OD0 = OC_s: overcurrent fault on channel s,
- bit OD1 = SC_s: severe short-circuit on channel s,
- bit OD3 = OS_s: output shorted to V_{PWR} on channel s,
- bit OD4 = OLOFF_s: OpenLoad in OFF state on channel s,
- bit OD5 = OLON_s: OpenLoad in ON state on channel s. (The threshold value above which this fault is triggered depends on the selected current sense ratio; for CSR0 @ 150 mA typ. and for CSR1 @ 7.0 mA typ.).

The Fault Status pin (FSB) is set to 0 (active Low) upon occurrence of any of the above mentioned faults. Latched faults can only be delatched by the procedure described in Fault delatching.

The FAULTR_s register is reset when it is read out, provided that the failure cause has disappeared and latched faults have been delatched.

6.3.15 Previous address SOA_3:SOA_0 = $A_0$010 (PWMR_s)

The device outputs the contents of the addressed PWMR_s register (A_0 = 0 for bank 0 and A_0 = 1 for bank 1).

6.3.16 Previous address SOA_3:SOA_0 = $A_0$011 (CONFR_s)

The device outputs the contents of the addressed CONFR_s register (A_0 = 0 for bank 0 and A_0 = 1 for bank 1).

6.3.17 Previous address SOA_3:SOA_0 = $A_0$100 (OCR_s)

The device outputs the contents of the addressed OCR_s register (A_0 = 0 for bank 0 and A_0 = 1 for bank 1).

6.3.18 Previous address SOA_3:SOA_0 = $A_0$101 (RETRYR_s)

The device outputs the contents of the addressed RETRYR_s register (A_0 = 0 for bank 0 and A_0 = 1 for bank 1).

Bit OD8 contains the value of the OFP bit (offset positive), used for current sense offset compensation. Bits OD7:OD4 contain the real time value of the auto-retry counter. When these bits contain [0000], either auto-retry has not been enabled or Auto-retry did not occur.

6.3.19 Previous address $SOA_3:SOA_0$ = 0110 (GCR)

The device outputs the contents of the general configuration register (GCR) common to both channels.

6.3.20 Previous address $SOA_3:SOA_0$ = 0111 (DIAGR_s)

Bit OD8 (Ch. 1 = CONF1) and bit OD7 (Ch. 0 = CONF0) of the DIAGR_s register contain the values of the channels' configuration bits (0 = bulb, 1 = DC motor).

For 20XS4200FK, 20XS4200BFK, and 20XS4200DFK

- Bits OD6:OD5 contain the product identification (ID) number, equal to 01 for the present dual 20 mΩ product.

For 20XS4200BAFK and 20XS4200BDFK

- Bits OD6:OD5 contain the product identification (ID) number, equal to 00 for the present dual 20 mΩ product.

Bits OD4:OD3 report the logic state of the direct inputs IN[1:0] in real time (1 = On, 0 = OFF), OD4 = Ch. 1, OD3 = Ch. 0.

Bit OD2 reports a logic [1] in case an external clock error occurred (if an external clock was selected by Clock_int = 0).

Bit OD1:OD0 report logic [1] in case a calibration failure occurred during calibration of a channel's internal clock period.

7 Typical applications

Figure 23 shows the electrical circuit of a typical truck application. As an example, an external circuit is added that takes over load control in case Fail-safe mode is activated (FSOB goes low). This circuit allows keeping full control of both channels in case of SPI failure.

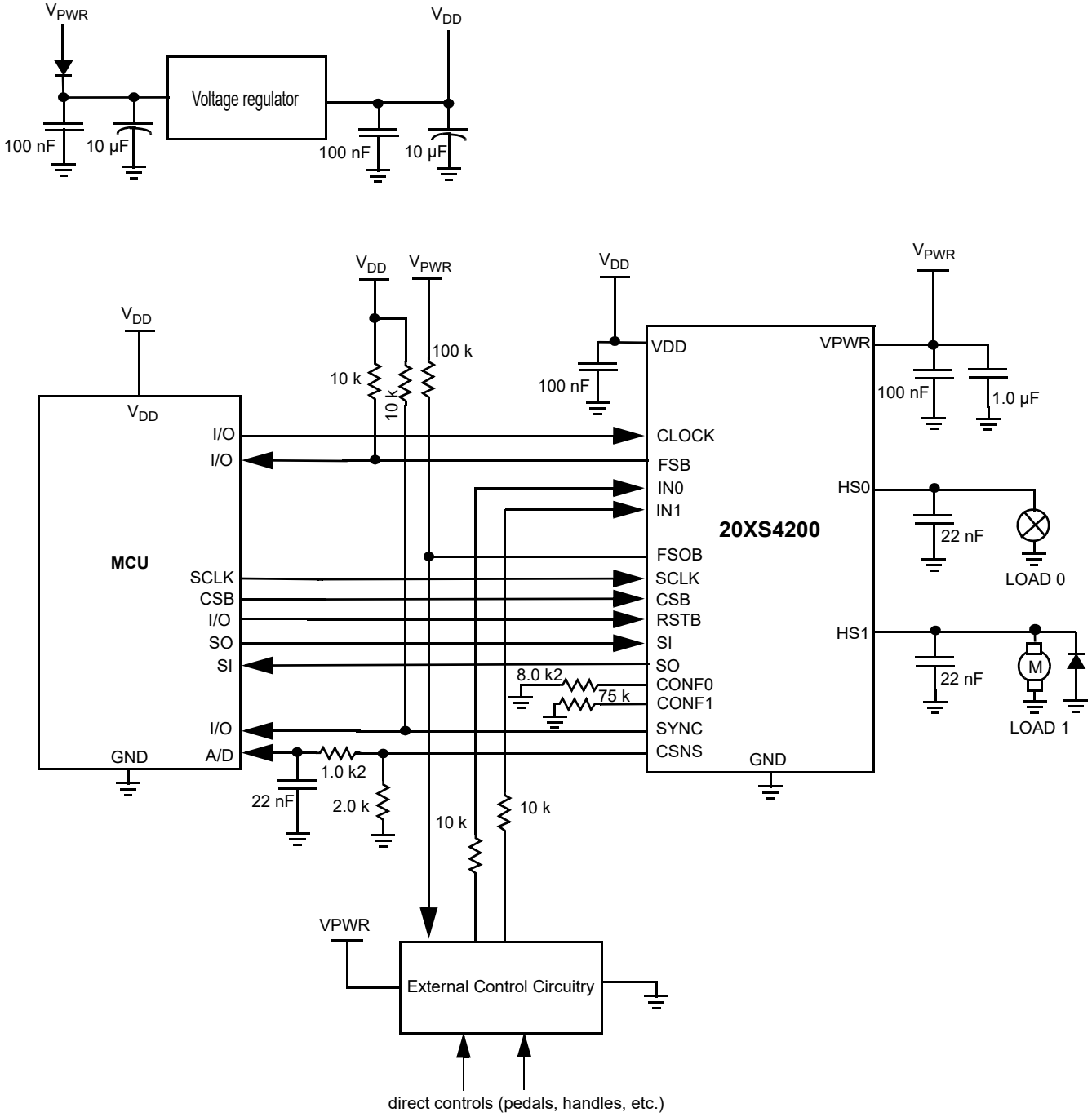


Figure 23. Typical application with two different load types

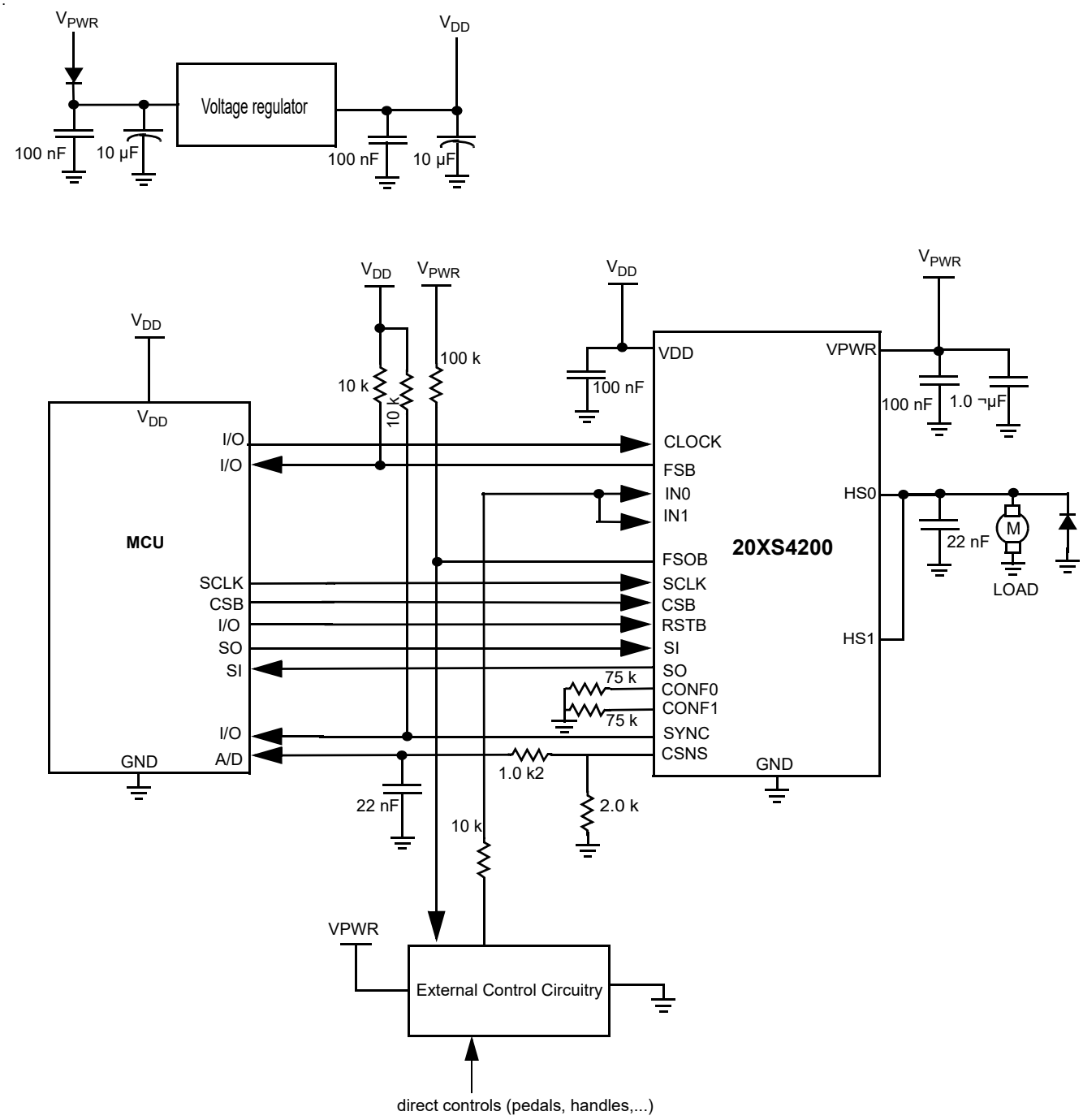


Figure 24. Two channels in parallel/recommended external current sense circuit

8 Packaging

8.1 Soldering information

The FK package is a surface mount power package (PQFN), intended to be soldered directly on the printed circuit board.

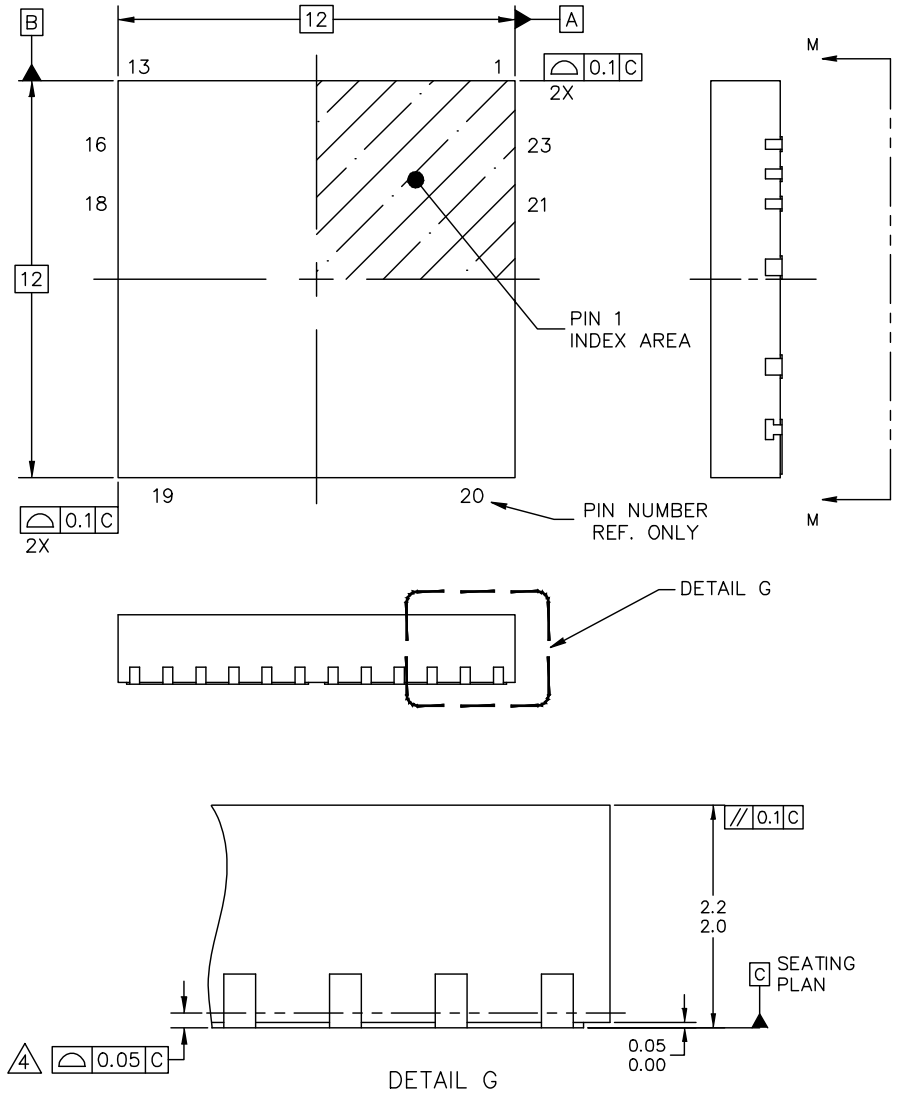
The AN2467 provides guidelines for Printed Circuit Board design and assembly.

8.2 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 24. Packaging information

Package	Suffix	Package outline drawing number
23-pin PQFN	FK	98ASA00428D



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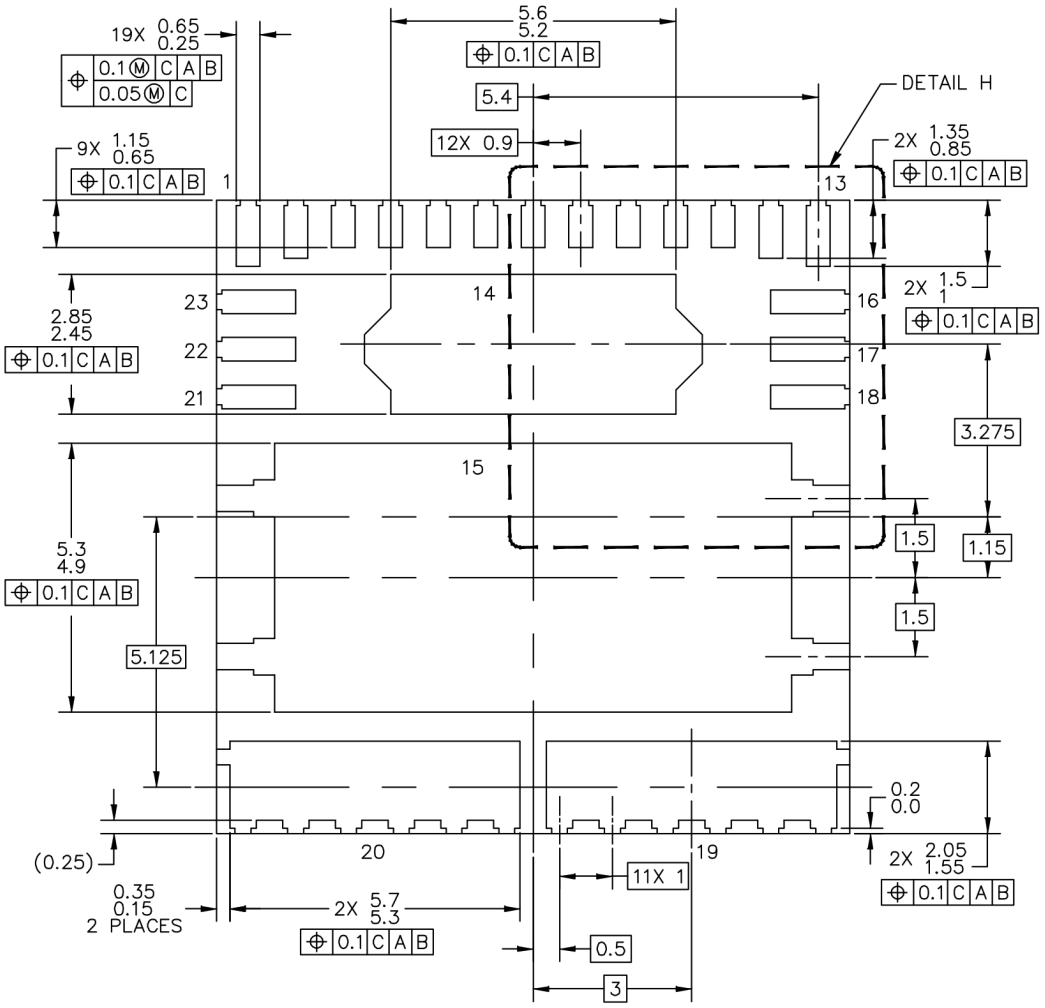
TITLE: PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	DOCUMENT NO: 98ASA00428D	REV: D
	STANDARD: NON-JEDEC	
	SOT1938-1	03 JUL 2018



VIEW M–M

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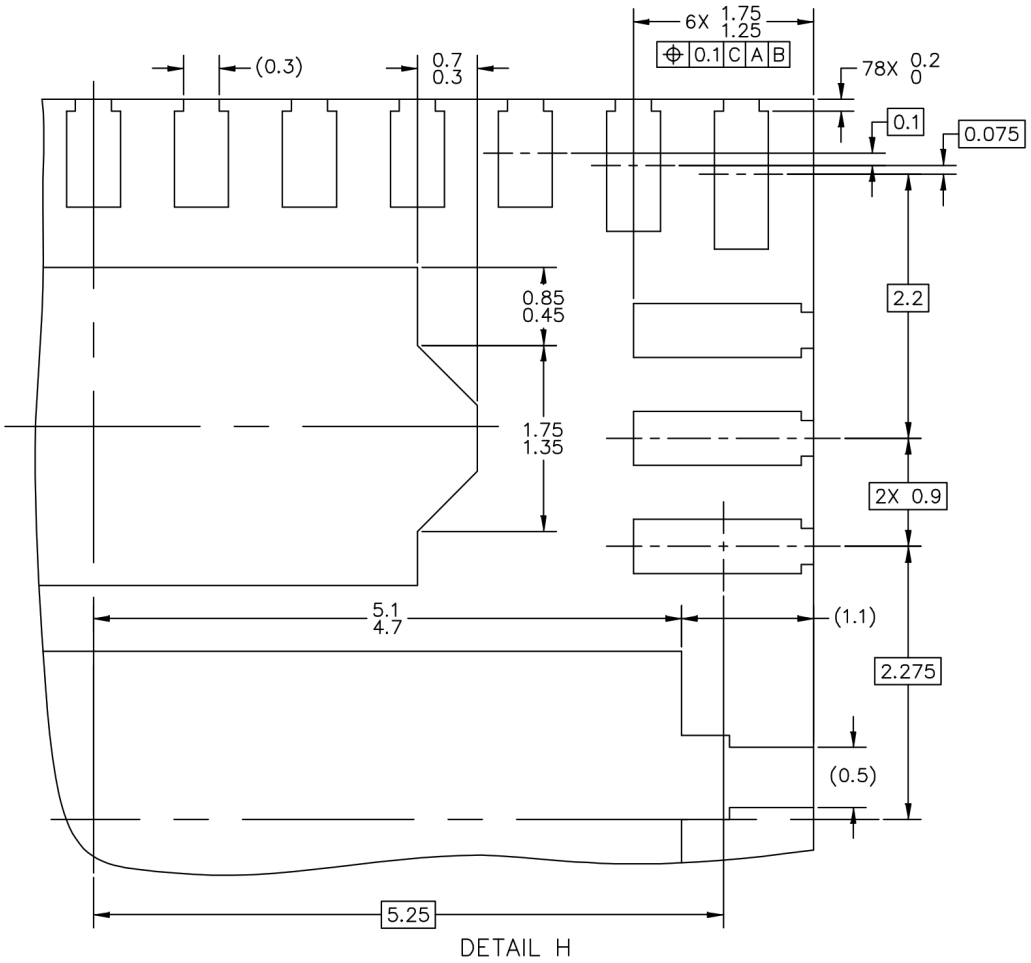
TITLE: PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	DOCUMENT NO: 98ASA00428D	REV: D
	STANDARD: NON–JEDEC	
	SOT1938–1	03 JUL 2018



DETAIL H

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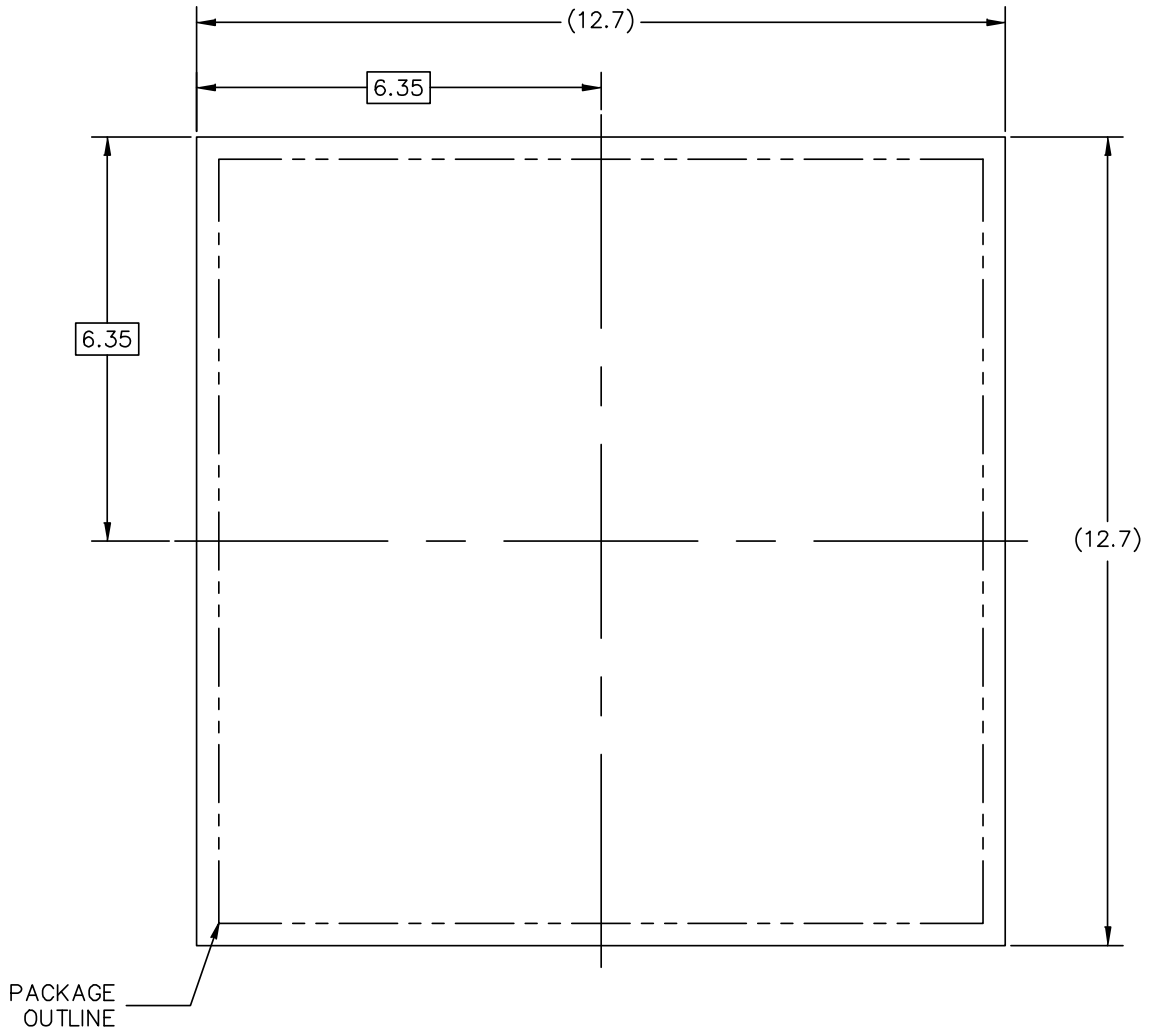
TITLE: PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	DOCUMENT NO: 98ASA00428D	REV: D
	STANDARD: NON-JEDEC	
	SOT1938-1	03 JUL 2018

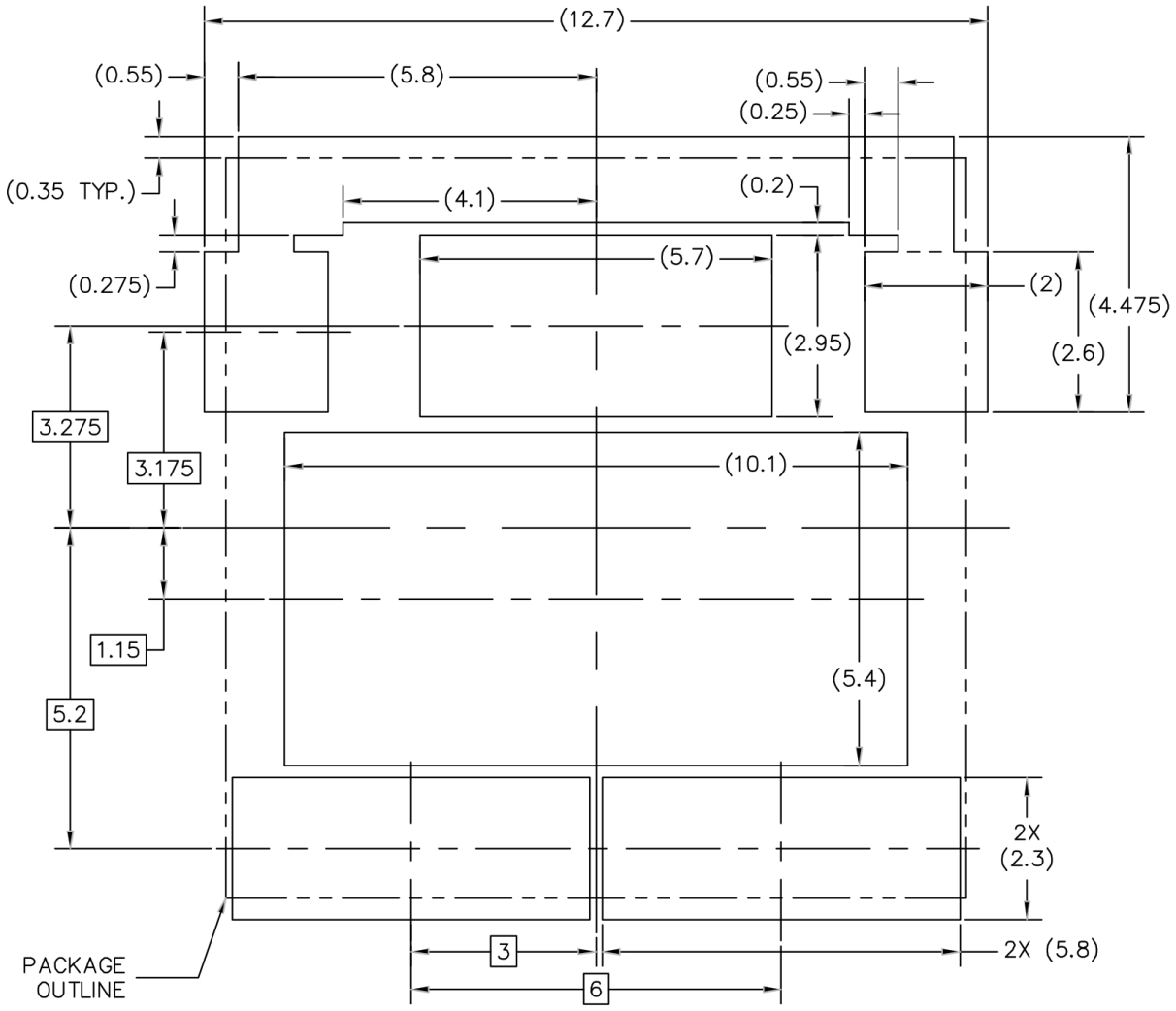


PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN 1

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL / SPECIFIC REQUIREMENTS.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	DOCUMENT NO: 98ASA00428D REV: D
	STANDARD: NON–JEDEC
	SOT1938–1 03 JUL 2018

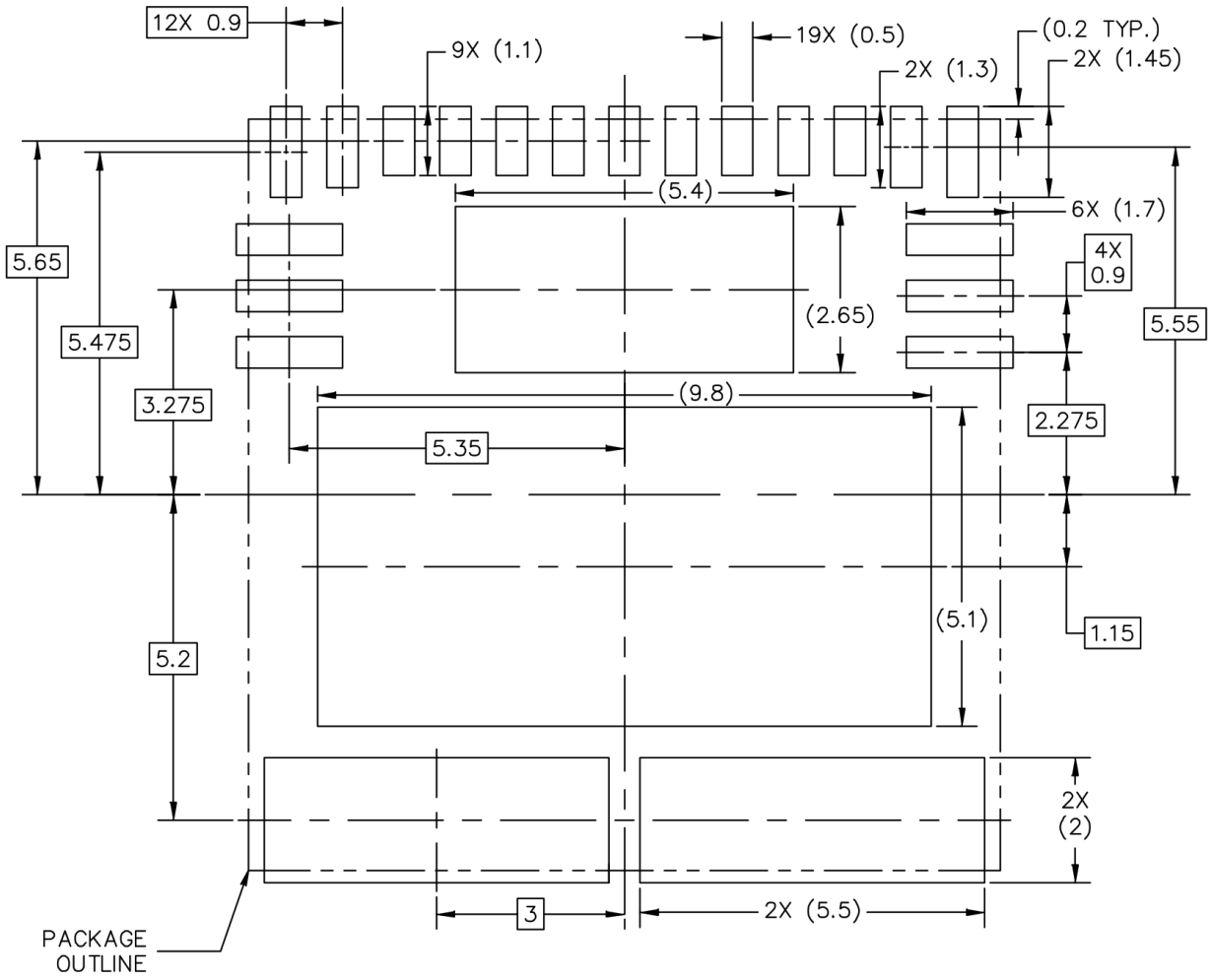


PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN 2

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL / SPECIFIC REQUIREMENTS.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA00428D	REV: D
PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	STANDARD: NON-JEDEC	
	SOT1938-1	03 JUL 2018



PCB CU GUIDELINES – I/O PADS & SOLDERABLE AREAS

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL / SPECIFIC REQUIREMENTS.

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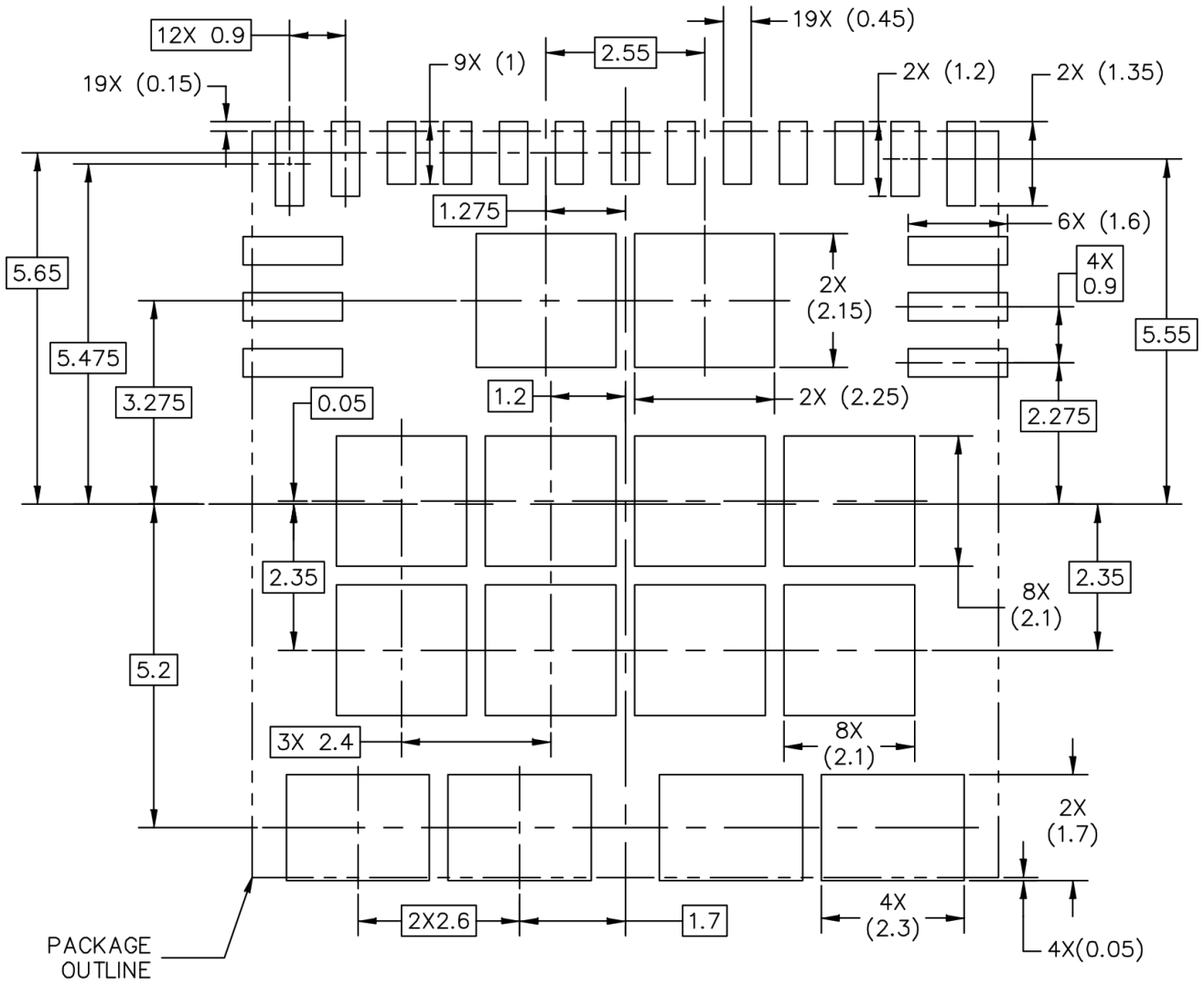
TITLE: PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	DOCUMENT NO: 98ASA00428D	REV: D
	STANDARD: NON–JEDEC	
	SOT1938–1	03 JUL 2018



SOLDER PASTE STENCIL GUIDELINES

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL / SPECIFIC REQUIREMENTS.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA00428D	REV: D
PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	STANDARD: NON-JEDEC	
	SOT1938-1	03 JUL 2018

20XS4200

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP IS GUARANTEED TO BE 0.25 MM.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA00428D	REV: D
PQFN, 12X12X2.1, 0.9 PITCH, 23 TERMINAL	STANDARD: NON–JEDEC	
	SOT1938–1	03 JUL 2018

9 Revision history

Revision	Date	Description of Changes
1.0	5/2012	• Initial release
2.0	6/2012	• Updated values in Table 4, Static electrical characteristics
3.0	5/2013	• Grammatical accuracy and form consistency changes made. No changes to content. • Revised back page. Updated document properties. Added SMARTMOS sentence to first paragraph.
4.0	8/2013	• Added a table • Introduction of parameters related to 20XS4200 device (Table 1). • Removed R_{DSON} values at 1.0 A. • Rectification of the inversion between Δt_{DLY} values at slow and medium slew rate. • Added the 20XS4200 to the Systematic offset error (see Current sense errors) parameter.
5.0	11/2013	• Removed EK package information • Removed all references to the SOIC package • Added 20XS4200BAFK to the ordering information • Introduction of parameters related to 20XS4200BAFK device • Removed Ecl_rep energy values • Update Ecl_sing value
6.0	5/2018	• Updated as per CIN 201805019I • Changed steady state current value from 3.0 to 4.4 A listed under features on page 1 • Updated $I_{HS[0:1]}$ value in Table 3 (changed 3.0 to 4.4) • Added clarification for diagnostic range to Table 5 • Updated load dump duration (changed 500 ms to 350 ms) and changed V_{PWR} from 14 V to 28 V in Table 3 • Updated Track & Hold current sensing mode • Typo correction in Table 4 (corrected current limit range for E_{SR0_ERR})
7.0	10/2022	• Updated as per CIN 202209028I • Added Orderable part numbers in Table 1: MC20XS4200DFK and MC20XS4200BDFK • Added footnote to Table 1 • Updated part numbers under VPWR supply voltage range and Voltage (continuous, max. allowable) on output pins (HS [0:1]) in Table 3: Second bullet under each heading changed from 20XS4200BFK, and 20XS4200BAFK to 20XS4200BFK and 20XS4200DFK, 20XS4200BAFK and 20XS4200BDFK • Updated Table 4 to include new part numbers • Updated Table 5 to include new part numbers • Updated footnote in Table 12 • Updated footnote in Table 13 • Updated part numbers in Previous address SOA3:SOA0 = 0111 (DIAGR_s) • Updated images in Package mechanical dimensions
8.0	11/2022	• Updated as per CIN 202209028I • Updated Table 4 to include new part numbers

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11/2022