

MC14067B

Analog Multiplexers / Demultiplexers

The MC14067 multiplexer/demultiplexer is a digitally controlled analog switch featuring low ON resistance and very low leakage current. This device can be used in either digital or analog applications.

The MC14067 is a 16-channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1-of-16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

Features

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	- 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	- 55 to + 125	$^{\circ}C$
T_{stg}	Storage Temperature Range	- 65 to + 150	$^{\circ}C$
T_L	Lead Temperature (8-Second Soldering)	260	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

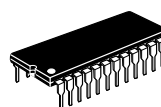
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



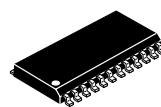
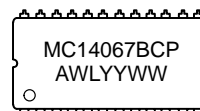
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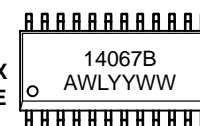
MARKING DIAGRAMS



PDIP-24
P SUFFIX
CASE 709



SOIC-24
DW SUFFIX
CASE 751E



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

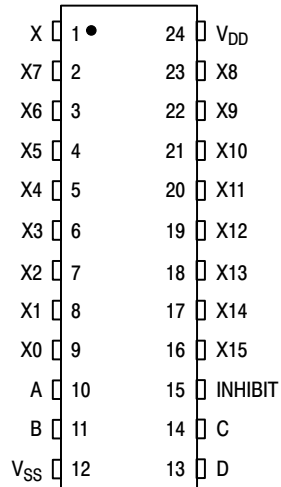
See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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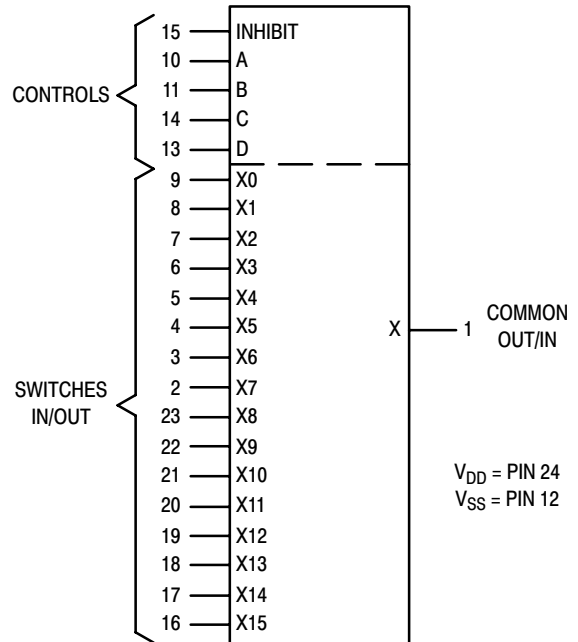
TRUTH TABLE

Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

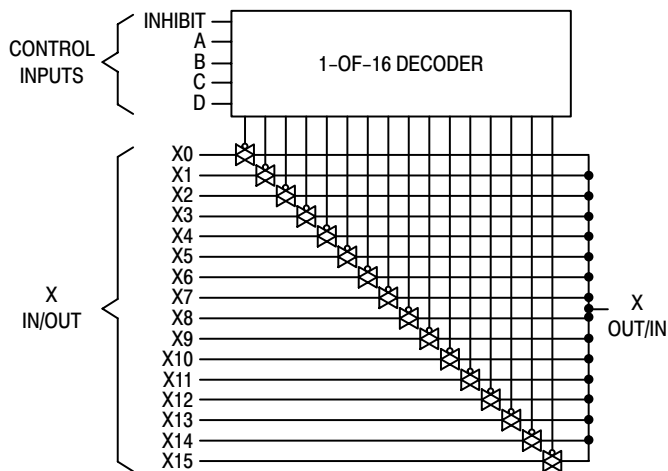
PIN ASSIGNMENT



16-Channel Analog Multiplexer/Demultiplexer



FUNCTIONAL DIAGRAM



MC14067B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V _{DD}	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (2)	Max	Min	Max	

SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})

Power Supply Voltage Range	V _{DD}	–		3.0	18	3.0	–	18	3.0	18	V
Quiescent Current Per Package	I _{DD}	5.0	Control Inputs: V _{in} = V _{SS} or V _{DD} , Switch I/O: V _{SS} ≤ V _{I/O} ≤ V _{DD} , and ΔV _{switch} ≤ 500 mV (3)	–	5.0	–	0.005	5.0	–	150	μA
		10		–	10	–	0.010	10	–	300	
		15		–	20	–	0.015	20	–	600	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I _{D(AV)}	5.0 10 15	T _A = 25°C only (The channel component, (V _{in} – V _{out})/R _{on} , is not included.)	Typical (0.07 μA/kHz) f + I _{DD} (0.20 μA/kHz) f + I _{DD} (0.36 μA/kHz) f + I _{DD}						μA	

CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V_{SS})

Low-Level Input Voltage	V _{IL}	5.0	R _{on} = per spec, I _{off} = per spec	–	1.5	–	2.25	1.5	–	1.5	V
		10		–	3.0	–	4.50	3.0	–	3.0	
		15		–	4.0	–	6.75	4.0	–	4.0	
High-Level Input Voltage	V _{IH}	5.0	R _{on} = per spec, I _{off} = per spec	3.5	–	3.5	2.75	–	3.5	–	V
		10		7.0	–	7.0	5.50	–	7.0	–	
		15		11	–	11	8.25	–	11	–	
Input Leakage Current	I _{in}	15	V _{in} = 0 or V _{DD}	–	±0.1	–	±0.00001	±0.1	–	1.0	μA
Input Capacitance	C _{in}	–		–	–	–	5.0	7.5	–	–	pF

SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V_{SS})

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V _{I/O}	–	Channel On or Off	0	V _{DD}	0	–	V _{DD}	0	V _{DD}	V _{p-p}
Recommended Static or Dynamic Voltage Across the Switch (3) (Figure 1)	ΔV _{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V _{OO}	–	V _{in} = 0 V, No Load	–	–	–	10	–	–	–	μV
ON Resistance	R _{on}	5.0	ΔV _{switch} ≤ 500 mV (3), V _{in} = V _{IL} or V _{IH} (Control), and V _{in} 0 to V _{DD} (Switch)	–	800	–	250	1050	–	1300	Ω
		10		–	400	–	120	500	–	550	
		15		–	220	–	80	280	–	320	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR _{on}	5.0		–	70	–	25	70	–	135	Ω
		10		–	50	–	10	50	–	95	
		15		–	45	–	10	45	–	65	
Off-Channel Leakage Current (Figure 2)	I _{off}	15	V _{in} = V _{IL} or V _{IH} (Control) Channel to Channel or Any One Channel	–	±100	–	±0.05	±100	–	±1000	nA
Capacitance, Switch I/O	C _{I/O}	–	Inhibit = V _{DD}	–	–	–	10	–	–	–	pF
Capacitance, Common O/I	C _{O/I}	–	Inhibit = V _{DD} (MC14067B) (MC14097B)	–	–	–	100	–	–	–	pF
				–	–	–	60	–	–	–	
Capacitance, Feedthrough (Channel Off)	C _{I/O}	–	Pins Not Adjacent	–	–	–	0.47	–	–	–	pF
		–		Pins Adjacent	–	–	–	–	–	–	

- Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
- For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

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ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	$V_{DD} - V_{SS}$ V_{dc}	Typ (4)	Max	Unit
Propagation Delay Times Channel Input-to-Channel Output ($R_L = 200 \text{ k}\Omega$) MC14067B	t_{PLH} , t_{PHL} (Figure 3)	5.0 10 15	35 15 12	90 40 30	ns
Control Input-to-Channel Output Channel Turn-On Time ($R_L = 10 \text{ k}\Omega$) MC14067B	t_{PZH} , t_{PZL} (Figure 4)	5.0 10 15	240 115 75	600 290 190	ns
Channel Turn-Off Time ($R_L = 300 \text{ k}\Omega$) MC14067B	t_{PHZ} , t_{PLZ} (Figure 4)	5.0 10 15	250 120 75	625 300 190	ns
Any Pair of Address Inputs to Output MC14067B	t_{PLH} , t_{PHL}	5.0 10 15	280 115 85	700 290 215	ns
Second Harmonic Distortion ($R_L = 10 \text{ k}\Omega$, $f = 1 \text{ kHz}$, $V_{in} = 5 V_{p-p}$)	–	10	0.3	–	%
ON Channel Bandwidth [$R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{SS})$ p-p (sine-wave)] $20 \text{ Log}_{10} (V_{out}/V_{in}) = -3 \text{ dB}$ MC14067B	BW (Figure 5)	10	15	–	MHz
Off Channel Feedthrough Attenuation [$R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{SS})$ p-p (sine-wave)] $f_{in} = 20 \text{ MHz}$ – MC14067B	– (Figure 5)	10	– 40	–	dB
Channel Separation [$R_L = 1 \text{ k}\Omega$, $V_{in} = 1/2 (V_{DD} - V_{SS})$ p-p (sine-wave)] $f_{in} = 20 \text{ MHz}$	– (Figure 6)	10	– 40	–	dB
Crosstalk, Control Inputs-to-Common O/I ($R_1 = 1 \text{ k}\Omega$, $R_L = 10 \text{ k}\Omega$, Control $t_r = t_f = 20 \text{ ns}$, Inhibit = V_{SS})	– (Figure 7)	10	30	–	mV

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

ORDERING INFORMATION

Device	Package	Shipping†
MC14067BCP	PDIP-14	500 Units / Rail
MC14067BCPG	PDIP-14 (Pb-Free)	500 Units / Rail
MC14067BDW	SOIC-14	55 Units / Rail
MC14067BDWG	SOIC-14 (Pb-Free)	55 Units / Rail
MC14067BDWR2	SOIC-14	2500 Units / Tape & Reel
MC14067BDWR2G	SOIC-14 (Pb-Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

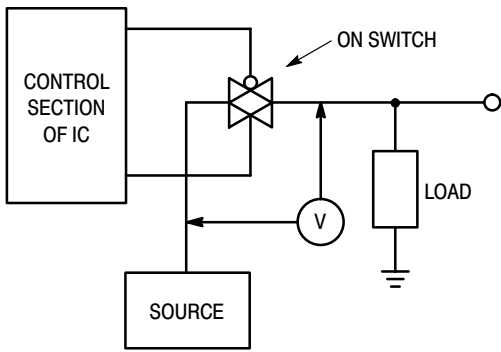


Figure 1. ΔV Across Switch

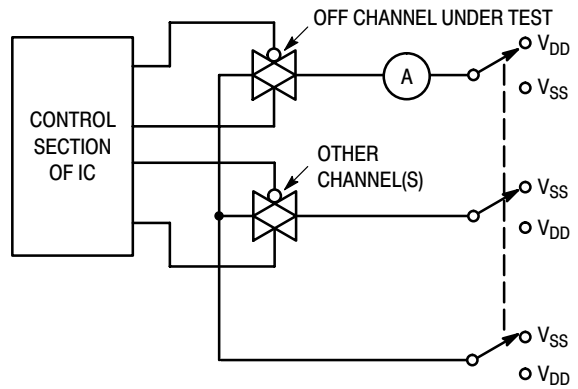


Figure 2. Off Channel Leakage

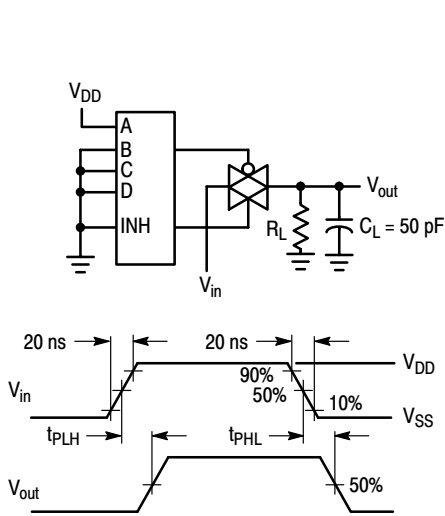


Figure 3. Propagation Delay Test Circuit and Waveforms V_{in} to V_{out}

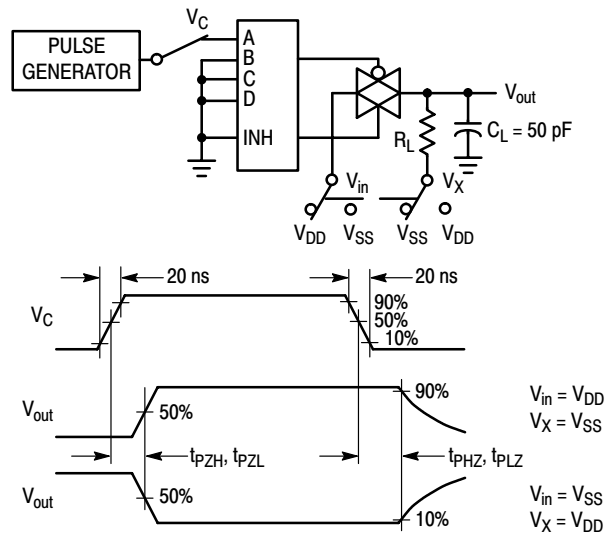


Figure 4. Turn-On and Delay Turn-Off Test Circuit and Waveforms

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A, B, and C inputs used to turn ON or OFF the switch under test.

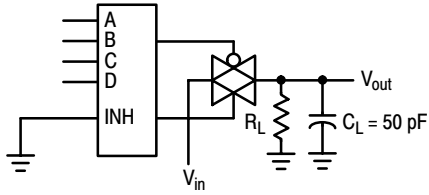


Figure 5. Bandwidth and Off-Channel Feedthrough Attenuation

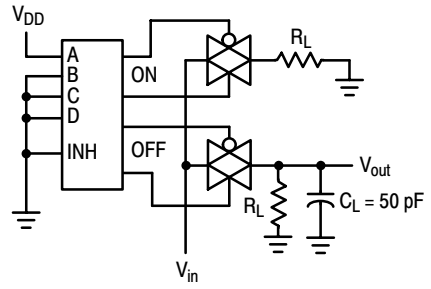


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

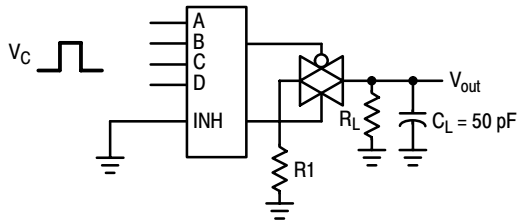


Figure 7. Crosstalk, Control to Common O/I

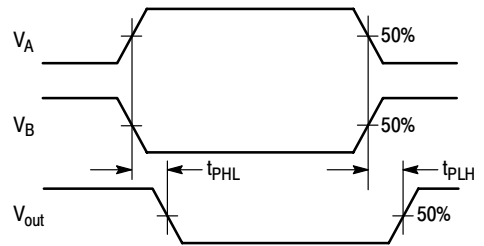
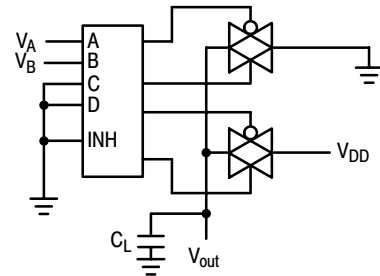


Figure 9. Propagation Delay, Any Pair of Address Inputs to Output

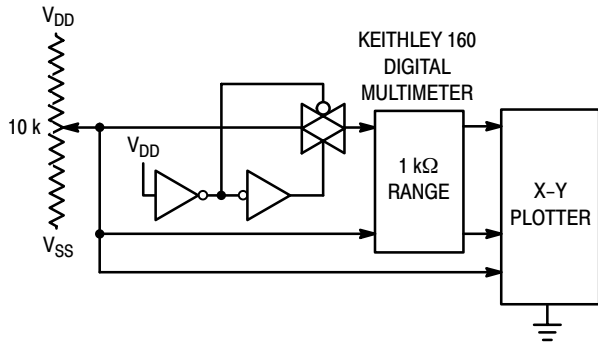


Figure 8. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

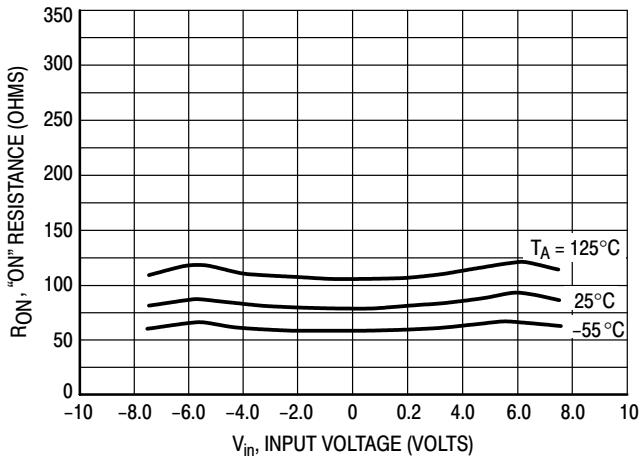


Figure 10. $V_{DD} = 7.5\text{ V}$, $V_{SS} = -7.5\text{ V}$

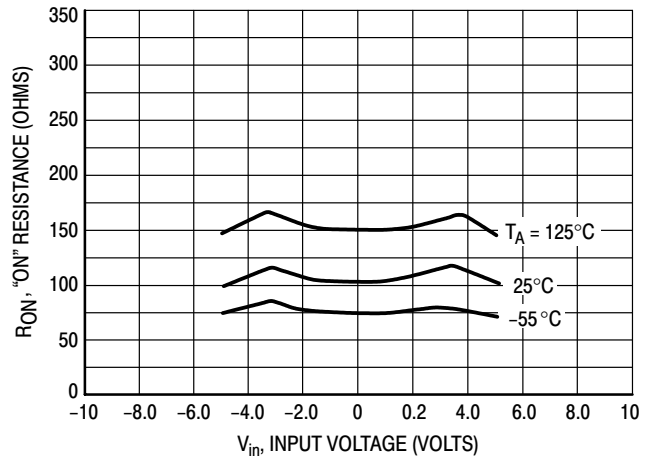


Figure 11. $V_{DD} = 5.0\text{ V}$, $V_{SS} = -5.0\text{ V}$

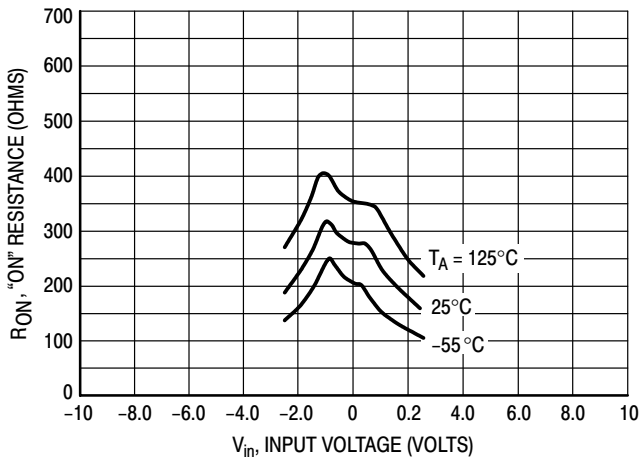


Figure 12. $V_{DD} = 2.5\text{ V}$, $V_{SS} = -2.5\text{ V}$

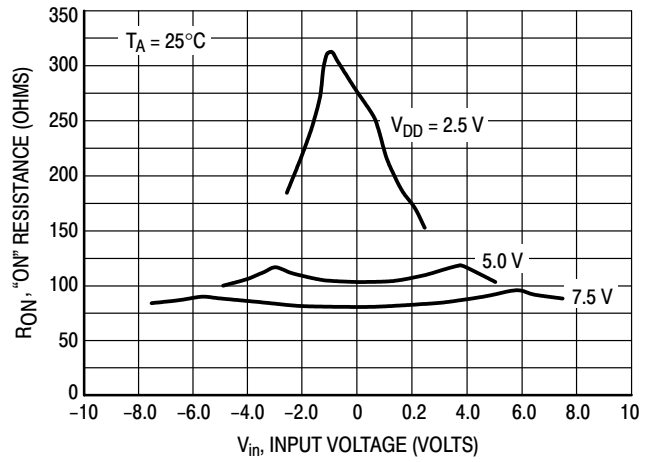


Figure 13. Comparison at 25°C, $V_{DD} = -V_{SS}$

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer / Demultiplexer. The 0-to-5 V Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS}. The example shows a 5 V_{p-p}

signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V_{DD} and V_{SS}.

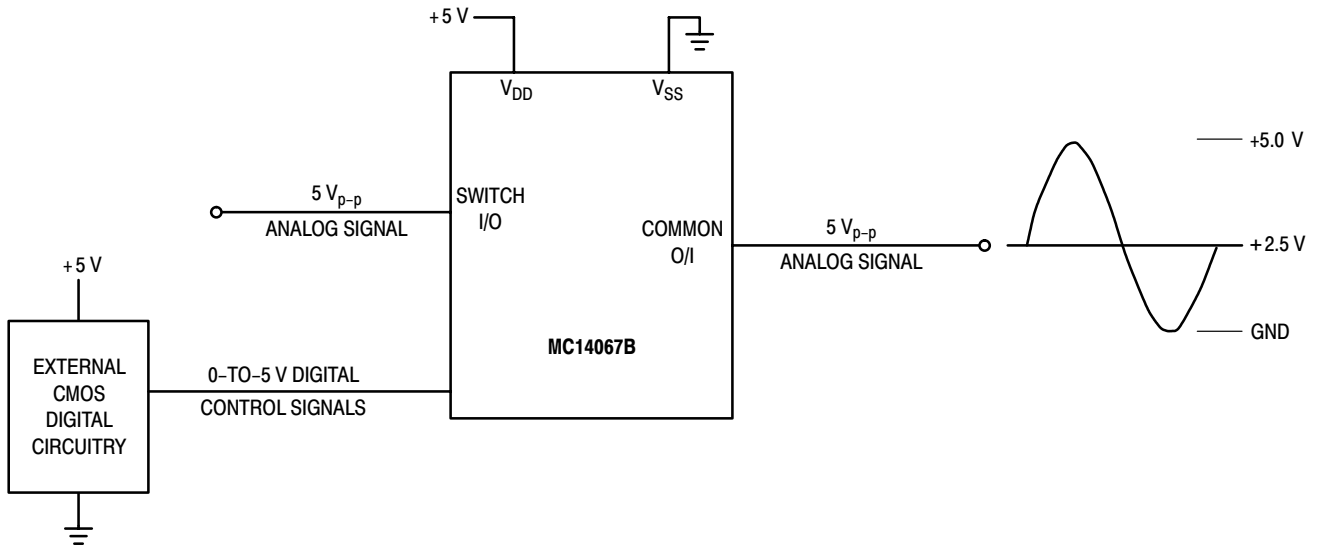


Figure A. Application Example

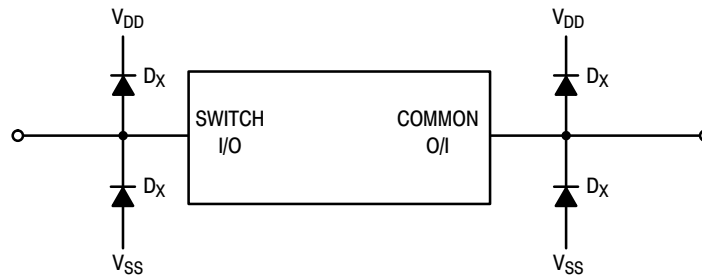
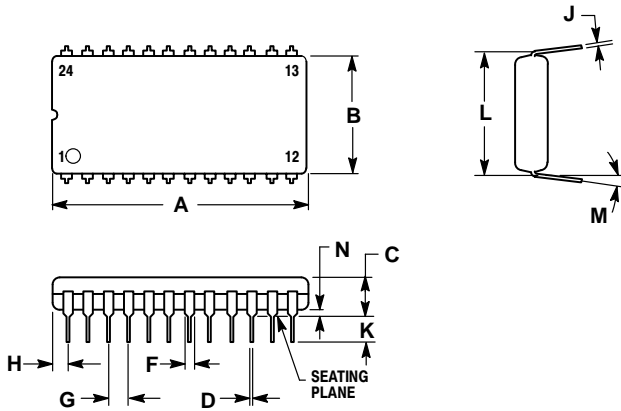


Figure B. External Germanium or Schottky Clipping Diodes

MC14067B

PACKAGE DIMENSIONS

PDIP-24
P SUFFIX
CASE 709-02
ISSUE C

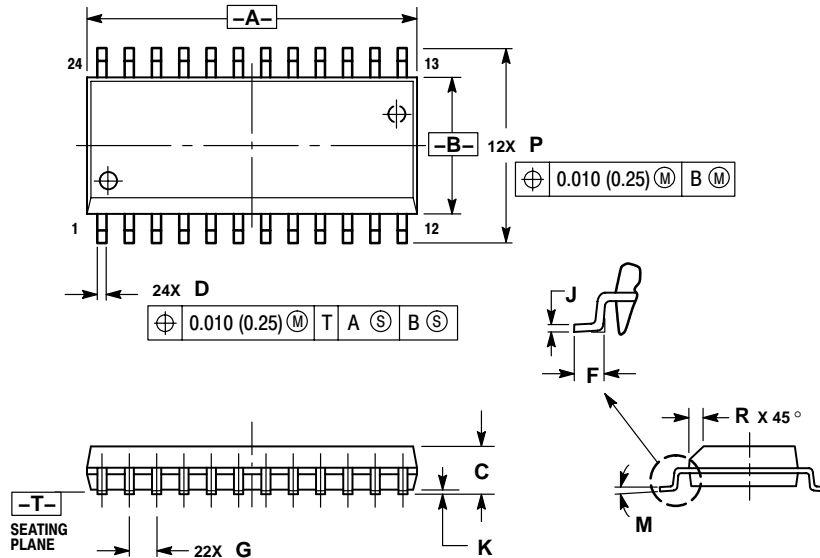


NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.235	1.265	31.37	32.13
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.080	1.65	2.03
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

SOIC-24
DW SUFFIX
CASE 751E-04
ISSUE E




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

MC14067B

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