Not Recommended for New Designs

This product was manufactured for Maxim by an outside wafer foundry using a process that is no longer available. It is not recommended for new designs. The data sheet remains available for existing users.

A Maxim replacement or an industry second-source may be available. Please see the QuickView data sheet for this part or contact technical support for assistance.

For further information, contact Maxim's Applications Tech Support.

19-2399; Rev 2; 6/90

MAXIM

Single/Dual, Very Fast TTL Output Comparators

General Description

The MAX9686 (single)/MAX9698 (dual) are very fast TTL comparators manufactured with a high-frequency bipolar process (f_T = 6GHz) that are capable of very short propagation delays, yet maintain the excellent DC matching characteristics that are normally found only in slower comparators. The MAX9698 is a dual version of the MAX9686.

The MAX9686/MAX9698 have differential inputs and complementary outputs that are fully compatible with TTL logic levels. The extremely short propagation delays allow signal processing at frequencies in excess of 200MHz.

When the latch enable input goes high, the outputs go to the states defined by the input condition at the time of the latch transition. The outputs remain latched as long as the LE pin remains high. If the latch enable function is not used, the LE pin must be tied to ground.

Applications

High-Speed Analog-to-Digital Converters

High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

Features

- **6ns Propagation Delay**
- **2ns Latch Setup Time**
- **+5V, -5.2V Power Supplies**
- **Pin Compatible to LT1016, Am686**
- **Available in Commercial and Military Versions**
- **Available in SO**

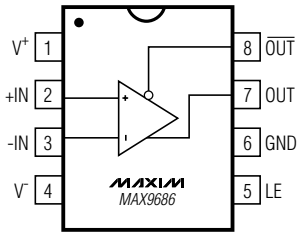
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE*
MAX9686CPA	0°C to +70°C	8 Plastic Dip
MAX9686CJA	0°C to +70°C	8 CERDIP
MAX9686CSA	0°C to +70°C	8 SO
MAX9686C/D	0°C to +70°C	Dice
MAX9686CTV	0°C to +70°C	8 TO-99 Metal Can
MAX9686MJA	-55°C to +125°C	8 CERDIP
MAX9686MTV	-55°C to +125°C	8 TO-99 Metal Can
MAX9698CPE	0°C to +70°C	16 Plastic Dip
MAX9698CJE	0°C to +70°C	16 CERDIP
MAX9698CSE	0°C to +70°C	16 SO
MAX9698C/D	0°C to +70°C	Dice
MAX9698MJE	-55°C to +125°C	16 CERDIP

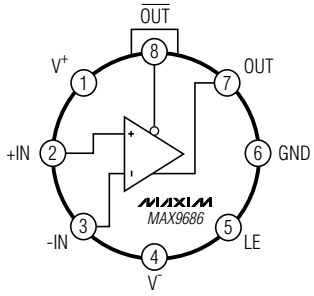
**Contact factory for availability of 20-lead LCC.*

Pin Configurations

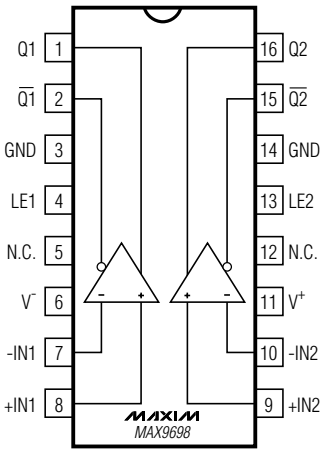
TOP VIEW



PLASTIC DIP, CERDIP, SO



TO-99 METAL CAN



PLASTIC DIP, CERDIP, SO

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±6V
Power Dissipation (Notes 1, 2) 336mW
Input Voltages ..... ±5V
Differential Input Voltages 5V
Output Current 20mA

Operating Temperature Ranges:
Commercial (MAX9686C/MAX9698M) ..... 0°C to +70°C
Military (MAX9686M/MAX9698M) ..... -55°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10s) ..... 300°C

Note 1: Power derating above T_A = +70°C is based on a maximum junction temperature of +150°C and the following thermal resistance factors.

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)
DIP	75	180
SO	115	180
TO-99	115	150

Note 2: Continuous short-circuit protection is allowed to the following case and ambient temperatures: for MAX9698, continuous short circuit is allowed on one comparator at a time up to case temperature of +85°C and ambient temperatures of +30°C.

PACKAGE	T_C (°C)	T_A (°C)
DIP	110	70
SO	95	70
TO-99	95	30

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

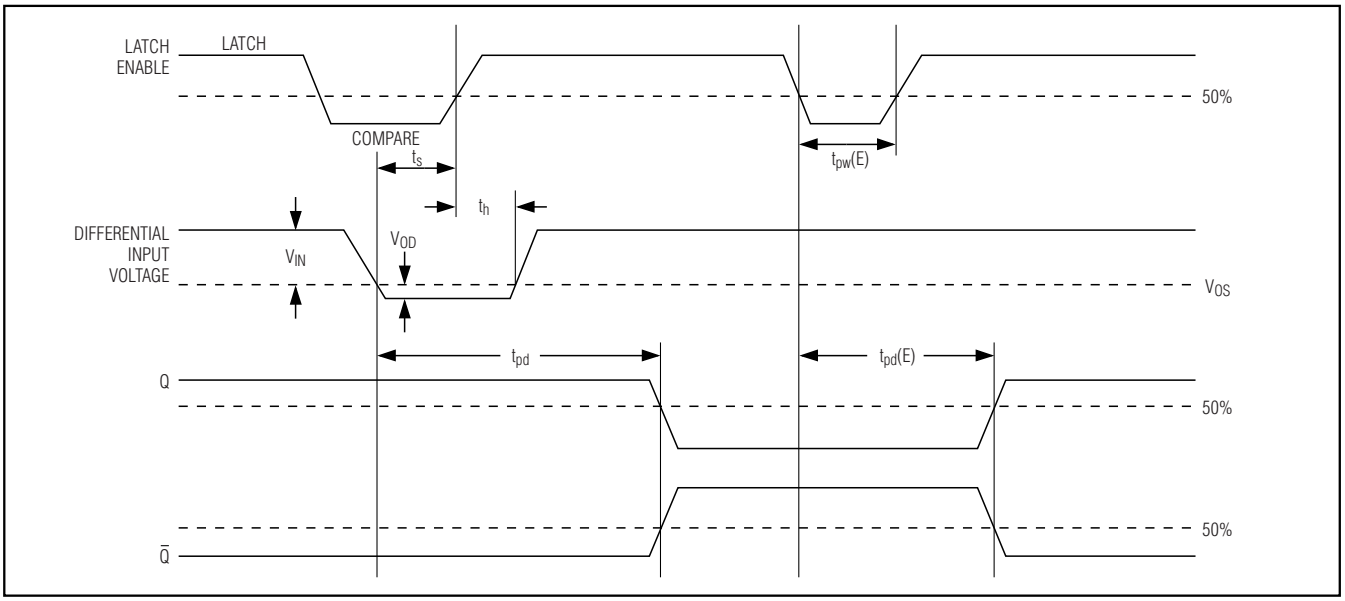
(V_S = ±5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX9686C/9698C			MAX9686M/9698M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	R_S = 100Ω	-3		+3	-3		+3	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$			4			4		µV/°C
Input Offset Current	I_{OS}				5.0			5.0	µA
Input Bias Current	I_B				25			25	µA
Common-Mode Rejection Ratio	CMRR		80	96		80	96		dB
Power-Supply Rejection Ratio	PSRR		70	85		70	85		dB
Input Voltage Range			-3.0		+3.0	-3.0		+3.0	V
Latch High Input Voltage			2.0			2.0			V
Latch Low Input Voltage					0.8			0.8	V
Latch Low Input Current					-750			-750	µA
I/O Logic Levels (Output High Voltage)	V_{OH}	I_{OUT} = -3mA	2.4	3.0		2.4	3.0		V
I/O Logic Levels (Output Low Voltage)	V_{OL}	I_{OUT} = 8mA			0.5			0.5	V
Positive Supply Current	I_{CC}	MAX9686		16	25		16	25	mA
		MAX9698		32	50		32	50	
Negative Supply Current	I_{EE}	MAX9686		13	20		13	20	mA
		MAX9698		26	40		26	40	

ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX9686C/9698C			MAX9686M/9698M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS (EACH COMPARATOR FOR MAX9698)									
Propagation Delays (Guaranteed Over Full Temperature Range) Input to Output High	t_{pd+}	100mV pulse; 10mV overdrive		6.0	9.0		6.0	9.0	ns
Input to Output Low	t_{pd-}	100mV pulse; 10mV overdrive		5.7	8.5		5.7	8.5	ns
Propagation Delay Skew	$t_{pd+} - t_{pd-}$			0.3			0.3		ns
Latch Setup	t_S			2			2		ns



MAX9686 and MAX9698 Timing Diagram (worst case)

Applications Information

Layout

Because of the large gain-bandwidth characteristic of the MAX9686 and MAX9698, special precautions need to be taken if the high-speed capabilities of the devices are to be realized. A PC board with ground plane should be considered mandatory. All decoupling capacitors should be mounted as close as possible to the power-supply pins. For low-impedance applications, microstrip layout at the input may be helpful. Close attention should be paid to the bandwidth of the decoupling and terminating components. Chip components to minimize lead inductance can be used as an advantage. An unused latch enable pin must be connected to ground.

Input Slew-Rate Requirements

As with all high-speed comparators, the high gain-bandwidth product of these devices creates oscillation problems when the input traverses through the linear region. For clean switching without oscillation or steps in the output waveform, the input must meet certain minimum slew-rate requirements. The tendency of the part to oscillate is a function of the layout and the source impedance of the circuit employed. Both poor layout and larger source impedance will increase the minimum slew-rate requirement.

Single/Dual, Very Fast TTL Output Comparators

Definition of Terms

V_{OS} Input Offset Voltage—The voltage required between the input terminals to obtain 0V dif ferential at the output.

V_{IN} Input Voltage Pulse Amplitude

V_{OD} Input Voltage Overdrive

t_{pd+} Input to Output High Delay—The propagation delay measured from the time the input sig nal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} Input to Output Low Delay—The propagation delay measured from the time the input sig nal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

t_{pd+}(E) Latch Enable to Output High Delay—The propagation delay measured from the 50% point of the Latch-Enable signal HIGH LOtransition to the 50% point of an output LOW to HIGH transition.

t_{pd-}(E) Latch Enable to Output Low Delay—The prop agation delay measured from the 50% point of the Latch-Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

t_{pw}(E) Minimum Latch Enable Pulse Width—The minimum time the Latch-Enable signal must be LOW to acquire and hold an input signal.

t_s Minimum Setup Time—The minimum time, before the positive transition of the Latch-Enable pulse, that an input signal must be present to be acquired and held at the outputs.

t_h Minimum Hold Time—The minimum time, after the positive transition of the Latch-Enable signal, than an input signal must remain unchanged to be acquired and held at the output.