19-1945; Rev 5; 3/09

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

General Description

The MAX4691–MAX4694 are low-voltage CMOS analog ICs configured as an 8-channel multiplexer (MAX4691), two 4-channel multiplexers (MAX4692), three single-pole/double-throw (SPDT) switches (MAX4693), and four SPDT switches (MAX4694).

The MAX4691/MAX4692/MAX4693 operate from either a single +2V to +11V power supply or dual ±2V to ±5.5V power supplies. When operating from ±5V supplies they offer 25Ω on-resistance (R_{ON}), 3.5Ω (max) R_{ON} flatness, and 3Ω (max) matching between channels. The MAX4694 operates from a single +2V to +11V supply. Each switch has rail-to-rail signal handling and a low 1nA leakage current.

All digital inputs are 1.8V logic-compatible when operating from a +3V supply and TTL compatible when operating from a +5V supply.

The MAX4691–MAX4694 are available in 16-pin, 4mm × 4mm QFN and TQFN and 16-bump UCSP packages. The chip-scale package (UCSP™) occupies a 2mm × 2mm area, significantly reducing the required PC board area.

Applications

Audio and Video Signal Routing

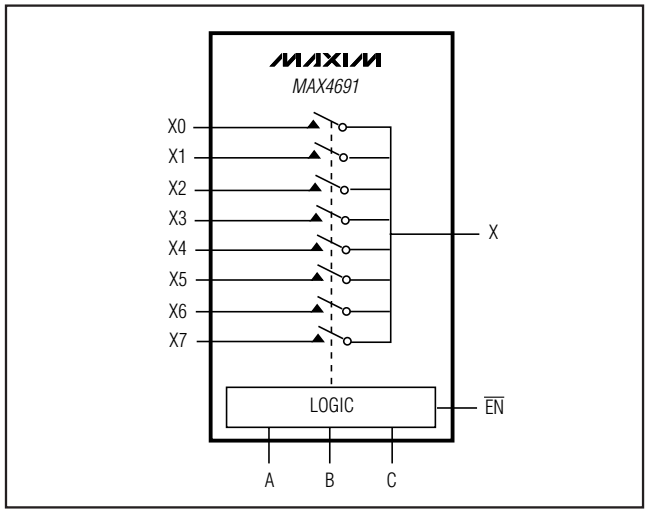
Cellular Phones

Battery-Operated Equipment

Communications Circuits

Modems

Functional Diagrams



Pin Configurations appear at end of data sheet.

Functional Diagrams continued at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- **16 Bump, 0.5mm-Pitch UCSP (2mm x 2mm)**
- **1.8V Logic Compatibility**
- **Guaranteed On-Resistance**
  - **70Ω (max) with +2.7V Supply**
  - **35Ω (max) with +5V Supply**
  - **25Ω (max) with ±4.5V Dual Supplies**
- **Guaranteed Match Between Channels**
  - **5Ω (max) with +2.7V Supply**
  - **3Ω (max) with ±4.5V Dual Supplies**
- **Guaranteed Flatness Over Signal Range**
  - **3.5Ω (max) with ±4.5V Dual Supplies**
- **Low Leakage Currents Over Temperature**
  - **20nA (max) at +85°C**
- **Fast 90ns Transition Time**
- **Guaranteed Break-Before-Make**
- **Single-Supply Operation from +2V to +11V**
- **Dual-Supply Operation from ±2V to ±5.5V (MAX4691/MAX4692/MAX4693)**
- **V+ to V- Signal Handling**
- **Low Crosstalk: -90dB (100kHz)**
- **High Off-Isolation: -88dB (100kHz)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX4691EBE+T	-40°C to +85°C	16-Bump UCSP*
MAX4691EGE+	-40°C to +85°C	16 QFN-EP†
MAX4691ETE+T	-40°C to +85°C	16 TQFN-EP†
MAX4692EBE+T	-40°C to +85°C	16-Bump UCSP*
MAX4692EGE+	-40°C to +85°C	16 QFN-EP†
MAX4692ETE+T	-40°C to +85°C	16 TQFN-EP†
MAX4693EBE+T	-40°C to +85°C	16-Bump UCSP*
MAX4693EGE+	-40°C to +85°C	16 QFN-EP†
MAX4693ETE+T	-40°C to +85°C	16 TQFN-EP†
MAX4694EBE+T	-40°C to +85°C	16-Bump UCSP*
MAX4694EGE+	-40°C to +85°C	16 QFN-EP†
MAX4694ETE+T	-40°C to +85°C	16 TQFN-EP†

**UCSP reliability is integrally linked to the user's assembly methods, circuit board, and environment. See the UCSP Reliability section for more information.*

†EP = Exposed pad.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +12V
V+ to V- (MAX4691/MAX4692/MAX4693) .....-0.3V to +12V
Voltage into any Terminal (Note 1) ..... (V- - 0.3V) to (V+ + 0.3V)
Continuous Current into any Terminal ..... ±20mA
Peak Current W_, X_, Y_, Z_ (pulsed at 1ms, 10% duty cycle).....±40mA
ESD per Method 3015.7.....> 2kV
Continuous Power Dissipation (T_A = +70°C)
16-Bump UCSP (derate 8.3mW/°C above +70°C) 659mW
16-Pin QFN (derate 18.5mW/°C above +70°C) 1481mW
16-Pin TQFN (derate 16.9mW/°C above +70°C) 1349mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering)
16-Bump UCSP Infrared (15s)..... +220°C
Vapor Phase (60s)..... +215°C
16-Pin QFN..... +300°C
16-Pin TQFN..... +300°C

Note 1: Voltages exceeding V+ or V- on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0, V_{IH} = +1.4V, V_{IL} = +0.4V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_W, V_X, V_Y, V_Z, $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$		-40°C to +85°C	0		V+	V
On-Resistance (Note 5)	R_{ON}	V+ = 2.7V; I_W, I_X, I_Y, I_Z = 1mA $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1.5V	+25°C		45	70	Ω
			-40°C to +85°C			80	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = 2.7V; I_W, I_X, I_Y, I_Z = 1mA $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1.5V	+25°C		2	5	Ω
			-40°C to +85°C			6	
W_, X_, Y_, Z_ Off-Leakage Current (Note 7)	$I_{W\_}$, $I_{X\_}$, $I_{Y\_}$, $I_{Z\_}$	V+ = 3.6V; V_W, V_X, V_Y, V_Z = 3V, 0.6V; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0.6V, 3V	+25°C	-1		+1	nA
			-40°C to +85°C	-10		+10	
W, X, Y, Z Off-Leakage Current (Note 7)	$I_{W(OFF)}$, $I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V+ = 3.6V; V_W, V_X, V_Y, V_Z = 3V, 0.6V; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0.6V, 3V	+25°C	-2		+2	nA
			-40°C to +85°C	-20		+20	
W, X, Y, Z On-Leakage Current (Note 7)	$I_{W(ON)}$, $I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V+ = 3.6V; V_W, V_X, V_Y, V_Z = 0.6V, 3V; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0.6V, 3V, or unconnected	+25°C	-2		+2	nA
			-40°C to +85°C	-20		+20	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V- = 0, V_{IH} = +1.4V, V_{IL} = +0.4V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP	MAX	UNITS
Input Off-Capacitance	$C_{W\_(OFF)}$, $C_{X\_(OFF)}$, $C_{Y\_(OFF)}$, $C_{Z\_(OFF)}$	f = 1MHz, Figure 7		+25°C		9		pF
Output Off-Capacitance	$C_{X(OFF)}$, $C_{Y(OFF)}$, $C_{Z(OFF)}$	f = 1MHz, Figure 7	MAX4691	+25°C		68		pF
			MAX4692			36		
			MAX4693			20		
On-Capacitance	$C_{W(ON)}$, $C_{X(ON)}$, $C_{Y(ON)}$, $C_{Z(ON)}$	f = 1MHz, Figure 7	MAX4691	+25°C		78		pF
			MAX4692			46		
			MAX4693			30		
DYNAMIC								
Enable Turn-On Time (MAX4691/MAX4692/ MAX4693)	t_{ON}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		180	300	ns
				-40°C to +85°C			350	
Enable Turn-Off Time (MAX4691/MAX4692/ MAX4693)	t_{OFF}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 2		+25°C		70	100	ns
				-40°C to +85°C			120	
Address Transition Time	t_{TRANS}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0, 1.5V; R_L = 300Ω, C_L = 35pF, Figure 3		+25°C		200	350	ns
				-40°C to +85°C			400	
Break-Before-Make	t_{BBM}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 4		+25°C	2	90		ns
				-40°C to +85°C	2			
Charge Injection	Q	V_{GEN} = 0; R_{GEN} = 0; C_L = 1nF, Figure 5		+25°C		0.1		pC
Off-Isolation (Note 8)	V_{ISO}	f = 0.1MHz, R_L = 50Ω, C_L = 5pF, Figure 6		+25°C		-70		dB
Crosstalk (Note 9)	V_{CT}	f = 0.1MHz, R_L = 50Ω, C_L = 5pF, Figure 6		+25°C		-75		dB
DIGITAL I/O								
Input Logic-High	V_{IH}				1.4			V
Input Logic-Low	V_{IL}						0.4	V
Input Leakage Current	I_{IN}	V_A, V_B, V_C, $V_{\overline{EN}}$ = 0 or V+			-1		+1	µA
SUPPLY								
Positive Supply Current	I+	V+ = 3.6V, V_A, V_B, V_C, $V_{\overline{EN}}$ = 0 or V+		+25°C			0.1	µA
				-40°C to +85°C			1	

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0, V_{IH} = +2V, V_{IL} = +0.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_W, V_X, V_Y, V_Z, $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$		-40°C to +85°C	0		V+	V
On-Resistance (Note 5)	R_{ON}	V+ = 4.5V; I_W, I_X, I_Y, I_Z = 1mA; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3.5V	+25°C		25	35	Ω
			-40°C to +85°C			40	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = 4.5V; I_W, I_X, I_Y, I_Z = 1mA; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3.5V	+25°C		2	4	Ω
			-40°C to +85°C			5	
On-Resistance Flatness (Note 10)	$R_{FLAT(ON)}$	V+ = 4.5V; I_W, I_X, I_Y, I_Z = 1mA; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 2.25V, 3.5V	+25°C		2	6	Ω
			-40°C to +85°C			8	
W_, X_ , Y_, Z_ Off-Leakage Current (Note 7)	$I_{W\_}$, $I_{X\_}$, $I_{Y\_}$, $I_{Z\_}$	V+ = 5.5V; V_W, V_X, V_Y, V_Z = 4.5V, 1V_; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 4.5V	+25°C	-1		+1	nA
			-40°C to +85°C	-10		+10	
W, X, Y, Z Off-Leakage Current (Note 7)	$I_{W(OFF)}$, $I_{X(OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V+ = 5.5V; V_W, V_X, V_Y, V_Z = 4.5V, 1V_; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 4.5V	+25°C	-2		+2	nA
			-40°C to +85°C	-20		+20	
W, X, Y, Z On-Leakage Current (Note 7)	$I_{W(ON)}$, $I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V+ = 5.5V; V_W, V_X, V_Y, V_Z = 1V, 4.5V_; $V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 1V, 4.5V, or floating	+25°C	-2		+2	nA
			-40°C to +85°C	-20		+20	
DYNAMIC							
Enable Turn-On Time (MAX4691/MAX4692/MAX4693)	t_{ON}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		90	130	ns
			-40°C to +85°C			150	
Enable Turn-Off Time (MAX4691/MAX4692/MAX4693)	t_{OFF}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		45	60	ns
			-40°C to +85°C			70	
Address Transition Time	t_{TRANS}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0, 3V; R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		100	140	ns
			-40°C to +85°C			160	
Break-Before-Make	t_{BBM}	$V_{W\_}$, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V; R_L = 300Ω, C_L = 35pF, Figure 4	+25°C	2	35		ns
			-40°C to +85°C	2			
Charge Injection	Q	V_{GEN} = 0; R_{GEN} = 0; C_L = 1nF, Figure 5	+25°C		0.2		pC

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.5V to +5.5V, V- = 0, V_{IH} = +2V, V_{IL} = +0.8V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Off-Isolation (Note 8)	V_{ISO}	f = 0.1MHz, R_L = 50Ω, C_L = 5pF Figure 6	+25°C		-80		dB
Crosstalk (Note 9)	V_{CT}	f = 0.1MHz, R_L = 50Ω, C_L = 5pF Figure 6	+25°C		-87		dB
DIGITAL I/O							
Input Logic-High	V_{IH}			2			V
Input Logic-Low	V_{IL}					0.8	V
Input Leakage Current	$I_{LEAKAGE}$	$V_{IN\_}$ = 0 or V+		-1		+1	µA
SUPPLY							
Positive Supply Current	I+	V+ = 5.5V; $V_{IN\_}$ = 0 or V+	+25°C			0.1	µA
			-40°C to +85°C	-1		1	

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (MAX4691/MAX4692/MAX4693 only)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{IH} = +2V, V_{IL} = +0.8V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_X, V_Y, V_Z, $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$		-40°C to +85°C	V-		V+	V
On-Resistance (Note 5)	R_{ON}	V+ = 4.5V; I_X, I_Y, I_Z = 10mA; V- = -4.5V; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3.5V	+25°C		18	25	Ω
			-40°C to +85°C			30	
On-Resistance Match Between Channels (Notes 5, 6)	ΔR_{ON}	V+ = 4.5V; V- = -4.5V; I_X, I_Y, I_Z = 10mA; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3.5V	+25°C		2	3	Ω
			-40°C to +85°C			4	
On-Resistance Flatness (Note 10)	$R_{FLAT(ON)}$	V+ = 4.5V; V- = -4.5V; I_X, I_Y, I_Z = 10mA; V_X, V_Y, V_Z = 3.5V, 0, -3.5V	+25°C		2.5	3.5	Ω
			-40°C to +85°C			4	
X_ , Y_, Z_ Off-Leakage Current (Note 7)	$I_{X\_}$, $I_{Y\_}$, $I_{Z\_}$	V+ = 5.5V; V- = -5.5V; V_X, V_Y, V_Z = ±4.5V; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = ±4.5V	+25°C	-1		+1	nA
			-40°C to +85°C	-10		+10	
X, Y, Z Off-Leakage Current (Note 7)	$I_{X\ (OFF)}$, $I_{Y(OFF)}$, $I_{Z(OFF)}$	V+ = 5.5V; V- = -5.5V; V_X, V_Y, V_Z = ±4.5V; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = ±4.5V	+25°C	-2		+2	nA
			-40°C to +85°C	-20		+20	

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

ELECTRICAL CHARACTERISTICS—Dual ±5V Supplies (continued) (MAX4691/MAX4692/MAX4693 only)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{IH} = +2V, V_{IL} = +0.8V, T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
X, Y, Z On-Leakage Current (Note 7)	$I_{X(ON)}$, $I_{Y(ON)}$, $I_{Z(ON)}$	V+ = 5.5V; V- = -5.5V; V_X, V_Y, V_Z = ±4.5V; $V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = ±4.5V, or unconnected	+25°C	-2		2	nA
			-40°C to +85°C	-20		20	
DYNAMIC							
Enable Turn-On Time	t_{ON}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		55	80	ns
			-40°C to +85°C			90	
Enable Turn-Off Time	t_{OFF}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		35	50	ns
			-40°C to +85°C			60	
Address Transition Time	t_{TRANS}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 0, 3V; R_L = 300Ω, C_L = 35pF, Figure 3	+25°C		60	90	ns
			-40°C to +85°C			100	
Break-Before-Make	t_{BBM}	$V_{X\_}$, $V_{Y\_}$, $V_{Z\_}$ = 3V; R_L = 300Ω, C_L = 35pF, Figure 4	+25°C	2	20		ns
			-40°C to +85°C	2			
Charge Injection	Q	V_{GEN} = 0; R_{GEN} = 0; C_L = 1nF, Figure 5	+25°C		1.8		pC
Off-Isolation (Note 8)	V_{ISO}	f = 0.1MHz, R_L = 50Ω, C_L = 5pF, Figure 6	+25°C		-82		dB
Crosstalk (Note 9)	V_{CT}	f = 0.1MHz, R_L = 50Ω, C_L = 5pF, Figure 7	+25°C		-84		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, V_X, V_Y, V_Z = 5Vp-p; R_L = 600Ω,	+25°C		0.02		%
DIGITAL I/O							
Input Logic-High	V_{IH}			2			V
Input Logic-Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}	V_A, V_B, V_C, $V_{\overline{EN}}$ = 0 or V+		-1		+1	µA
SUPPLY							
Positive Supply Current	I+	V+ = 5.5V; V- = 5.5V; V_A, V_B, V_C, $V_{\overline{EN}}$ = 0 or V+	+25°C			0.1	µA
			-40°C to +85°C			1	

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.

Note 3: UCSP parts are 100% tested at T_A = +25°C. Limits across the full temperature range are guaranteed by correlation.

Note 4: QFN and TQFN parts are 100% tested at T_A = +85°C. Limits across the full temperature range are guaranteed by correlation.

Note 5: UCSP R_{ON} and R_{ON} match are guaranteed by design.

Note 6: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 7: Leakage parameters are guaranteed by design.

Note 8: Off-isolation = $20\log_{10} (V_{W,X,Y,Z} / V_{W\_,X\_,Y\_,Z\_})$, $V_{W,X,Y,Z}$ = output, $V_{W\_,X\_,Y\_,Z\_}$ = input to off switch.

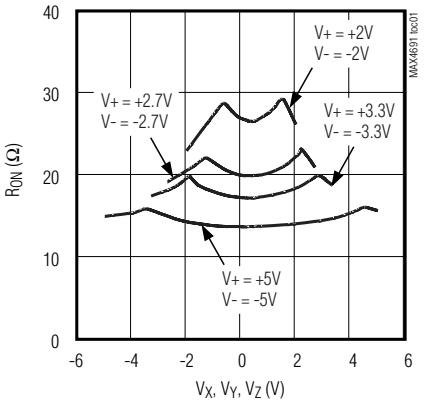
Note 9: Between any two switches.

Note 10: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

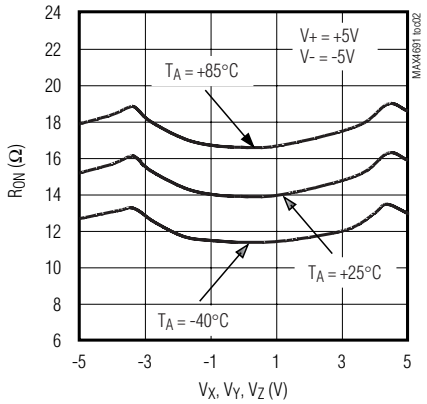
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

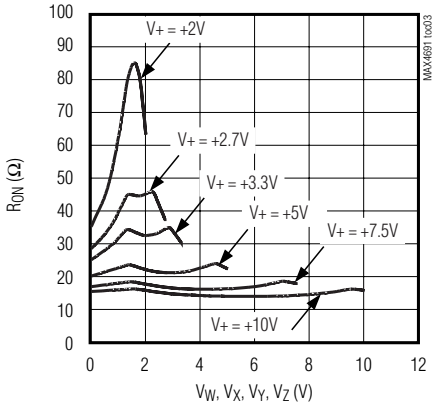
ON-RESISTANCE vs. V_X, V_Y, V_Z (DUAL SUPPLIES)



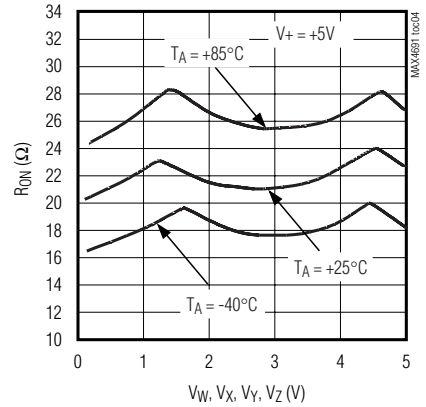
ON-RESISTANCE vs. V_X, V_Y, V_Z AND TEMPERATURE (DUAL SUPPLIES)



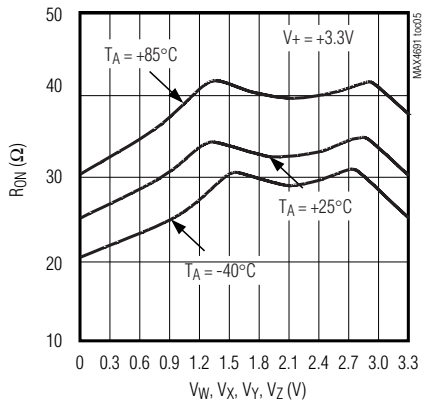
ON-RESISTANCE vs. V_W, V_X, V_Y, V_Z (SINGLE SUPPLY)



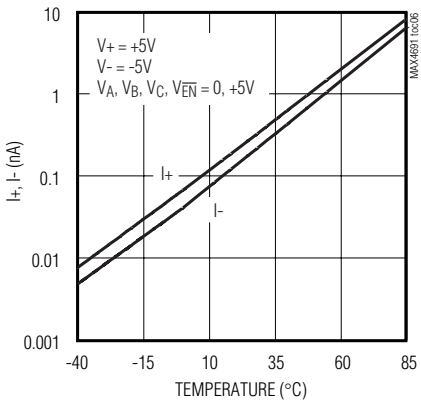
ON-RESISTANCE vs. V_W, V_X, V_Y, V_Z AND TEMPERATURE (SINGLE SUPPLY)



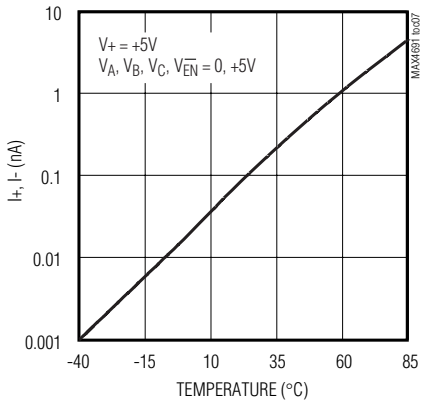
ON-RESISTANCE vs. V_W, V_X, V_Y, V_Z AND TEMPERATURE (SINGLE SUPPLY)



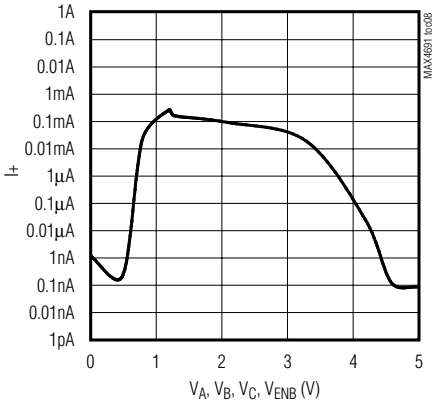
SUPPLY CURRENT vs. TEMPERATURE (DUAL SUPPLIES)



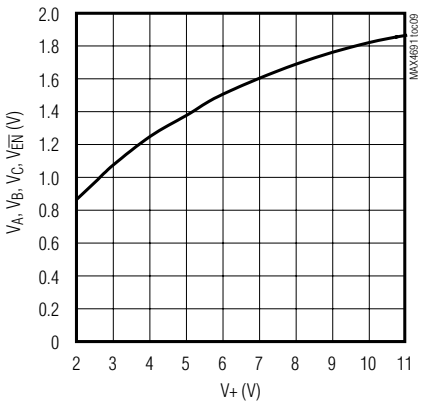
SUPPLY CURRENT vs. TEMPERATURE (SINGLE SUPPLY)



I+ vs. LOGIC LEVEL



LOGIC-LEVEL THRESHOLD vs. V+

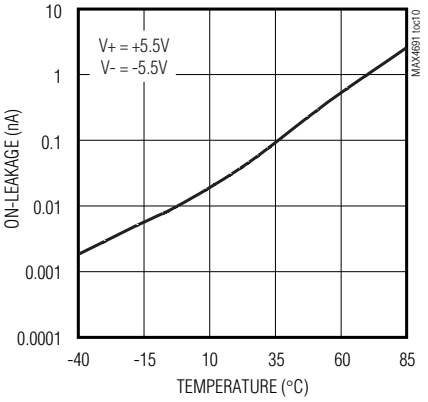


Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

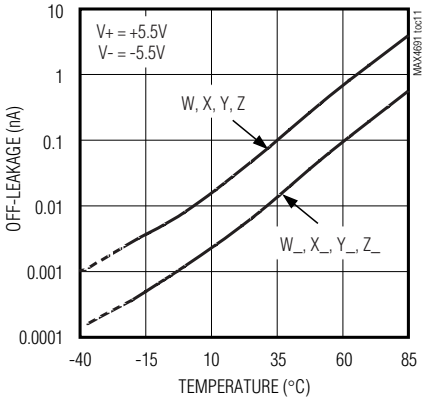
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

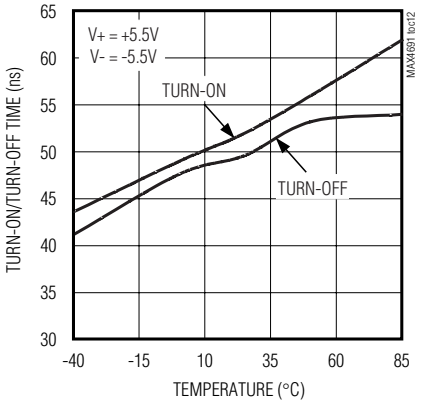
ON-LEAKAGE CURRENT vs. TEMPERATURE



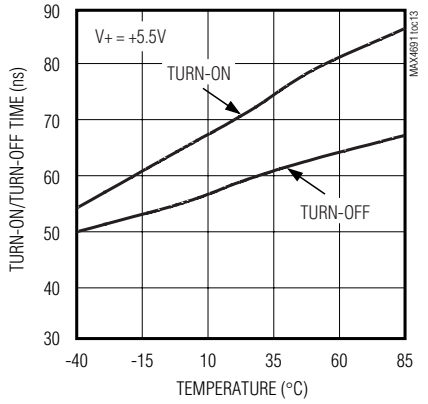
OFF-LEAKAGE CURRENT vs. TEMPERATURE



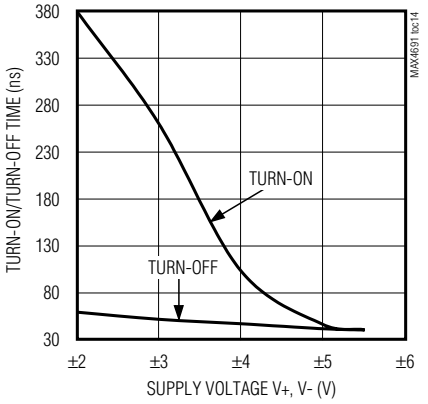
TURN-ON/TURN-OFF TIME vs. TEMPERATURE (DUAL SUPPLY)



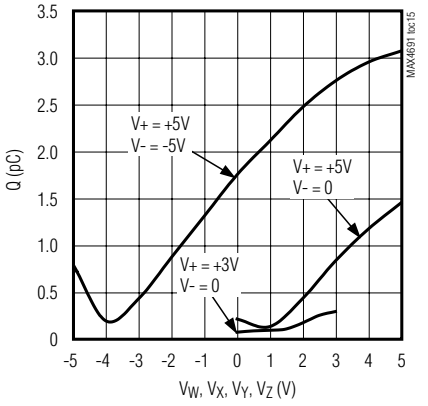
TURN-ON/TURN-OFF TIME vs. TEMPERATURE (SINGLE SUPPLY)



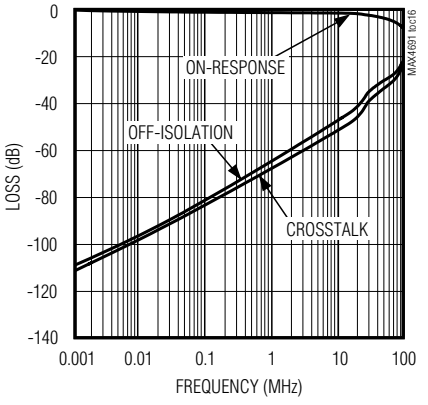
TURN-ON/TURN-OFF TIME vs. SUPPLY VOLTAGE



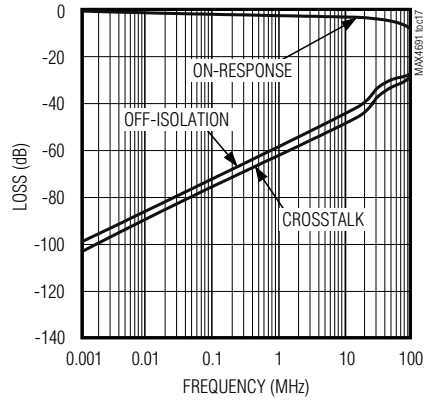
CHARGE INJECTION vs. V_W, V_X, V_Y, V_Z



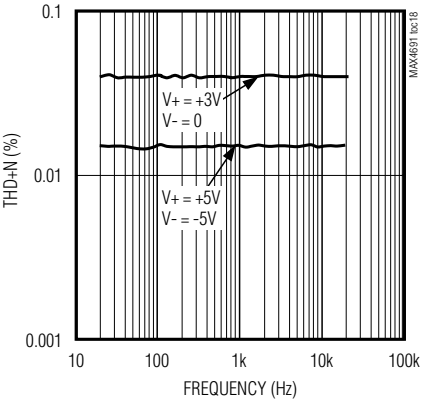
FREQUENCY RESPONSE vs. ±5V SUPPLIES



FREQUENCY RESPONSE vs. +3V SUPPLIES



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



Pin Description

MAX4691

PIN		NAME	FUNCTION
UCSP	QFN-EP/ TQFN-EP		
A4, B4, C4, D4, A1, B1, C1, D1	16, 1, 3, 4, 12, 11, 9, 8	X0–X7	Analog Switch Inputs 0–7
A2	13	X	Analog Switch Common
D3, D2, A3	5, 7, 15	A, B, C	Digital Address Inputs
B2	14	V-	Negative Analog Supply Voltage Input. Connect V- to GND for single-supply operation.
B3	2	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
C2	10	$\overline{EN}$	Digital Enable Input. Normally connect $\overline{EN}$ to GND. $\overline{EN}$ can be driven to logic high to set all switches off.
C3	6	V+	Positive Analog and Digital Supply Voltage Input
—	—	EP	Exposed Pad. Connect EP to V+.

MAX4692

PIN		NAME	FUNCTION
UCSP	QFN-EP/ TQFN-EP		
A1, B1, C1, D1	12, 11, 9, 8	X0–X3	Analog Switch “X” Inputs 0–3
A4, B4, C4, D4	16, 1, 3, 4	Y0–Y3	Analog Switch “Y” Inputs 0–3
A2	13	X	Analog Switch “X” Common
A3	15	Y	Analog Switch “Y” Common
D3, D2	5, 7	A, B	Digital Address Inputs for both “X” and “Y” Analog Switches
B2	14	V-	Negative Analog Supply Voltage Input. Connect V- to GND for single-supply
B3	2	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
C2	10	$\overline{EN}$	Digital Enable Input. Normally connect $\overline{EN}$ to GND. $\overline{EN}$ can be driven to logic high to set all switches off.
C3	6	V+	Positive Analog and Digital Supply Voltage Input
—	—	EP	Exposed Pad. Connect EP to V+.

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

Pin Description (continued)

MAX4693

PIN		NAME	FUNCTION
UCSP	QFN-EP/ TQFN-EP		
A1	12	X0	Analog Switch “X” Normally Closed Input
B1	11	X1	Analog Switch “X” Normally Open Input
A4	16	Y0	Analog Switch “Y” Normally Closed Input
B4	1	Y1	Analog Switch “Y” Normally Open Input
D1	8	Z0	Analog Switch “Z” Normally Closed Input
C1	9	Z1	Analog Switch “Z” Normally Open Input
A2	13	X	Analog Switch “X” Common
A3	15	Y	Analog Switch “Y” Common
D2	7	Z	Analog Switch “Z” Common
C4	3	A	Analog Switch “X” Digital Control Input
D4	4	B	Analog Switch “Y” Digital Control Input
D3	5	C	Analog Switch “Z” Digital Control Input
B2	14	V-	Negative Analog Supply Voltage Input. Connect V- to GND for single-supply operation.
B3	2	GND	Ground. Connect GND to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
C2	10	$\overline{EN}$	Digital Enable Input. Normally connect $\overline{EN}$ to GND. $\overline{EN}$ can be driven to logic high to set all switches off.
C3	6	V+	Positive Analog and Digital Supply Voltage Input
—	—	EP	Exposed Pad. Connect EP to V+.

Pin Description (continued)

MAX4694

PIN		NAME	FUNCTION
USCP	QFN-EP/ TQFN-EP		
D4	4	W0	Analog Switch “W” Normally Closed Input
C4	3	W1	Analog Switch “W” Normally Open Input
A1	12	X0	Analog Switch “X” Normally Closed Input
B1	11	X1	Analog Switch “X” Normally Open Input
A4	16	Y0	Analog Switch “Y” Normally Closed Input
B4	1	Y1	Analog Switch “Y” Normally Open Input
D1	8	Z0	Analog Switch “Z” Normally Closed Input
C1	9	Z1	Analog Switch “Z” Normally Open Input
D3	5	W	Analog Switch “W” Common
A2	13	X	Analog Switch “X” Common
A3	15	Y	Analog Switch “Y” Common
D2	7	Z	Analog Switch “Z” Common
B2	14	GND	Ground
B3	2	A	Analog Switch “W” and “Y” Digital Control Input
C2	10	B	Analog Switch “X” and “Z” Digital Control Input
C3	6	V+	Positive Analog and Digital Supply Voltage Input
—	—	EP	Exposed Pad. Connect EP to V+.

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

Table 1. Truth Table/Switch Programming

$\overline{EN}$[1]	ADDRESS BITS			ON SWITCHES			
	C[2]	B	A	MAX4691	MAX4692	MAX4693	MAX4694
1	X	X	X	All switches open	All switches open	All switches open	—
0	0	0	0	X-X0	X-X0, Y-Y0	X-X0, Y-Y0, Z-Z0	W-W0, X-X0, Y-Y0, Z-Z0
0	0	0	1	X-X1	X-X1, Y-Y1	X-X1, Y-Y0, Z-Z0	W-W1, X-X0, Y-Y1, Z-Z0
0	0	1	0	X-X2	X-X2, Y-Y2	X-X0, Y-Y1, Z-Z0	W-W0, X-X1, Y-Y0, Z-Z1
0	0	1	1	X-X3	X-X3, Y-Y3	X-X1, Y-Y1, Z-Z0	W-W1, X-X1, Y-Y1, Z-Z1
0	1	0	0	X-X4	X-X0, Y-Y0	X-X0, Y-Y0, Z-Z1	W-W0, X-X0, Y-Y0, Z-Z0
0	1	0	1	X-X5	X-X1, Y-Y1	X-X1, Y-Y0, Z-Z1	W-W1, X-X0, Y-Y1, Z-Z0
0	1	1	0	X-X6	X-X2, Y-Y2	X-X0, Y-Y1, Z-Z1	W-W0, X-X1, Y-Y0, Z-Z1
0	1	1	1	X-X7	X-X3, Y-Y3	X-X1, Y-Y1, Z-Z1	W-W1, X-X1, Y-Y1, Z-Z1

X = Don't care

1. EN is not present on the MAX4694.

2. C is not present on the MAX4692 and MAX4694.

Detailed Description

The MAX4691–MAX4694 are low-voltage CMOS analog ICs configured as an 8-channel multiplexer (MAX4691), two 4-channel multiplexers (MAX4692), three SPDT switches (MAX4693), and four SPDT switches (MAX4694). All switches are bidirectional.

The MAX4691/MAX4692/MAX4693 operate from either a single +2V to +11V power supply or dual ±2V to ±5.5V power supplies. When operating from ±5V supplies they offer 25Ω on-resistance (R_{ON}), 3.5Ω max R_{ON} flatness, and 3Ω max matching between channels. The MAX4694 operates from a single +2V to +11V supply. Each switch has rail-to-rail signal handling, fast switching times of t_{ON} = 80ns, t_{OFF} = 50ns, and a low 1nA leakage current.

All digital inputs are 1.8V logic-compatible when operating from a +3V supply and TTL-compatible when operating from a +5V supply.

Digital Inputs

The MAX4691 and MAX4692 include address pins that allow control of the multiplexers. For the MAX4691, pins A, B, C determine which switch is closed. The two 4-1 muxes in the MAX4692 are controlled by the same address pins (A and B). (Table 1)

The MAX4693 and MAX4694 offer SPDT switches in triple and quadruple packages. In the MAX4693, each switch has a unique control input. The MAX4694 has two digital control inputs: A (for switches "W" and "Y") and B (for switches "X" and "Z"). (Table 1)

Applications Information

Power-Supply Considerations

Overview

The MAX4691–MAX4694 construction is typical of most CMOS analog switches. V+ and V-* are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct.

**V- is found only on the MAX4691/MAX4692/MAX4693.*

During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog signal path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and V- signals to drive the gates of the analog signals. This drive signal is the only connection between the logic supplies (and signals) and the analog supplies. V+ and V- have ESD-protection diodes on GND.

Bipolar Supplies

The MAX4691/MAX4692/MAX4693 operate with bipolar supplies between ±2V and ±5.5V. The V+ and V- supplies need not be symmetrical, but their difference cannot exceed the absolute maximum rating of +12V.

Single Supply

These devices operate from a single supply between +2V and +11V when V- is connected to GND. All of the bipolar precautions must be observed. At room temperature, they operate with a single supply at near or below +2V, although as supply voltage decreases, switch on-resistance and switching times become very high.

Always bypass supplies with a 0.1µF capacitor.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs and by W, X, Y, Z. If power-supply sequencing is not possible, add two small signal diodes (D1, D2) in series with the supply pins for overvoltage protection (Figure 1).

Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 12V. These protection diodes are not recommended when using a single supply if signal levels must extend to ground.

UCSP Reliability

The chip-scale package (UCSP) represents a unique package that greatly reduces board space compared to other packages. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering a UCSP. Performance through Operating Life Test and Moisture Resistance is equal to conventional package technology as it is primarily determined by the wafer-fabrication process. However, this form factor may not perform equally to a packaged product through traditional mechanical reliability tests.

Mechanical stress performance is a greater consideration for a UCSP. UCSP solder joint contact integrity must be considered since the package is attached through direct solder contact to the user's PC board. Testing done to characterize the UCSP reliability performance shows that it is capable of performing reliably through environmental stresses. Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website, at www.maxim-ic.com.

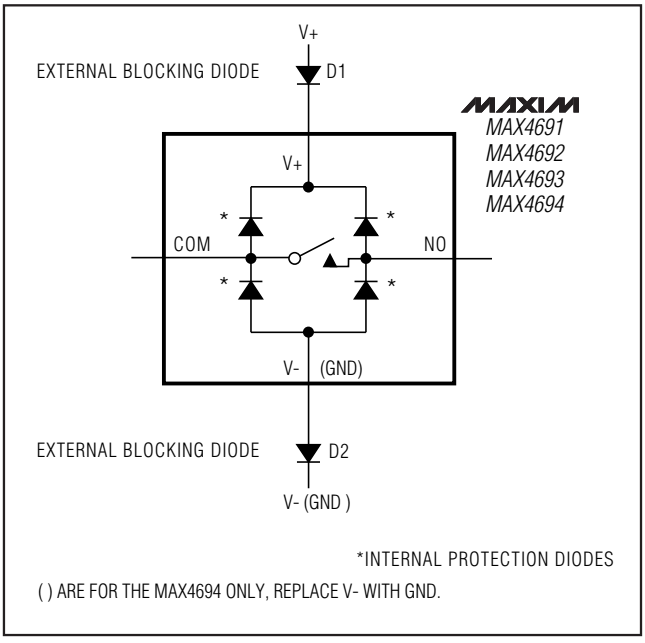
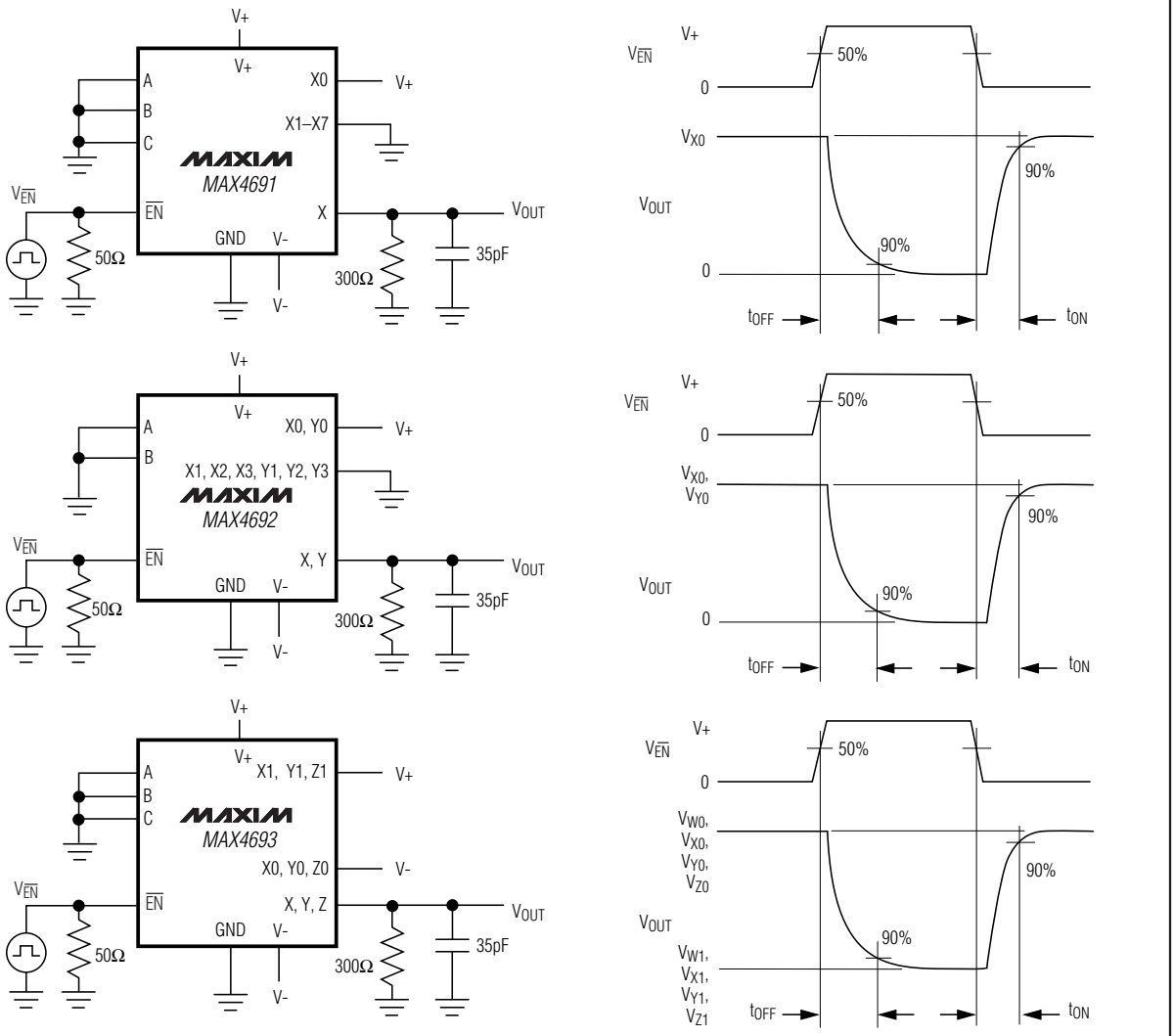


Figure 1. Overvoltage Protection

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

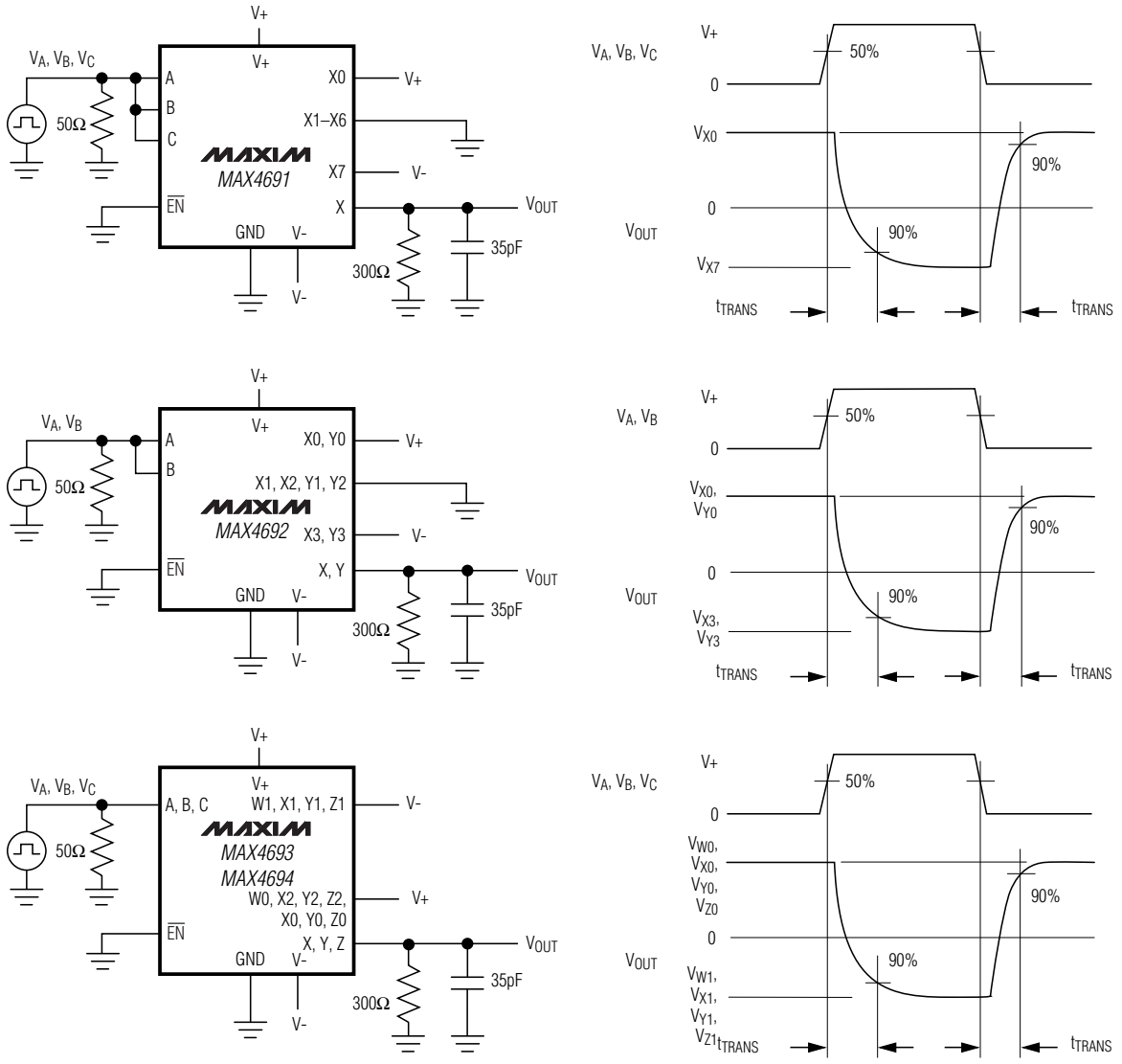
Test Circuits/Timing Diagrams



V- = 0 FOR SINGLE-SUPPLY OPERATION.
TEST EACH SECTION INDIVIDUALLY.

Figure 2. Enable Transition Time

Test Circuits/Timing Diagrams (continued)



V- = 0 FOR SINGLE-SUPPLY OPERATION. (NOT PRESENT ON THE MAX4694)
TEST EACH SECTION INDIVIDUALLY.

Figure 3. Address Transition Time

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

Test Circuits/Timing Diagrams (continued)

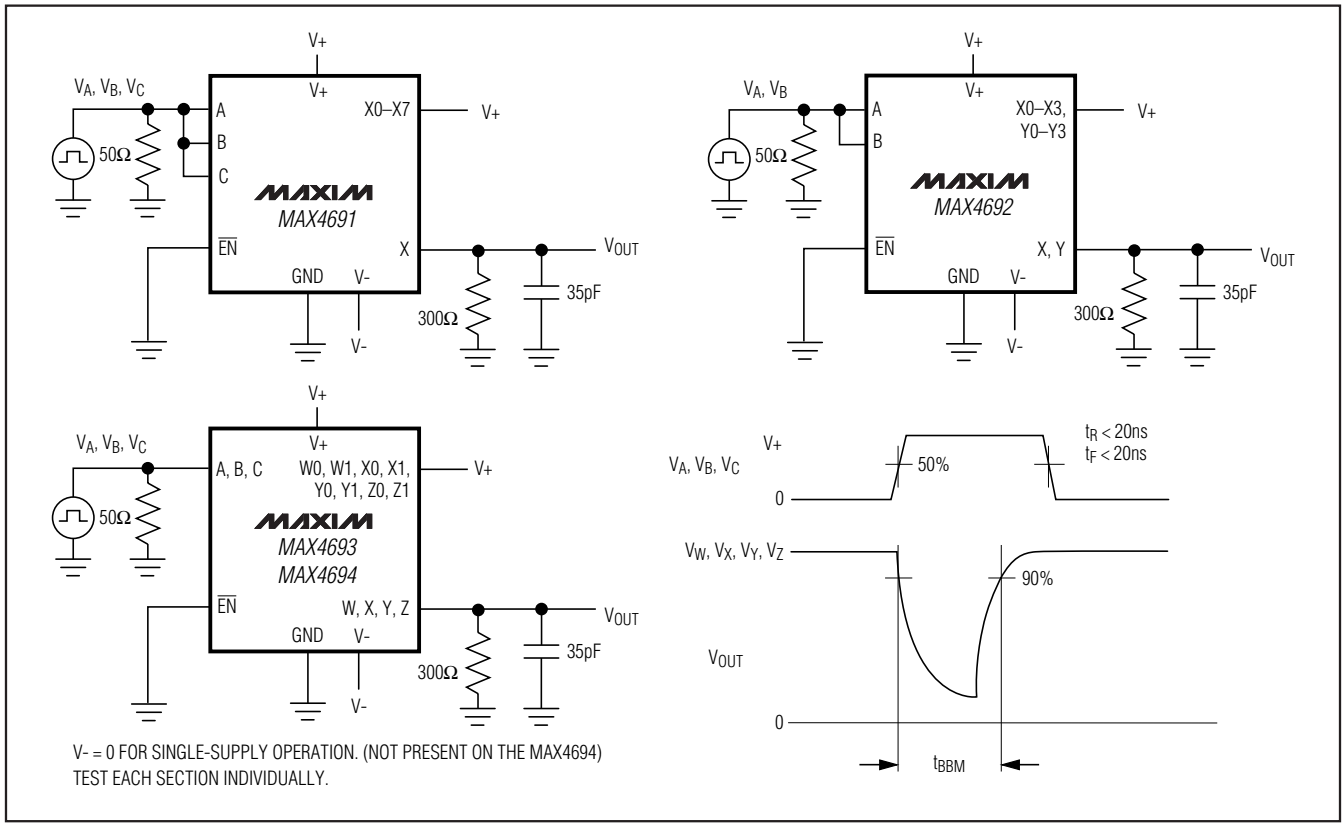


Figure 4. Break-Before-Make Interval

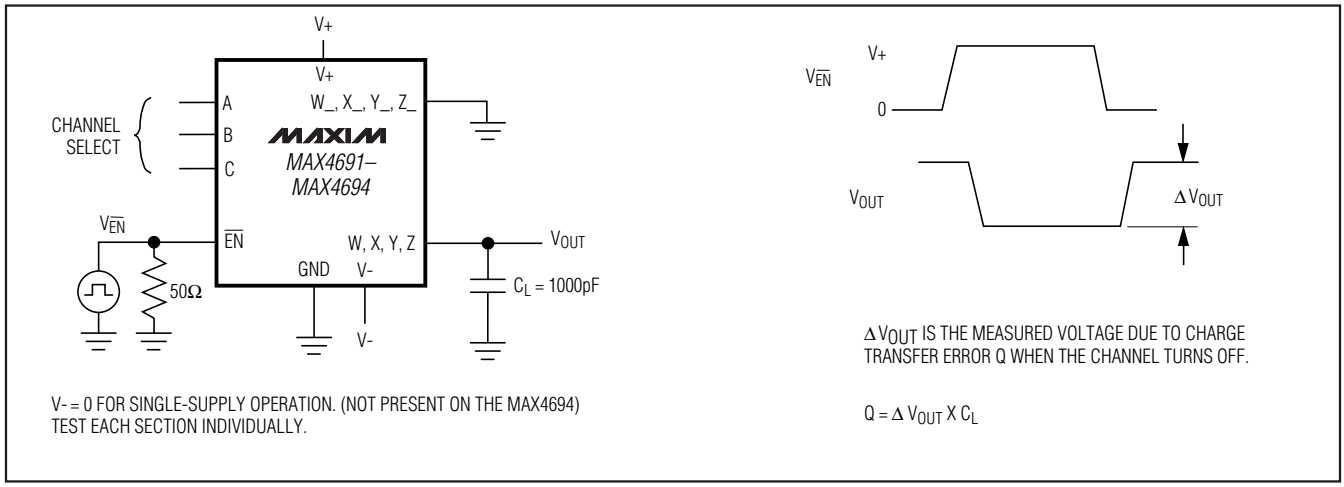
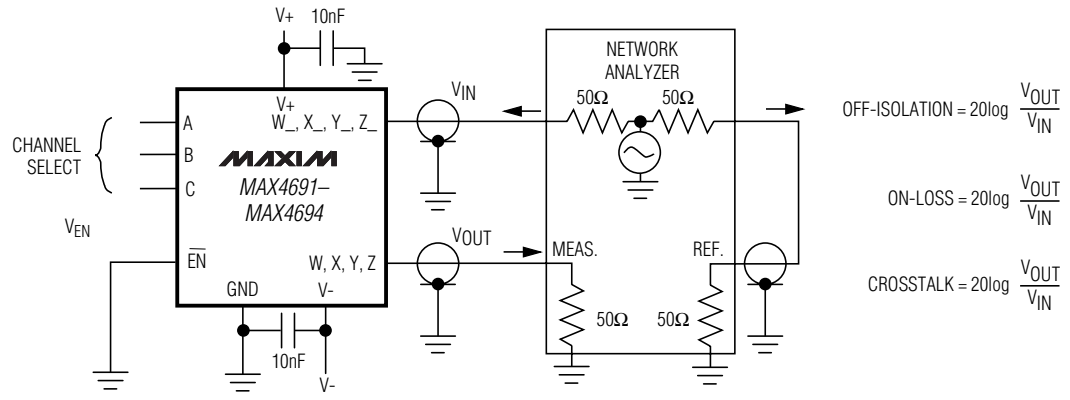


Figure 5. Charge Injection

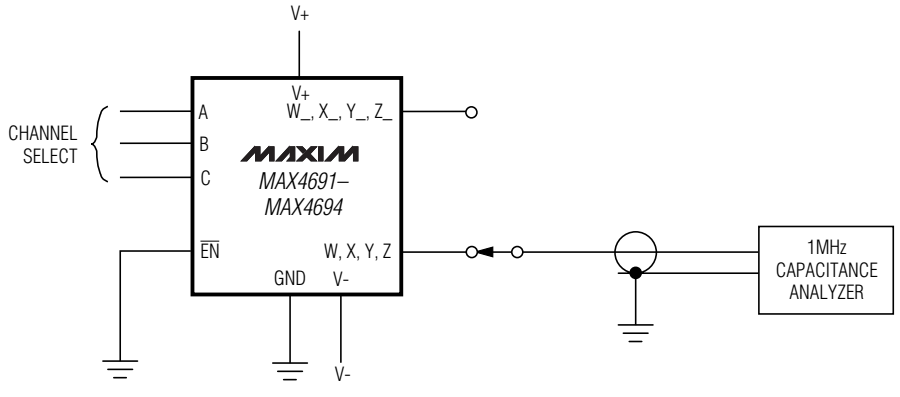
Test Circuits/Timing Diagrams (continued)



MEASUREMENTS ARE STANDARDIZED AGAINST SHORT AT SOCKET TERMINALS.
OFF-ISOLATION IS MEASURED BETWEEN COM AND "OFF" NO TERMINAL ON EACH SWITCH.
ON LOSS IS MEASURED BETWEEN COM AND "ON" NO TERMINAL ON EACH SWITCH.
CROSSTALK IS MEASURED FROM ONE CHANNEL (A, B, C) TO ALL OTHER CHANNELS.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

V- IS NOT PRESENT ON THE MAX4694.

Figure 6. Off-Isolation, On-Loss, and Crosstalk

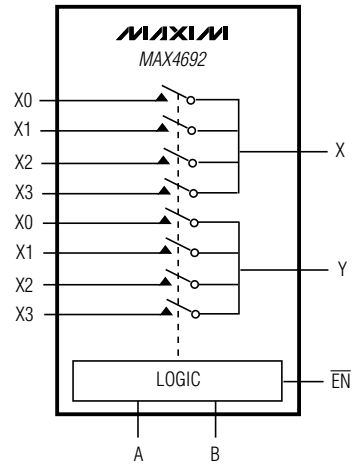


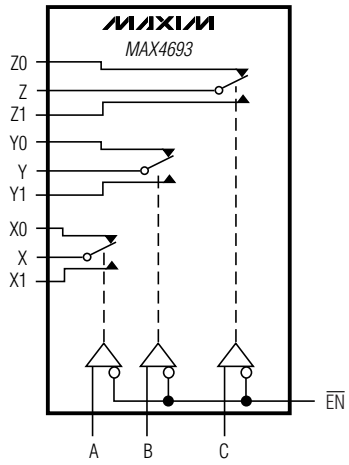
V- IS NOT PRESENT ON THE MAX4694.

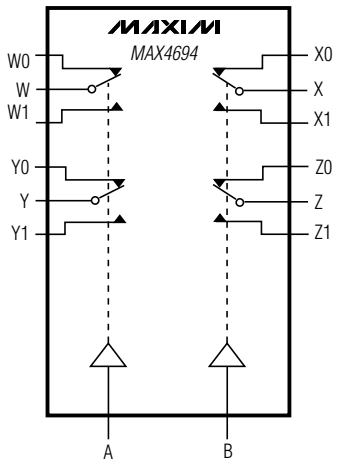
Figure 7. Capacitance

Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

Functional Diagrams (continued)







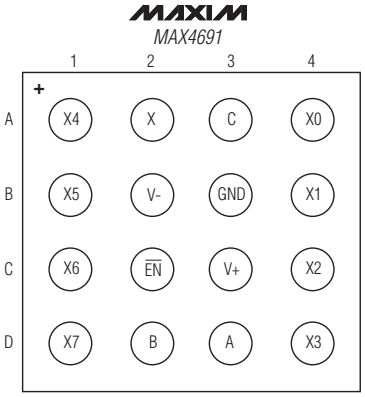
Chip Information

PROCESS: BiCMOS

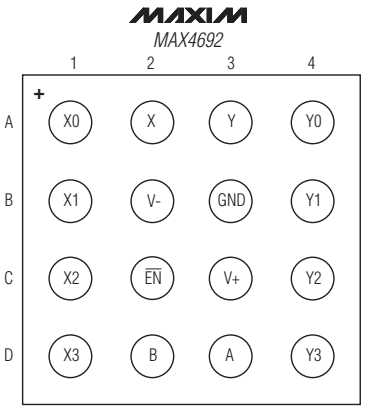
Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

Pin Configurations

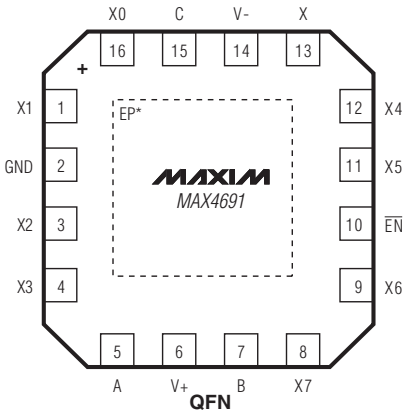
TOP VIEW



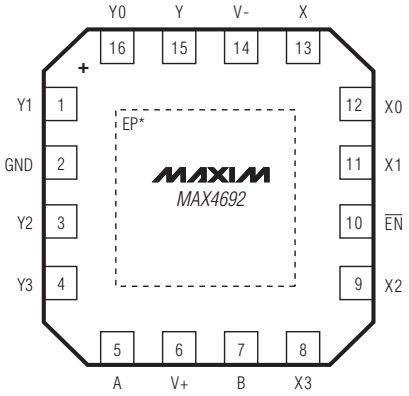
UCSP



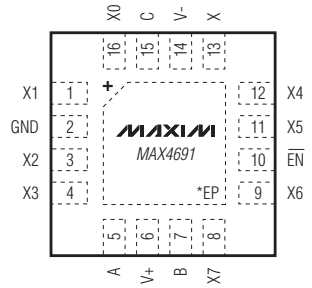
UCSP



QFN
*EXPOSED PAD.
CONNECT EP TO V+.



QFN
*EXPOSED PAD.
CONNECT EP TO V+.



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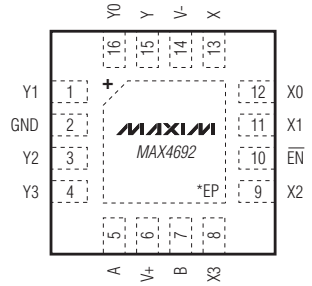
CONNECT EP TO V+.

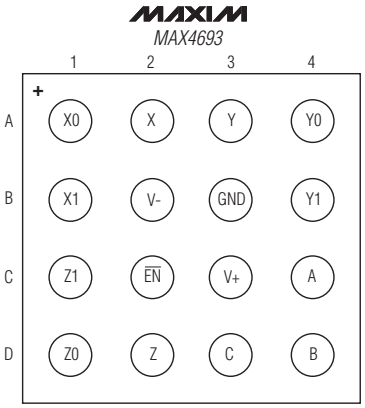


TQFN
*EXPOSED PAD.
CONNECT EP TO V+.

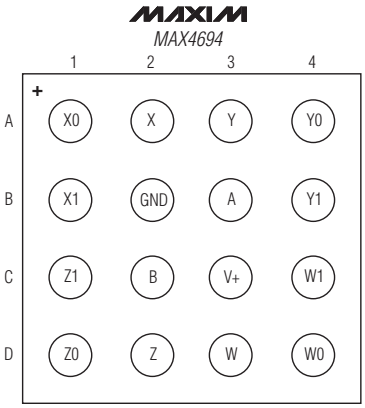
Low-Voltage 8:1 Mux/Dual 4:1 Mux/Triple SPDT/ Quad SPDT in UCSP Package

Pin Configurations (continued)

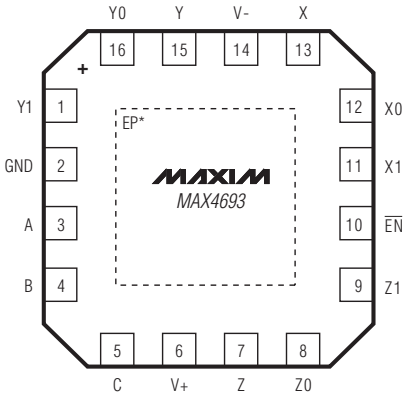
TOP VIEW



UCSP



UCSP



QFN
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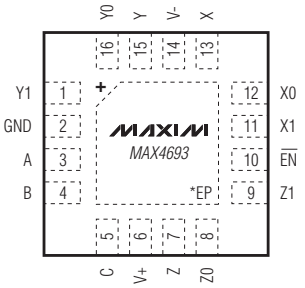
CONNECT EP TO V+.



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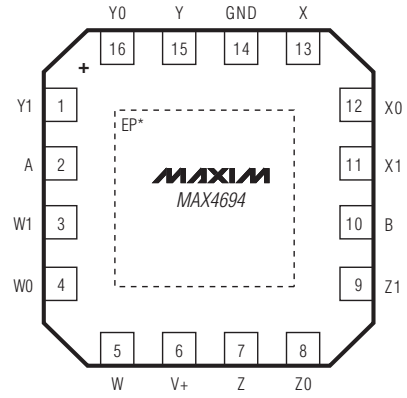
CONNECT EP TO V+.



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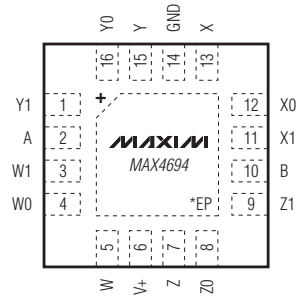
CONNECT EP TO V+.



TQFN
*EXPOSED PAD.
CONNECT EP TO V+..

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 QFN	B16+1	**21-0101**
16 TQFN-EP	G1644+1	**21-0106**
16 UCSP	T1644+4	**21-0139**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/01	Initial release	—
1	7/01	Added UCSP Package	—
2	2/03	Removed statement in *Features* section with UCSP now qualified	—
3	12/06	Exposed Paddle Connection information edited, style changes	1, 9, 10, 11, 19, 21, 22
4	8/08	Added part numbers, package diagram, and TQFN packaging	1–26
5	3/09	Added lead-free packaging, edited *Pin Description*, revised *Chip Information*, changed “floating” to “unconnected,” style changes	1–6, 9, 10, 11, 18–21