19-1612; Rev 0; 3/00

Ultra-Small, +1.8V, µPower, Rail-to-Rail I/O Op Amps

General Description

The MAX4291/MAX4292/MAX4294 family of micropower operational amplifiers operates from a +1.8V to +5.5V single supply or ±0.9V to ±2.75V dual supplies and has Rail-to-Rail® input/output capabilities. These amplifiers provide a 500kHz gain-bandwidth product and 120dB open-loop voltage gain while using only 100µA of supply current per amplifier. The combination of low input offset voltage (±400µV) and high-open-loop gain makes them suitable for low-power/low-voltage high-precision applications.

The MAX4291/MAX4292/MAX4294 have an input common-mode range that extends to each supply rail, and their outputs typically swing within 20mV of the rails with a 2kΩ load. Although the minimum operating voltage is specified at +1.8V, these devices typically operate down to +1.5V. The combination of ultra-low-voltage operation, rail-to-rail inputs/output, and low-power consumption makes these devices ideal for any portable/two-cell battery-powered system.

The single MAX4291 is offered in an ultra-small 5-pin SC70 package and the dual MAX4292 is offered in a space-saving 8-pin µMAX package.

Applications

- 2-Cell Battery-Operated Systems
- Portable Electronic Equipment
- Battery-Powered Instrumentation
- Digital Scales
- Strain Gauges
- Sensor Amplifiers
- Cellular Phones

Selector Guide

PART	AMPLIFIERS PER PACKAGE	PIN-PACKAGE
MAX4291	1	5-pin SC70/SOT23
MAX4292	2	8-pin µMAX/SO
MAX4294	4	14-pin SO/TSSOP

Features

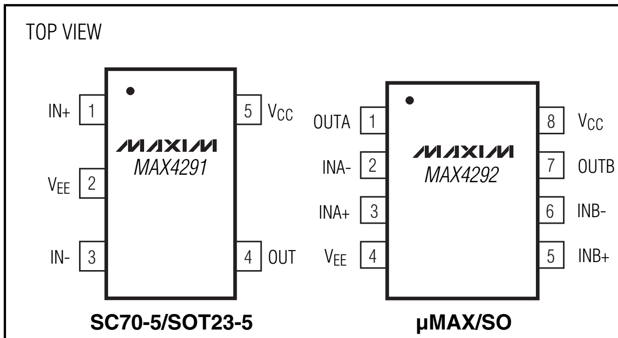
- ♦ **Ultra-Low Voltage Operation—Guaranteed Down to +1.8V**
- ♦ **100µA Supply Current per Amplifier**
- ♦ **500kHz Gain-Bandwidth Product**
- ♦ **120dB Open-Loop Voltage Gain (R_L = 100kΩ)**
- ♦ **0.017% THD + Noise at 1kHz**
- ♦ **Rail-to-Rail Input Common-Mode Range**
- ♦ **Rail-to-Rail Output Drives 2kΩ Load**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Unity-Gain Stable for Capacitive Loads up to 100pF**
- ♦ **400µV Input Offset Voltage**
- ♦ **Single Available in Ultra-Small 5-Pin SC70**
  Dual Available in Space-Saving 8-Pin µMAX

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX4291EXK-T	-40°C to +85°C	5 SC70-5	AAD
MAX4291EUK-T	-40°C to +85°C	5 SOT23-5	ADML
MAX4292EUA*	-40°C to +85°C	8 µMAX	—
MAX4292ESA*	-40°C to +85°C	8 SO	—
MAX4294ESD*	-40°C to +85°C	14 SO	—
MAX4294EUD*	-40°C to +85°C	14 TSSOP	—

**Future product—contact factory for availability.*

Pin Configurations



Pin Configurations continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})..+6V
All Other Pins ....(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration......................................Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 2.5mW/°C above +70°C) 200mW
5-Pin SOT23 (derate 7.1mW/°C above +70°C)...............571mW
8-Pin µMAX (derate 4.10mW/°C above +70°C).............330mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin TSSOP (derate 6.3mW/°C above +70°C) 500mW
Operating Temperature Range............................-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.8V to +5.5V, V_{EE} = V_{CM} = 0, V_{OUT} = V_{CC} / 2, R_L = 100kΩ connected to V_{CC} / 2, **T_A = +25°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from PSRR test		1.8		5.5	V
Quiescent Supply Current (per Amplifier)	I_Q	V_{CC} = 1.8V			100	210	µA
		V_{CC} = 5.0V			110	225	
Input Offset Voltage	V_{OS}	MAX4291EXK, MAX4291EUK			±400	±2500	µV
		MAX4292EUA, MAX4294EUD			±400	±1500	
		MAX4292ESA, MAX4294ESD			±400	±1500	
Input Bias Current	I_B	V_{CC} = 5.0V, 0 ≤ V_{CM} ≤ 5.0V			±15	±55	nA
Input Offset Current	I_{OS}	V_{CC} = 5.0V, 0 ≤ V_{CM} ≤ 5.0V			±1	±7	nA
Differential Input Resistance	R_{IN}	$\lvert V_{IN+} - V_{IN-} \rvert$ < 10mV			0.75		MΩ
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test		0		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	Tested for 0 ≤ V_{CM} ≤ 1.8V; V_{CC} = 1.8V	MAX4291EXK, MAX4291EUK	50	80		dB
			MAX4292EUA, MAX4294EUD	65	85		
			MAX4292ESA, MAX4294ESD	65	85		
		Tested for 0 ≤ V_{CM} ≤ 5.0V, V_{CC} = 5.0V	MAX4291EXK, MAX4291EUK	60	90		dB
			MAX4292EUA, MAX4294EUD	70	90		
			MAX4292ESA, MAX4294ESD	70	90		
Power-Supply Rejection Ratio	PSRR	MAX4291EXK, MAX4291EUK		80	100		dB
		MAX4292EUA, MAX4294EUD		80	100		
		MAX4292ESA, MAX4294ESD		80	100		

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.8V to +5.5V, V_{EE} = V_{CM} = 0, V_{OUT} = V_{CC} / 2, R_L = 100kΩ connected to V_{CC} / 2, **T_A = +25°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_V	V_{CC} = 1.8V	R_L = 100kΩ, 0.015V ≤ V_{OUT} ≤ V_{CC} - 0.015V	80	120		dB
			R_L = 2kΩ, 0.1V ≤ V_{OUT} ≤ V_{CC} - 0.1V	80	110		
		V_{CC} = 5.0V	R_L = 100kΩ, 0.015V ≤ V_{OUT} ≤ V_{CC} - 0.015V	80	130		
			R_L = 2kΩ, 0.1V ≤ V_{OUT} ≤ V_{CC} - 0.1V	80	120		
Output Voltage Swing High	V_{OH}	Specified as $\|V_{CC} - V_{OH}\|$	R_L = 100kΩ to V_{CC} / 2		2	20	mV
			R_L = 2kΩ to V_{CC} / 2		15	40	
Output Voltage Swing Low	V_{OL}	Specified as $\|V_{EE} - V_{OL}\|$	R_L = 100kΩ to V_{CC} / 2		3	15	mV
			R_L = 2kΩ to V_{CC} / 2		18	40	
Output Short-Circuit Current	$I_{OUT(SC)}$	Sourcing or sinking			20		mA
Channel-to-Channel Isolation	CH_{ISO}	Specified at f = 10kHz (MAX4292/MAX4294 only)			100		dB
Gain Bandwidth Product	GBW				500		kHz
Phase Margin	ϕ_M				65		degrees
Gain Margin	G_M				12		dB
Slew Rate	SR				0.2		V/µs
Input Voltage Noise Density	e_n	f = 10kHz			70		nV/√Hz
Input Current Noise Density	i_n	f = 10kHz			0.05		pA/√Hz
Capacitive-Load Stability		A_{VCL} = +1V/V, no sustained oscillations			100		pF

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.8V to +5.5V, V_{EE} = V_{CM} = 0, V_{OUT} = V_{CC} / 2, R_L = 100kΩ connected to V_{CC} / 2, **T_A = T_{MIN} to T_{MAX}**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from PSRR test	1.8		5.5	V
Quiescent Supply Current (per Amplifier)	I_Q	V_{CC} = 1.8V			240	µA
		V_{CC} = 5.0V			270	
Input Offset Voltage	V_{OS}	MAX4291EXK, MAX4291EUK			±3000	µV
		MAX4292EUA, MAX4294EUD			±1500	
		MAX4292ESA, MAX4294ESD			±1500	

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.8V to +5.5V, V_{EE} = V_{CM} = 0, V_{OUT} = V_{CC} / 2, R_L = 100kΩ connected to V_{CC} / 2, **T_A = T_{MIN} to T_{MAX}**, unless otherwise noted.) (Note 1)

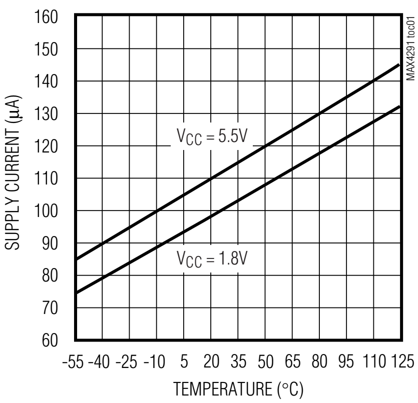
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage Drift	TCV_{OS}				1.2		µV/°C
Input Bias Current	I_B	V_{CC} = 5.0V, 0 ≤ V_{CM} ≤ 5.0V				±80	nA
Input Offset Current	I_{OS}	V_{CC} = 5.0V, 0 ≤ V_{CM} ≤ 5.0V				±10	nA
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test		0		V_{CC}	V
Common-Mode Rejection Ratio	CMRR	Tested for 0 ≤ V_{CM} ≤ 1.8V, V_{CC} = 1.8V	MAX4291EXK, MAX4291EUK	50			dB
			MAX4292EUA, MAX4294EUD	60			
			MAX4292ESA, MAX4294ESD	60			
		Tested for 0 ≤ V_{CM} ≤ 5.0V, V_{CC} = 5.0V	MAX4291EXK, MAX4291EUK	60			dB
			MAX4292EUA, MAX4294EUD	65			
			MAX4292ESA, MAX4294ESD	65			
Power-Supply Rejection Ratio	PSRR	MAX4291EXK, MAX4291EUK		78			dB
		MAX4292EUA, MAX4294EUD		80			
		MAX4292ESA, MAX4294ESD		80			
Large-Signal Voltage Gain	A_V	V_{CC} = 1.8V	R_L = 100kΩ, 0.015V ≤ V_{OUT} ≤ V_{CC} - 0.015V	80			dB
			R_L = 2kΩ, 0.1V ≤ V_{OUT} ≤ V_{CC} - 0.1V	80			
		V_{CC} = 5.0V	R_L = 100kΩ, 0.015V ≤ V_{OUT} ≤ V_{CC} - 0.015V	80			
			R_L = 2kΩ, 0.1V ≤ V_{OUT} ≤ V_{CC} - 0.1V	80			
Output Voltage Swing High	V_{OH}	Specified as $\|V_{CC} - V_{OH}\|$	R_L = 100kΩ to V_{CC} / 2			20	mV
			R_L = 2kΩ to V_{CC} / 2			40	
Output Voltage Swing Low	V_{OL}	Specified as $\|V_{EE} - V_{OL}\|$	R_L = 100kΩ to V_{CC} / 2			15	mV
			R_L = 2kΩ to V_{CC} / 2			40	

Note 1: All devices are 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.

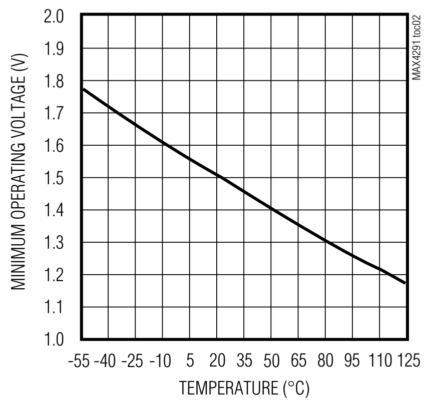
Typical Operating Characteristics

(V_{CC} = +2.4V, V_{EE} = V_{CM} = 0, V_{OUT} = V_{CC} / 2, no load, T_A = +25°C, unless otherwise noted.)

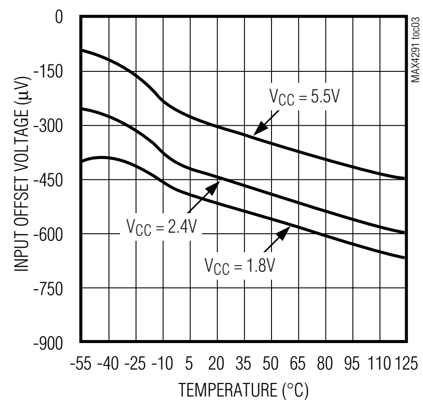
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



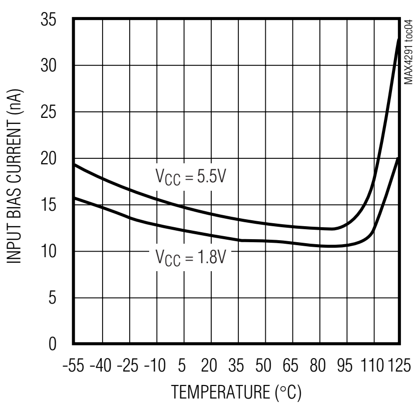
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE (PSRR ≥80dB)



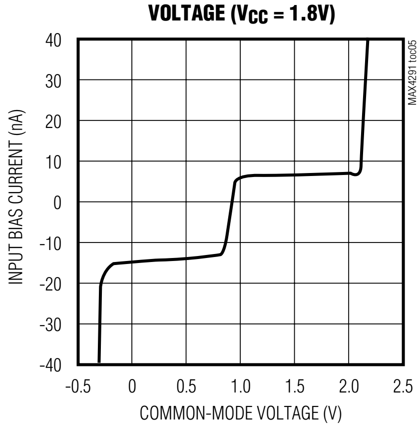
INPUT OFFSET VOLTAGE vs. TEMPERATURE



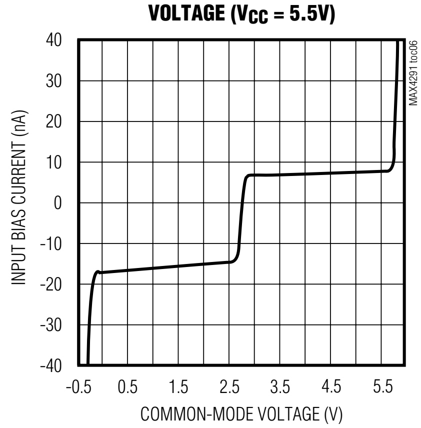
INPUT BIAS CURRENT vs. TEMPERATURE



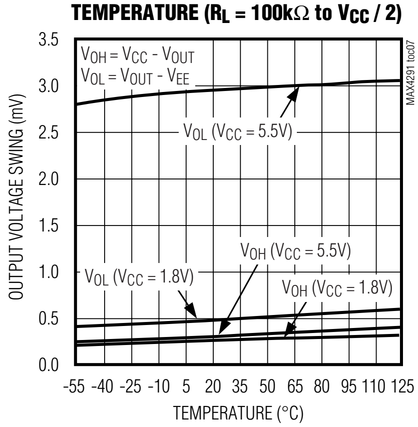
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE (V_{CC} = 1.8V)



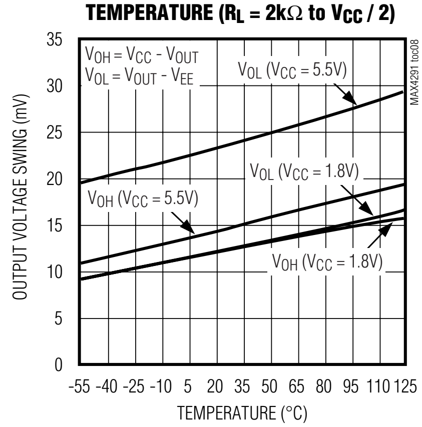
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE (V_{CC} = 5.5V)



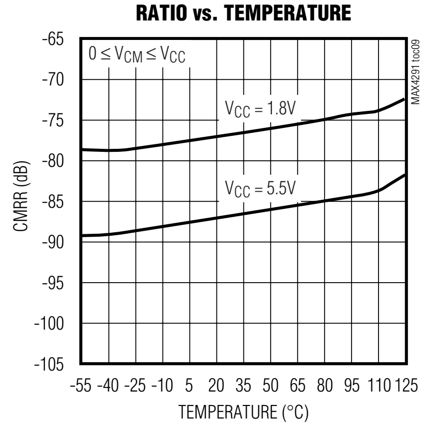
OUTPUT VOLTAGE SWING vs. TEMPERATURE (R_L = 100kΩ to V_{CC} / 2)



OUTPUT VOLTAGE SWING vs. TEMPERATURE (R_L = 2kΩ to V_{CC} / 2)



COMMON-MODE REJECTION RATIO vs. TEMPERATURE

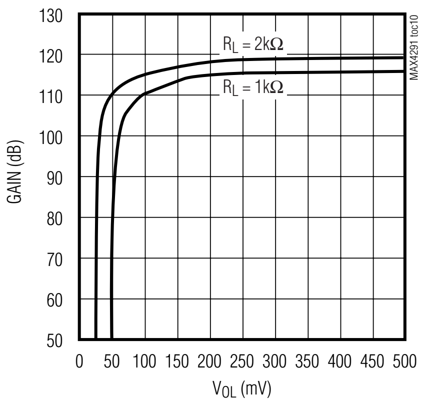


Ultra-Small, +1.8V, µPower, Rail-to-Rail I/O Op Amps

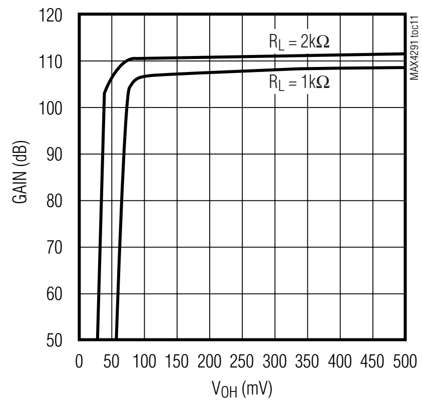
Typical Operating Characteristics (continued)

(V_{CC} = +2.4V, V_{EE} = V_{CM} = 0, V_{OUT} = V_{CC} / 2, no load, T_A = +25°C, unless otherwise noted.)

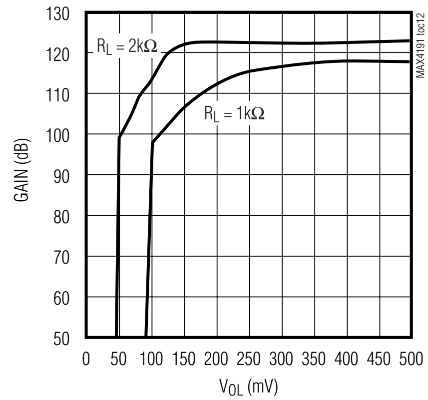
OPEN-LOOP GAIN vs. OUTPUT SWING LOW (V_{CC} = +1.8V, R_L CONNECTED TO V_{CC})



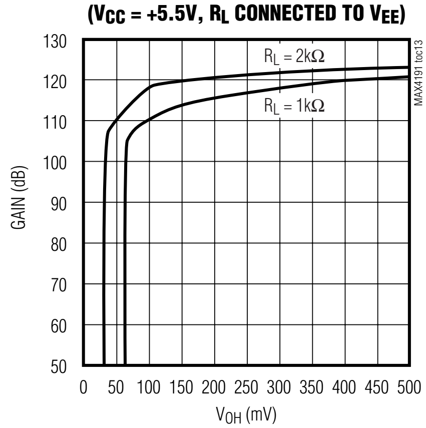
OPEN-LOOP GAIN vs. OUTPUT SWING HIGH (V_{CC} = +1.8V, R_L CONNECTED TO V_{EE})



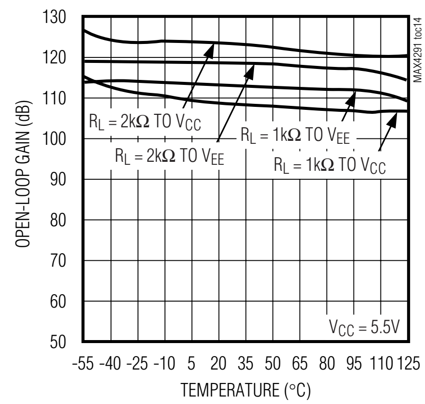
OPEN-LOOP GAIN vs. OUTPUT SWING LOW (V_{CC} = +5.5V, R_L CONNECTED TO V_{CC})



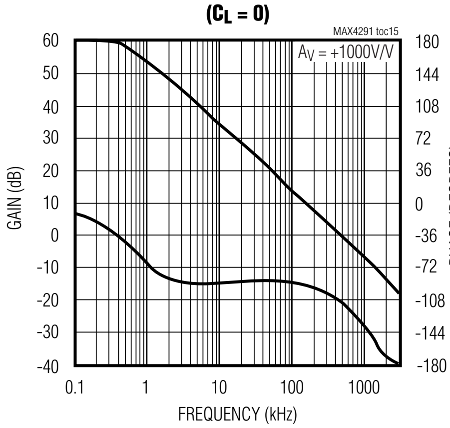
OPEN-LOOP GAIN vs. OUTPUT SWING HIGH (V_{CC} = +5.5V, R_L CONNECTED TO V_{EE})



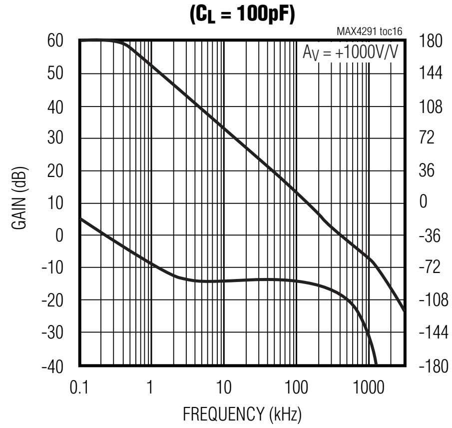
OPEN-LOOP GAIN vs. TEMPERATURE



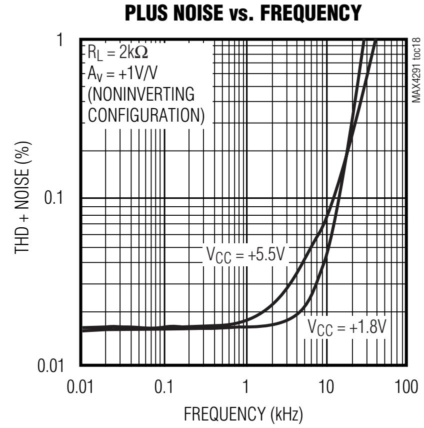
GAIN AND PHASE vs. FREQUENCY (C_L = 0)



GAIN AND PHASE vs. FREQUENCY (C_L = 100pF)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY

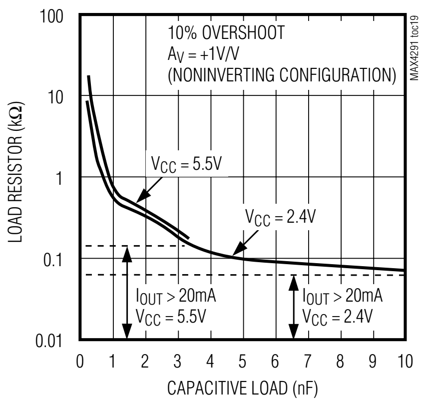


MAXIM

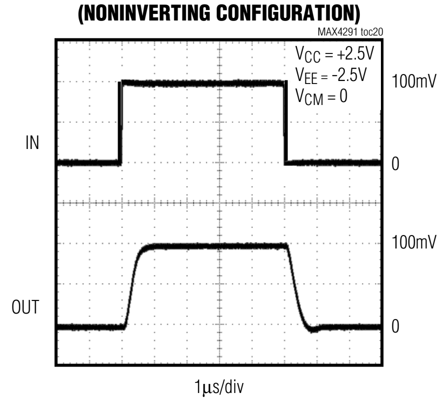
Typical Operating Characteristics (continued)

(V_{CC} = +2.4V, V_{EE} = V_{CM} = 0, V_{OUT} = V_{CC} / 2, no load, T_A = +25°C, unless otherwise noted.)

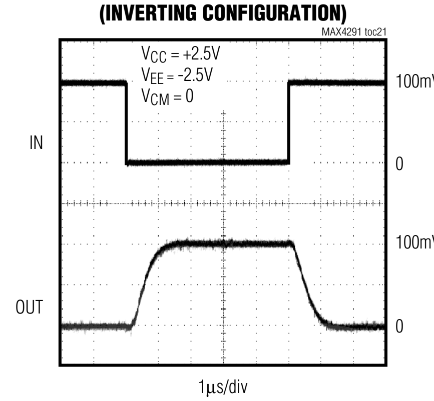
LOAD RESISTOR vs. CAPACITIVE LOAD



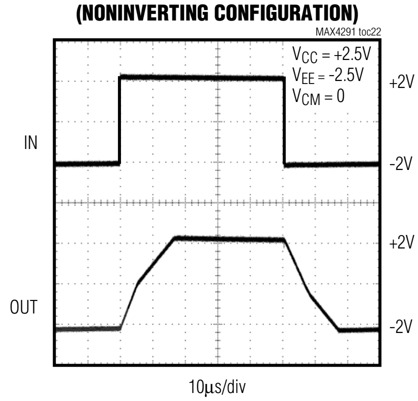
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING CONFIGURATION)



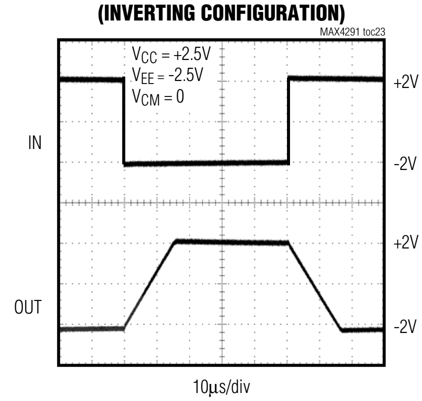
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING CONFIGURATION)



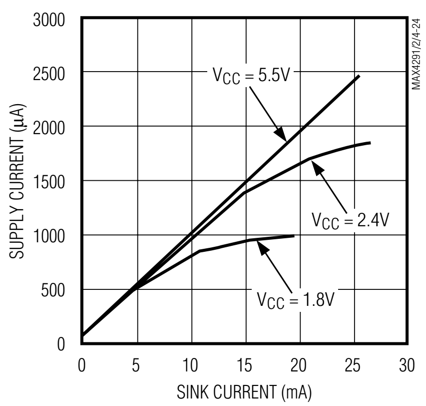
LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING CONFIGURATION)



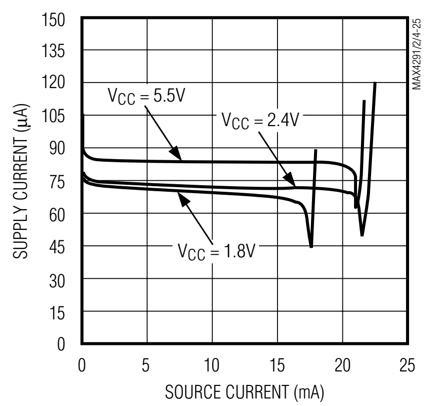
LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING CONFIGURATION)



SUPPLY CURRENT vs. SINK CURRENT



SUPPLY CURRENT vs. SOURCE CURRENT



Pin Description

PIN			NAME	FUNCTION
MAX4291	MAX4292	MAX4294		
1	–	–	IN+	Noninverting Input
2	4	11	V_{EE}	Negative Supply. Connect to ground for single-supply operation.
3	–	–	IN-	Inverting Input
4	–	–	OUT	Amplifier Output
5	8	4	V_{CC}	Positive Supply
–	1, 7	1, 7	OUTA, OUTB	Outputs for Amplifiers A and B
–	2, 6	2, 6	INA-, INB-	Inverting Inputs to Amplifiers A and B
–	3, 5	3, 5	INA+, INB+	Noninverting Inputs to Amplifiers A and B
–	–	8, 14	OUTC, OUTD	Outputs for Amplifiers C and D
–	–	9, 13	INC-, IND-	Inverting Inputs to Amplifiers C and D
–	–	10, 12	INC+, IND+	Noninverting Inputs to Amplifiers C and D

Detailed Description

Rail-to-Rail Input Stage

The MAX4291/MAX4292/MAX4294 have rail-to-rail inputs and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which operate together to provide a common-mode range extending to both supply rails. The crossover region of these two pairs occurs halfway between V_{CC} and V_{EE}. The input offset voltage is typically ±400µV. Low operating supply voltage, low supply current, rail-to-rail common-mode input range, and rail-to-rail outputs make this family of operational amplifiers (op amps) an excellent choice for precision or general-purpose, low-voltage, battery-powered systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the common-mode voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error caused by input bias currents flowing through external source impedances (Figures 1a and 1b).

The combination of high source impedance plus input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that produces an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response in this case.

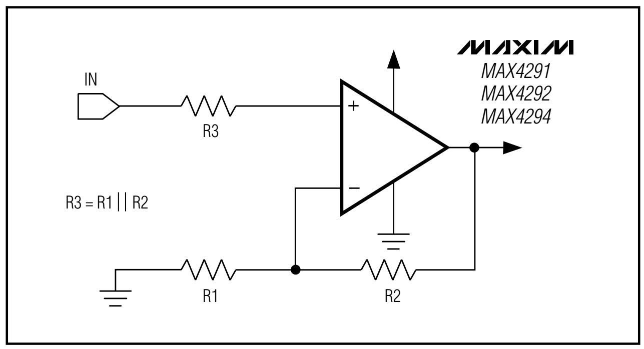


Figure 1a. Minimizing Offset Error Due to Input Bias Current (Noninverting)

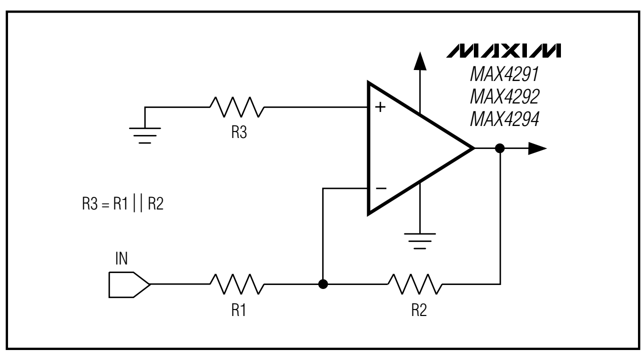


Figure 1b. Minimizing Offset Error Due to Input Bias Current (Inverting)

Table 1. MAX4291 Characteristics with Typical Battery Systems

BATTERY TYPE	RECHARGE-ABLE	V_{FRESH} (V)	$V_{END\text{-}OF\text{-}LIFE}$ (V)	CAPACITY, AA SIZE (mA-h)	MAX4291 OPERATING TIME IN NORMAL MODE (h)
Alkaline (2 cells)	No	3.0	1.8	2000	20,000
Nickel-Cadmium (2 cells)	Yes	2.4	1.8	750	7500
Lithium-Ion (1 cell)	Yes	3.5	2.7	1000	10,000
Nickel-Metal-Hydride (2 cells)	Yes	2.4	1.8	1000	10,000

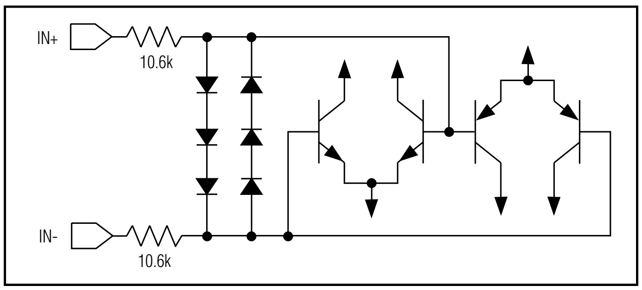


Figure 2. Input Protection Circuit

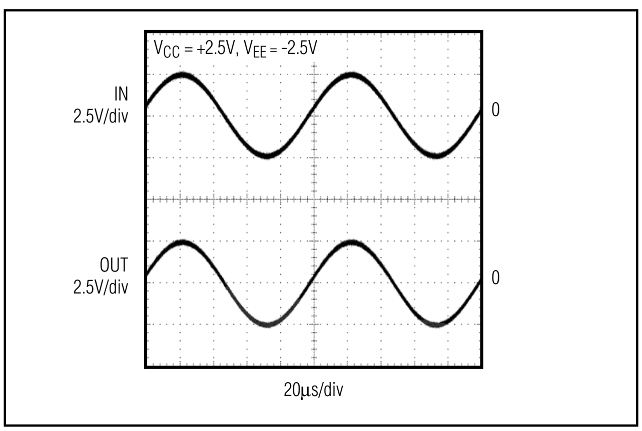


Figure 3. Rail-to-Rail Input/Output Voltage Range

The MAX4291/MAX4292/MAX4294 family's inputs are protected from large differential input voltages by internal 10.6kΩ series resistors and back-to-back triple-diode stacks across the inputs (Figure 2). For differential input voltages (much less than 1.8V), input resistance is typically 0.75MΩ. For differential input voltages greater than 1.8V, input resistance is around 21.2kΩ, and the input bias current can be approximated by the following equation:

$$I_{BIAS} = \frac{(V_{DIFF} - 1.8V)}{21.2k\Omega}$$

In the region where the differential input voltage approaches 1.8V, the input resistance decreases exponentially from 0.75MΩ to 21.2kΩ as the diode block begins to conduct. Conversely, the bias current increases with the same curve.

In unity-gain configuration, high slew rate input signals may capacitively couple to the output through the triple-diode stacks.

Rail-to-Rail Output Stage

The MAX4291/MAX4292/MAX4294 output stage can drive up to a 2kΩ load and still swing to within 20mV of the rails. Figure 3 shows the output voltage swing of a MAX4291 configured as a unity-gain buffer, powered from a ±2.5V supply. The output for this setup typically swings from (V_{EE} + 3mV) to (V_{CC} - 2mV) with a 100kΩ load.

Applications Information

Power-Supply Considerations

The MAX4291/MAX4292/MAX4294 operate from a single +1.8V to +5.5V supply (or dual ±0.9V to ±2.75V supplies) and consume only 100µA of supply current per amplifier. A high power-supply rejection ratio of 80dB allows the amplifiers to be powered directly off a decaying battery voltage, simplifying design and extending battery life.

The MAX4291/MAX4292/MAX4294 are ideally suited for use with most battery-powered systems. Table 1 lists a variety of typical battery types showing voltage when fresh, voltage at end-of-life, capacity, and approximate operating time from a MAX4291 (assuming nominal conditions).

Ultra-Small, +1.8V, µPower, Rail-to-Rail I/O Op Amps

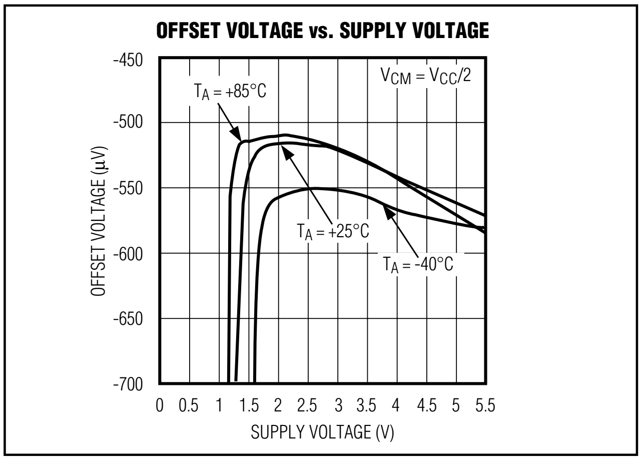


Figure 4. Offset Voltage vs. Supply Voltage

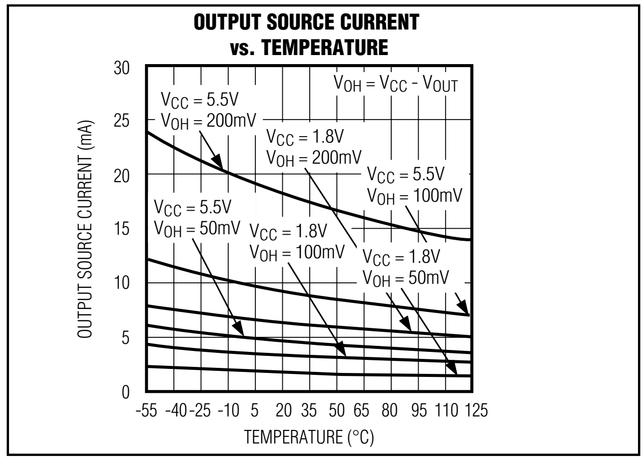


Figure 6a. Output Source Current vs. Temperature

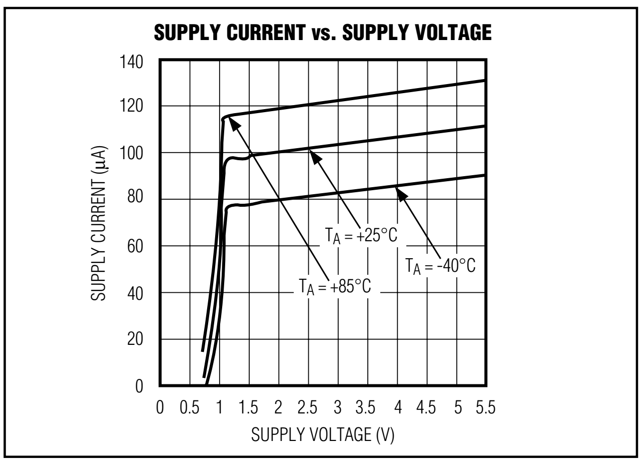


Figure 5. Supply Current vs. Supply Voltage

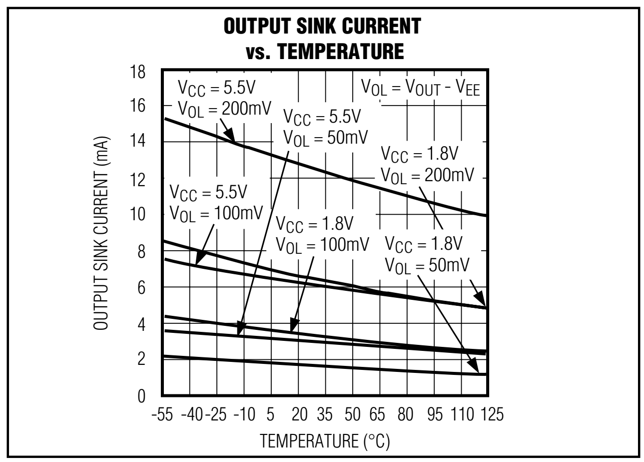


Figure 6b. Output Sink Current vs. Temperature

Although the amplifiers are fully guaranteed over temperature for operation down to a +1.8V single supply, even lower voltage operation is possible in practice. Figures 4 and 5 show the offset voltage and supply current as a function of supply voltage and temperature.

Load-Driving Capability

The MAX4291/MAX4292/MAX4294 are fully guaranteed over temperature and supply voltage range to drive a maximum resistive load of 2kΩ to $V_{CC}/2$, although heavier loads can be driven in many applications. The rail-to-rail output stage of the amplifier can be modeled as a current source when driving the load toward V_{CC}, and as a current sink when driving the load toward V_{EE}. The limit of this current source/sink varies with supply voltage, ambient temperature, and lot-to-lot variations of the units.

Figures 6a and 6b show the typical current source and sink capabilities of the MAX4291/MAX4292/MAX4294 family as a function of supply voltage and ambient temperature. The contours on the graph depict the output current value, based on driving the output voltage to within 50mV, 100mV, and 200mV of either power-supply rail.

For example, a MAX4291 running from a single +1.8V supply, operating at T_A = +25°C can source 3.5mA to within 100mV of V_{CC} and is capable of driving a 485Ω load resistor to V_{EE}:

$$R_L = \frac{(1.8V - 0.1V)}{3.5mA} = 485\Omega \text{ to } V_{EE}$$

The same application can drive a 220kΩ load resistor when terminated in $V_{CC}/2$ (+0.9V in this case).

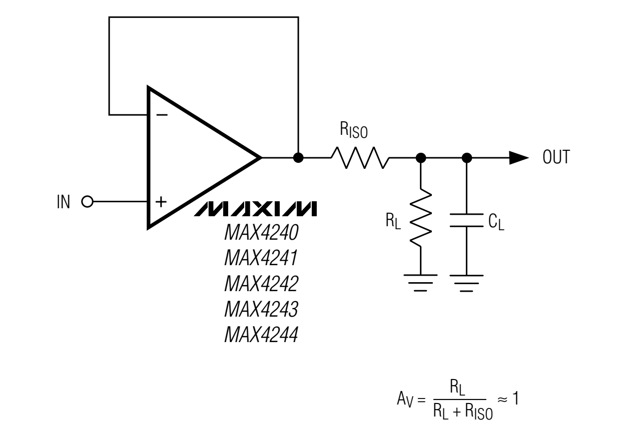


Figure 7a. Using a Resistor to Isolate a Capacitive Load from the Op Amp

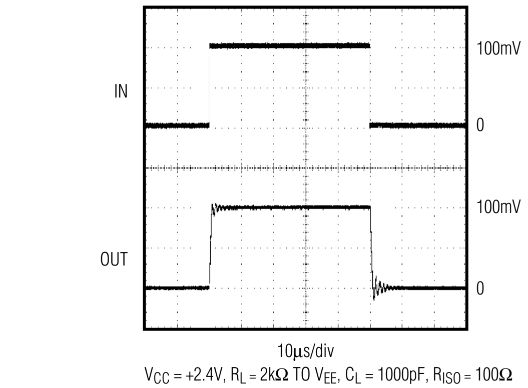


Figure 7c. Pulse Response with Isolating Resistor (100 Ω)

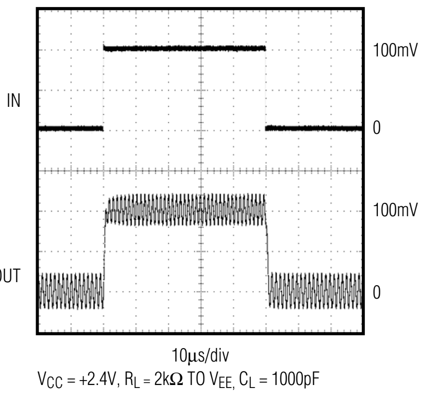


Figure 7b. Pulse Response Without Isolating Resistor

Driving Capacitive Loads

The MAX4291/MAX4292/MAX4294 are unity-gain stable for loads up to 100pF (see the Load Resistor vs. Capacitive Load graph in the *Typical Operating Characteristics*). Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load (Figure 7). Note that this alternative results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the load resistor.

Power-Supply Bypassing and Layout

The MAX4291/MAX4292/MAX4294 family operates from either a single +1.8V to +5.5V supply or dual ±0.9V to ±2.75V supplies. For single-supply operation, bypass the power supply with a 100nF capacitor to V_{EE} (in this case GND). For dual-supply operation, both the V_{CC} and the V_{EE} supplies should be bypassed to ground with separate 100nF capacitors.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close as possible to the op amp. Surface-mount components are an excellent choice.

Using the MAX4291/MAX4292/MAX4294 as Comparators

Although optimized for use as operational amplifiers, the MAX4291/MAX4292/MAX4294 can also be used as rail-to-rail I/O comparators. Typical propagation delay depends on the input overdrive voltage, as shown in Figure 8. External hysteresis can be used to minimize the risk of output oscillation. The positive feedback circuit, shown in Figure 9, causes the input threshold to change when the output voltage changes state. The two thresholds create a hysteresis band that can be calculated by the following equations:

$$V_{HYST} = V_{HI} - V_{LO}$$

$$V_{HI} = \left[1 + \frac{R1}{R2} + \frac{R1}{R_{HYST}}\right] V_{REF}$$

$$V_{LO} = V_{HI} - \left(\frac{R1}{R_{HYST}}\right) V_{CC}$$

When the output of the comparator is low, the supply current increases. The output stage has biasing circuitry to monitor the output current. When the amplifier is

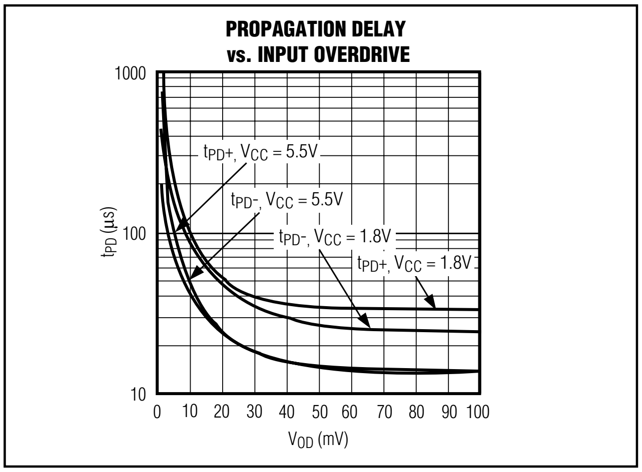


Figure 8. Propagation Delay vs. Input Overdrive

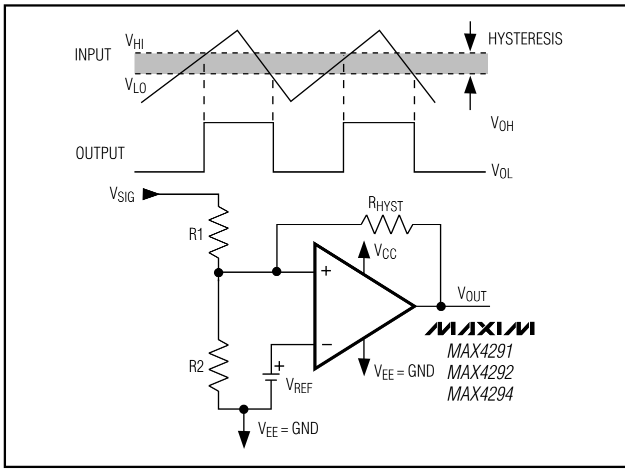


Figure 9. Hysteresis Comparator Circuit

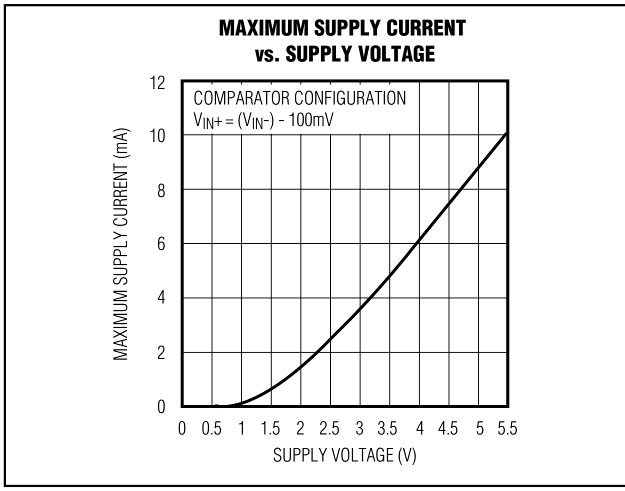


Figure 10. Maximum Supply Current vs. Supply Voltage

used as a comparator, the output stage is overdriven and the current through the biasing circuitry increases to maximum. For the MAX4291, typical supply currents increase to 1.5mA with V_{CC} = 1.8V and to 9mA when V_{CC} = 5.0V (Figure 10).

Using the MAX4291/MAX4292/MAX4294 as Low-Power Current Monitors

The MAX4291/MAX4292/MAX4294 are ideal for applications powered from a two-cell battery stack. Figure 11 shows an application circuit in which the MAX4291 is used for monitoring the current of a two-cell battery stack. In this circuit, a current load is applied, and the voltage drop at the battery terminal is sensed.

The voltage on the load side of the battery stack is equal to the voltage at the emitter of Q1 due to the feedback loop containing the op amp. As the load current increases, the voltage drop across R1 and R2 increases. Thus, R2 provides a fraction of the load current (set by the ratio of R1 and R2) that flows into the emitter of the PNP transistor. Neglecting PNP base current, this current flows into R3, producing a ground-referenced voltage proportional to the load current. To minimize errors, scale R1 to give a voltage drop that is large enough in comparison to the op amp's V_{OS}.

Calculate the output voltage of the application using the following equation:

$$V_{OUT} = \left[I_{LOAD} \times \left(\frac{R1}{R2} \right) \right] \times R3$$

For a 1V output and a current load of 50mA, the choice of resistors can be R1 = 2Ω, R2 = 100kΩ, and R3 = 1MΩ.

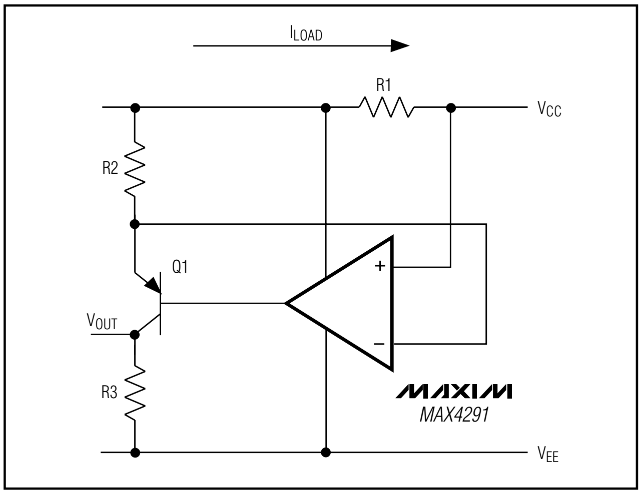
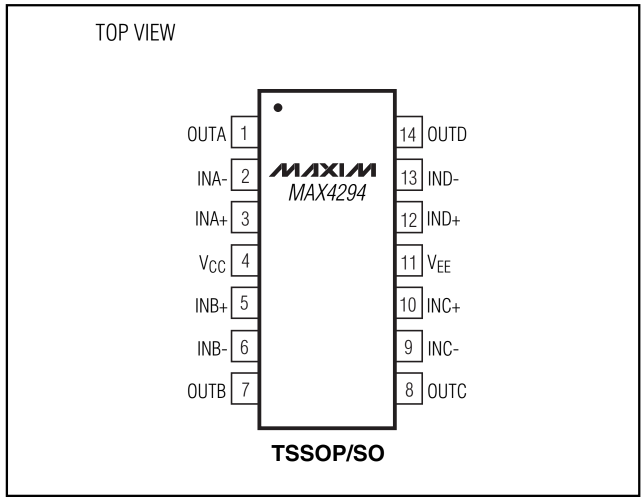


Figure 11. Current Monitor for a 2-Cell Battery Stack

Pin Configurations (continued)



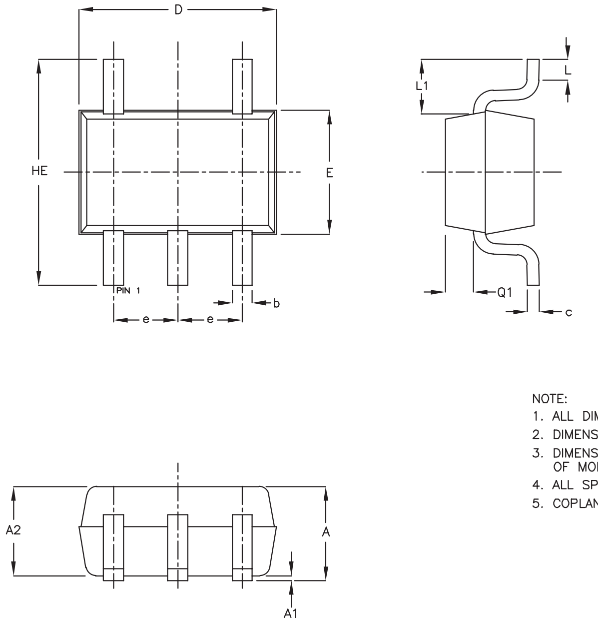
Chip Information

MAX4291 TRANSISTOR COUNT: 149

MAX4292 TRANSISTOR COUNT: 356

MAX4294 TRANSISTOR COUNT: 747

Package Information

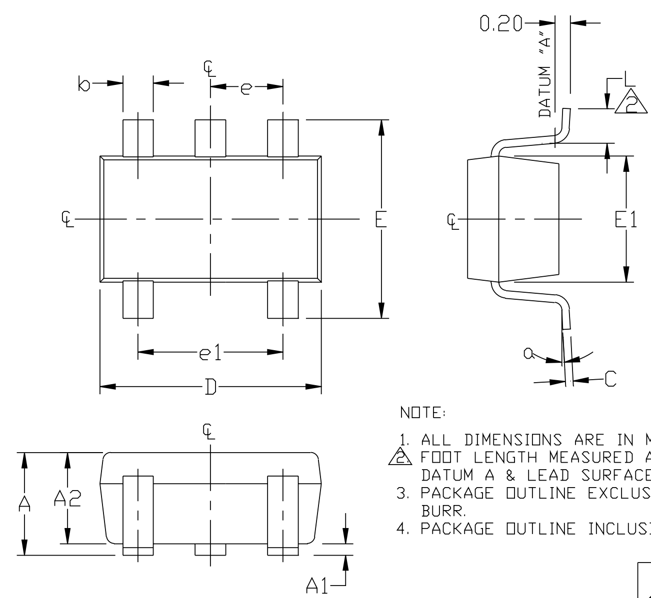


SYMBOL	MIN	MAX
e	0.65 BSC	
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425 TYP.	

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
5. COPLANARITY 4 MILS. MAX.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SC70, 5L
APPROVAL | DOCUMENT CONTROL NO. 21-0076 | REV B | 1/1

SC70, 5L.EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
a	0°	10°

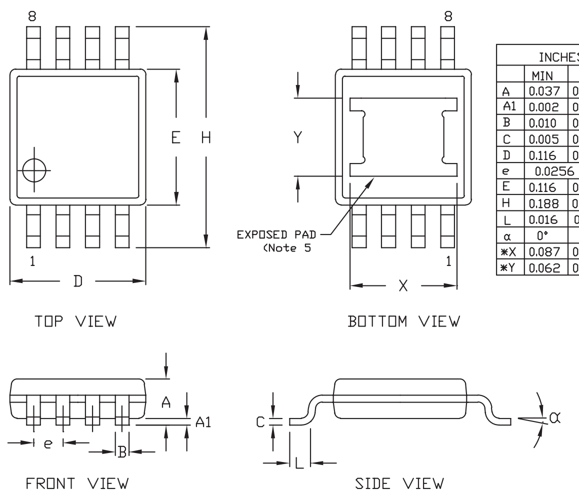
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, SOT23, 5L
APPROVAL | DOCUMENT CONTROL NO. 21-0057 | REV B | 1/1

SOT5L.EPS

Package Information (continued)

8LUMAXD.EPS



	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515				
*Y	0.062	0.074	1.575	1.880				

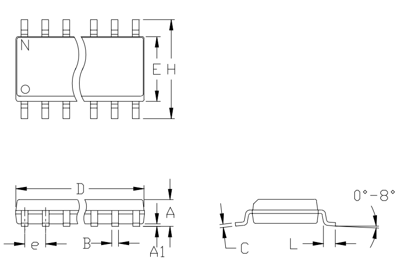
* EXPOSED PAD (Note 5)

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.
5. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 8L uMAX WITH EP OPTION
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV H | 1/1

Note: *The MAX4292 does not have an exposed pad.*

SOICN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

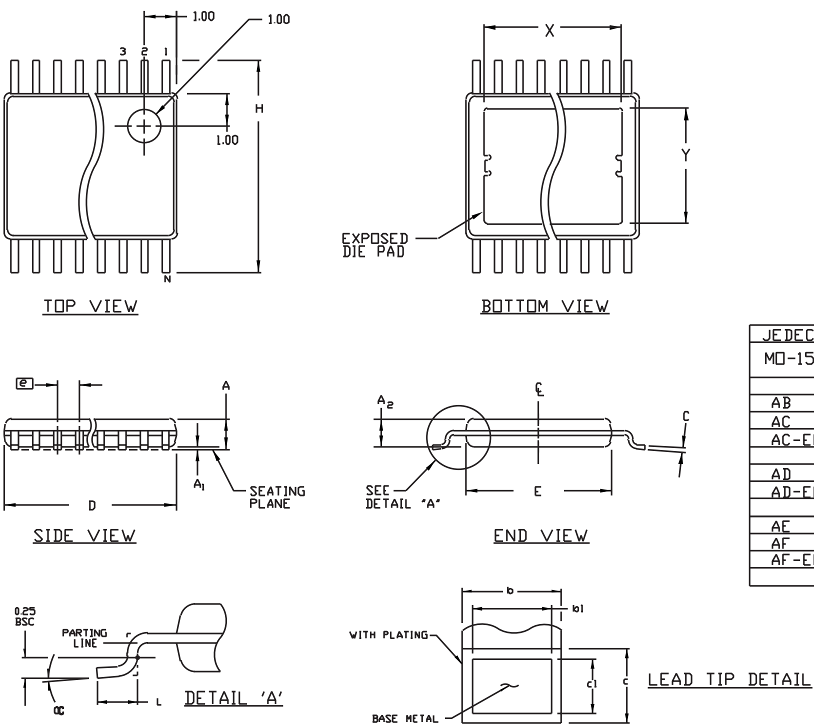
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM
120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION
PACKAGE FAMILY OUTLINE: SOIC .150" | TITLE | 1/1 | 21-0041 A | DOCUMENT CONTROL NUMBER | REV

Package Information (continued)

TSSOP.EPS



SYMBOL	COMMON DIMENSIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC MO-153	N		VARIATIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV C | 1/1

Note: *The MAX4294 does not have an exposed pad.*