Click here to ask an associate for production status of specific part numbers.

MAX25460

Automotive 1.5A Step-Down Converter with USB Protection/Host Charger Adapter Emulator

General Description

The MAX25460 combines a 1.5A high-efficiency, automotive-grade, step-down converter, a USB BC1.2 host charger emulator, and high-bandwidth USB protection switches for automotive USB 2.0 host applications. The device also includes a USB load current-sense amplifier and a configurable feedback adjustment circuit that provides automatic USB voltage compensation for voltage drops in captive cables often found in automotive applications. The device limits the USB load current using both a fixed internal peak-current threshold and a user-configurable external current-sense USB load threshold.

The MAX25460 is optimized for 2.2MHz operation allowing optimization of efficiency, noise, and board space based on the application requirements. The DC-DC converter integrates a high-side MOSFET and uses a low forward-drop freewheeling Schottky diode for rectification. There is a small low-side n-channel switch to maintain fixed frequency under light loads. The IC includes an external SYNC input/output, and can be configured for spread-spectrum operation.

The MAX25460 allows flexible configuration and advanced diagnostic options for both standalone and supervised applications. The device can be programmed using either external programming resistors and/or internal I^2C registers through the I^2C bus.

The MAX25460 is available in a small 4mm x 5mm 24-pin TQFN package and is designed to minimize required external components and layout area.

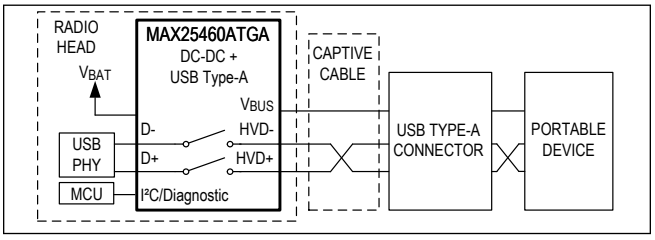
Applications

- Automotive Radio and Navigation
- USB Port for Host and Hub Applications
- Automotive Connectivity/Telematics

Benefits and Features

- One-Chip Type-A Solution Directly from Car Battery to Portable Device
  - 1GHz Bandwidth USB 2.0 Data Switches
  - 4.5V to 28V (40V Load Dump) Operating Voltage
  - 5V to 6V, 1.5A Output Capability
- Optimal USB Charging and Communication for Portable Devices
  - User-Programmable Voltage Gain Adjusts Output for Up to 474mΩ Cable Resistance
  - User-Programmable USB Current Limit
  - Supports USB BC1.2 CDP and SDP Modes
  - Compatible with USB On-the-Go Specification and Apple CarPlay®
- Low-Noise Features Prevent Interference with AM Band and Portable Devices
  - Fixed-Frequency 2.2MHz Operation
  - Fixed-Pulse-Width Modulation (PWM) Option at No Load
  - Spread Spectrum for Electromagnetic Interference (EMI) Reduction
  - SYNC Input/Output for Frequency Parking
- Robust Design Keeps Vehicle System and Portable Device Safe in an Automotive Environment
  - Short-to-Battery Protection on V_{BUS}, HVD± Pins
  - Advanced Diagnostics through I^2C Bus
  - ±15kV Air/±8kV Contact ISO 10605 (330pF, 2kΩ)*
  - ±15kV Air/±8kV Contact IEC 61000-4-2 (150pF, 330Ω)*
  - Overtemperature Protection and Warning
  - -40°C to +125°C Operating Temperature Range

Simplified Block Diagram



***Ordering Information* appears at end of data sheet.**

**Tested in Typical Application Circuit as used on the MAX25460 Evaluation Kit with 1m captive cable.*

19-101710; Rev 0; 6/23

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

SUPSW to PGND ..... -0.3V to +40V
HVEN to PGND ..... -0.3V to V_{SUPSW}+0.3V
LX to PGND (*Note 1*)..... -0.3V to V_{SUPSW}+0.3V
SYNC to AGND .....-0.3V to V_{BIAS}+0.3V
SENSN, SENSP to AGND ..... -0.3V to V_{SUPSW}+0.3V
AGND to PGND..... -0.3V to +0.3V
BST to PGND ..... -0.3V to +46V
BST to LX..... -0.3V to +6V
IN, CONFIG1, ENBUCK, SDA (CONFIG2), SCL (CONFIG3), BIAS, DATA_MODE, FAULT, INT(ATTACH) to AGND....-0.3V to +6V
HVDP, HVDM to AGND..... -0.3V to +18V
DP, DM to AGND.....-0.3V to V_{IN}+0.3V
IC to AGND..... -0.3V to +16V
LX Continuous RMS Current 1.7A
Output Short-Circuit Duration.....Continuous
Thermal Charactaristics
Continuous Power Dissipation - Single-Layer Board (T_A = +70°C, 24-TQFN (derate 20.8mW/°C above +70°C)) .... 1666.7 mW
Continuous Power Dissipation - Multilayer Board (T_A = +70°C, 24-TQFN (derate 28.6mW/°C above +70°C)) .....2285.7 mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range.....-40°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: Self-protected from transient voltages exceeding these limits for ≤ 50ns in circuit under normal operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

24 Pin TQFN 4x5x0.75mm

Package Code	T2445+2C
Outline Number	21-0201
Land Pattern Number	90-0083
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	1.80°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	1.80°C/W

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*.

Electrical Characteristics

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY AND ENABLE						
Supply Voltage Range	V_{SUPSW}	(*Note 2*)	4.5		28	V
Load Dump Event Supply Voltage Range	V_{SUPSW_LD}	< 1s			40	V

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current - Off State	I_{SUPSW}	V_{SUPSW} = 18V; V_{HVEN} = 0V; V_{IN} = 0V; Off State		10	20	µA
Supply Current - Buck Off	I_{SUPSW}	V_{HVEN} = 14V; V_{ENBUCK} = 0V		1.1		mA
Supply Current - Skip Mode	I_{SUPSW}	V_{HVEN} = 14V; buck switching; no load		1.8		mA
Supply Current - FPWM	I_{SUPSW}	V_{HVEN} = 14V; buck switching; no load		28		mA
BIAS Voltage	V_{BIAS}	5.75V ≤ V_{SUPSW} ≤ 28V	4.5	4.7	5.25	V
BIAS Current Limit			50	150		mA
BIAS Undervoltage Lockout	V_{UV_BIAS}	V_{BIAS} rising	3.0	3.3	3.6	V
BIAS Undervoltage Lockout Hysteresis				0.2		V
SUPSW Undervoltage Lockout	V_{UV_SUPSW}	V_{SUPSW} rising	3.9		4.42	V
SUPSW Undervoltage Lockout Hysteresis				0.2		V
IN Voltage Range	V_{IN}		3		3.6	V
IN Overvoltage Lockout	V_{IN_OVLO}	V_{IN} rising	3.8	4	4.3	V
IN Input Current	I_{IN}				10	µA
HVEN Rising Threshold	V_{HVEN_R}		0.6	1.5	2.4	V
HVEN Falling Threshold	V_{HVEN_F}				0.4	V
HVEN Hysteresis	V_{HVEN}			0.2		V
HVEN Delay Rising	t_{HVEN_R}		2.5		15	µs
HVEN Delay Falling	t_{HVEN_F}		5	12	25	µs
HVEN Input Leakage		V_{HVEN} = V_{SUPSW} = 18V, V_{HVEN} = 0V			10	µA
DP, DM ANALOG USB SWITCHES						
On-Channel -3dB Bandwidth	BW	R_L = R_S = 50Ω		1000		MHz
Analog Signal Range			0		3.6	V
HVDP, HVDM Protection Trip Threshold	V_{OV_D}		4.05	4.2	4.3	V
Protection Response Time	t_{FP_D}	V_{IN} = 4.0V, $V_{HVD±}$ = 3.3V to 4.3V step, R_L = 15kΩ on D±, delay to $V_{D±}$ < 3V		2		µs
On-Resistance Switch A	R_{ON_SA}	I_L = 10mA, $V_{D±}$ = 0V to V_{IN}, V_{IN} = 3.0V to 3.6V		4	8	Ω
On-Resistance Match between Channels Switch A	ΔR_{ON_SA}	I_L = 10mA, $V_{D±}$ = 1.5V or 3.0V			0.2	Ω
On-Resistance Flatness Switch A	$R_{FLAT(ON)A}$	I_L = 10mA,$V_{D\_}$ = 0V or 0.4V		0.01		Ω

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On Resistance of HVD+/HVD- short	R_{SHORT}	V_{DP} = 1V, I_{DM} = 500µA		90	180	Ω
HVD+/HVD- On-Leakage Current	I_{HVD_ON}	$V_{HVD±}$ = 3.6V or 0V	-7		7	µA
HVD+/HVD- Off-Leakage Current	I_{HVD_OFF}	$V_{HVD±}$ = 18V, $V_{D±}$ = 0V			150	µA
D+/D- Off-Leakage Current	I_{D_OFF}	$V_{HVD±}$ = 18V, $V_{D±}$ = 0V	-1		1	µA
CURRENT-SENSE AMPLIFIER (SENSP, SENSN)						
Gain		10mV < V_{SENSP} - V_{SENSN} < 110mV, GAIN[4:0] = 0b11111		19.4		V/V
Cable Compensation LSB	R_{LSB}			18		mΩ
Overcurrent Threshold	ILIM_SET	ILIM[2:0] = 0b111, R_{SENSE} = 33mΩ	1.62	1.7	1.78	A
		ILIM[2:0] = 0b110, R_{SENSE} = 33mΩ	1.62	1.7	1.78	
		ILIM[2:0] = 0b101, R_{SENSE} = 33mΩ	1.62	1.7	1.78	
		ILIM[2:0] = 0b100, R_{SENSE} = 33mΩ	1.62	1.7	1.78	
		ILIM[2:0] = 0b011, R_{SENSE} = 33mΩ	1.05	1.13	1.21	
		ILIM[2:0] = 0b010, R_{SENSE} = 33mΩ	0.8	0.86	0.92	
		ILIM[2:0] = 0b001, R_{SENSE} = 33mΩ	0.55	0.6	0.65	
		ILIM[2:0] = 0b000, R_{SENSE} = 33mΩ	0.3	0.33	0.36	
Overcurrent Debounce Timer	ILIM_SET Timer	ILIM_DEB[1:0] = 0b00	1.1	1.5		ms
SENSN Discharge Current	I_{SENSN_DIS}		11	18	32	mA
Startup Wait Time	t_{BUCK_WAIT}			2		s
SENSN Discharge Time	t_{DIS_CD}	DCDC_ON toggle		2		s
Forced Buck Off-Time	$t_{BUCKOFF\_CD}$	DCDC_ON toggle; see *Reset Criteria* section		2		s
Attach Comparator Load Current Rising Threshold		Common mode input = 5.15V	5	16	28	mA
Attach Comparator Hysteresis		Common mode input = 5.15V		2.5		mA
SENSN Undervoltage Threshold (Falling)	V_{UV_SENSN}		4	4.375	4.75	V
SENSN Overvoltage Threshold (Rising)	V_{OV_SENSN}		7	7.46	7.9	V
SENSN Short-Circuit Threshold (Falling)	V_{SHT_SENSN}		1.75	2	2.25	V
SENSN Undervoltage Fault Blanking Time				16		ms

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SENSN Overvoltage Fault Blanking Time	t_{B,OV_SENSN}	From overvoltage condition to $\overline{FAULT}$ asserted		3	6	µs
SENSN Discharge Threshold Falling		V_{SENSN} falling	0.47	0.51	0.57	V
DIGITAL INPUTS (SDA, SCL, ENBUCK, DATA_MODE)						
Input Leakage Current		V_{PIN} = 5.5V, 0V	-5		5	µA
Logic High	V_{IH}		1.6			V
Logic Low	V_{IL}				0.5	V
USB 2.0 HOST CHARGER EMULATOR (HVD+/HVD-, D+/D-)						
Input Logic High	V_{IH}		2.0			V
Input Logic Low	V_{IL}				0.8	V
Data Sink Current	I_{DAT_SINK}	V_{DAT_SINK} = 0.25V to 0.4V	50	100	150	µA
Data Detect Voltage High	V_{DAT_REFH}		0.4			V
Data Detect Voltage Low	V_{DAT_REFL}				0.25	V
Data Detect Voltage Hysteresis	V_{DAT_HYST}			60		mV
Data Source Voltage	V_{DAT_SRC}	I_{SRC} = 200µA	0.5		0.7	V
STEP-DOWN DC-DC CONVERTER						
PWM Output Voltage	V_{SENSP}	7V ≤ V_{SUPSW} ≤ 28V, no load		5.15		V
Skip Mode Output Voltage	V_{SENSP_SKIP}	7V ≤ V_{SUPSW} ≤ 18V, no load (*Note 2*)		5.25		V
Load Regulation	R_{LR}	7V ≤ V_{SUPSW} ≤ 18V, for 5V nominal output setting		51		mΩ
Output Voltage Accuracy		8V ≤ V_{SUPSW} ≤ 18V, 1.5A, V_{SENSP} - V_{SENSN} = 49.5mV , GAIN[4:0] = 0b11111 cable compensation.	5.721		6.001	V
Spread Spectrum Range		SS Enabled		±3.4		%
SYNC Switching Threshold High	V_{SYNC_HI}	Rising	1.4			V
SYNC Switching Threshold Low	V_{SYNC_LO}	Falling			0.4	V
SYNC Internal Pulldown				200		kΩ
SYNC Input Clock Acquisition Time	t_{SYNC}	(*Note 3*)		1		Cycles
High-Side Switch On-Resistance	R_{ONH}	I_{LX} = 1A		111	196	mΩ
Low-Side Switch On-Resistance	R_{ONL}	I_{LX} = 1A		1.5	3	Ω
BST Input Current	I_{BST}	V_{BST} – V_{LX} = 5V, High-side on		2.2		mA

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Current-Limit Threshold				3.5		A
Skip Mode Peak-Current Threshold	I_{SKIP_TH}			1		A
Negative Current Limit				0.7		A
Soft-Start Ramp Time	t_{SS}			8		ms
LX Rise Time		(*Note 3*)		3		ns
LX Fall Time		(*Note 3*)		4		ns
$\overline{FAULT}$, $\overline{INT}$ ($\overline{ATTACH}$), SYNC OUTPUTS						
Output-High Leakage Current		$\overline{FAULT}$, $\overline{INT}$($\overline{ATTACH}$) = 5.5V	-10		10	µA
Output Low Level		Sinking 1mA			0.4	V
SYNC Output High Level		Sourcing 1mA, SYNC configured as output	V_{BIAS} - 0.4			V
CONFIG RESISTORS CONVERTER						
CONFIG1-3 Current Leakage		V_{CONFIG} = 0V to 4V			±5	µA
OSCILLATORS						
Buck Oscillator Frequency	f_{SW}		1.95	2.2	2.45	MHz
THERMAL OVERLOAD						
Thermal Warning Temperature				140		°C
Thermal Warning Hysteresis				10		°C
Thermal Shutdown Temperature				165		°C
Thermal Shutdown Hysteresis				10		°C
I²C						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns

Electrical Characteristics (continued)

(V_{SUPSW} = 14V, V_{IN} = 3.3V, V_{ENBUCK} = 3.3V, Temperature = T_A = T_J = -40°C to +125°C, unless otherwise noted., Actual typical values may vary and are not guaranteed.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0.3		0.6	µs
Pulse Width of Spike Suppressed	t_{SP}			50		ns
ESD PROTECTION (ALL PINS)						
ESD Protection Level	V_{ESD}	Human body model		±2		kV
ESD PROTECTION (HVDP, HVDM)						
ESD Protection Level	V_{ESD}	ISO 10605 Air Gap (330pF, 2kΩ)		±15		kV
		ISO 10605 Contact (330pF, 2kΩ)		±8		
		IEC 61000-4-2 Air Gap (150pF, 330Ω)		±15		
		IEC 61000-4-2 Contact (150pF, 330Ω)		±8		

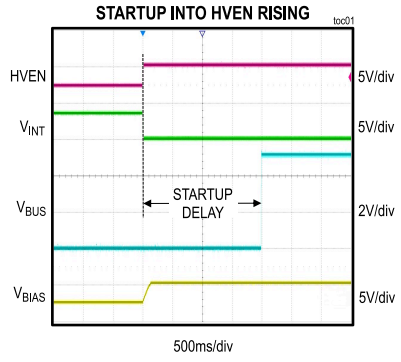
Note 2: Device is designed for use in applications with continuous operation of 14V. Device meets electrical table up to maximum supply voltage.

Note 3: Guaranteed by design and bench characterization; not production tested.

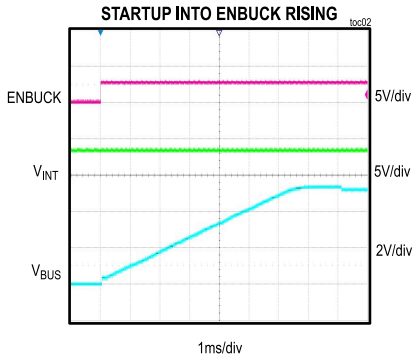
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

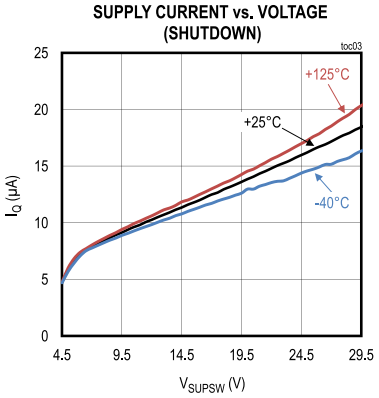
STARTUP INTO HVEN RISING



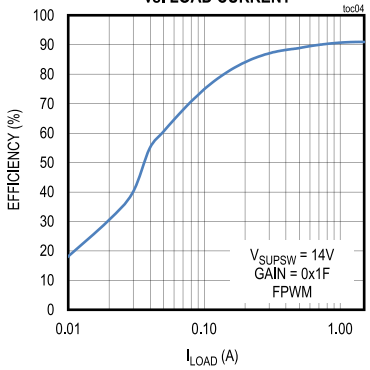
STARTUP INTO ENBUCK RISING



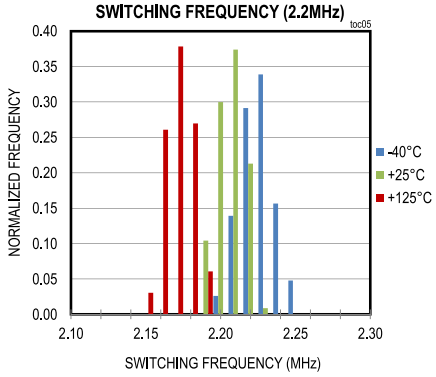
SUPPLY CURRENT vs. VOLTAGE (SHUTDOWN)



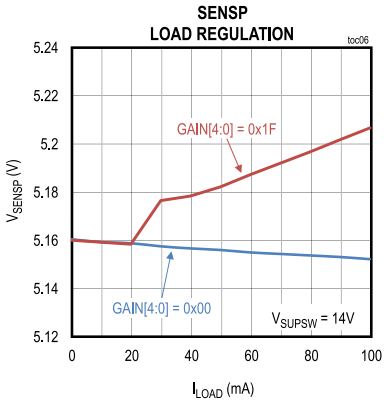
BUCK EFFICIENCY vs. LOAD CURRENT



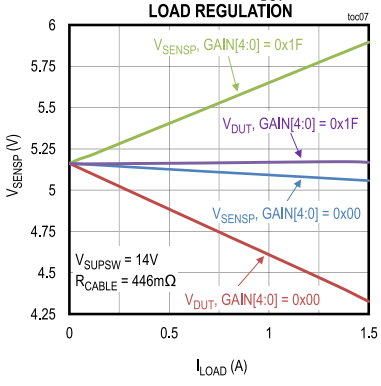
SWITCHING FREQUENCY (2.2MHz)



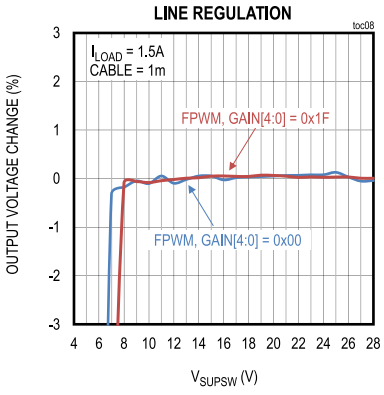
SENSP LOAD REGULATION



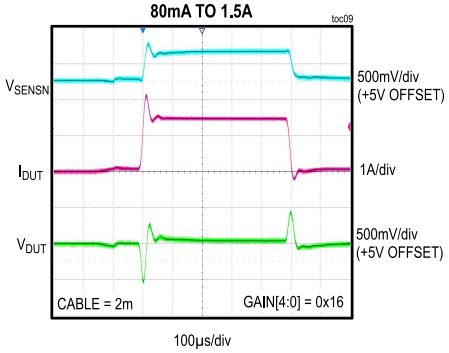
SENSP AND V_{DUT} LOAD REGULATION



LINE REGULATION



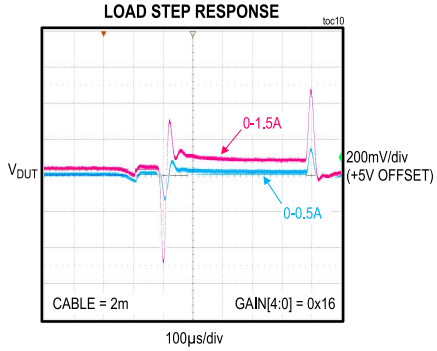
LOAD STEP RESPONSE 80mA TO 1.5A



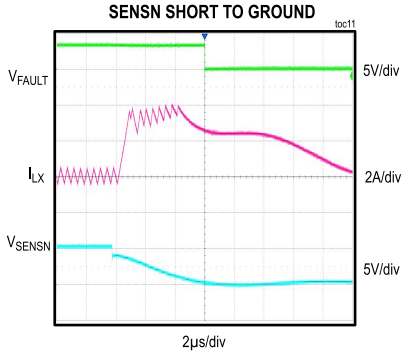
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

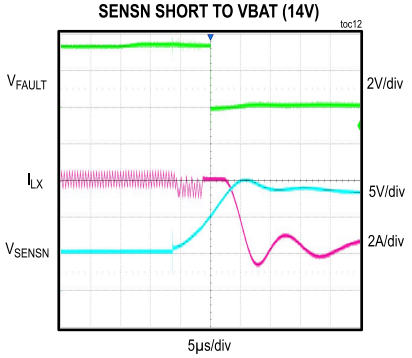
LOAD STEP RESPONSE



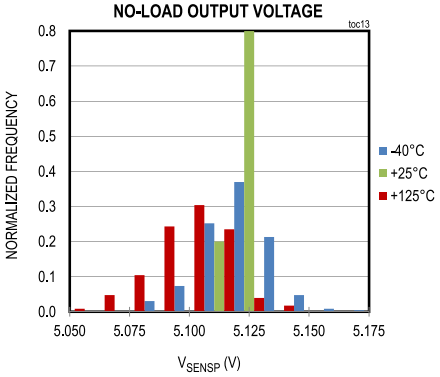
SENSN SHORT TO GROUND



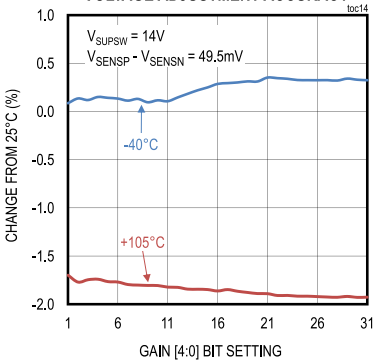
SENSN SHORT TO VBAT (14V)



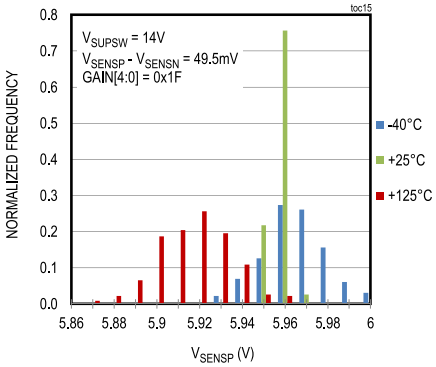
NO-LOAD OUTPUT VOLTAGE



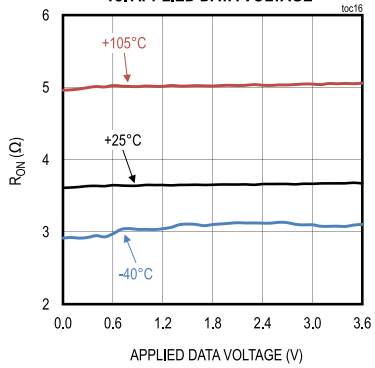
VOLTAGE ADJUSTMENT ACCURACY



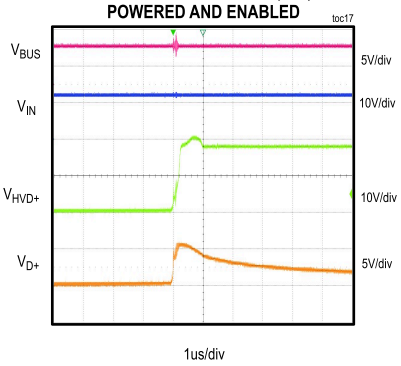
OUTPUT VOLTAGE ACCURACY



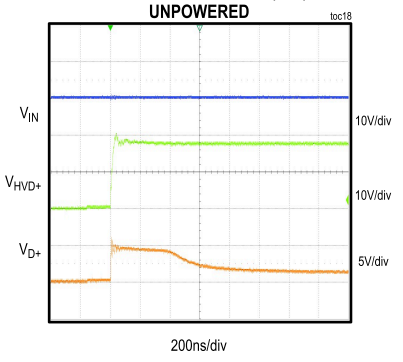
DATA SWITCH R_{ON} vs. APPLIED DATA VOLTAGE



HVD+/- SHORT TO VBAT (18V) POWERED AND ENABLED

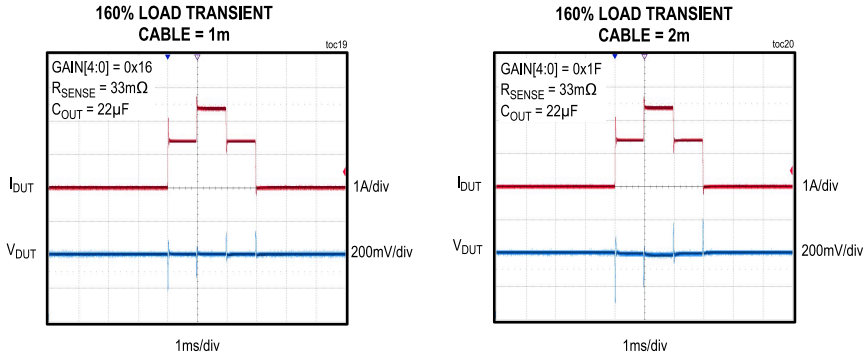


HVD+/- SHORT TO VBAT (18V) UNPOWERED



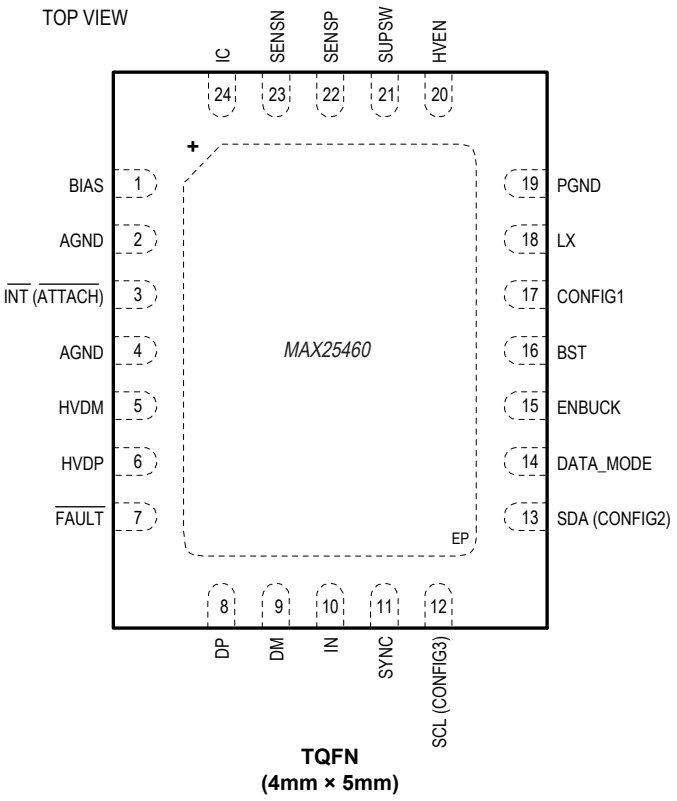
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)



Pin Configuration

MAX25460



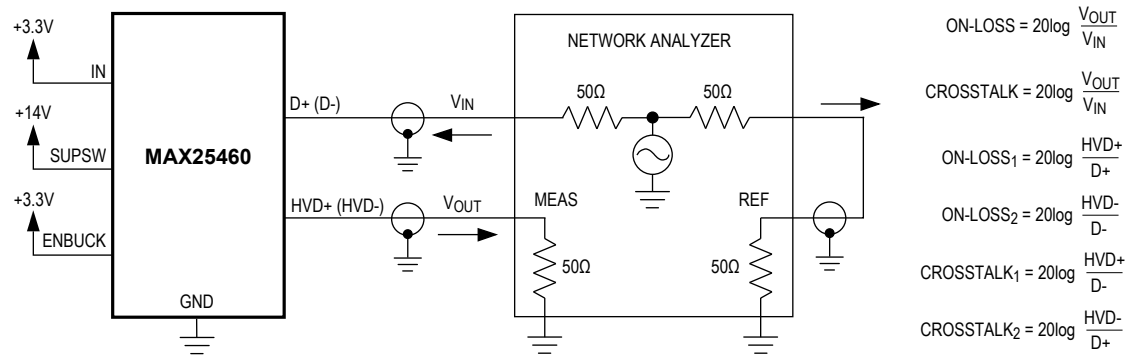
TQFN
(4mm × 5mm)

Pin Description

PIN	NAME	FUNCTION
1	BIAS	5V linear regulator output. Connect a 2.2µF ceramic capacitor from BIAS to GND. BIAS powers the internal circuitry.
2, 4	AGND	Analog Ground.
3	$\overline{INT}$ ($\overline{ATTACH}$)	In the I²C variant, functions as an active-low $\overline{INT}$ Pin. In stand-alone variants, functions as active-low Attach. Connect a 100kΩ pullup resistor to IN.
5	HVDM	High-Voltage-Protected USB Differential Data D- Output. Connect HVD- to the downstream USB connector D- pin.
6	HVDP	High-Voltage-Protected USB Differential Data D+ Output. Connect HVD+ to the downstream USB connector D+ pin.
7	$\overline{FAULT}$	Active-low, open-drain,fault indicator output. Connect a 100kΩ pullup resistor to the IN pin.
8	DP	USB Differential Data D+ Input. Connect D+ to the low-voltage USB transceiver D+ pin.
9	DM	USB Differential Data D- Input. Connect D- to the low-voltage USB transceiver D- pin.
10	IN	Logic Enable Input. Connect to I/O voltage of USB transceiver. IN is also used for clamping during overvoltage events on HVD+ or HVD-. Connect a 1µF-10µF ceramic capacitor from IN to GND.
11	SYNC	Switching frequency Input/Output for synchronization with other supplies.
12	SCL (CONFIG3)	In the I²C Variant, this serves as the I²C SCL Pin. In stand-alone variants, this serves as CONFIG3 pin. See Table 6.
13	SDA (CONFIG2)	In the I²C Variant, this serves as the I²C SDA Pin. In stand-alone variants, this serves as CONFIG2 pin. See Table 6.
14	DATA_MODE	This pin selects between the two modes of data switch operation. The modes are defined in Table 2 and Table 3.
15	ENBUCK	DC-DC Enable Input. Drive high/low to enable/disable the buck converter.
16	BST	High-Side Driver Supply. Connect a 0.1µF capacitor from BST to LX.
18	LX	Inductor connection. Connect a rectifying Schottky diode between LX and GND. Connect an inductor from LX to the DC-DC converter output (SENSP).
19	PGND	Power Ground.
17	CONFIG1	Configuration. Connect a resistor to GND to set default configuration. See Table 4 and Table 5.
20	HVEN	Active-high system enable pin. HVEN is battery-voltage tolerant.
21	SUPSW	Internal High-Side Switch Supply Input. V_{SUPSW} provides power to the internal switch and LDO. Connect a 4.7µF ceramic capacitor in parallel with a 22µF electrolytic capacitor from SUPSW to PGND.
22	SENSP	DC-DC converter feedback input and current-sense amplifier positive input. DC-DC bulk capacitance placed here. Connect to positive terminal of current-sense resistor (R_{SENSE}) and the main output of the converter. Used for internal voltage regulation loop.
23	SENSN	Current-sense amplifier negative input. Connect to negative terminal of current-sense resistor (R_{SENSE}).
24	IC	Connect to Ground.
EP	EP	Exposed pad. Connect EP to multiple GND planes with 3 x 3 via grid (minimum).

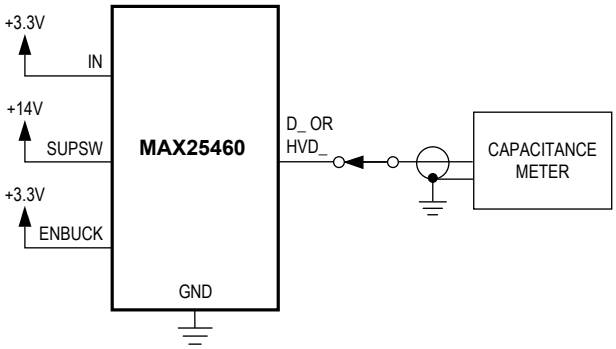
Functional Diagrams

On-Channel -3dB Bandwidth and Crosstalk

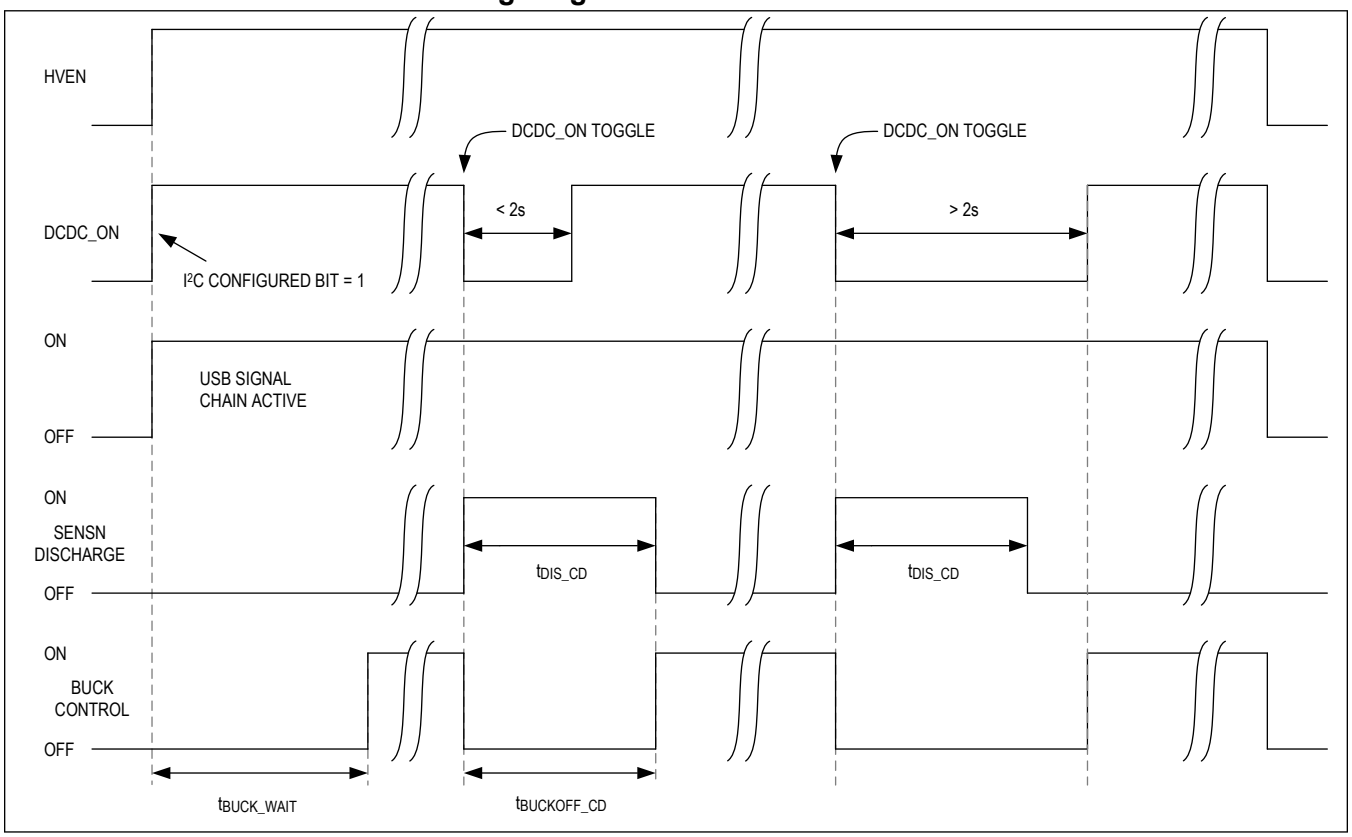


ON-LOSS IS MEASURED BETWEEN D+ AND HVD+, OR D- AND HVD-.
CROSSTALK IS MEASURED FROM ONE CHANNEL TO THE OTHER CHANNEL.
SIGNAL DIRECTION THROUGH SWITCH IS REVERSED; WORST VALUES ARE RECORDED.

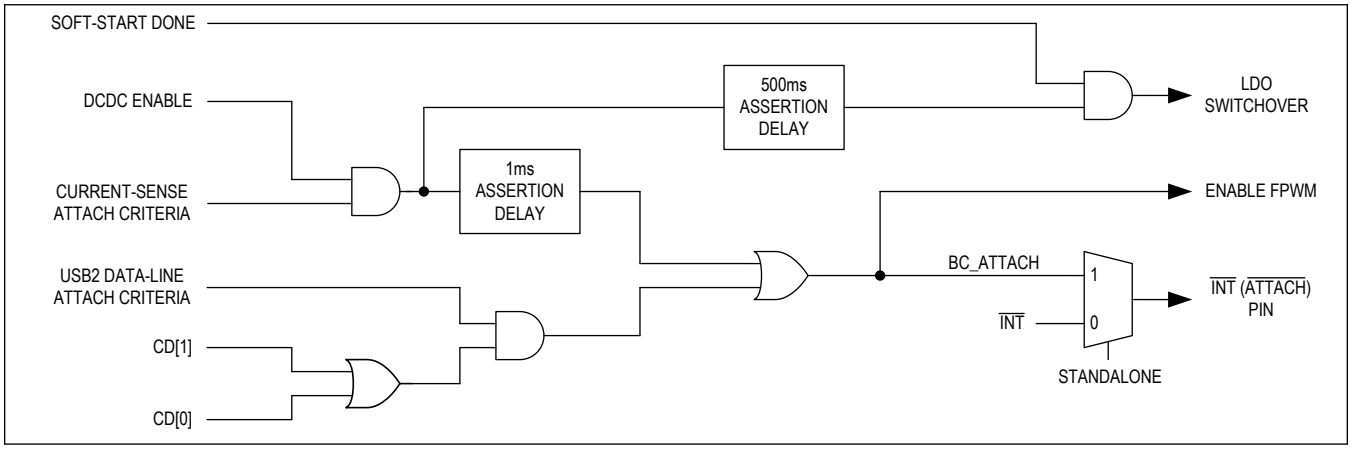
On-Capacitance



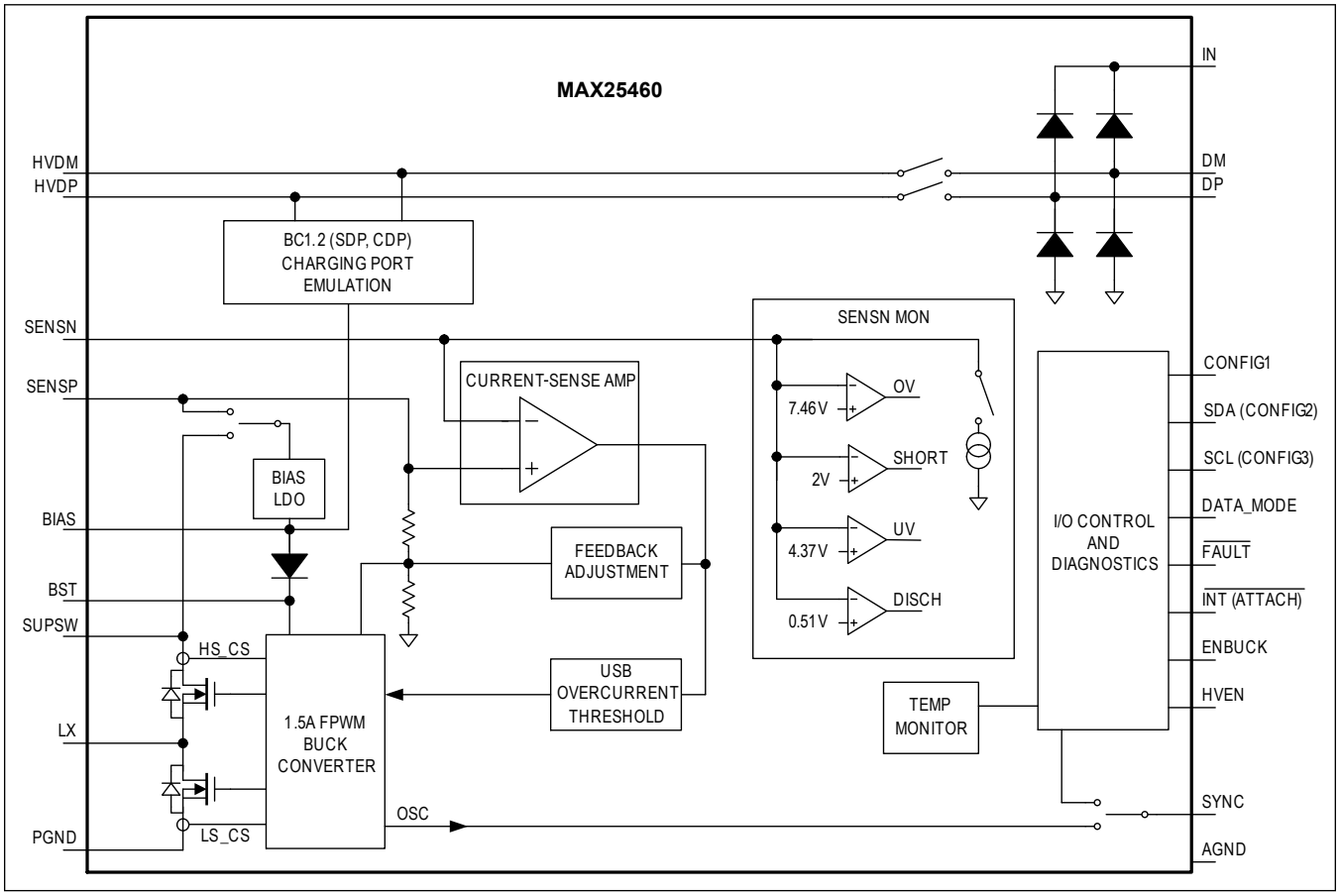
ENBUCK Reset Behavior and Timing Diagram



ATTACH Logic Diagram



Detailed Block Diagram



Detailed Description

The MAX25460 combines a 5V/1.5A automotive-grade step-down converter, a USB host charger emulator, and USB protection switches. The device variants offer options for both standalone/GPIO and I^2C configuration and control. This device family is designed for high-power USB ports in automotive radio, navigation, connectivity, USB hub, and dedicated charging applications.

The MAX25460 features high-voltage, high-ESD, 1GHz bandwidth data switches. The MAX25460 protects up to 18V and includes internal ESD protection circuitry.

The data switches of all device variants protect the sensitive 3.3V pins of the USB transceiver and support USB low-speed (1.5Mbps), full-speed (12Mbps), and hi-speed (480Mbps) communication modes. The internal host charger port-detection circuitry offers automatic sensing and conformance to multiple standards. All variants enable USB-IF OTG, Apple CarPlay, and Android Auto conformance while retaining industry-leading protection features and automotive-grade robustness.

The high-efficiency step-down DC-DC converter operates with an input voltage up to 28V, and is protected from load dump transients up to 40V. The DC-DC converter is optimized for 2.2MHz switching frequency. The converter can deliver 1.5A of continuous current at 125°C.

The MAX25460 features a high-side current-sense amplifier and a programmable feedback-adjustment circuit that provides automatic USB voltage adjustment to compensate for voltage drops in captive cables associated with automotive applications. The precision current-sense allows for an accurate DC output current limit that minimizes the solution component size and cost.

Power-Up and Enabling

System Enable (HVEN)

HVEN is used as the main enable to the device and initiates system start-up and configuration. If HVEN is at a logic-low level, SUPSW power consumption is reduced and the device enters a standby, low quiescent current level. HVEN is compatible with inputs from 3.3V logic up to automotive battery. After a system reset (e.g., HVEN toggle, BIAS UV), the I^2C variant asserts the $\overline{INT}$ pin to indicate that the IC has not been configured. The buck converter is forced off until the CONFIGURED bit of SETUP_4 is written to a 1. This ensures that a portable device cannot attach before the IC registers are correctly set for the application.

DC-DC Enable (ENBUCK)

The buck regulator on the MAX25460 is controlled by the ENBUCK pin for stand-alone variants, and by both the ENBUCK pin and the I^2C interface for I^2C variants. DCDC_ON, the logical AND of ENBUCK, and EN_DCDC determines if the buck converter is enabled. On stand-alone variants, EN_DCDC is always high and only ENBUCK can be used to enable the buck converter. On I^2C variants, setting ENBUCK low overrides an I^2C EN_DCDC enable command, which allows compatibility with USB hub controllers. For a typical USB hub application, connect ENBUCK to the enable output of the USB hub controller. This allows the USB hub controller to enable and disable the USB power port using software commands. ENBUCK can be directly connected to the BIAS or IN pin for applications that do not require GPIO control of the DC-DC converter enable.

3.3V Input (IN)

IN is used to clamp the D+ and D- pins during an ESD or overvoltage event on the HVD+ and HVD- pins. This clamping protects the downstream USB transceiver. The presence of these clamping diodes requires that IN remain set to 3.3V at all times for USB communication to occur. The IN pin features an overvoltage lockout that disables the data switches if IN is above V_{IN_OVLO}. Bypass IN with a 1µF ceramic capacitor, place it close to the IN pin, and connect it to the same 3.3V supply that is shared with the multimedia processor or hub transceiver.

Linear Regulator Output (BIAS)

BIAS is the output of a 5V linear regulator that powers the internal logic and control circuitry for the device. BIAS is internally powered from SUPSW or SENSP and automatically powers up when HVEN is high and SUPSW voltage exceeds V_{UV_SUPSW}. The BIAS output contains an undervoltage lockout that keeps the internal circuitry disabled when

BIAS is below V_{UV_BIAS}. The linear regulator automatically powers down when HVEN is low, and a low shutdown current mode is entered. Bypass BIAS to GND with a 2.2µF ceramic capacitor.

Power-On Sequencing

HVEN, ENBUCK, and IN do not have a power-up sequence requirement by design. However, the desired system behavior should be considered for the state of these pins at startup. The D+ and D- pins are clamped to IN, therefore IN should be set to 3.3V before any USB communication is required. It is recommended that IN is set to 3.3V before HVEN is set high. ENBUCK acts as the main disable for the DC-DC converter. If ENBUCK is low when HVEN is set high, all variants keep the buck converter in the disabled state until ENBUCK is set high.

Step-Down DC-DC Regulator

Step-Down Regulator

The MAX25460 features a current-mode, step-down converter with integrated high-side MOSFET and 1.5Ω (typ) low-side MOSFET used with an external Schottky diode. The low-side MOSFET enables fixed-frequency, forced-PWM operation under light loads. The DC-DC regulator features a cycle-by-cycle current limit and intelligent transition from skip mode to forced-PWM mode that makes the device ideal for automotive applications.

Wide Input Voltage Range

The device is specified for a wide 4.5V to 28V input voltage range. SUPSW provides power to the internal BIAS linear regulator and internal power switch. Certain conditions such as cold cranking can cause the voltage at the output to drop below the programmed output voltage. Under such conditions, the device operates in a high duty-cycle mode to facilitate minimum dropout from input to output.

Maximum Duty-Cycle Operation

The MAX25460 has a maximum duty cycle of 98% (typ). The IC monitors the off-time (time for which the low-side FET is on) in both PWM and skip modes for every switching cycle. Once the off-time of 150ns (typ) is detected continuously for 7.5µs, the low-side FET is forced on for 60ns (typ) every 7.5µs. The input voltage at which the device enters dropout changes depending on the input voltage, output voltage, switching frequency, load current, and design efficiency. The input voltage at which the devices enter dropout can be approximated as follows:

$$V_{SUPSW} = \frac{V_{OUT} + \left(I_{LOAD} \times R_{ONH}\right)}{0.98}$$

Note: The equation does not take into account the efficiency and switching frequency but provides a good first-order approximation. Use the R_{ONH} (max) in the *Electrical Characteristics* table.

Output Voltage (SENSP)

The device features a precision internal feedback network that is connected to SENSP and that is used to set the output voltage of the DC-DC converter. The network nominally sets the average DC-DC converter output voltage to 5.15V.

Soft-Start

When the DC-DC converter is enabled, the regulator soft-starts by gradually ramping up the output voltage from 0V to 5.15V over approximately 8ms. This soft-start feature reduces inrush current during startup. Soft-start is guaranteed into compliant USB loads (see the *USB Loads* section).

Reset Behavior

The MAX25460 implements a discharge function on SENSN any time that the DC-DC regulator is disabled for any reason. When the discharge function is activated, current (I_{SENSN_DIS}) is drained through a current-limited FET, and a reset timer is also started. This timer prevents the DC-DC regulator from starting up again until the timer has expired. This allows for easy compatibility with USB specifications and removes the need for long discharge algorithms to be implemented in system software. See *ENBUCK Reset Behavior and Timing Diagram* for reset timer details.

Reset Criteria

The MAX25460 DC-DC converter automatically resets for all undervoltage, overvoltage, overcurrent, and overtemperature fault conditions. See Table 8 for details. The fault retry timer is configurable in the SETUP_3 register. This timer is activated after a fault condition is removed and prevents the buck converter from switching on until the timer expires.

With the standalone variant, a 2s timer is activated after a fault condition is removed and prevents the buck converter from switching on until the timer expires. Another internal retry timer is enabled after DCDC_ON is set low, preventing the buck from switching on until the 2s timer expires.

Switching Frequency Configuration

The DC-DC switching frequency can be referenced to an internal oscillator or from an external clock signal on the SYNC pin. The internal oscillator frequency is set to 2.2MHz.

Switching Frequency Synchronization (SYNC Pin)

When the SYNC pin is configured to operate as an output, skip mode operation is disallowed, and the internal oscillator drives the SYNC pin. This allows other devices to synchronize with the MAX25460, 180 degrees out of phase, for EMI reduction.

When SYNC is configured as an input, the SYNC pin becomes a logic-level input that can be used for both operating-mode selection and frequency control. Connecting SYNC to GND or an external clock enables fixed-frequency, forced-PWM mode. Connecting SYNC to a logic-high signal allows intelligent skip-mode operation. The device can be externally synchronized to frequencies within ±20% of the programmed internal oscillator frequency.

Forced-PWM Operation

In forced-PWM mode, the device maintains fixed-frequency PWM operation over all load conditions, including no-load conditions.

Intelligent Skip-Mode Operation and Attach Detection

When the SYNC pin is configured as an input, but neither a clocked signal nor a logic-low level exists on the SYNC pin, the MAX25460 operates in skip mode at very light load/no load conditions. Intelligent device attach detection is used to determine when a device is attached to the USB port. The device intelligently exits skip mode and enters forced-PWM mode when a device is attached and remains in forced-PWM mode as long as the attach signal persists. This minimizes the EMI concerns caused by automotive captive USB cables and poorly shielded consumer USB cables. The device attach event is also signaled by the $\overline{INT}$ ($\overline{ATTACH}$) pin (stand-alone variants) or ATTACH bits (I^2C variants). The criteria for device attach detection and intelligent skip-mode operation are shown in Table 1.

Table 1. DC-DC Converter Intelligent Skip Mode Truth Table

SYNC PIN	SYNC_ DIR BIT	DATA SWITCH CHARGE DETECTION MODE	CDP ATTACH DETECTION	CURRENT-SENSE ATTACH DETECTION	DC-DC CONVERTER OPERATION
x	OUT	x	x	x	Forced-PWM Mode: Continuous
0	IN	x	x	x	Forced-PWM Mode: Continuous
Clocked	IN	x	x	x	Forced-PWM Mode: Continuous
1	IN	High-Speed Pass Thru (SDP) Mode	x	0	Intelligent Skip Mode: No Device Attached
1	IN	High-Speed Pass Thru (SDP) Mode	x	1	Forced-PWM Mode: Device Attached
1	IN	BC1.2 Auto CDP Mode	0	0	Intelligent Skip Mode: No Device Attached
1	IN	BC1.2 Auto CDP Mode	1	x	Forced-PWM Mode: Device Attached

Table 1. DC-DC Converter Intelligent Skip Mode Truth Table (continued)

SYNC PIN	SYNC_ DIR BIT	DATA SWITCH CHARGE DETECTION MODE	CDP ATTACH DETECTION	CURRENT-SENSE ATTACH DETECTION	DC-DC CONVERTER OPERATION
1	IN	BC1.2 Auto CDP Mode	x	1	Forced-PWM Mode: Device Attached

Spread-Spectrum Option

Spread-spectrum operation is offered to improve the EMI performance of the MAX25460. Spread-spectrum operation is enabled by the SS_EN bit of the SETUP_0 register, which is preloaded on startup from the CONFIG1 pin for both stand-alone and I^2C variants. The internal operating frequency modulates the switching frequency by up to ±3.4% relative to the internally generated operating frequency. This results in a total spread-spectrum range of 6.8%. Spread-spectrum mode is only active when operating from the internal oscillator. Spread-spectrum clock dithering is not possible when operating from an external clock.

Current Limit

The MAX25460 limits the USB load current using both a fixed internal peak current threshold of the DC-DC converter and a user-programmable external DC load current-sense amplifier threshold. This allows the current limit to be adjusted between 300mA and 1.5A depending on the application requirements, while protecting the system in the event of a fault. Upon exceeding either the DC-DC peak or the 1.5ms debounce timer of the user-programmable current thresholds, the high-side FET is immediately switched off and current-limit algorithms are initiated. When the external current limit lasts for longer than 16ms, the $\overline{FAULT}$ pin asserts and the VBUS_ILIM bit of the IRQ_1 register is set. Once the load current exceeds the programmed threshold, the DC-DC converter acts as a constant current source. This may cause the output voltage to droop. The ILIM_ITRIP bit of the SETUP_2 register determines the output voltage droop required to initiate a DC-DC converter reset during VBUS_ILIM. When ILIM_ITRIP = 0, the USB current limit is detected for 16ms and the output voltage falls below V_{UV_SENSN}, the DC-DC converter resets. The DC-DC converter also resets if the internal LX peak current threshold is exceeded for four consecutive switching cycles and the output voltage droops to less than 2V.

Output Short-Circuit Protection

The DC-DC converter output (SENSP, SENSN) is protected against both short-to-ground and short-to-battery conditions. If a short-to-ground or undervoltage condition is encountered, the DC-DC converter immediately resets, asserts the $\overline{FAULT}$ pin, flags the fault in the IRQ_1 register, and then reattempts soft-start after the reset delay. This pattern repeats until the short circuit has been removed.

If a short-to-battery is encountered ($V_{SENSN} > V_{OV\_SENSN}$), the buck converter shuts down, the $\overline{FAULT}$ pin is asserted, and the fault is flagged in the IRQ_1 register. The buck converter stays shut down until the fault condition resolves and the 2s timer expires.

Thermal Overload Protection

Thermal overload protection limits the total power dissipated by the device. A thermal-protection circuit monitors the die temperature. If the die temperature exceeds +165°C, the device shuts down, so it can cool. Once the device has cooled by 10°C, the device is enabled again. This results in a pulsed output during continuous thermal overload conditions, protecting the device during fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature of +150°C.

Pre-Thermal Overload Warning

The MAX25460 I^2C variant features a thermal overload warning flag which sets the THM_WARN bit of the IRQ_2 register when the die temperature crosses +140°C. This allows a system software implementation of thermal foldback or load shedding algorithms to prevent a thermal overload condition.

USB Current Limit and Output Voltage Adjustment

Current-Sense Amplifier (SENSP, SENSN)

The MAX25460 features an internal USB load current-sense amplifier to monitor the DC load current delivered to the USB port. The V_{SENSE} voltage (V_{SENSP} - V_{SENSN}) is used internally to provide precision DC current-limit and voltage-

compensation functionality. A 33mΩ sense resistor (R_{SENSE}) should be placed between SENSP and SENSN.

USB DC Limit Configuration

The MAX25460 allows configuration of the precision DC limit by the ILIM[2:0] bits of the SETUP_2 register. The I²C configuration enables selection of five discrete DC limit values. See *SETUP_2* for current limit configuration values.

Stand-alone variants of the device allow selection of a subset of the five available current limit options by reading the CONFIG3 resistor. See Table 6 and the *Applications Information* section for more information.

Voltage Feedback Adjustment Configuration

The MAX25460 compensates voltage drop for up to 474mΩ of USB cable in typical USB charging applications. The I²C variants of the device allow this configuration by the GAIN[4:0] bits of the SETUP_1 register. Stand-alone variants of the device allow configuration by the CONFIG2 resistor, which sets GAIN[3:0], and the CONFIG3 resistor, which sets GAIN[4]. See the *SETUP_1* register map and the *Applications Information* section for more information.

USB Protection Switches and BC1.2 Host Charger Emulation

USB Protection Switches

The MAX25460 provides automotive-grade ESD and short-circuit protection for the low-voltage USB data lines of high-integration multimedia processors. The HVDP/HVDM protection consists of ESD and OVP (overvoltage protection) for 1.5Mbps, 12Mbps, and 480Mbps USB transceiver applications. This is accomplished with a very low-capacitance FET in series with the D+ and D- data path.

The MAX25460 does not require an external ESD array and protects the HVD+ and HVD- pins to ±15kV Air-Gap/±8kV Contact Discharge with the 150pF/330Ω IEC 61000-4-2 model, as well as protects up to ±15kV Air-Gap/±8kV Contact Discharge with the 330pF/2kΩ ISO 10605 model. The MAX25460 provides robust, automotive-grade protection while maintaining a 1GHz -3dB insertion loss. This ensures optimum eye diagram at the end of a captive cable.

The HVD+ and HVD- short-circuit protection features include protection for a short to the USB +5V BUS and a short to the +18V car battery. These protection features prevent damage to the low-voltage USB transceiver when shorts occur in the vehicle harness or customer USB connector/cable. Short-to-GND protection is provided by the upstream USB transceiver.

USB Host Charger Emulator

The USB protection switches integrate the latest USB-IF Battery Charging Specification Revision 1.2 CDP and SDP circuitry.

Table 2. Data Switch Mode Truth Table (I²C Variant, ATGA)

DEVICE INPUTS					SA	SB	DATA SWITCH MODE
HVEN	IN	CD[1]	CD[0]	DATA_MODE			
0	X	X	X	X	0	0	Off
1	0	X	X	1	Invalid Mode (IN = 3.3V required for all modes)		
1	0	0	X	0	Invalid Mode (IN = 3.3V required for all modes)		
1	1	0	0	0	1	0	Hi-Speed Pass-Through (SDP)
1	1	0	1	0	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)
1	1	X	X	1	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)

Table 3. Data Switch Mode Truth Table (Stand-Alone Variant, ATGB)

DEVICE INPUTS			SA	SB	DATA SWITCH MODE
HVEN	IN	DATA_MODE			
0	X	X	0	0	Off

Table 3. Data Switch Mode Truth Table (Stand-Alone Variant, ATGB) (continued)

1	0	X	Invalid Mode (IN = 3.3V required for all modes)		
1	1	0	1	0	Hi-Speed Pass-Through (SDP)
1	1	1	On if CDP = 0	On if CDP = 1	BC1.2 Auto-CDP (CDP)

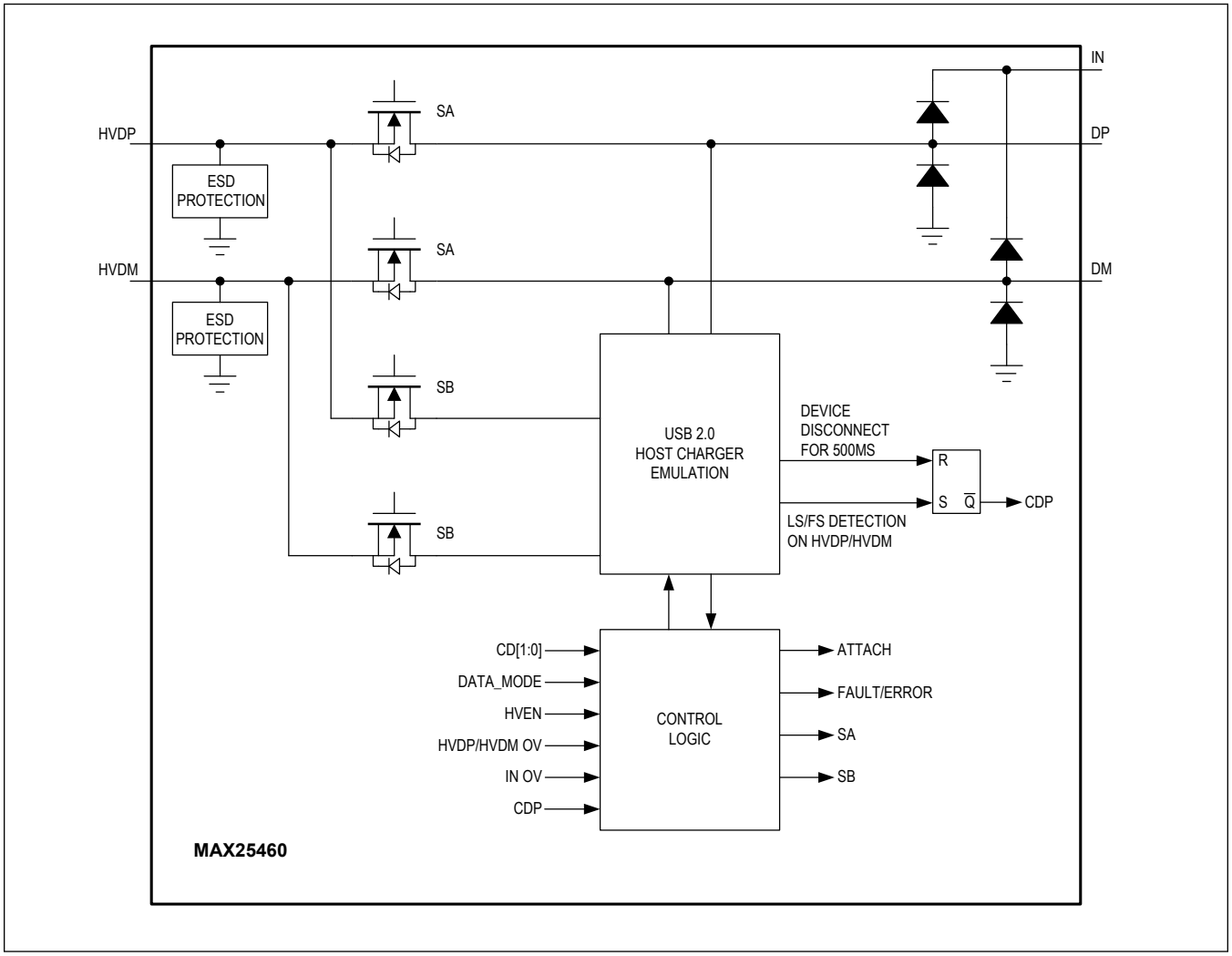


Figure 1. Data Switch and Charge-Detection Block Diagram

USB On-the-Go and Dual-Role Applications

The MAX25460 is fully compatible with USB on-the-go (OTG) and dual-role applications. A negotiated role swap (HNP or Apple CarPlay) requires no software interaction with the IC. When there is no negotiation before the SOC enters peripheral mode, the MAX25460 must be in hi-speed pass-through (SDP mode) before and during the role swap. All variants default to SDP mode on startup if the DATA_MODE pin is logic-low. This configuration allows a role swap immediately on startup without microcontroller interaction.

I²C, Control, and Diagnostics

I²C Configuration (CONFIG1 and I²C)

The MAX25460 I²C variants allow basic device configuration through a 1% resistor placed to GND on the CONFIG1 pin. The configuration parameters correlating to the chosen resistor are pre-loaded into their respective I²C registers on startup when HVEN is toggled high. After startup, the user is free to change the affected I²C registers as desired.

For I²C variants, CONFIG1 sets the startup value of the DC-DC spread-spectrum enable bit SS_EN and the SYNC direction control bit SYNC_DIR. CONFIG1 also sets the LSBs of the I²C target address. The configuration table for the I²C variant CONFIG table is shown in Table 4.

Table 4. CONFIG1 Pin Table (I²C Version)

RESISTANCE (Ω, 1%)	STEP	SS_EN	SYNC_DIR	I²C_ADDR LSBs
Short to GND	**0**	1 (ON)	1 (IN)	00
590	**1**	1 (ON)	1 (IN)	01
931	**2**	1 (ON)	1 (IN)	10
1300	**3**	1 (ON)	1 (IN)	11
1740	**4**	1 (ON)	0 (OUT)	00
2260	**5**	1 (ON)	0 (OUT)	01
2940	**6**	1 (ON)	0 (OUT)	10
3740	**7**	1 (ON)	0 (OUT)	11
4750	**8**	0 (OFF)	1 (IN)	00
6040	**9**	0 (OFF)	1 (IN)	01
7870	**10**	0 (OFF)	1 (IN)	10
10500	**11**	0 (OFF)	1 (IN)	11
14700	**12**	0 (OFF)	0 (OUT)	00
22600	**13**	0 (OFF)	0 (OUT)	01
43200	**14**	0 (OFF)	0 (OUT)	10
Short to BIAS (or R > 71.5kΩ)	**15**	0 (OFF)	0 (OUT)	11

Stand-Alone Configuration (CONFIG1–CONFIG3)

The MAX25460 stand-alone variants allow full device configuration from three 1% resistors placed among the three CONFIG pins and GND. For stand-alone variants, SDA and SCL serve as CONFIG2 and CONFIG3, respectively.

CONFIG1 sets the internal oscillator switching frequency, SYNC pin direction, and DC-DC spread spectrum mode. CONFIG2 sets the four LSBs of the voltage adjustment gain (GAIN[3:0]). CONFIG3 sets the USB DC current limit and MSB of voltage adjustment gain (GAIN[4]). See the following tables for stand-alone variant CONFIG options. See the *Applications Information* section for setting selection and *Ordering Information* for variant part number information.

Table 5. CONFIG1 Pin Table (Stand-Alone Variants)

RESISTANCE (Ω, 1%)	STEP	SS_EN	SYNC_DIR	FSW (kHz)
Short to GND	**0**	ON	IN	2200
1740	**4**	ON	OUT	2200
4750	**8**	OFF	IN	2200
14700	**12**	OFF	OUT	2200

Table 6. CONFIG2 and CONFIG3 Pin Table (Stand-Alone Variants)

		CONFIG2	CONFIG3	
RESISTANCE (Ω, 1%)	**STEP**	**GAIN[3:0]**	**GAIN[4]**	**CURRENT LIMIT ILIM_SET (A)**
Short to GND	**0**	0b0000	0	0.55

Table 6. CONFIG2 and CONFIG3 Pin Table (Stand-Alone Variants) (continued)

590	**1**	0b0001	0	1.62
931	**2**	0b0010	0	1.62
1300	**3**	0b0011	0	1.62
1740	**4**	0b0100	1	0.55
2260	**5**	0b0101	1	1.62
2940	**6**	0b0110	1	1.62
3740	**7**	0b0111	1	1.62
4750	**8**	0b1000	0	0.55
6040	**9**	0b1001	0	1.62
7870	**10**	0b1010	0	1.62
10500	**11**	0b1011	0	1.62
14700	**12**	0b1100	1	0.55
22600	**13**	0b1101	1	1.62
43200	**14**	0b1110	1	1.62
Short to BIAS (or R > 71.5kΩ)	**15**	0b1111	1	1.62

I²C Diagnostics and Event Handling

The I²C-based diagnostic functionality is independent of the $\overline{\text{FAULT}}$ pin. Setting the IRQMASK bit for a specific fault condition does not mask the $\overline{\text{FAULT}}$ pin for the respective fault. IRQMASK register functionality affects only the behavior of the $\overline{\text{INT}}$ pin. This allows the $\overline{\text{FAULT}}$ pin to be tied to overcurrent fault input of a hub controller or SoC while the I²C interface is simultaneously used by the system software for advanced diagnostic functionality.

Interrupt and Attach Output ($\overline{\text{INT}}$($\overline{\text{ATTACH}}$))

The MAX25460 $\overline{\text{INT}}$($\overline{\text{ATTACH}}$) pin functions as an interrupt ($\overline{\text{INT}}$) for I²C variants. The $\overline{\text{INT}}$ pin asserts an interrupt based on the configuration of the IRQ_MASK_0, IRQ_MASK_1, and IRQ_MASK_2 registers. Interrupt configuration allows the $\overline{\text{INT}}$ pin to assert any of the featured fault detection, as well as on device attachment. The $\overline{\text{INT}}$ pin only asserts while a masked IRQ bit is asserted, which means its behavior is also dependent on the AUTOCLR bit.

Stand-alone variants of the MAX25460 feature an open-drain, active-low, $\overline{\text{ATTACH}}$ output that serves as the attach detection pin. For stand-alone variants, the $\overline{\text{ATTACH}}$ pin can be used for GPIO input to a microprocessor or to drive an LED for attach/charge indication.

The $\overline{\text{INT}}$($\overline{\text{ATTACH}}$) assertion logic is shown in *ATTACH Logic Diagram*.

I²C Interface

The MAX25460 features an I²C, two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX25460 and the controller at clock rates up to 400kHz. The controller, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 2 shows the two-wire interface timing diagram.

A controller device communicates to the MAX25460 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8-bit long and is always followed by an acknowledge clock pulse. The MAX25460 SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus.

The MAX25460 SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple controllers on the bus, or if the controller in a single-controller system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

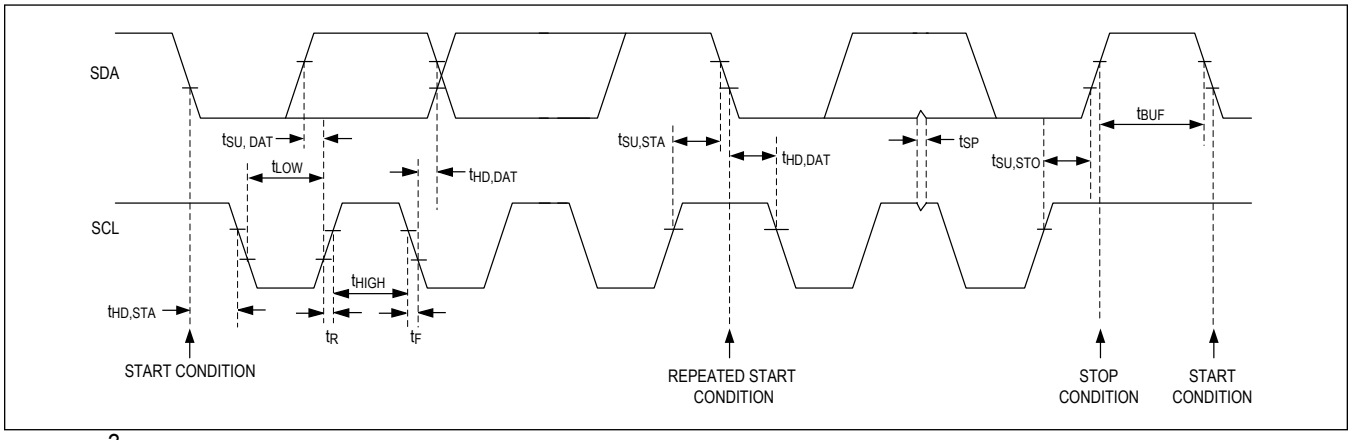


Figure 2. I²C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are considered control signals (see the *STOP and START Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

STOP and START Conditions

A controller device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 3). A START (S) condition from the controller signals the beginning of a transmission to the MAX25460. The controller terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

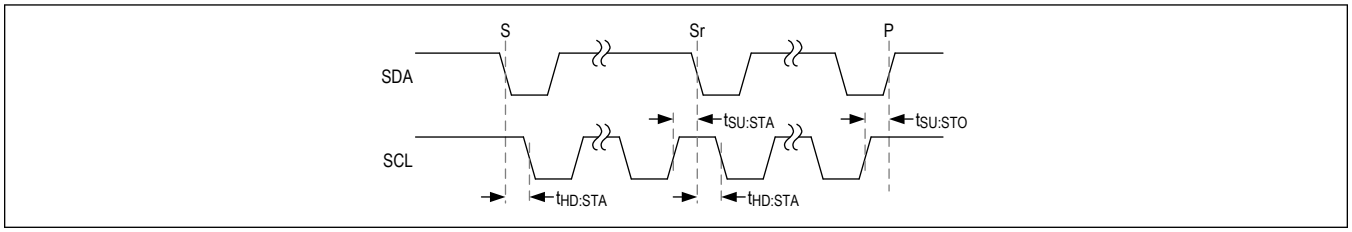


Figure 3. START, STOP, and REPEATED START Conditions

Early STOP Condition

The MAX25460 recognizes a STOP condition at any point during data transmission unless the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow target devices to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called clock stretching. The MAX25460 does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The MAX25460 does not implement the I²C specifications general call address. If the MAX25460 sees the general call address (0b0000_0000), it does not issue an acknowledge.

I²C Target Addressing

Once the device is enabled, the I²C target address is set by the CONFIG1 pin.

The address is defined as the 7 most significant bits (MSBs) followed by the R/$\overline{W}$ bit. Set the R/$\overline{W}$ bit to 1 to configure the device to read mode. Set the R/$\overline{W}$ bit to 0 to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

Table 7. I²C Target Addresses

CONFIG1 CODE	A6	A5	A4	A3	A2	A1	A0	7-BIT ADDRESS	WRITE	READ
0b00	0	1	1	0	0	0	0	0x30	0x60	0x61
0b01	0	1	1	0	0	0	1	0x31	0x62	0x63
0b10	0	1	1	0	0	1	0	0x32	0x64	0x65
0b11	0	1	1	0	0	1	1	0x33	0x66	0x67

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 4). The device pulls down SDA during the controller-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller can reattempt communication.

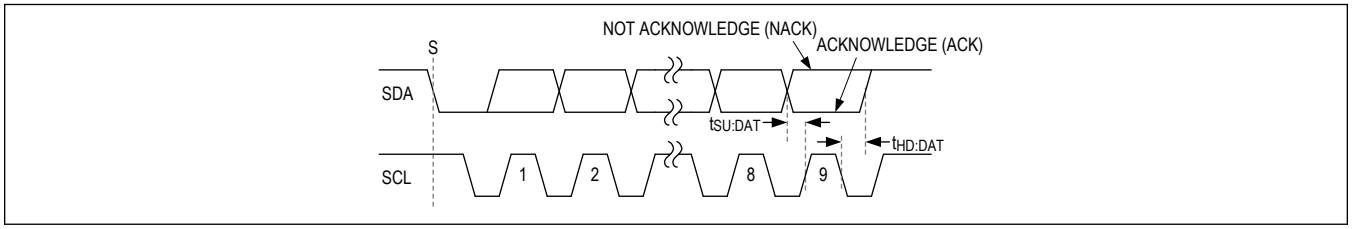


Figure 4. Acknowledge Condition

Write Data Format

A write to the device includes transmission of a START condition, the target address with the write bit set to 0, one byte of data to a register address, one byte of data to the command register, and a STOP condition. Figure 5 illustrates the proper format for one frame.

Read Data Format

A read from the device includes transmission of a START condition, the target address with the write bit set to 0, one byte of data from a register address, restart condition, the target address with read bit set to 1, one byte of data to the command register, and a STOP condition. Figure 5 illustrates the proper format for one frame.

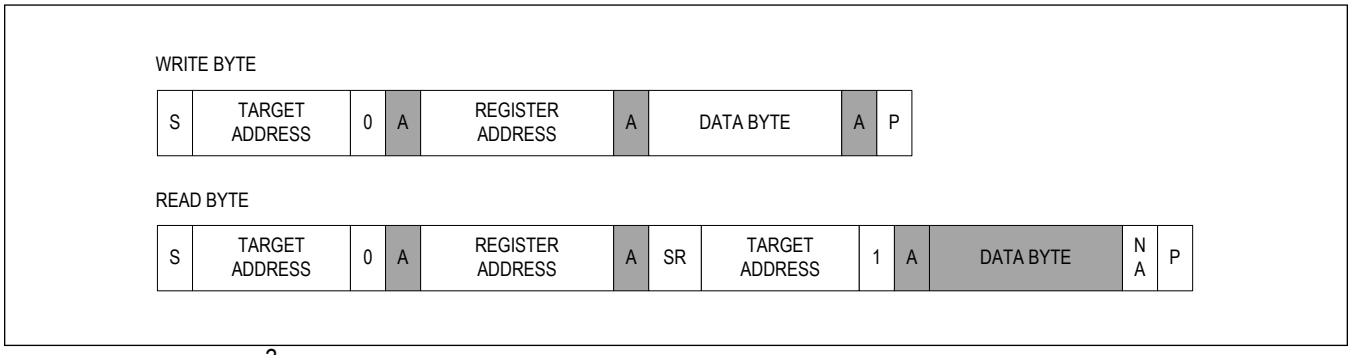


Figure 5. Data Format of I²C Interface

Fault Detection and Diagnostics

Fault Detection

The MAX25460 features advanced device protection features with automatic fault handing and recovery. Table 8 summarizes the conditions that generate a fault, and the actions taken by the device. For all variants, the $\overline{FAULT}$ output remains asserted as long as a fault condition persists.

For I²C variants, the IRQ registers provide detailed information on the source of the fault condition, and the IRQMASK registers allow selection of the criteria for assertion of the I²C Interrupt pin, $\overline{INT}$. The IRQ register bits clear when read. However, the IRQ bits that represent a present fault condition continue to reassert after they are cleared, so long as the fault condition persists. If the IRQMASK registers are configured to assert $\overline{INT}$ for a present fault, the $\overline{INT}$ pin deasserts when the IRQ register that asserted the interrupt is read. The $\overline{INT}$ pin subsequently reasserts if the fault condition persists.

Fault Output Pin ($\overline{FAULT}$)

The MAX25460 features an open-drain, active-low $\overline{FAULT}$ output. The MAX25460 is designed to eliminate false $\overline{FAULT}$ reporting by using an internal deglitch and fault blanking timer. This ensures that $\overline{FAULT}$ is not incorrectly asserted during normal operation such as starting into high-capacitance loads. The $\overline{FAULT}$ pin can be tied directly to the overcurrent fault input of a hub controller or SoC.

Table 8. Fault Conditions

EVENT	IRQ REGISTER BITS (I²C ONLY)	DEBOUNCE PRIOR TO ACTION	ACTION TAKEN
Thermal Shutdown	THM_SHD	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and disable R_P. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, enable R_P and the DC-DC converter.
Thermal Warning/ Foldback	THM_WARN	20ms	Assert associated IRQ bit. When fault resolves and RETRY_TMR expires.
IN Overvoltage	IN_OV	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and reset BC1.2. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, close data switches, enable the DC-DC converter.
HVDP/HVDM Overvoltage	DATA_OV	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, open data switches, and reset BC1.2. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, close data switches, enable the DC-DC converter.
USB DC Overcurrent	VBUS_ILIM	16ms + ILIM_SET Timer	Assert $\overline{FAULT}$ pin and associated IRQ bit after overcurrent condition persists for 16ms. When overcurrent resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.

Table 8. Fault Conditions (continued)

EVENT	IRQ REGISTER BITS (I^2C ONLY)	DEBOUNCE PRIOR TO ACTION	ACTION TAKEN
USB DC Overcurrent and SENSN < 4.38V	VBUS_ILIM_UV	16ms + ILIM_SET Timer	ILIM_ITRIP = 0: Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter after overcurrent and undervoltage condition persists for 16ms. Release $\overline{FAULT}$ pin, enable DC-DC converter once RETRY_TMR expires after shutdown. I^2C variant and ILIM_ITRIP = 1: Assert $\overline{FAULT}$ pin and associated IRQ bit after overcurrent condition persists for 16ms. When overcurrent resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.
SENSN < 4.38V	VBUS_UV	16ms	Assert $\overline{FAULT}$ pin and associated IRQ bit after undervoltage condition persists for 16ms. When undervoltage resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin.
USB DC Overcurrent and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, and open data switches. Release $\overline{FAULT}$ pin, enable DC-DC converter once RETRY_TMR expires after shutdown.
LX Overcurrent for 4 Consecutive Cycles and SENSN < 2V	VBUS_SHT_GND	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, and open data switches. Release $\overline{FAULT}$ pin, enable DC-DC converter once RETRY_TMR expires after shutdown.
SENSN Overvoltage	VBUS_OV	Immediate	Assert $\overline{FAULT}$ pin and associated IRQ bit, shut down DC-DC converter, and open data switches. When fault resolves and RETRY_TMR expires, release $\overline{FAULT}$ pin, DC-DC converter, and data switches.

Register Map

Summary Table

ADDRESS	NAME	MSB							LSB
USER_CMDS									
0x00	SETUP_0[7:0]	–	–	EN_DCDC	–	–	–	SYNC_DIR	SS_EN
0x01	SETUP_1[7:0]	–	–	–	GAIN[4:0]				
0x02	SETUP_2[7:0]	ILIM_DEB[1:0]		–	ILIM_ITRIP	–	ILIM[2:0]		
0x03	SETUP_3[7:0]	RETRY_TMR[1:0]		CD[1:0]		–	–	–	–
0x04	SETUP_4[7:0]	–	–	–	–	–	–	–	CONFIGURED
0x07	IRQ_MASK_0[7:0]	IRQ_AUTOCLR	–	–	–	EN_BC_ATTACH_IRQ	–	EN_BC_ATTACH_EV	–
0x08	IRQ_MASK_1[7:0]	–	–	EN_VBUS_ILIM_UV	EN_VBUS_ILIM	EN_VBUS_OV	EN_VBUS_UV	EN_VBUS_SHT_GND	EN_THM_SHD
0x09	IRQ_MASK_2[7:0]	–	–	–	–	EN_THM_WARN	EN_IN_OV	EN_DATA_OV	–
0x0A	IRQ_0[7:0]	UNCONFIGURED	–	–	–	BC_ATTACH_IRQ	–	BC_ATTACH_EV	–
0x0B	IRQ_1[7:0]	–	–	VBUS_ILIM_UV	VBUS_ILIM	VBUS_OV	VBUS_UV	VBUS_SHT_GND	THM_SHD
0x0C	IRQ_2[7:0]	–	–	–	–	THM_WARN	IN_OV	DATA_OV	–
0x0D	STATUS[7:0]	–	–	–	–	BC_ATTACH	–	–	–

Register Details

SETUP_0 (0x0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	EN_DCDC	–	–	–	SYNC_DIR	SS_EN
Reset	–	–	0b1	–	–	–		
Access Type	–	–	Write, Read	–	–	–	Write, Read, Dual	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION	DECODE
EN_DCDC	5	DC/DC Converter Enable. Internally AND'ed with the ENBUCK pin.	0 = Disable V_{BUS} Buck Converter 1 = Enable V_{BUS} Buck Converter
SYNC_DIR	1	SYNC Pin Direction Selection Initial value set by CONFIG1 resistor.	0 = Output 1 = Input
SS_EN	0	Spread Spectrum Enable Initial value set by CONFIG1 resistor.	0 = Disable Spread Spectrum Function 1 = Enable Spread Spectrum Function

SETUP_1 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	GAIN[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read, Dual				

BITFIELD	BITS	DESCRIPTION	DECODE
GAIN	4:0	The gain of the voltage correction applied to the buck converter output (based on DC load sensed by current-sense amp). R_{SENSE} = 33mΩ.	0: 0mΩ 1: 18mΩ 2: 36mΩ 3: 54mΩ 4: 72mΩ 5: 90mΩ 6: 108mΩ 7: 126mΩ 8: 144mΩ 9: 162mΩ 10: 180mΩ 11: 198mΩ 12: 216mΩ 13: 234mΩ 14: 252mΩ 15: 270mΩ 16: 288mΩ 17: 306mΩ 18: 324mΩ 19: 342mΩ 20: 360mΩ 21: 378mΩ 22: 396mΩ 23: 414mΩ 24: 432mΩ 25: 450mΩ 26: 468mΩ 27: 486mΩ 28: 504mΩ 29: 522mΩ 30: 540mΩ 31: 558mΩ

SETUP_2 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	ILIM_DEB[1:0]		–	ILIM_ITRIP	–	ILIM[2:0]		
Reset	0b00		–	0b0	–	0b111		
Access Type	Write, Read		–	Write, Read, Dual	–	Write, Read, Dual		

BITFIELD	BITS	DESCRIPTION	DECODE
ILIM_DEB	7:6	Debounce Timer for USB DC Current-Limit Threshold	Debounce Timer for USB DC Current-Limit Threshold 0b00 = 1.1ms (min) 0b01 = 5.5ms (min) 0b10 = 11ms (min) 0b11 = No Debounce
ILIM_ITRIP	4	Determines the buck's retry behavior under USB DC current limit conditions.	0 = VBUS_ILIM_UV fault enabled. 1 = VBUS_ILIM_UV fault disabled.
ILIM	2:0	USB DC Current-Limit Threshold, R_{SENSE} = 33mΩ.	USB DC Current-Limit Threshold 0b000 = 0.3A (min) 0b001 = 0.55A (min) 0b010 = 0.8A (min) 0b011 = 1.05A (min) 0b100 = 1.62A (min) 0b101 = 1.62A (min) 0b110 = 1.62A (min) 0b111 = 1.62A (min)

SETUP_3 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	RETRY_TMR[1:0]		CD[1:0]		–	–	–	–
Reset	0b00				–	–	–	–
Access Type	Write, Read, Dual		Write, Read, Dual		–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
RETRY_TMR	7:6	Determines the length of the RETRY timer after a fault condition.	0b00 = 2.0s 0b01= 1.0s 0b10 = 0.5s 0b11= 16ms
CD	5:4	BC1.2 Charge Detection Configuration Selection. This register is pre-loaded based on the part number variant and the status of the DATA_MODE pin.	0b00 = High Speed Pass Through (SDP) 0b01 = Auto-CDP 0b10 = Reserved 0b11 = Reserved

SETUP_4 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	CONFIGURED
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CONFIGURED	0	I^2C configuration complete indicator Upon power-up, the buck converter is prevented from turning on until this bit is written to a one, indicating the part is fully configured for its intended mode of operation.	0 = I^2C Configuration Pending 1 = I^2C Configuration Complete

IRQ_MASK_0 (0x7)

A Read-Write register that configures which of the conditions in the IRQ_0 register will assert an Interrupt. See the IRQ_0 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	IRQ_AUTOCLR	–	–	–	EN_BC_ATTACH_IRQ	–	EN_BC_ATTACH_EV	–
Reset	0b0	–	–	–	0b0	–	0b0	–
Access Type	Write, Read	–	–	–	Write, Read	–	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
IRQ_AUTOCLR	7	IRQ Auto Clear	0 = IRQ register flags are latched on until read. 1 = IRQ register flags are automatically cleared when the error condition is removed.
EN_BC_ATTACH_IRQ	3	BC1.2 ATTACH STATUS Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_BC_ATTACH_EV	1	BC1.2 ATTACH EVENT Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_MASK_1 (0x8)

A Read-Write register that configures which of the conditions in the IRQ_1 register will assert an Interrupt. See the IRQ_1 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	–	EN_VBUS_ILIM_UV	EN_VBUS_ILIM	EN_VBUS_OV	EN_VBUS_UV	EN_VBUS_SHT_GND	EN_THM_SHD
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VBUS_ILIM_UV	5	VBUS_ILIM_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_ILIM	4	VBUS_ILIM Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_OV	3	VBUS_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_UV	2	VBUS_UV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_VBUS_SHT_GND	1	VBUS_SHT_GND Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_THM_SHD	0	THM_SHD Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_MASK_2 (0x9)

A Read-Write register that configures which of the conditions in the IRQ_2 register will assert an Interrupt. See the IRQ_2 register for condition descriptions.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN_THM_WARN	EN_IN_OV	EN_DATA_OV	–
Reset	–	–	–	–	0b0	0b0	0b0	–
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	–

BITFIELD	BITS	DESCRIPTION	DECODE
EN_THM_WARN	3	THM_WARN Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_IN_OV	2	IN_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt
EN_DATA_OV	1	DATA_OV Interrupt Enable	0 = Not included in Interrupt 1 = Included in Interrupt

IRQ_0 (0xA)

A read only register that includes flags which indicate a number of operating conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

IRQ_0 holds notifications of expected operations rather than error/fault conditions.

BIT	7	6	5	4	3	2	1	0
Field	UNCONFIGURED	–	–	–	BC_ATTACH_IRQ	–	BC_ATTACH_EV	–
Reset	0b1	–	–	–	0b0	–	0b0	–
Access Type	Read Clears All	–	–	–	Read Clears All	–	Read Clears All	–

BITFIELD	BITS	DESCRIPTION	DECODE
UNCONFIGURED	7	I^2C Unconfigured Indicator Bit	0 = Device is fully configured (CONFIGURED written to 1) 1 = Device is not fully configured (CONFIGURED has not been written to 1)
BC_ATTACH_IRQ	3	BC1.2 ATTACH Indicator This bit indicates a BC1.2 device attach is observed via the HVDP/HVDM pins.	0 = No device attached 1 = Device attached
BC_ATTACH_EV	1	BC1.2 ATTACH Event Detected This bit indicates a BC1.2 device attach was initiated and/or terminated as observed via the HVDP/HVDM pins.This bit differs from BC_ATTACH (which indicates the current BC1.2 attach status in real time) in that it is issued only when the status changes from unattached to attached or vice-versa. Clear on Read. Not affected by IRQ_AUTOCLR.	0 = No attach or detach event detected since least read 1 = New attach and/or detach event detected

IRQ_1 (0xB)

A read only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	VBUS_ILIM_UV	VBUS_ILIM	VBUS_OV	VBUS_UV	VBUS_SHT_GND	THM_SHD
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
VBUS_ILIM_UV	5	V_{BUS} Current Limit and SENSN UV Fault Detected Disabled when ILIM_ITRIP = 1. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_ILIM	4	V_{BUS} Current Limit Condition Detected Disabled when ILIM_ITRIP = 0. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_OV	3	V_{BUS} Overvoltage Fault Detected Detected on SENSN pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_UV	2	V_{BUS} Under Voltage Fault Detected Detected on SENSN pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
VBUS_SHT_GND	1	V_{BUS} Short to Ground Fault Detected Detected on SENSN pin. Clear on Read if condition is resolved.	0 = No event 1 = Event detected
THM_SHD	0	Over Temperature Fault Detected Asserts when the die temperature exceeds 165°C (typ). Clear on Read if condition is resolved.	0 = No event 1 = Event detected

IRQ_2 (0xC)

A read only register that includes flags which indicate a number of error conditions. These flags can assert an interrupt by setting the corresponding bit in the MASK register.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	THM_WARN	IN_OV	DATA_OV	–
Reset	–	–	–	–	0b0	0b0	0b0	–
Access Type	–	–	–	–	Read Clears All	Read Clears All	Read Clears All	–

BITFIELD	BITS	DESCRIPTION	DECODE
THM_WARN	3	Thermal Warning Condition Detected Asserts when the temperature has reached 140°C (typ). Clear on Read if condition is resolved.	0 = No event since least read 1 = New event detected
IN_OV	2	IN Pin Overvoltage Fault Detected Clear on Read if condition is resolved.	0 = No event 1 = Event detected
DATA_OV	1	DATA Pin Overvoltage Fault Detected Clear on Read if condition is resolved.	0 = No event 1 = Event detected

STATUS (0xD)

A read only register that includes information on the current status of the IC.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	BC_ATTACH	–	–	–
Reset	–	–	–	–	0b0	–	–	–
Access Type	–	–	–	–	Read Only	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
BC_ATTACH	3	BC1.2 ATTACH Status Indicator This bit indicates the current device attach status via the HVDP/HVDM pins.	0 = No device currently attached 1 = Device currently attached

Applications Information

DC-DC Switching Frequency Selection

The switching frequency (f_{SW}) for MAX25460 is fixed at 2.2MHz. Higher switching frequencies allow for smaller PCB area designs with lower inductor values and less output capacitance. Consequently, peak currents and I^2R losses are lower at higher switching frequencies, but core losses, gate charge currents, and switching losses increase.

DC-DC Input Capacitor Selection

The input capacitor supplies the instantaneous current needs of the buck converter and reduces the peak currents drawn from the upstream power source. The input bypass capacitor is a determining factor in the input voltage ripple.

The input capacitor RMS current rating requirement ($I_{IN(RMS)}$) is defined by the following equation:

$$I_{IN(RMS)} = I_{LOAD}\frac{\sqrt{V_{SENSP} \times \left(V_{SUPSW} - V_{SENSP}\right)}}{V_{SUPSW}}$$

$I_{IN(RMS)}$ has a maximum value when the input voltage equals twice the output voltage ($V_{SUPSW} = 2 \cdot V_{SENSP}$), so $I_{IN(MAX)} = \frac{1}{2} \cdot I_{LOAD(MAX)}$. I_{LOAD} is the measured operating load current while $I_{LOAD(MAX)}$ refers to the maximum load current.

Choose an input capacitor that exhibits less than 10ºC self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple comprises V_Q (caused by the capacitor discharge) and V_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple current capability at the input. Assume that the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{\left(V_{SUPSW} - V_{SENSP}\right) \times V_{SENSP}}{V_{SUPSW} \times f_{SW} \times L}$$

and

$$C_{IN} = \frac{I_{LOAD(MAX)} \times D\left(1 - D\right)}{\Delta V_Q \times f_{SW}} \text{ where } D = \frac{V_{SENSP}}{V_{SUPSW}}$$

Where D is the buck converter duty cycle.

Bypass SUPSW with 0.1µF parallel to 4.7µF of ceramic capacitance close to the SUPSW and PGND pins. The ceramic input capacitor of a buck converter has a high $\frac{di}{dt}$, minimize the PCB current-loop area to reduce EMI. Bypass SUPSW with 22µF of bulk electrolytic capacitance to dampen line transients.

DC-DC Output Capacitor Selection

To ensure stability and compliance with the USB and Apple specifications, follow the recommended output filters listed in Table 9. For proper functionality, a minimum amount of ceramic capacitance must be used regardless of f_{SW}. Additional capacitance for lower switching frequencies can be low-ESR electrolytic types (< 0.25Ω).

DC-DC Output Inductor Selection

Three key inductor parameters must be considered when selecting an inductor: inductance value (L), inductor saturation

current (I_{SAT}), and DC resistance (R_{DCR}). To select the proper inductance value, the ratio of inductor peak-to-peak AC to DC average current (LIR) must be selected. A small LIR reduces the RMS current in the output capacitor and results in small output ripple voltage, but this requires a larger inductor. A good compromise between size and loss is LIR = 0.35 (35%). Determine the inductor value using the following equation:

$$L = \frac{V_{SENSP} \times \left(V_{SUPSW} - V_{SENSP}\right)}{V_{SUPSW} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

where V_{SUPSW} and V_{SENSP} are typical values (such that efficiency is optimum for nominal operating conditions). Ensure the inductor I_{SAT} is above the buck converter's cycle-by-cycle peak current limit.

Table 9. Recommended Output Filters

f_{SW} (kHz)	L_{OUT} (µH)	RECOMMENDED C_{OUT}
2200	1.5	22µF ceramic

DC-DC Diode Selection

The device requires an external Schottky diode rectifier as a freewheeling diode. Connect this rectifier close to the MAX25460 using short PCB traces. In FPWM mode, the Schottky diode helps minimize efficiency losses by diverting the inductor current that would otherwise flow through the low-side MOSFET. Choose a rectifier with a reverse voltage rating greater than the maximum expected input voltage, V_{SUPSW}, while minimizing forward voltage drop. Use a low forward-voltage-drop Schottky rectifier to limit the negative voltage at LX. Choose a Schottky rectifier with a low diode capacitance at the reverse voltage operating point to minimize EMI caused from the diode ringing at turn-off.

Layout Considerations

Proper PCB layout is critical for robust system performance. See the MAX25460 EV kit data sheet for an example layout. Minimize the current-loop area and the parasitics of the DC-DC conversion circuitry to reduce EMI. The input capacitor placement should be prioritized because in a buck converter, the ceramic input capacitor has high $\frac{di}{dt}$. Place the input capacitor, power inductor, and output capacitor as close as possible to the IC SUPSW and PGND pins. Shorter traces should be prioritized over wider traces.

A low-impedance ground connection between the input and output capacitor is required (route through the ground pour on the exposed pad). Connect the exposed pad to ground. Place multiple vias in the pad to connect to all other ground layers for proper heat dissipation. Failure to do so can result in the IC repeatedly reaching thermal shutdown. Do not use separate power and analog ground planes. Instead, use a single common ground and manage currents through component placement. High-frequency return current flows through the path of least impedance (through the ground pour directly underneath the corresponding traces).

The USB traces must be routed as a 90Ω differential pair with an appropriate keep-out area. Avoid routing USB traces near clocks and high-frequency switching nodes. The length of the routing should be minimized and avoid 90° turns, excessive vias, and RF stubs.

Determining USB System Requirements

The nominal cable resistance (with tolerance) for both the USB power wire (BUS) and return GND should be determined from the cable manufacturer. In addition, be sure to include the resistance from any inline or PCB connectors. Determine the desired operating temperature range for the application, and consider the change in resistance over temperature.

A typical application presents a 200mΩ BUS resistance with a matching 200mΩ resistance in the ground path. In this application, the voltage drop at the far end of the captive cable is 600mV when the load current is 1.5A. This voltage drop requires the voltage-adjustment circuitry of the IC to increase the output voltage to comply with the USB and Apple specifications.

USB Loads

The MAX25460 is compatible with both USB-compliant and non-compliant loads. A compliant USB device is not allowed to sink more than 30mA and must not present more than 10µF of capacitance when initially attached to the port. The device then begins its HVD+/HVD- connection and enumeration process. After completion of the connect process, the

device can pull 100mA/150mA and must not present a capacitance greater than 10µF. This is considered the hot-inserted, USB-compliant load of 44Ω in parallel with 10µF.

For non-compliant USB loads, the ICs can also support both a hot insertion and soft-start into a USB load of 4.75Ω in parallel with 330µF.

USB Output Current Limit

The USB load current is monitored by an internal current-sense amplifier through the voltage created across R_{SENSE}. The MAX25460 offers a digitally adjustable USB current-limit threshold. See *SETUP_2* or Table 6 to select an appropriate register or resistor value for the desired current limit.

USB Voltage Adjustment

Figure 6 shows a DC model of the voltage-correction function of the MAX25460. Without voltage adjustment (V_{ADJ} = 0, GAIN[4:0] = 0), the voltage seen by the device at the end of the cable decreases linearly as load current increases. To compensate for this, the output voltage of the buck converter should increase linearly with load current. The slope of SENSP is called R_{COMP} such that $V_{ADJ} = R_{COMP} \cdot I_{LOAD}$ and $R_{COMP} = GAIN[4:0] \cdot R_{LSB} \cdot \frac{R_{SENSE}}{33m\Omega}$ (see Figure 7). The R_{COMP} adjustment values available on the MAX25460 are listed in the GAIN[4:0] register description and are based on a 33mΩ sense resistor.

For $V_{DUT} = V_{NO\_LOAD}$; $0 \le I_{LOAD}$, R_{COMP} must equal the sum of the system resistances. Calculate the minimum R_{COMP} for the system so that V_{DUT} stays constant:

$$R_{COMP\_SYS} = R_{LR} + R_{SENSE} + R_{PCB} + R_{CABLE\_VBUS} + R_{CABLE\_GND}$$

Where $R_{CABLE\_VBUS} + R_{CABLE\_GND}$ is the round-trip resistance of the USB cable (including the effect from the cable shield, if it conducts current), R_{LR} is the buck converter's load regulation expressed in mΩ (51mΩ typ.), and R_{PCB} is the resistance of any additional V_{BUS} parasitics (the V_{BUS} FET, PCB trace, ferrites, and the USB connectors). Find the setting for GAIN[4:0] using the minimum R_{COMP}.

$$GAIN[4:0] = ceiling\left(\frac{R_{COMP\_SYS}}{R_{LSB}} \cdot \frac{33m\Omega}{R_{SENSE}}\right)$$

The nominal DUT voltage can then be estimated at any load current by the following equation:

$$V_{DUT} = V_{NO\_LOAD} + R_{LSB} \cdot GAIN[4:0] \cdot \frac{R_{SENSE}}{33m\Omega} \cdot I_{LOAD} - R_{COMP\_SYS} \cdot I_{LOAD}$$

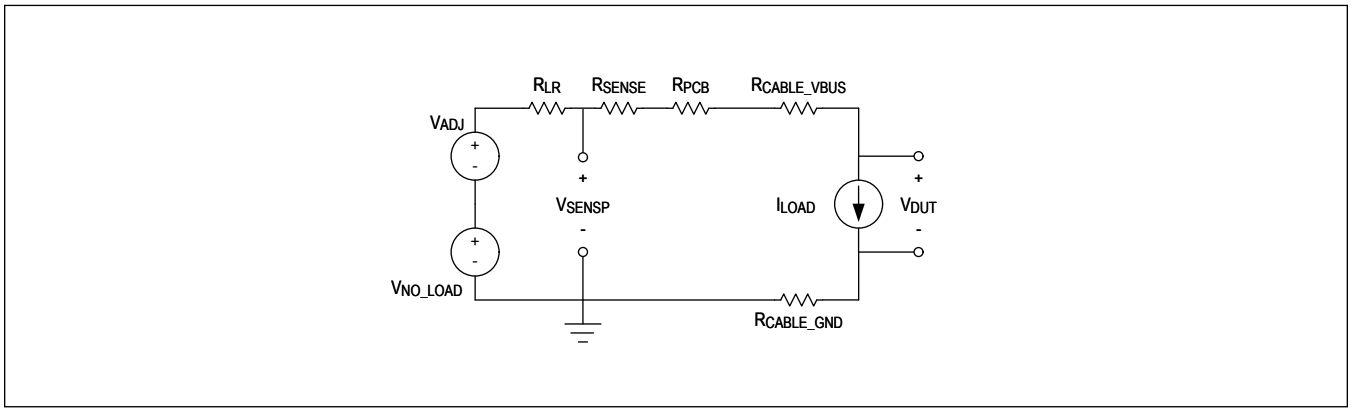


Figure 6. DC Voltage Adjustment Model

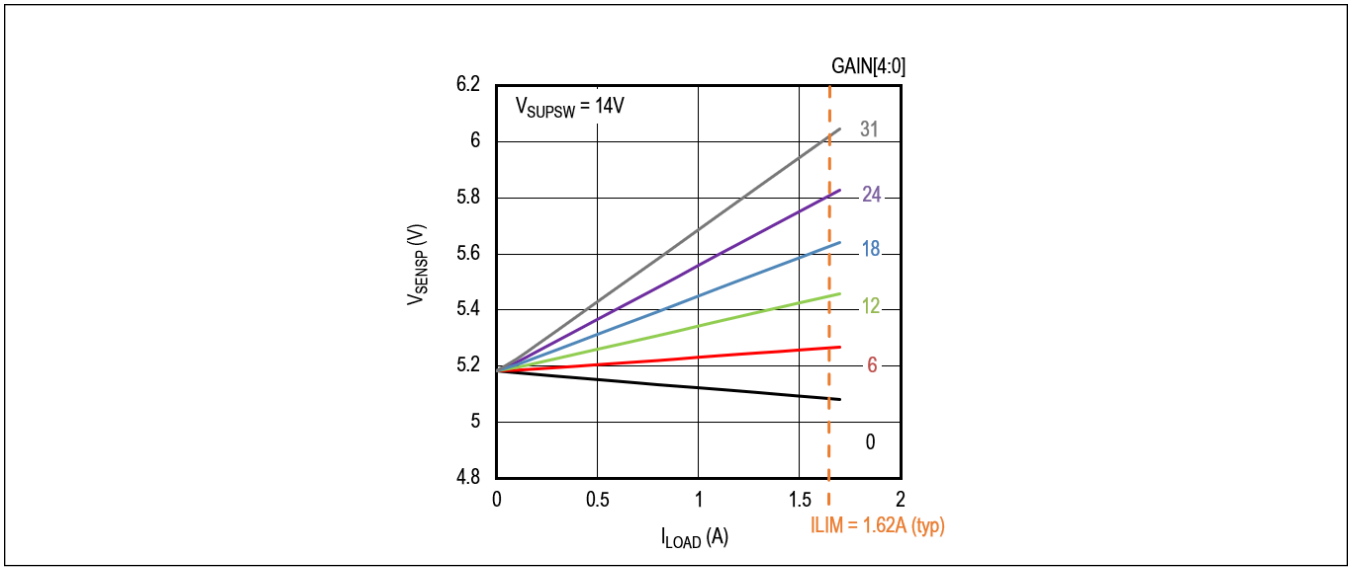


Figure 7. Increase in SENSP vs. USB Current

Tuning of USB Data Lines

The USB hi-speed mode requires careful PCB layout with 90Ω controlled differential impedance, matched traces of equal length, and with no stubs or test points. The MAX25460 includes high-bandwidth USB data switches (>1GHz). This means data-line tuning is generally not required. However, all designs are recommended to include pads that would allow LC components to be mounted on the data lines so that tuning can easily be performed later, if necessary. Tuning components should be placed as close as possible to the IC data pins, on the same layer of the PCB as the IC. The proper configuration of the tuning components is shown in Figure 8. Figure 9 shows the reference eye diagram used in the test setup. Figure 10 shows the MAX25460 high-voltage eye diagram on the standard EV kit with no tuning components. Tuning inductors should be high-Q wire-wound inductors. Contact Analog Devices, Inc.'s application team for assistance with the tuning process for your specific application.

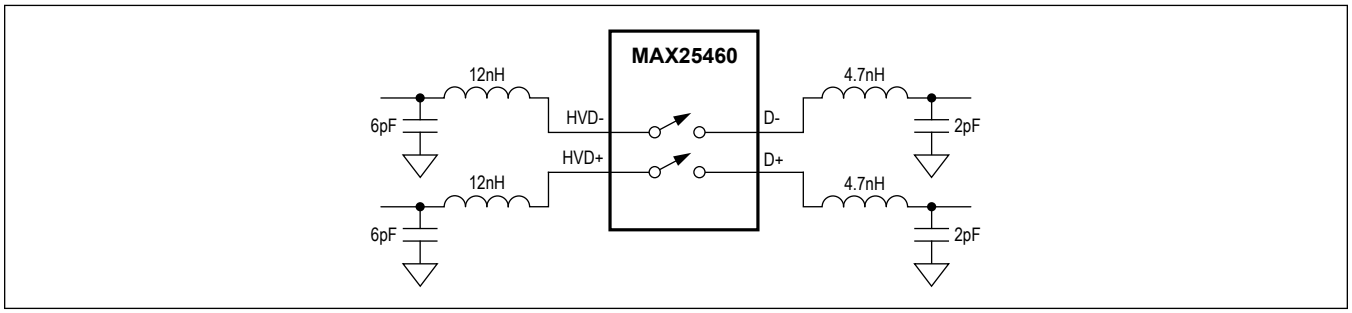


Figure 8. Tuning of Data Lines

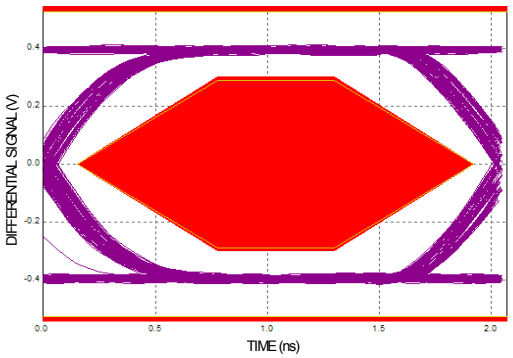


Figure 9. Near-Eye Diagram (with No Switch)

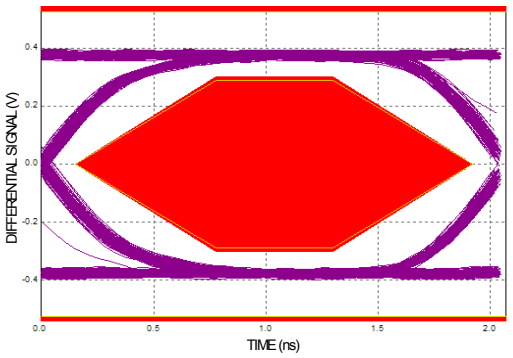


Figure 10. Untuned Near-Eye Diagram (with MAX25460)

USB Data Line Common-Mode Choke Placement

Most automotive applications use a USB-optimized common-mode choke to mitigate EMI signals from both leaving and entering the module. Optimal placement for this EMI choke is at the module's USB connector. This common-mode choke does not replace the need for the tuning inductors mentioned earlier.

ESD Protection

The MAX25460 requires no external ESD protection. The MAX25460 incorporates ESD structures to protect against electrostatic discharges encountered during handling and assembly. While competing, solutions can latch-up and require the power to be cycled after an ESD event, and the MAX25460 continues to work without latch-up. When used with the configuration shown in the *Typical Application Circuit*, the MAX25460 is characterized for protection to the following limits:

- ±15kV ISO 10605 (330pF, 2kΩ) Air Gap
- ±8kV ISO 10605 (330pF, 2kΩ) Contact
- ±15kV IEC 61000-4-2 (150pF, 330Ω) Air Gap
- ±8kV IEC 61000-4-2 (150pF, 330Ω) Contact

Note: All application-level ESD testing is performed on the standard evaluation kit with 1m captive cable.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Analog Devices for test setup, test methodology, and test results.

Human Body Model

Figure 11 shows the Human Body Model, and Figure 13 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX25460 helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the Human Body Model and IEC 61000-4-2 is a higher peak current in IEC 61000-4-2. As the series resistance is lower in the IEC 61000-4-2 ESD test model Figure 12, the ESD withstand-voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 14 shows the current waveform for the 8kV, IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

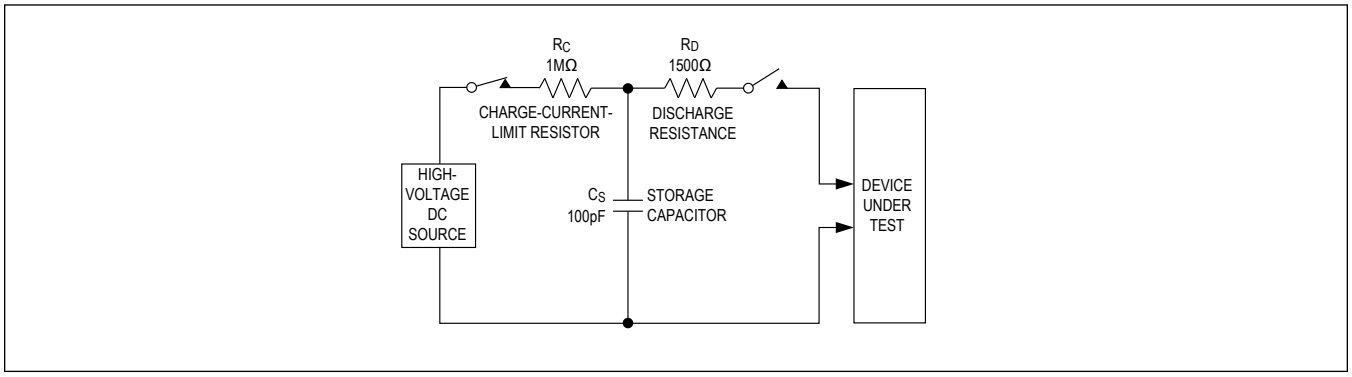


Figure 11. Human Body ESD Test Model

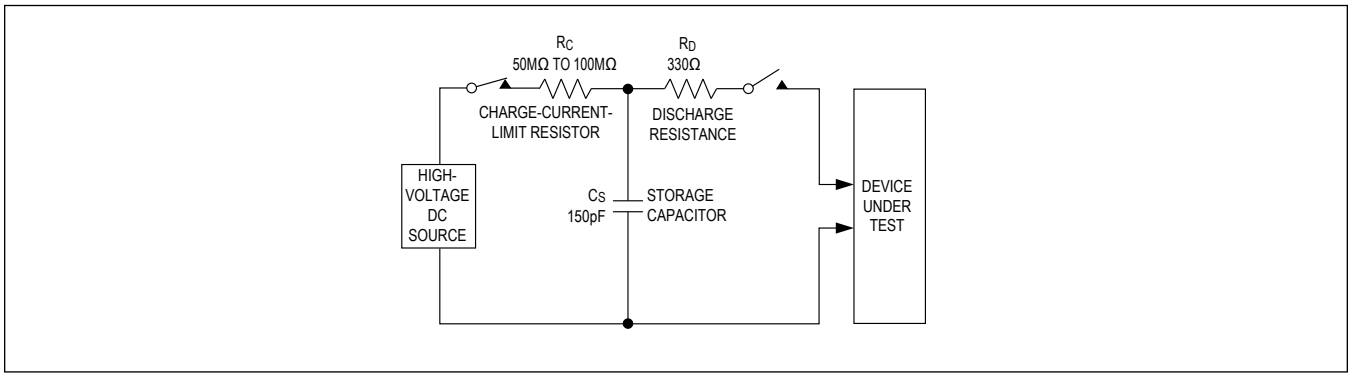


Figure 12. IEC 61000-4-2 ESD Test Model

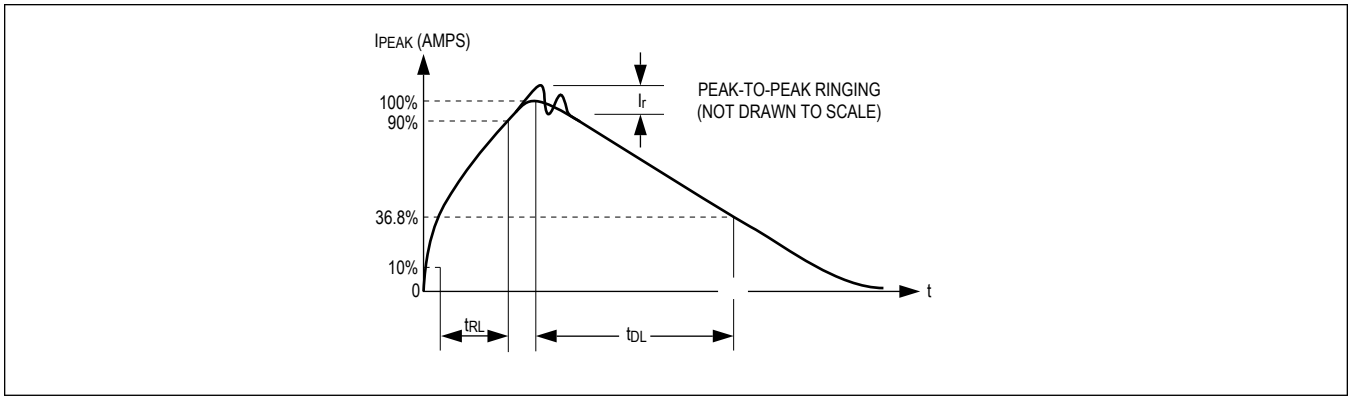


Figure 13. Human Body Current Waveform

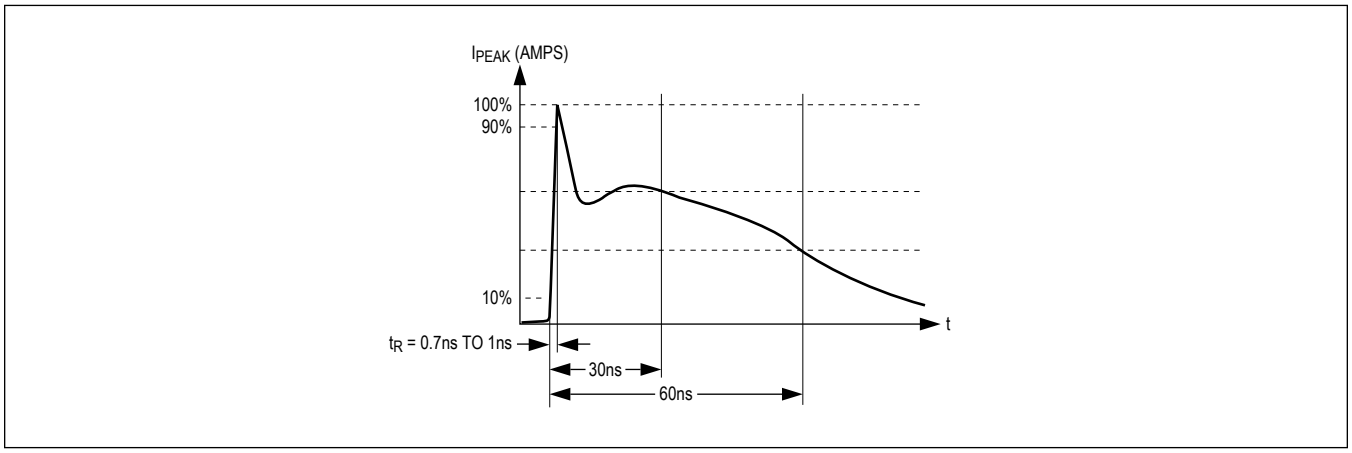
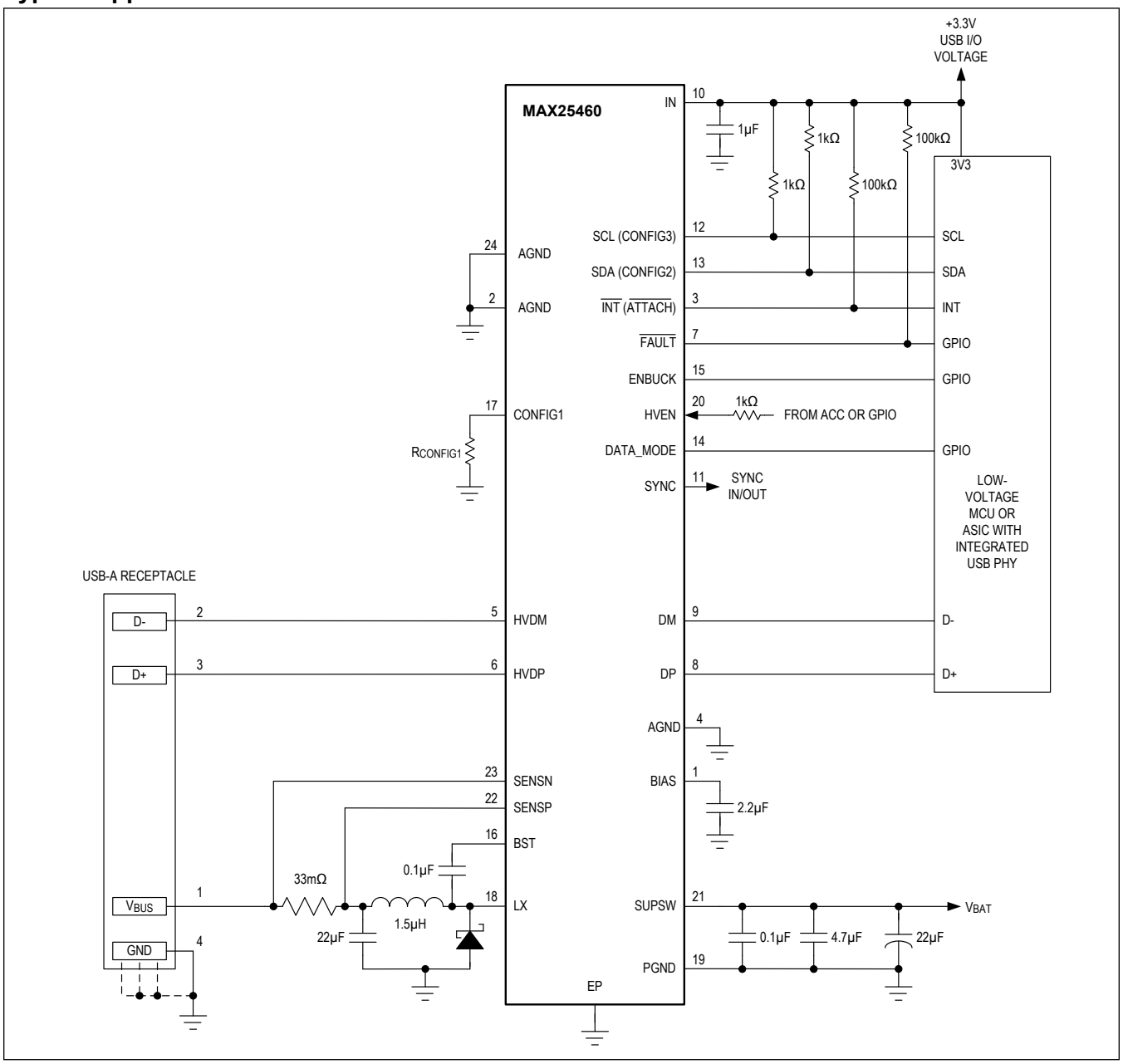


Figure 14. IEC 61000-4-2 Current Waveform

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	STARTUP MODE (DATA_MODE PIN = 0)	I^2C
MAX25460ATGA/V+T	-40°C to +125°C	24 TQFN-EP	HS Mode	Yes

/V Denotes Automotive Qualified Parts

+ Denotes a lead(Pb)-free/RoHS-compliant package.

EP = Exposed Pad.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/23	Release for Market Intro	—