19-4717; Rev 0; 7/09

MAXIM

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

General Description

The MAX16065/MAX16066 flash-configurable system managers monitor and sequence multiple system voltages. The MAX16065/MAX16066 can also accurately monitor (±2.5%) one current channel using a dedicated high-side current-sense amplifier. The MAX16065 manages up to twelve system voltages simultaneously, and the MAX16066 manages up to eight supply voltages. These devices integrate a selectable differential or single-ended analog-to-digital converter (ADC) and configurable outputs for sequencing power supplies. Device configuration information, including overvoltage and undervoltage limits, timing settings, and the sequencing order is stored in nonvolatile flash memory. During a fault condition, fault flags and channel voltages can be automatically stored in the nonvolatile flash memory for later read-back.

The internal 1% accurate 10-bit ADC measures each input and compares the result to one overvoltage, one undervoltage, and one early warning limit that can be configured as either undervoltage or overvoltage. A fault signal asserts when a monitored voltage falls outside the set limits. Up to three independent fault output signals are configurable to assert under various fault conditions.

Because the MAX16065/MAX16066 support a power-supply voltage of up to 14V, they can be powered directly from the 12V intermediate bus in many systems.

The integrated sequencer provides precise control over the power-up and power-down order of up to twelve (MAX16065) or up to eight (MAX16066) power supplies. Eight outputs (EN_OUT1–EN_OUT8) are configurable with charge-pump outputs to directly drive external n-channel MOSFETs.

The MAX16065/MAX16066 include eight/six programmable general-purpose inputs/outputs (GPIO_s). GPIO_s are flash configurable as dedicated fault outputs, as a watchdog input or output, or as a manual reset.

The MAX16065/MAX16066 feature nonvolatile fault memory for recording information during system shutdown events. The fault logger records a failure in the internal flash and sets a lock bit protecting the stored fault data from accidental erasure. An SMBus™ or a JTAG serial interface configures the MAX16065/MAX16066. The MAX16065 is available in a 48-pin, 7mm x 7mm, TQFN package, and the MAX16066 is available in a 40-pin, 6mm x 6mm, TQFN package. Both devices are fully specified from -40°C to +85°C.

SMBus is a trademark of Intel Corp.

Features

- **Operate from 2.8V to 14V**
- **±2.5% Current-Monitoring Accuracy**
- **1% Accurate 10-Bit ADC Monitors 12/8 Voltage Inputs**
- **Single-Ended or Differential ADC for System Voltage/Current Monitoring**
- **Integrated High-Side Current-Sense Amplifier**
- **12/8 Monitored Inputs with Overvoltage/Undervoltage/Early Warning Limit**
- **Nonvolatile Fault Event Logger**
- **Power-Up and Power-Down Sequencing Capability**
- **Independent Secondary Sequence Block**
- **12/8 Outputs for Sequencing/Power-Good Indicators**
- **Two Programmable Fault Outputs and One Reset Output**
- **Eight General-Purpose Inputs/Outputs Configurable as:**
  - **Dedicated Fault Outputs**
  - **Watchdog Timer Function**
  - **Manual Reset**
  - **Margin Enable**
- **SMBus (with Timeout) or JTAG Interface**
- **Flash Configurable Time Delays and Thresholds**
- **-40°C to +85°C Operating Temperature Range**

Applications

Networking Equipment

Telecom Equipment (Base Stations, Access)

Storage/Raid Systems

Servers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16065ETM+	-40°C to +85°C	48 TQFN-EP*
MAX16066ETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration and Typical Operating Circuits appear at end of data sheet.

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

ABSOLUTE MAXIMUM RATINGS

V_{CC}, CSP, CSM to GND.....-0.3V to +15V
CSP to CSM.....-0.7V to +0.7V
MON_, GPIO_, SCL, SDA, A0, RESET, EN_OUT9–EN_OUT12 to GND (programmed as open-drain outputs).....-0.3V to +6V
EN, TCK, TMS, TDI to GND .....-0.3V to +4V
DBP, ABP to GND...-0.3V to the lower of +3V and (V_{CC} + 0.3V)
EN_OUT1–EN_OUT8 to GND (programmed as open-drain outputs) .....-0.3V to +15V
TDO, EN_OUT_, GPIO_, RESET (programmed as push-pull outputs)..... -0.3V to (V_{DBP} + 0.3V)
Input/Output Current 20mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 26.3mW/°C above +70°C).....2105mW
48-Pin TQFN (derate 27.8mW/°C above +70°C).....2222mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at ABP = DBP = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	Reset output asserted low	1.2			V
		(Note 2)	2.8		14	
Undervoltage Lockout (Rising)	V_{UVLO}	Minimum voltage on V_{CC} to ensure the device is flash configurable			2.7	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}			100		mV
Minimum Flash Operating Voltage	V_{flash}	Minimum voltage on V_{CC} to ensure flash erase and write operations		2.7		V
Supply Current	I_{CC}	No load on output pins		4.5	7	mA
		During flash writing cycle		10	14	
ABP Regulator Voltage	V_{ABP}	C_{ABP} = 1µF, no load, V_{CC} = 5V	2.85	3	3.15	V
DBP Regulator Voltage	V_{DBP}	C_{ABP} = 1µF, no load, V_{CC} = 5V	2.8	3	3.1	V
Boot Time	t_{BOOT}	V_{CC} > V_{UVLO}		200	350	µs
Flash Writing Time		8-byte word		122		ms
Internal Timing Accuracy		(Note 3)	-8		+8	%
EN Input Voltage	$V_{TH\_EN\_R}$	EN voltage rising		1.41		V
	$V_{TH\_EN\_F}$	EN voltage falling	1.365	1.39	1.415	
EN Input Current	I_{EN}		-0.5		+0.5	µA
Input Voltage Range			0		5.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at ABP = DBP = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC DC ACCURACY							
Resolution						10	Bits
Gain Error	ADC_{GAIN}	T_A = +25°C				0.35	%
		T_A = -40°C to +85°C				0.70	
Offset Error	ADC_{OFF}					1	LSB
Integral Nonlinearity	ADC_{INL}					1	LSB
Differential Nonlinearity	ADC_{DNL}					1	LSB
ADC Total Monitoring Cycle Time	t_{CYCLE}	No MON_ fault detected			40	50	µs
ADC IN_ Ranges		1 LSB = 5.43mV			5.56		V
		1 LSB = 2.72mV			2.78		
		1 LSB = 1.36mV			1.39		
CURRENT SENSE							
CSP Input-Voltage Range	V_{CSP}			3		14	V
Input Bias Current	I_{CSP}				14	25	µA
	I_{CSM}	V_{CSP} = V_{CSM}			3	5	
CSP Total Unadjusted Error	CSP_{ERR}	(Note 4)				2	%FSR
Overcurrent Differential Threshold	OVC_{TH}	V_{CSP} - V_{CSM}	Gain = 48	21.5	25	30.5	mV
			Gain = 24	46	51	56	
			Gain = 12	94	101	108	
			Gain = 6	190	202	210	
V_{SENSE} Fault Threshold Hysteresis	OVC_{HYS}				0.5		% OVC_{TH}
Secondary Overcurrent Threshold Timeout	OVC_{DEL}	r73h[6:5] = '00'			0		ms
		r73h[6:5] = '01'		3	4	5	
		r73h[6:5] = '10'		12	16	20	
		r73h[6:5] = '11'		50	64	60	
V_{SENSE} Ranges		Gain = 6			232		mV
		Gain = 12			116		
		Gain = 24			58		
		Gain = 48			29		
ADC Current Measurement Accuracy		V_{SENSE} = 150mV (gain = 6 only)		-2.5	±0.2	+2.5	%
		V_{SENSE} = 50mV, gain = 12		-4	±0.2	+4	
		V_{SENSE} = 25mV, gain = 24			±0.5		
		V_{SENSE} = 10mV, gain = 48			±1		
Gain Accuracy		V_{SENSE} = 20mV to 100mV, V_{CSP} = 5V, gain = 6		-1.5		+1.5	%
Common-Mode Rejection Ratio	$CMRR_{SNS}$	V_{CSP} > 4V			80		dB
Power-Supply Rejection Ratio	$PSRR_{SNS}$				80		dB

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at ABP = DBP = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS (EN_OUT_, RESET, GPIO_)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
		I_{SINK} = 10mA, GPIO_ only			0.7	
		V_{CC} = 1.2V, I_{SINK} = 100µA (RESET only)			0.3	
Maximum Output Sink Current		Total current into EN_OUT_, RESET, GPIO_, V_{CC} = 3.3V			30	mA
Output-Voltage High (Push-Pull)		I_{SOURCE} = 100µA	2.4			V
Output Leakage (Open Drain)					1	µA
		EN_OUT1–EN_OUT8 = 13.2V			5	
OUT_ Overdrive (Charge Pump) (EN_OUT1–EN_OUT8 Only)		$I_{GATE\_}$ = 1µA	10	11	13	V
OUT_ Pullup Current (Charge Pump)	I_{CH_UP}	During power up, V_{GATE} = 1V	2.5	4		µA
SMBus INTERFACE						
Logic-Input Low Voltage	V_{IL}	Input voltage falling			0.8	V
Logic-Input High Voltage	V_{IH}	Input voltage rising	2.0			V
Input Leakage Current		IN = GND or V_{CC}	-1		+1	µA
Output Sink Current	V_{OL}	I_{SINK} = 3mA			0.4	V
Input Capacitance	C_{IN}			5		pF
SMBus Timeout	$t_{TIMEOUT}$	SCL time low for reset	25		35	ms
INPUTS (A0, GPIO_)						
Input Logic-Low	V_{IL}				0.8	V
Input Logic-High	V_{IH}		2.0			V
WDI Pulse Width	t_{WDI}		100			ns
$\overline{MR}$ Pulse Width	t_{MR}		1			µs
$\overline{MR}$ to RESET Delay				0.5		µs
$\overline{MR}$ Glitch Rejection				100		ns
SMBus TIMING						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at ABP = DBP = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Fall Time	t_{OF}	C_{BUS} = 10pF to 400pF			250	ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0.3		0.9	µs
Pulse Width of Spike Suppressed	t_{SP}			30		ns
JTAG INTERFACE						
TDI, TMS, TCK Logic-Low Input Voltage	V_{IL}	Input voltage falling			0.8	V
TDI, TMS, TCK Logic-High Input Voltage	V_{IH}	Input voltage rising	2			V
TDO Logic-Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
TDO Logic-Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	2.4			V
TDI, TMS Pullup Resistors	R_{PU}	Pullup to DBP	40	50	60	kΩ
I/O Capacitance	$C_{I/O}$			5		pF
TCK Clock Period	t_1				1000	ns
TCK High/Low Time	t_2, t_3		50	500		ns
TCK to TMS, TDI Setup Time	t_4		15			ns
TCK to TMS, TDI Hold Time	t_5		10			ns
TCK to TDO Delay	t_6				500	ns
TCK to TDO High-Z Delay	t_7				500	ns

Note 1: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 2: For V_{CC} of 3.6V or lower, connect V_{CC}, DBP, and ABP together. For higher supply applications, connect only V_{CC} to the supply rail.

Note 3: Applies to RESET, fault, autoretry, sequence delays, and watchdog timeout.

Note 4: Total unadjusted error is a combination of gain, offset, and quantization error.

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

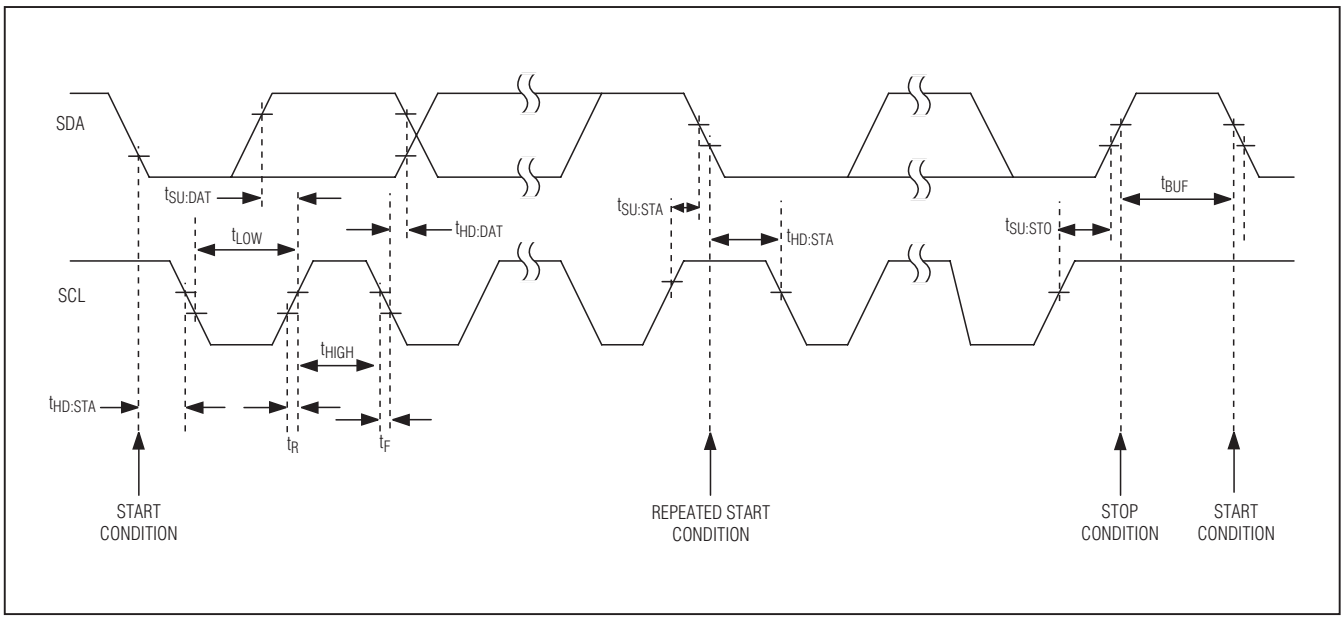


Figure 1. SMBus Timing Diagram

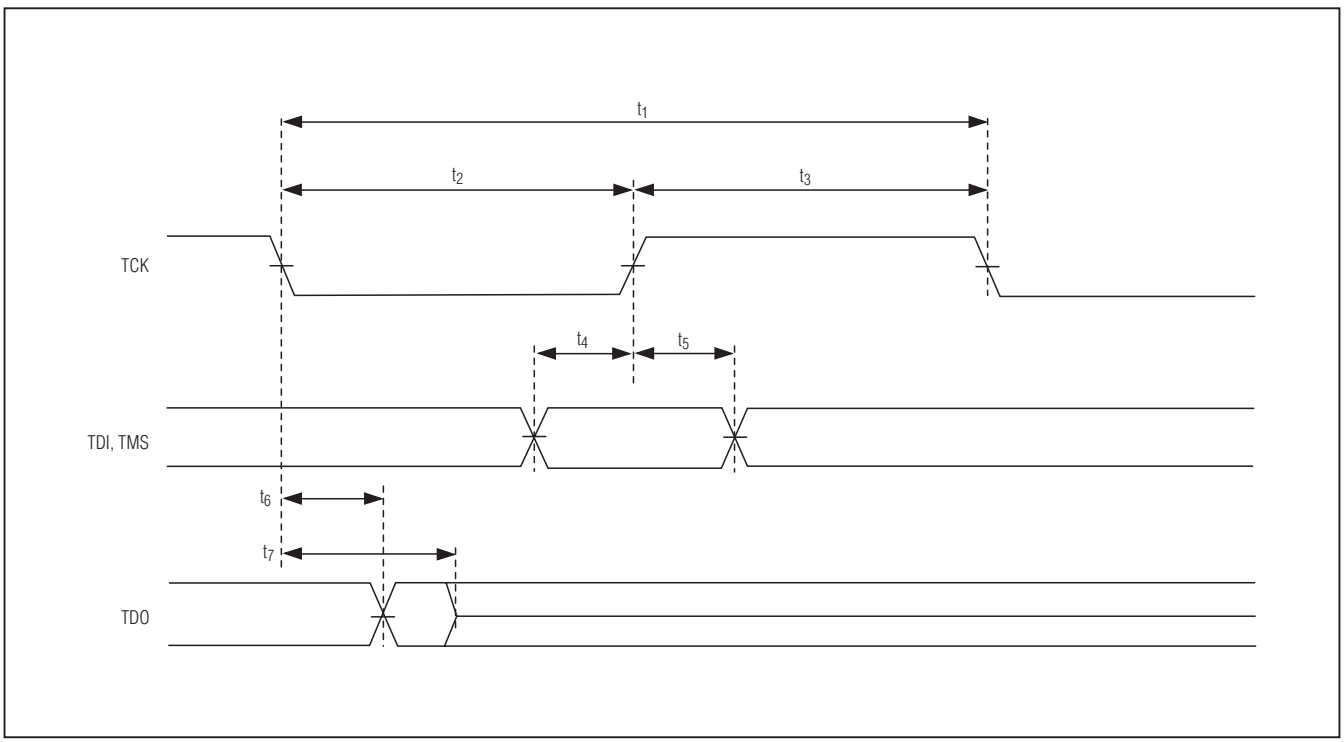


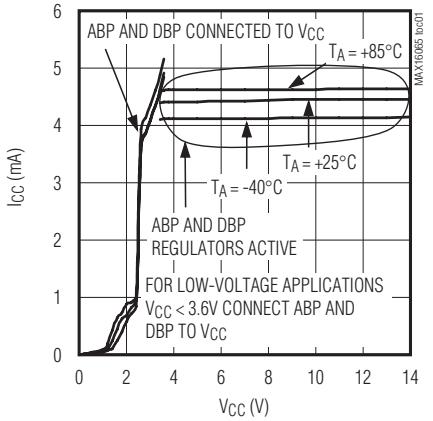
Figure 2. JTAG Timing Diagram

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

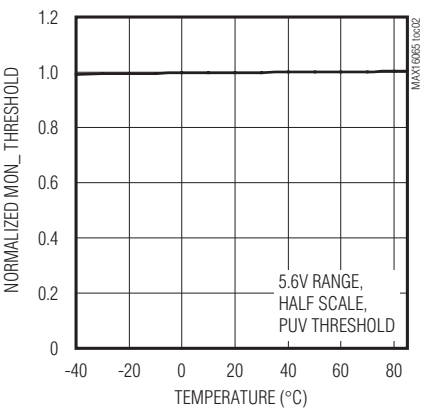
Typical Operating Characteristics

(Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

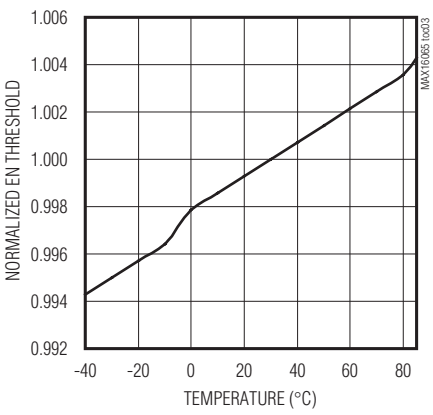
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



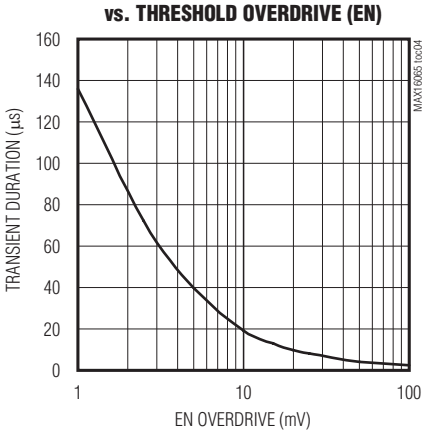
NORMALIZED MON_ THRESHOLD vs. TEMPERATURE



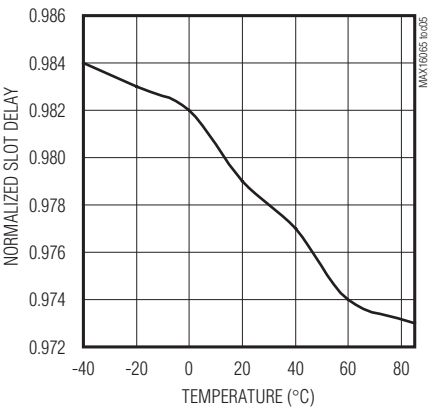
NORMALIZED EN THRESHOLD vs. TEMPERATURE



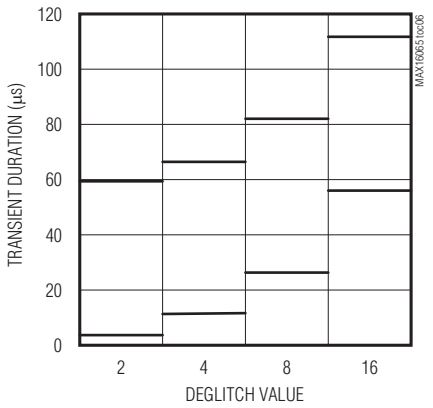
TRANSIENT DURATION vs. THRESHOLD OVERDRIVE (EN)



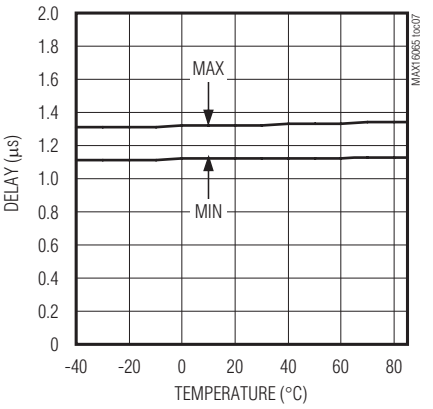
NORMALIZED TIMING ACCURACY vs. TEMPERATURE



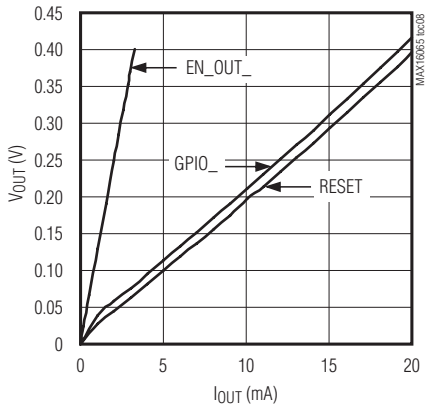
MON_ DEGLITCH vs. TRANSIENT DURATION



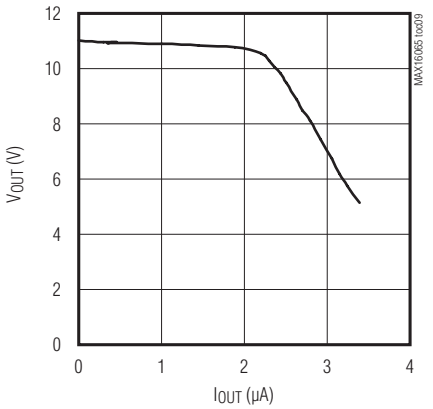
$\overline{MR}$ TO RESET PROPAGATION DELAY vs. TEMPERATURE



OUTPUT VOLTAGE vs. SINK CURRENT (OUT = LOW)



OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (CHARGE-PUMP OUTPUT)

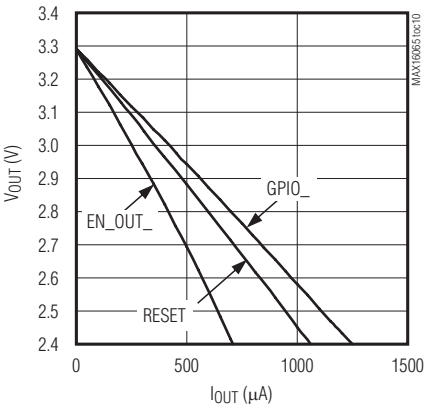


12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

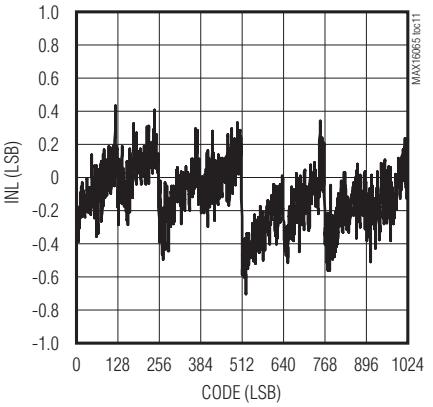
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

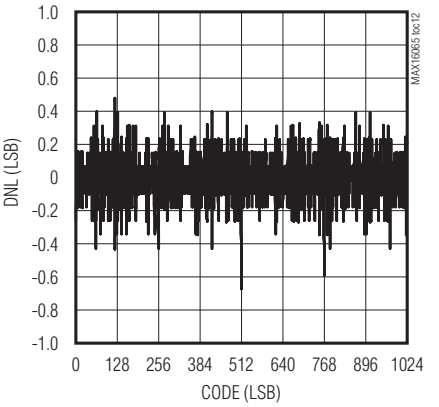
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



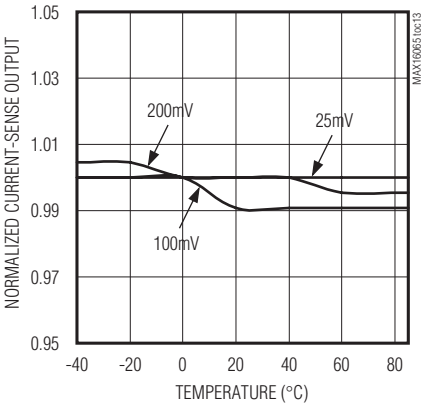
INTEGRAL NONLINEARITY vs. CODE



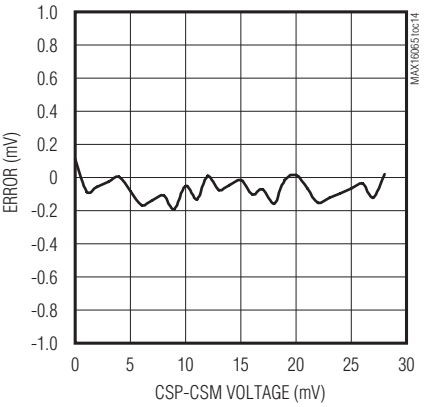
DIFFERENTIAL NONLINEARITY vs. CODE



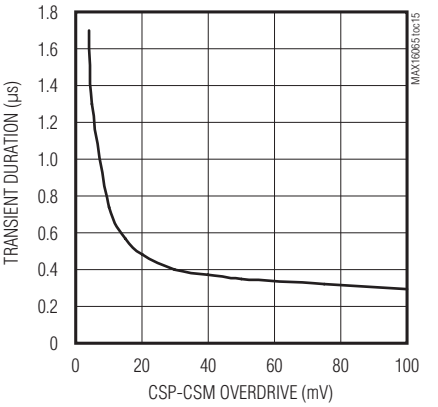
NORMALIZED CURRENT-SENSE ACCURACY vs. TEMPERATURE



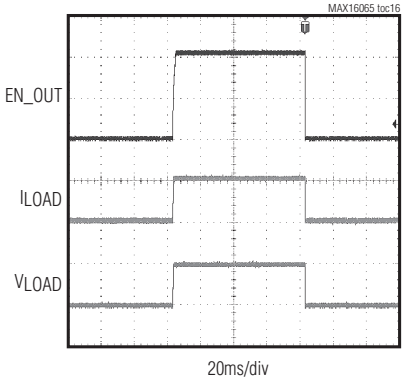
CURRENT-SENSE ACCURACY vs. CSP-CSM VOLTAGE



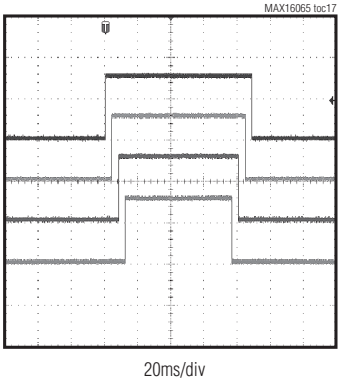
CURRENT-SENSE TRANSIENT DURATION vs. CSP-CSM OVERDRIVE



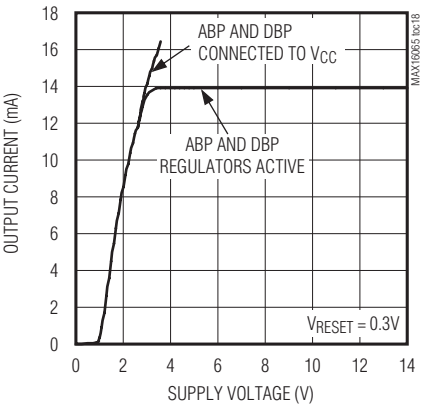
FET TURN-ON WITH CHARGE PUMP



SEQUENCING MODE



RESET OUTPUT CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN		NAME	FUNCTION
MAX16065	MAX16066		
1–6, 43–46	1–5, 36–40	MON1–MON10	Monitor Voltage Inputs. Set monitor voltage range through configuration registers. Measured value written to ADC register can be read back through the SMBus or JTAG interface.
47, 48	—	MON11, MON12	Monitor Voltage Inputs. Set monitor voltage range through configuration registers. Measured value written to ADC register can be read back through the SMBus or JTAG interface.
7	6	CSP	Current-Sense Amplifier Positive Input. Connect CSP to the source side of the external sense resistor.
8	7	CSM	Current-Sense Amplifier Negative Input. Connect CSM to the load side of the external sense resistor.
9	8	RESET	Configurable Reset Output
10	9	TMS	JTAG Test Mode Select
11	10	TDI	JTAG Test Data Input
12	11	TCK	JTAG Test Clock
13	12	TDO	JTAG Test Data Output
14	13	SDA	SMBus Serial-Data Open-Drain Input/Output
15	14	A0	Four-State SMBus Address. Address sampled upon POR.
16	15	SCL	SMBus Serial-Clock Input
17, 42	16, 35	GND	Ground
20–25	17–22	GPIO1–GPIO6	General-Purpose Input/Outputs. GPIO_s can be configured to act as a TTL input, a push-pull, open-drain, or high-impedance output or a pulldown circuit during a fault event.
18, 19	—	GPIO7, GPIO8	General-Purpose Input/Outputs. GPIO_s can be configured to act as a TTL input, a push-pull, open-drain, or high-impedance output or a pulldown circuit during a fault event or reverse sequencing.
26–29	—	EN_OUT12–EN_OUT9	Outputs. Set EN_OUT_ with active-high/active-low logic and with push-pull or open-drain configuration. EN_OUT_ can be asserted by a combination of IN_ voltages configurable through the flash.
30–37	23–30	EN_OUT1–EN_OUT8	Outputs. Set EN_OUT_ with active-high/active-low logic and with push-pull or open-drain configuration. EN_OUT_ can be asserted by a combination of IN_ voltages configurable through the flash. EN_OUT1–EN_OUT8 can be configured with a charge-pump output (+10V above GND) that can drive an external n-channel MOSFET.
38	31	EN	Analog Enable Input. All outputs deassert when V_{EN} is below the enable threshold.
39	32	DBP	Digital Bypass. All push-pull outputs are referenced to DBP. Bypass DBP with a 1µF capacitor to GND.
40	33	V_{CC}	Device Power Supply. Connect V_{CC} to a voltage from 2.8V to 14V. Bypass V_{CC} with a 10µF capacitor to GND.
41	34	ABP	Analog Bypass. Bypass ABP with a 1µF ceramic capacitor to GND.
—	—	EP	Exposed Pad. Internally connected to GND. Connect to ground, but do not use as the main ground connection.

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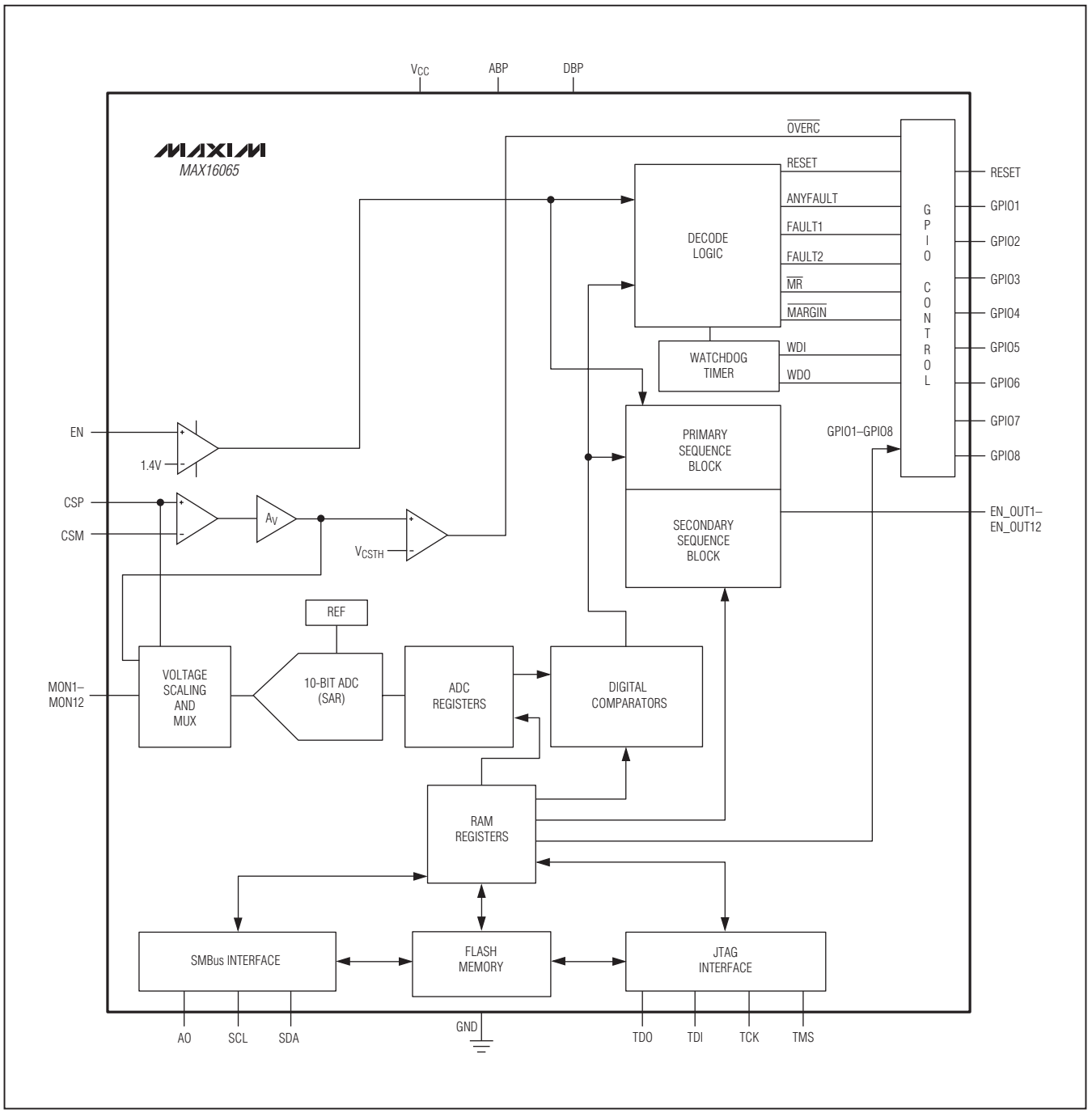
Functional Diagram



Detailed Description

The MAX16065 manages up to twelve system power supplies and the MAX16066 can manage up to eight system power supplies. After boot-up, if EN is high and the software enable bit is set to '1,' a power-up sequence begins based on the configuration stored in flash and the EN_OUT_s are controlled accordingly. When the power-up sequence is successfully completed, the monitoring phase begins. An internal multiplexer cycles through each MON_ input. At each multiplexer stop, the 10-bit ADC converts the monitored analog voltage to a digital result and stores the result in a register. Each time a conversion cycle (50µs, max) completes, internal logic circuitry compares the conversion results to the overvoltage and undervoltage thresholds stored in memory. When a result violates a programmed threshold, the conversion can be configured to generate a fault. GPIO_ can be programmed to assert on combinations of faults. Additionally, faults can be configured to shut off the system and trigger the nonvolatile fault logger, which writes all fault information automatically to the flash and write-protects the data to prevent accidental erasure.

The MAX16065/MAX16066 contain both SMBus and JTAG serial interfaces for accessing registers and flash. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *SMBus-Compatible Interface* and *JTAG Serial Interface* sections. The memory map is divided into three pages with access controlled by special SMBus and JTAG commands.

The factory-default values at POR (power-on reset) for all RAM registers are '0's. POR occurs when V_{CC} reaches the undervoltage-lockout threshold (UVLO) of 2.8V (max). At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and flash contents are copied to the respective register locations. During boot-up, the MAX16065/MAX16066 are not accessible through the serial interface. The boot-up sequence takes up to 150µs, after which the device is ready for normal operation. RESET is asserted low up to the boot-up phase and remains asserted for its programmed timeout period once sequencing is completed and all monitored channels are within their respective thresholds. Up to the boot-up phase, the GPIO_s and EN_OUT_s are high impedance.

Power

Apply 2.8V to 14V to V_{CC} to power the MAX16065/MAX16066. Bypass V_{CC} to ground with a 10µF capacitor. Two internal voltage regulators, ABP and DBP, supply power to the analog and digital circuitry within the device. For operation at 3.6V or lower, disable the regulators by connecting ABP and DBP to V_{CC}.

ABP is a 3.0V (typ) voltage regulator that powers the internal analog circuitry. Bypass ABP to GND with a 1µF ceramic capacitor installed as close to the device as possible.

DBP is an internal 3.0V (typ) voltage regulator. DBP powers flash and digital circuitry. All push-pull outputs refer to DBP. DBP supplies the input voltage to the internal charge pump when the programmable outputs are configured as charge-pump outputs. Bypass the DBP output to GND with a 1µF ceramic capacitor installed as close as possible to the device.

Do not power external circuitry from ABP or DBP.

Sequencing

To sequence a system of power supplies safely, the output voltage of a power supply must be good before the next power supply may turn on. Connect EN_OUT_ outputs to the enable input of an external power supply and connect MON_ inputs to the output of the power supply for voltage monitoring. More than one MON_ can be used if the power supply has multiple outputs.

Sequence Order

The MAX16065/MAX16066 provide a system of ordered slots to sequence multiple power supplies. To determine the sequence order, assign each EN_OUT_ to a slot ranging from Slot 1 to Slot 12. EN_OUT_(s) assigned to Slot 1 are turned on first, followed by outputs assigned to Slot 2, and so on through Slot 12. Multiple EN_OUT_s assigned to the same slot turn on at the same time.

Each slot includes a built-in configurable sequence delay (registers r77h to r7Dh) ranging from 20µs to 1.6s. During a reverse sequence, slots are turned off in reverse order starting from Slot 12. The MAX16065/MAX16066 can be configured to power-down in simultaneous mode or in reverse sequence mode as set in r75h[0]. See Tables 5 and 6 for the EN_OUT_ slot assignment bits, and Tables 3 and 4 for the sequence delays.

During power-up or power-down sequencing, the current sequencer state can be found in r21h[4:0].

Table 1. Current Sequencer Slot

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
21h	[4:0]	Current Sequencer State: 00000 = Slot 0 00001 = Slot 1 00010 = Slot 2 00011 = Slot 3 00100 = Slot 4 00101 = Slot 5 00110 = Slot 6 00111 = Slot 7 01000 = Slot 8 01001 = Slot 9 01010 = Slot 10 01011 = Slot 11 01100 = Slot 12 01101 = Secondary sequence monitoring mode 01110 = Primary sequence fault 01111 = Primary sequence monitoring mode 10000 = Secondary sequence fault 10001 to 11111 = Reserved
	[7:5]	Reserved

Multiple Sequencing Groups

The MAX16065/MAX16066 sequencing slots can be split into two groups: the primary sequence and the secondary sequence. The last slot of the primary sequence is selected using register bits r7Dh[7:4]. The secondary sequence begins at the slot after the one specified in register bits 7Dh[7:4]. The primary sequence is controlled by the EN input and the software enable bit in r73h[0]. Outputs assigned to slots in the primary sequence turn on, and monitoring begins for inputs assigned to these slots. RESET deasserts after the primary sequence and timeout period completes.

To initiate secondary sequencing and monitoring, set the software enable 73h[1] bit to 1. Additionally, if GPIO_ is configured as EN2 then both the software enable 2 and EN2 must be high. Outputs assigned to slots in the secondary sequence turn on, and monitoring begins for inputs assigned to these slots. If a GPIO_ is configured as the RESET2 output, it deasserts after the secondary sequence and timeout period completes.

If a critical fault occurs in the primary sequence group, both sequence groups automatically shut down. If a critical fault occurs in the secondary sequence group, then just the outputs assigned to slots in the secondary sequence turn off. The failing slot in secondary sequence is stored in r1Dh.

Multiple sequencing groups can be used to conserve power by powering down secondary systems when not in use.

Enable and Enable2

To initiate sequencing/tracking and enable monitoring, the voltage at EN must be above 1.4V and the software enable bit in r73h[0] must be set to '1.' To power down and disable monitoring, either pull EN below 1.35V or set the Software Enable bit to '0.' See Table 2 for the software enable bit configurations. Connect EN to ABP if not used.

If a fault condition occurs during the power-up cycle, the EN_OUT_ outputs are powered down immediately, regardless of the state of EN. In the monitoring state, if EN falls below the threshold, the sequencing state machine begins the power-down sequence. If EN rises above the threshold during the power-down sequence, the sequence state machine continues the power-down sequence until all the channels are powered off and then the device immediately begins the power-up sequence. When in the monitoring state, a register bit, ENRESET, is set to a '1' when EN falls below the undervoltage threshold. This register bit latches and must be cleared through software. This bit indicates if RESET asserted low due to EN going under the threshold. The POR state of ENRESET is '0'. The bit is only set on a falling edge

of the EN comparator output or the software enable bit. If operating in latch-on fault mode, toggle EN or toggle the Software Enable bit to clear the latch condition and restart the device once the fault condition has been removed.

To initiate secondary sequencing and monitoring set the software enable r73h[1] bit to 1. Additionally, if GPIO_ is configured as EN2 then both the software enable 2 bit and EN2 must be high. To power-down and disable monitoring, either drive EN2 low or set the Software Enable2 bit to '0.' See Table 2 for the software enable bit configurations.

When a fault condition occurs during the power-up cycle, the EN_OUT_ outputs are powered down immediately, independent of the state of EN2. Drive EN2 low to begin the secondary power-down sequence. When EN2 is driven high during the power-down sequence, the sequence state machine continues the power-down sequence until the secondary channels are powered off and then the device immediately begins the power-up sequence.

Monitoring Inputs While Sequencing

An enabled MON_ input can be assigned to a slot ranging from Slot 1 to Slot 12. EN_OUT_s are always asserted at the beginning of a slot. The supply voltages connected to the MON_ inputs must exceed the undervoltage threshold before the programmed timeout period expires otherwise a fault condition will occur. The undervoltage threshold checking cannot be disabled during power-up and power-down. See Tables 5 and 6 for the MON_ slot assignment bits. The programmed

Table 2. Software Enable Configurations

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[0]	Software enable 1 (primary sequence)
		[1]	Software enable 2 (secondary sequence)
		[2]	1 = Margin mode enabled
		[3]	Early warning threshold select 0 = Early warning is undervoltage 1 = Early warning is overvoltage
		[4]	Independent watchdog mode enable 1 = Watchdog timer is independent of sequencer 0 = Watchdog timer boots after sequence completes

Table 3. Slot Delay Register

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
77h	277h	[3:0]	Sequence Slot 0 Delay
		[7:4]	Sequence Slot 1 Delay
78h	278h	[3:0]	Sequence Slot 2 Delay
		[7:4]	Sequence Slot 3 Delay
79h	279h	[3:0]	Sequence Slot 4 Delay
		[7:4]	Sequence Slot 5 Delay
7Ah	27Ah	[3:0]	Sequence Slot 6 Delay
		[7:4]	Sequence Slot 7 Delay
7Bh	27Bh	[3:0]	Sequence Slot 8 Delay
		[7:4]	Sequence Slot 9 Delay
7Ch	27Ch	[3:0]	Sequence Slot 10 Delay
		[7:4]	Sequence Slot 11 Delay
7Dh	27Dh	[3:0]	Sequence Slot 12 Delay
		[7:4]	Grouped Sequence Split Location, Final Slot of Primary Sequence

Table 4. Power-Up/Power-Down Slot Delays

CODE	VALUE
0000	25µs
0001	500µs
0010	1ms
0011	2ms
0100	3ms
0101	4ms
0110	6ms
0111	8ms
1000	10ms
1001	12ms
1010	25ms
1011	100ms
1100	200ms
1101	400ms
1110	800ms
1111	1.6s

sequence delay is then counted before moving to the next slot.

Slot 0 does not monitor any MON_ input and does not control any EN_OUT_. Slot 0 waits for the Software Enable bit r73h[0] to be a logic-high and for the voltage on EN to rise above 1.4V before initiating the power-up sequence and counting its own sequence delay.

Any MON_ input that suffers a fault that occurs during power-up sequencing causes all the EN_OUT_s to turn off and the sequencer to shut down regardless of the state of the critical fault enables (see the *Faults* section for more information). If a MON_ input is less critical to system operation, it can be configured as "monitoring only" (see Table 6) for either the primary or secondary sequence. Monitoring for MON_ inputs assigned as "monitoring only" begins after sequencing is complete for that group, and can trigger a critical fault only if specifically configured to do so using the critical fault enables.

Power-Up

On power-up, when EN is high and the Software Enable bit is 1, the MAX16065/MAX16066 begin sequencing with Slot 0. After the sequencing delay for Slot 0 expires, the sequencer advances to Slot 1, and all EN_OUT_s assigned to the slot assert. All MON_ inputs assigned to Slot 1 are monitored and when the voltage rises above the UV fault threshold, the sequence delay counter is started.

When the t_{FAULT} counter expires before all MON_ inputs assigned to the slot are above the fault UV threshold, a fault asserts. EN_OUT_ outputs are disabled and the MAX16065/MAX16066 return to the power-off state. When the sequence delay expires, the MAX16065/MAX16066 proceed to the next slot.

After the voltages on all MON_ inputs assigned to the last slot exceed the UV fault threshold and the slot delay expires, the MAX16065/MAX16066 start the reset timeout counter. After the reset timeout, RESET deasserts. r75h[4:1] sets the t_{FAULT} delay. See Table 7 for details.

Power-Down

Power-down starts when EN is pulled low or the Software Enable bit is set to '0.' Power down EN_OUT_s simultaneously or in reverse-sequence mode by setting the Reverse Sequence bit (r75h[0]) appropriately.

Reverse-Sequence Mode

When the MAX16065/MAX16066 are fully powered up (including secondary sequence group, if enabled) and EN or the Software Enable bit is set to '0', the EN_OUT_s assigned to Slot 12 deassert, the MAX16065/MAX16066 wait for the Slot 12 sequence delay and then proceed to the previous slot (Slot 11), and so on until the EN_OUT_s assigned to Slot 1 turn off. When simultaneous power-down is selected (r75h[0] set to '0'), all EN_OUT_s turn off at the same time.

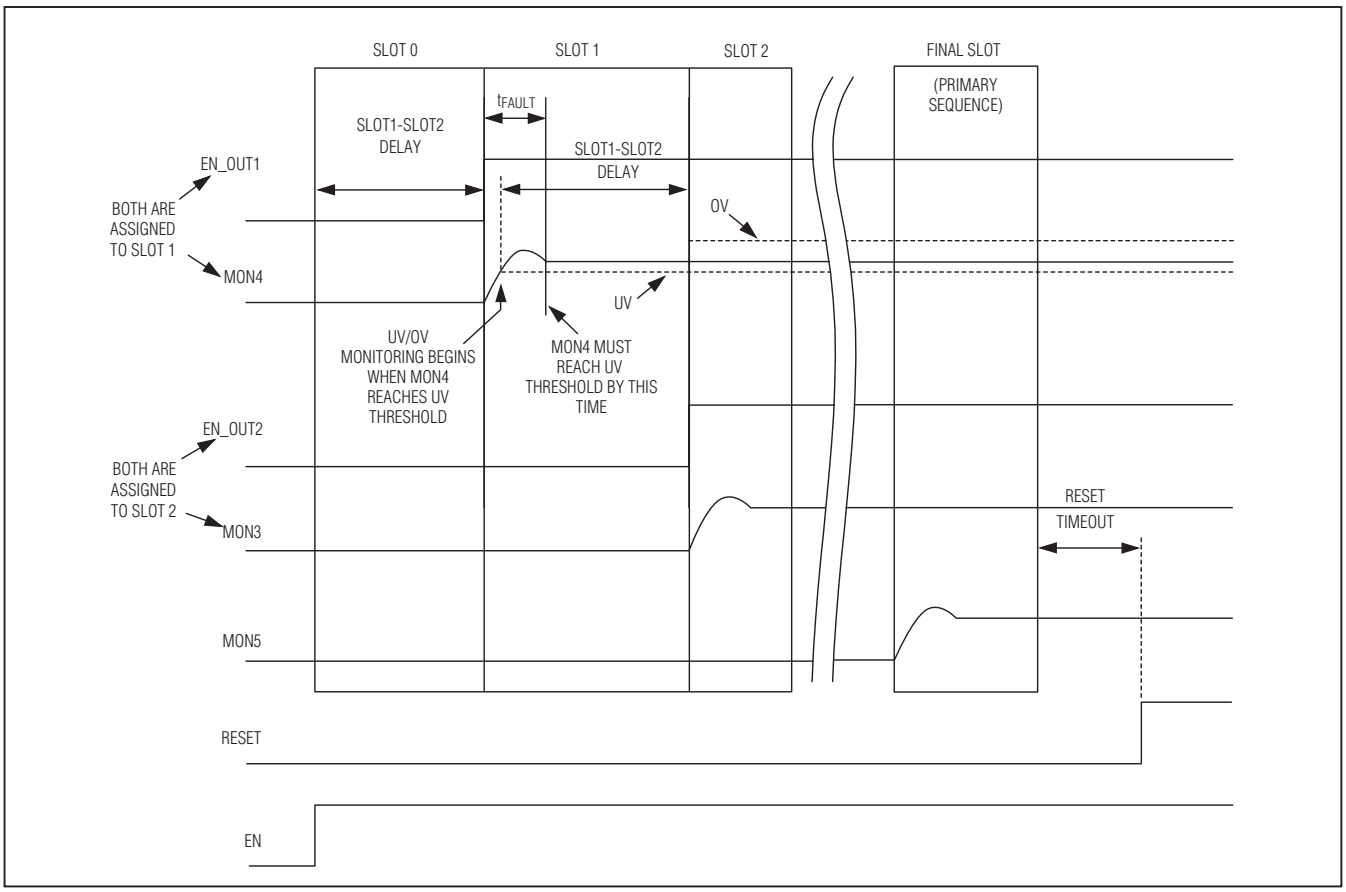


Figure 3. Delay and Reset Timing

Table 5. MON_ and EN_OUT_ Assignment Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
7Eh	27Eh	[3:0]	MON1
		[7:4]	MON2
7Fh	27Fh	[3:0]	MON3
		[7:4]	MON4
80h	280h	[3:0]	MON5
		[7:4]	MON6
81h	281h	[3:0]	MON7
		[7:4]	MON8
82h	282h	[3:0]	MON9
		[7:4]	MON10
83h	283h	[3:0]	MON11
		[7:4]	MON12

Table 5. MON_ and EN_OUT_ Assignment Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
84h	284h	[3:0]	EN_OUT1
		[7:4]	EN_OUT2
85h	285h	[3:0]	EN_OUT3
		[7:4]	EN_OUT4
86h	286h	[3:0]	EN_OUT5
		[7:4]	EN_OUT6
87h	287h	[3:0]	EN_OUT7
		[7:4]	EN_OUT8
88h	288h	[3:0]	EN_OUT9
		[7:4]	EN_OUT10
89h	289h	[3:0]	EN_OUT11
		[7:4]	EN_OUT12

Table 6. MON_ and EN_OUT_ Slot Assignment Codes

SLOT ASSIGNMENT		
CODE	MON_ DESCRIPTION	OUT_ DESCRIPTION
0000	Not assigned	Not assigned
0001	Slot 1	Slot 1
0010	Slot 2	Slot 2
0011	Slot 3	Slot 3
0100	Slot 4	Slot 4
0101	Slot 5	Slot 5
0110	Slot 6	Slot 6
0111	Slot 7	Slot 7
1000	Slot 8	Slot 8
1001	Slot 9	Slot 9
1010	Slot 10	Slot 10
1011	Slot 11	Slot 11
1100	Slot 12	Slot 12
1101	Monitoring only, primary sequence	General-purpose input (EN_OUT9–EN_OUT12 only)
1110	Monitoring only, secondary sequence	General-purpose output (EN_OUT9–EN_OUT12 only)
1111	Not assigned	Not assigned

Table 7. t_{FAULT} Delay Settings

CODE	DELAY
0000	120µs
0001	150µs
0010	250µs
0011	380µs
0100	600µs
0101	1ms
0110	1.5ms
0111	2.5ms
1000	4ms
1001	6ms
1010	10ms
1011	15ms
1100	25ms
1101	40ms
1110	60ms
1111	100ms

When the secondary sequence group is already powered down and EN or the Software Enable bit is set to '0', the reverse power-down sequence is similar to above, but starts from the last slot assigned to the primary sequence r7Dh[7:4]. After the last assigned slot is powered down the previous slot will power down and so on until Slot 0 is powered down.

To power down the secondary sequence group, drive EN2 low or set r75h[1] to '0'. The secondary reverse power-down sequence will start at Slot 12 and end at the primary sequence monitoring mode state at which point only the slots assigned to the primary sequence are active.

Voltage/Current Monitoring

The MAX16065/MAX16066 feature an internal 10-bit ADC that monitors the MON_ voltage inputs. An internal multiplexer cycles through each of the enabled inputs, taking less than 40µs for a complete monitoring cycle. Each acquisition takes approximately 3.2µs. At each multiplexer stop, the 10-bit ADC converts the analog input to a digital result and stores the result in a register. ADC conversion results are stored in registers r00h to r1Ah (see Table 10). Use the SMBus or JTAG serial interface to read ADC conversion results.

The MAX16065 provides twelve inputs, MON1–MON12, for voltage monitoring. The MAX16066 provides eight inputs, MON1–MON8, for voltage monitoring. Each input voltage range is programmable in registers r43h to r45h (see Table 9). When MON_ configuration registers are set to '11,' MON_ voltages are not monitored, and the multiplexer does not stop at these inputs, decreasing the total cycle time. These inputs cannot be configured to trigger fault conditions.

The three programmable thresholds for each monitored voltage include an overvoltage, an undervoltage, and a secondary warning threshold that can be set in r73h[3] to be either an undervoltage or overvoltage threshold. See the *Faults* section for more information on setting overvoltage and undervoltage thresholds. All voltage thresholds are 8 bits wide. The 8 MSBs of the 10-bit ADC conversion result are compared to these overvoltage and undervoltage thresholds.

For any undervoltage or overvoltage condition to be monitored and any faults detected, the MON_ input must be assigned to a sequence order or set to monitoring mode as described in the *Sequencing* section.

Inputs that are not enabled are not converted by the ADC; they contain the last value acquired before that channel was disabled.

The ADC conversion result registers are reset to 00h at boot-up. These registers are not reset when a reboot command is executed.

Configure the MAX16065/MAX16066 for differential mode in r46h (Table 9). The possible differential pairs

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are MON1/MON2, MON3/MON4, MON5/MON6, MON7/MON8, MON9/MON10, MON11/MON12 with the first input always being at a higher voltage than the second. Use differential voltage sensing to eliminate voltage offsets or measure supply current. See Figure 4. In differential mode, the odd-numbered MON_ input measures the absolute voltage with respect to GND while the result of the even input is the difference between the odd and even inputs. See Figure 4 for the typical differential measurement circuit.

Internal Current-Sense Amplifier

The current-sense inputs, CSP/CSM, and a current-sense amplifier facilitate power monitoring (see Figure 5). The voltage on CSP relative to GND is also monitored by the ADC when the current-sense amplifier is enabled with r47h[0]. The conversion results are located in registers r19h and r1Ah (see Table 10). There are two selectable voltage ranges for CSP set by r47h[1], see Table 8. Although the voltage can be monitored over SMBus or JTAG, this voltage has no threshold comparators and cannot trigger any faults. Regarding the current-sense amplifier, there are four selectable ranges and the ADC output for a current-sense conversion is:

$$X_{ADC} = (V_{SENSE} \times A_V)/1.4V \times (2^8 - 1)$$

where X_{ADC} is the 8-bit decimal ADC result in register r18h, V_{SENSE} is V_{CSP} - V_{CSM}, and A_V is the current-sense voltage gain set by r47h[3:2].

In addition, there are two programmable current-sense trip thresholds: primary overcurrent and secondary overcurrent. For fast fault detection, the primary overcurrent threshold is implemented with an analog comparator connected to the internal $\overline{OVERC}$ signal. The $\overline{OVERC}$ signal can be output on one of the GPIO_s. See the *General-Purpose Inputs/Outputs* section for configuring the GPIO_ to output the $\overline{OVERC}$ signal. The primary threshold is set by:

$$I_{TH} = V_{CSTH}/R_{SENSE}$$

where I_{TH} is the current threshold to be set, V_{CSTH} is the threshold set by r47h[3:2], and R_{SENSE} is the value of the sense resistor. See Table 8 for a description of r47h. $\overline{OVERC}$ depends only on the primary overcurrent threshold. The secondary overcurrent threshold is implemented through ADC conversions and digital comparison set by r6Ch. The secondary overcurrent threshold includes programmable time delay options located in r73h[6:5]. Primary and secondary current-sense faults are enabled/disabled through r47h[0].

General-Purpose Inputs/Outputs

GPIO1–GPIO8 are programmable general-purpose inputs/outputs. GPIO1–GPIO8 are configurable as a manual reset input, a watchdog timer input and output, logic inputs/outputs, fault-dependent outputs. When programmed as outputs, GPIO_s are open drain or push-pull. See Tables 12 and 13 for more detailed information on configuring GPIO1–GPIO8.

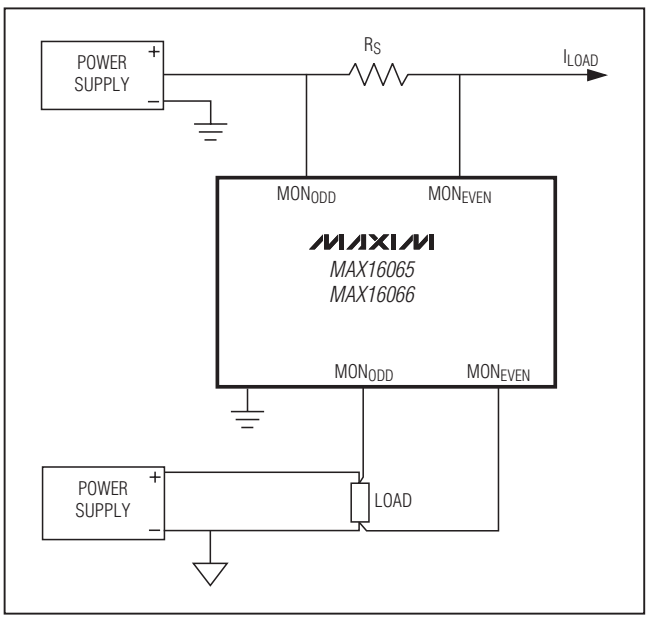

Figure 4. Differential Measurement Connections

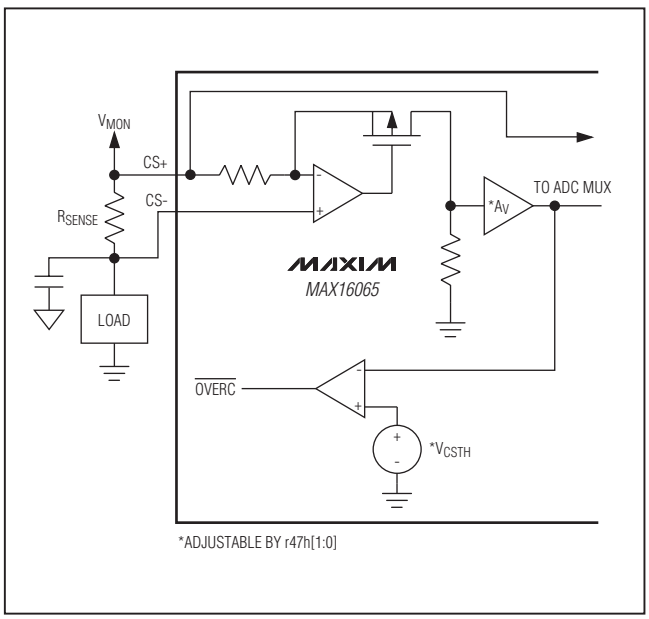

Figure 5. Current-Sense Amplifier

Table 8. Overcurrent Primary Threshold and Current-Sense Control

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
47h	247h	[0]	1 = Current sense is enabled 0 = Current sense is disabled
		[1]	1 = CSP full-scale range is 14V 0 = CSP full-scale range is 7V
		[3:2]	Overcurrent Primary Threshold and Current-Sense Gain Setting: 00 = 200mV threshold, A_V = 6V/V 01 = 100mV threshold, A_V = 12V/V 10 = 50mV threshold, A_V = 24V/V 11 = 25mV threshold, A_V = 48V/V
73h	273h	[6:5]	Overcurrent Secondary Threshold Deglitch: 00 = No delay 01 = 4ms 10 = 15ms 11 = 60ms

Table 9. ADC Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
43h	243h	[1:0]	ADC1 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC2 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC3 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC4 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted

Table 9. ADC Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
44h	244h	[1:0]	ADC5 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC6 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC7 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC8 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
45h	245h	[1:0]	ADC9 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC10 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC11 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC12 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted

Table 9. ADC Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
46h	246h	[0]	Differential Conversion ADC1–ADC2: 0 = Disabled 1 = Enabled
		[1]	Differential Conversion ADC3–ADC4: 0 = Disabled 1 = Enabled
		[2]	Differential Conversion ADC5–ADC6: 0 = Disabled 1 = Enabled
		[3]	Differential Conversion ADC7–ADC8: 0 = Disabled 1 = Enabled
		[4]	Differential Conversion ADC9–ADC10: 0 = Disabled 1 = Enabled
		[5]	Differential Conversion ADC11–ADC12: 0 = Disabled 1 = Enabled

Table 10. ADC Conversion Results (Read Only)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	ADC1 result (MSB) bits 9–2
01h	[7:6]	ADC1 result (LSB) bits 1–0
02h	[7:0]	ADC2 result (MSB) bits 9–2
03h	[7:6]	ADC2 result (LSB) bits 1–0
04h	[7:0]	ADC3 result (MSB) bits 9–2
05h	[7:6]	ADC3 result (LSB) bits 1–0
06h	[7:0]	ADC4 result (MSB) bits 9–2
07h	[7:6]	ADC4 result (LSB) bits 1–0
08h	[7:0]	ADC5 result (MSB) bits 9–2
09h	[7:6]	ADC5 result (LSB) bits 1–0
0Ah	[7:0]	ADC6 result (MSB) bits 9–2
0Bh	[7:6]	ADC6 result (LSB) bits 1–0
0Ch	[7:0]	ADC7 result (MSB) bits 9–2
0Dh	[7:6]	ADC7 result (LSB) bits 1–0
0Eh	[7:0]	ADC8 result (MSB) bits 9–2
0Fh	[7:6]	ADC8 result (LSB) bits 1–0
10h	[7:0]	ADC9 result (MSB) bits 9–2
11h	[7:6]	ADC9 result (LSB) bits 1–0
12h	[7:0]	ADC10 result (MSB) bits 9–2
13h	[7:6]	ADC10 result (LSB) bits 1–0
14h	[7:0]	ADC11 result (MSB) bits 9–2
15h	[7:6]	ADC11 result (LSB) bits 1–0
16h	[7:0]	ADC12 result (MSB) bits 9–2
17h	[7:6]	ADC12 result (LSB) bits 1–0
18h	[7:0]	Current-sense ADC result
19h	[7:0]	CSP ADC output (MSB) bits 9–2
1Ah	[7:6]	CSP ADC output (LSB) bits 1–0

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When GPIO1–GPIO8 are configured as general-purpose inputs/outputs, read values from the GPIO_ ports through r1Eh and write values to GPIO_s through r3Eh. Note that r3Eh has a corresponding flash register, which programs the default state of a general-purpose output. See Table 11 for more information on reading and writing to the GPIO_.

Fault1 and Fault2

GPIO1–GPIO8 are configurable as dedicated fault outputs, Fault1 or Fault2. Fault outputs can assert on one or more overvoltage, undervoltage, or early warning conditions for selected inputs, as well as the secondary overcurrent comparator. Fault1 and Fault2 dependencies are set using registers r36h to r3Ah. See Table 14. When a fault output depends on more than one MON_, the fault output asserts when one or more MON_ exceeds a programmed threshold voltage. These fault outputs act independently of the critical fault system, described in the *Critical Faults* section.

Table 11. GPIO_ State Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
1Eh	—	[0]	GPIO1 input state
		[1]	GPIO2 input state
		[2]	GPIO3 input state
		[3]	GPIO4 input state
		[4]	GPIO5 input state
		[5]	GPIO6 input state
		[6]	GPIO7 input state
		[7]	GPIO8 input state
3Eh	23Eh	[0]	GPIO1 output state
		[1]	GPIO2 output state
		[2]	GPIO3 output state
		[3]	GPIO4 output state
		[4]	GPIO5 output state
		[5]	GPIO6 output state
		[6]	GPIO7 output state
		[7]	GPIO8 output state

Table 12. GPIO_ Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
3Fh	23Fh	[2:0]	GPIO1 configuration
		[5:3]	GPIO2 configuration
		[7:6]	GPIO3 configuration (LSB)
40h	240h	[0]	GPIO3 configuration (MSB)
		[3:1]	GPIO4 configuration
		[6:4]	GPIO5 configuration
		[7]	GPIO6 configuration (LSB)

Table 12. GPIO_ Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
41h	241h	[1:0]	GPIO6 configuration (MSB)
		[4:2]	GPIO7 configuration
		[7:5]	GPIO8 configuration
42h	242h	[0]	Output Configuration for GPIO1: 0 = Push-pull 1 = Open drain
		[1]	Output Configuration for GPIO2: 0 = Push-pull 1 = Open drain
		[2]	Output Configuration for GPIO3: 0 = Push-pull 1 = Open drain
		[3]	Output Configuration for GPIO4: 0 = Push-pull 1 = Open drain
		[4]	Output Configuration for GPIO5: 0 = Push-pull 1 = Open drain
		[5]	Output Configuration for GPIO6: 0 = Push-pull 1 = Open drain
		[6]	Output Configuration for GPIO7: 0 = Push-pull 1 = Open drain
		[7]	Output Configuration for GPIO8: 0 = Push-pull 1 = Open drain

Table 13. GPIO_ Function Configuration Bits

	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7	GPIO8
000	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input
001	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output
010	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output
011	Fault1 output	Fault1 output	$\overline{\text{FAULTPU}}$ output	Fault1 output	Fault1 output	Fault1 output	Fault1 output	FAULTP output
100	$\overline{\text{ANY\_FAULT}}$ output	RESET2 output	$\overline{\text{ANY\_FAULT}}$ output	$\overline{\text{ANY\_FAULT}}$ output	$\overline{\text{ANY\_FAULT}}$ output	RESET2 output	$\overline{\text{ANY\_FAULT}}$ output	RESET2 output
101	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output
110	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output
111	WDI input	—	—	$\overline{\text{EXTFAULT}}$ input/output	$\overline{\text{EN2}}$ input	$\overline{\text{MARGIN}}$ input	EN2 input	$\overline{\text{EXTFAULT}}$ input/output

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$\overline{\text{ANY\_FAULT}}$

GPIO1, GPIO3, GPIO4, GPIO5, and GPIO7 are configurable to assert low during any fault condition. This includes power-up, power-down fault conditions as well as conditions where Fault1 or Fault2 assert.

Second Enable (EN2)

GPIO5 and GPIO7 are configurable as the enable input for the secondary sequence. See the *Multiple Sequencing Groups* section for more details.

Table 14. Fault1 and Fault2 Dependencies

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
36h	236h	0	1 = Fault1 depends on MON1
		1	1 = Fault1 depends on MON2
		2	1 = Fault1 depends on MON3
		3	1 = Fault1 depends on MON4
		4	1 = Fault1 depends on MON5
		5	1 = Fault1 depends on MON6
		6	1 = Fault1 depends on MON7
		7	1 = Fault1 depends on MON8
37h	237h	0	1 = Fault1 depends on MON9
		1	1 = Fault1 depends on MON10
		2	1 = Fault1 depends on MON11
		3	1 = Fault1 depends on MON12
		4	1 = Fault1 depends on the overvoltage thresholds of the inputs selected by r36h and r37h[3:0]
		5	1 = Fault1 depends on the undervoltage thresholds of the inputs selected by r36h and r37h[3:0]
		6	1 = Fault1 depends on the early warning thresholds of the inputs selected by r36h and r37h[3:0]
		7	0 = Fault1 is an active-low digital output 1 = Fault1 is an active-high digital output
38h	238h	[0]	1 = Fault2 depends on MON1
		[1]	1 = Fault2 depends on MON2
		[2]	1 = Fault2 depends on MON3
		[3]	1 = Fault2 depends on MON4
		[4]	1 = Fault2 depends on MON5
		[5]	1 = Fault2 depends on MON6
		[6]	1 = Fault2 depends on MON7
		[7]	1 = Fault2 depends on MON8

Table 14. Fault1 and Fault2 Dependencies (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
39h	239h	[0]	1 = Fault2 depends on MON9
		[1]	1 = Fault2 depends on MON10
		[2]	1 = Fault2 depends on MON11
		[3]	1 = Fault2 depends on MON12
		[4]	1 = Fault2 depends on the overvoltage thresholds of the inputs selected by r38h and r39h[3:0]
		[5]	1 = Fault2 depends on the undervoltage thresholds of the inputs selected by r38h and r39h[3:0]
		[6]	1 = Fault2 depends on the early warning thresholds of the inputs selected by r38h and r39h[3:0]
		[7]	0 = Fault2 is an active-low digital output 1 = Fault2 is an active-high digital output
3Ah	23Ah	[0]	1 = Fault1 depends on secondary overcurrent comparator
		[1]	1 = Fault2 depends on secondary overcurrent comparator
		[7:2]	Reserved

Overcurrent Comparator ($\overline{OVERC}$)

GPIO1 to GPIO8 are configurable to assert low when the voltage across CSP and CSM exceed the primary overcurrent threshold. See the *Internal Current-Sense Amplifier* section for more details.

Fault-On Power-Up ($\overline{FAULTPU}$)

GPIO3 and GPIO8 are configurable to indicate a fault during power-up or power-down on the secondary sequence. This output asserts low when a MON_ input exceeds the overvoltage or undervoltage threshold. The sequencer will still enter the fault state and turn off all the EN_OUT_ outputs assigned to the secondary sequence.

Manual Reset ($\overline{MR}$)

GPIO1, GPIO3, GPIO5, and GPIO7 are configurable to act as an active-low manual reset input, $\overline{MR}$. Drive $\overline{MR}$ low to assert RESET. RESET remains asserted for the selected reset timeout period after $\overline{MR}$ transitions from low to high. See the *RESET2 Output* section for more information on selecting a reset timeout period.

RESET2 Output

GPIO2, GPIO6, and GPIO8 are configurable to act as a reset indicator related to the secondary sequence. RESET2 asserts during power-up/power-down and deasserts following the reset timeout period once the power-up of the secondary sequence is complete. The secondary power-up sequence is completed when any MON_ inputs assigned to Slot 12 exceed the undervoltage thresholds and Slot 12 sequence delay expires. When no MON_ inputs are assigned to Slot 12, the power-up sequence is complete after the slot sequence delay expires. RESET2 shares configuration bits with RESET with the exception of polarity (active-high or active-low) and output type (push-pull or open drain), see Table 23.

During normal monitoring, RESET2 can be configured to assert when any combination of MON_ inputs violates configurable combinations of thresholds: undervoltage, overvoltage, or early warning. Select the combination of thresholds using r3Bh[1:0], and select the combination of MON_ inputs using 3Ch[7:1] and 3Dh[4:0]. Note that MON_ inputs in the secondary sequence configured as critical faults will always cause RESET2 to assert regardless of these configuration bits.

RESET2 can be configured as push-pull or open drain using the appropriate GPIO_ configuration bit in r42h (see Table 12), and is always active-low. Select the reset timeout for RESET and RESET2 by loading a value from Table 5 into r3Bh[7:4]. RESET and RESET2 can be forced to assert by writing a '1' into r3Ch[0]. RESET2 remains asserted for the reset timeout period after a '0' is written into r3Ch[0].

Watchdog Input (WDI) and Output ($\overline{WDO}$)

GPIO2, GPIO4, GPIO6, and GPIO8 are configurable as the watchdog timer output, $\overline{WDO}$. GPIO1 is configurable as WDI. See Table 24 for configuration details. $\overline{WDO}$ is an active-low output. See the *Watchdog Timer* section for more information about the operation of the watchdog timer.

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External Fault ($\overline{\text{EXTFAULT}}$)

GPIO4 and GPIO8 are configurable as the external fault input/output. When configured as push-pull, $\overline{\text{EXTFAULT}}$ signals that a critical fault has occurred on one or more monitored voltages or current. When configured as open-drain, $\overline{\text{EXTFAULT}}$ can be asserted low by an external circuit to trigger a critical fault. This signal can be used to cascade multiple MAX16065/MAX16066s.

Two configuration bits determine the behavior of the MAX16065/MAX16066 when $\overline{\text{EXTFAULT}}$ is pulled low by some other device. Register bit r72h[5], if set to a '1', causes the sequencer state machine to enter the fault state, deasserting all the outputs, when $\overline{\text{EXTFAULT}}$ is pulled low. When this happens, the flag bit r1Ch[5] gets set to indicate the cause of the fault. If register bit r6Dh[2] is set in addition to r72h[5], $\overline{\text{EXTFAULT}}$ going low triggers a nonvolatile fault log operation.

Faults

The MAX16065/MAX16066 monitor the input (MON_) channels and compare the results with an overvoltage threshold, an undervoltage threshold, and a selectable overvoltage or undervoltage early warning threshold. Based on these conditions, the MAX16065/MAX16066 assert various fault outputs and save specific information about the channel conditions and voltages into the nonvolatile flash. Once a critical fault event occurs, the failing channel condition, ADC conversions at the time of the fault, or both can be saved by configuring the event logger. The event logger records a single failure in the internal flash and sets a lock bit that protects the stored fault data from accidental erasure on a subsequent power-up.

An overvoltage event occurs when the voltage at a monitored input exceeds the overvoltage threshold for that input. An undervoltage event occurs when the voltage at a monitored input falls below the undervoltage threshold. Fault thresholds are set in registers r48h to r6Ch as shown in Table 15. Disabled inputs are not monitored for fault conditions and are skipped over by the input multiplexer. Only the upper 8 bits of a conversion result are compared with the programmed fault thresholds.

The general-purpose inputs/outputs (GPIO1 to GPIO8) can be configured as $\overline{\text{ANY\_FAULT}}$ outputs or dedicated Fault1 and Fault2 outputs to indicate fault conditions. These fault outputs are not masked by the critical fault enable bits shown in Table 18. See the *General-Purpose Inputs/Outputs* section for more information on configuring GPIO_s as fault outputs.

Deglitch

Fault conditions are detected at the end of each conversion. When the voltage on an input falls outside a monitored threshold for one acquisition, the input multiplexer remains on that channel and performs several successive conversions. To trigger a fault, the input must stay outside the threshold for a certain number of acquisitions as determined by the deglitch setting in r73h[6:5] and r74h[6:5] (see Table 16).

Fault Flags

Fault flags indicate the fault status of a particular input. The fault flag of any monitored input in the device can be read at any time from registers r1Bh and r1Ch, as shown in Table 17. Clear a fault flag by writing a '1' to the appropriate bit in the flag register. Unlike the fault signals sent to the fault outputs, these bits are masked by the critical fault enable bits (see Table 18). The fault flag is only set when the matching enable bit in the critical fault enable register is also set.

If a GPIO_ is configured as an open-drain $\overline{\text{EXTFAULT}}$ input/output, and $\overline{\text{EXTFAULT}}$ is pulled low by an external circuit, bit r1Ch[5] is set.

If a fault occurs during the secondary sequence group, the slot number where the failure occurred is stored in r1Dh.

The SMBus Alert bit is set if the MAX16065/MAX16066 have asserted the SMBus Alert output. Clear by writing a '1'. See the *SMBALERT* section for more details.

Table 15. Fault Threshold Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
48h	248h	[7:0]	MON1 secondary threshold
49h	249h	[7:0]	MON1 overvoltage threshold
4Ah	24Ah	[7:0]	MON1 undervoltage threshold
4Bh	24Bh	[7:0]	MON2 secondary threshold
4Ch	24Ch	[7:0]	MON2 overvoltage threshold
4Dh	24Dh	[7:0]	MON2 undervoltage threshold
4Eh	24Eh	[7:0]	MON3 secondary threshold
4Fh	24Fh	[7:0]	MON3 overvoltage threshold
50h	250h	[7:0]	MON3 undervoltage threshold
51h	251h	[7:0]	MON4 secondary threshold
52h	252h	[7:0]	MON4 overvoltage threshold
53h	253h	[7:0]	MON4 undervoltage threshold
54h	254h	[7:0]	MON5 secondary threshold
55h	255h	[7:0]	MON5 overvoltage threshold
56h	256h	[7:0]	MON5 undervoltage threshold
57h	257h	[7:0]	MON6 secondary threshold
58h	258h	[7:0]	MON6 overvoltage threshold
59h	259h	[7:0]	MON6 undervoltage threshold
5Ah	25Ah	[7:0]	MON7 secondary threshold
5Bh	25Bh	[7:0]	MON7 overvoltage threshold
5Ch	25Ch	[7:0]	MON7 undervoltage threshold
5Dh	25Dh	[7:0]	MON8 secondary threshold
5Eh	25Eh	[7:0]	MON8 overvoltage threshold
5Fh	25Fh	[7:0]	MON8 undervoltage threshold
60h	260h	[7:0]	MON9 secondary threshold
61h	261h	[7:0]	MON9 overvoltage threshold
62h	262h	[7:0]	MON9 undervoltage threshold
63h	263h	[7:0]	MON10 secondary threshold
64h	264h	[7:0]	MON10 overvoltage threshold
65h	265h	[7:0]	MON10 undervoltage threshold
66h	266h	[7:0]	MON11 secondary threshold
67h	267h	[7:0]	MON11 overvoltage threshold
68h	268h	[7:0]	MON11 undervoltage threshold
69h	269h	[7:0]	MON12 secondary threshold
6Ah	26Ah	[7:0]	MON12 overvoltage threshold
6Bh	26Bh	[7:0]	MON12 undervoltage threshold
6Ch	26Ch	[7:0]	Secondary overcurrent threshold

Table 16. Deglitch Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[6:5]	Overcurrent Comparator Deglitch Time: 00 = No deglitch 01 = 4ms 10 = 15ms 11 = 60ms
74h	274h	[6:5]	Voltage Comparator Deglitch Configuration: 00 = 2 cycles 01 = 4 cycles 10 = 8 cycles 11 = 16 cycles

Critical Faults

During normal operation, a fault condition can be configured to shut down all the EN_OUT_s and store fault information in the flash memory by setting the appropriate critical fault enable bits. During power-up and power-down, all sequenced MON_ inputs are considered critical. Faults during power-up and power-down always cause the EN_OUT_s to turn off and can store fault information in the flash memory, depending on the contents of r6Dh[1:0]. Set the appropriate critical fault enable bits in registers r6Eh to r72h (see Table 18) for a fault condition to trigger a critical fault.

Logged fault information is stored in flash registers r200h to r20Fh (see Table 19). After fault information is logged, the flash is locked and must be unlocked to enable a new fault log to be stored. Write a '0' to r8Ch[1] to unlock the FAULT flash. Fault information can be configured to store ADC conversion results and/or fault flags in registers. Select the critical fault configuration in r6Dh[1:0]. Set r6Dh[1:0] to '11' to turn off the fault logger. All stored ADC results are 8 bits wide.

Power-Up/Power-Down Faults

All EN_OUT_s deassert when an overvoltage or undervoltage fault is detected during power-up/power-down and the MAX16065/MAX16066 return to the power-off condition. Fault information can be stored to flash depending on r6D[1:0], see Table 18. GPIO3 and GPIO8 can be configured as power-up fault outputs ($\overline{\text{ANY\_FAULT}}$).

Autoretry/Latch Mode

The MAX16065/MAX16066 can be configured for one of two fault management methods: autoretry or latch-on fault. Set r74h[4:3] to '00' to select the latch-on-fault mode. In this configuration, EN_OUT_s deassert after a critical fault event. The device does not reinitiate the power-up sequence until EN is toggled or the Software Enable bit is toggled. See the *Enable* section for more information on setting the software enable bit.

Table 17. Fault Flags

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
1Bh	[0]	MON1
	[1]	MON2
	[2]	MON3
	[3]	MON4
	[4]	MON5
	[5]	MON6
	[6]	MON7
	[7]	MON8

Table 17. Fault Flags (continued)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
1Ch	[0]	MON9
	[1]	MON10
	[2]	MON11
	[3]	MON12
	[4]	Overcurrent
	[5]	External fault (EXTFAULT)
	[6]	SMB alert
1Dh	[4:0]	Slot where failure occurred during secondary sequence
	[7:5]	Reserved

Table 18. Critical Fault Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
6Dh	26Dh	[1:0]	Fault Information to Log: 00 = Save failed line flags and ADC values in flash 01 = Save only failed line flags in flash 10 = Save only ADC values in flash 11 = Do not save anything
		[2]	1 = Fault log triggered when EXTFAULT is pulled low externally
		[7:3]	Not used
6Eh	26Eh	[0]	1 = Fault log triggered when MON1 is below its undervoltage threshold
		[1]	1 = Fault log triggered when MON2 is below its undervoltage threshold
		[2]	1 = Fault log triggered when MON3 is below its undervoltage threshold
		[3]	1 = Fault log triggered when MON4 is below its undervoltage threshold
		[4]	1 = Fault log triggered when MON5 is below its undervoltage threshold
		[5]	1 = Fault log triggered when MON6 is below its undervoltage threshold
		[6]	1 = Fault log triggered when MON7 is below its undervoltage threshold
		[7]	1 = Fault log triggered when MON8 is below its undervoltage threshold
6Fh	26Fh	[0]	1 = Fault log triggered when MON9 is below its undervoltage threshold
		[1]	1 = Fault log triggered when MON10 is below its undervoltage threshold
		[2]	1 = Fault log triggered when MON11 is below its undervoltage threshold
		[3]	1 = Fault log triggered when MON12 is below its undervoltage threshold
		[4]	1 = Fault log triggered when MON1 is above its overvoltage threshold
		[5]	1 = Fault log triggered when MON2 is above its overvoltage threshold
		[6]	1 = Fault log triggered when MON3 is above its overvoltage threshold
		[7]	1 = Fault log triggered when MON4 is above its overvoltage threshold

Table 18. Critical Fault Configuration (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
70h	270h	[0]	1 = Fault log triggered when MON5 is above its overvoltage threshold
		[1]	1 = Fault log triggered when MON6 is above its overvoltage threshold
		[2]	1 = Fault log triggered when MON7 is above its overvoltage threshold
		[3]	1 = Fault log triggered when MON8 is above its overvoltage threshold
		[4]	1 = Fault log triggered when MON9 is above its overvoltage threshold
		[5]	1 = Fault log triggered when MON10 is above its overvoltage threshold
		[6]	1 = Fault log triggered when MON11 is above its overvoltage threshold
		[7]	1 = Fault log triggered when MON12 is above its overvoltage threshold
71h	271h	[0]	1 = Fault log triggered when MON1 is above/below the early threshold warning
		[1]	1 = Fault log triggered when MON2 is above/below the early threshold warning
		[2]	1 = Fault log triggered when MON3 is above/below the early threshold warning
		[3]	1 = Fault log triggered when MON4 is above/below the early threshold warning
		[4]	1 = Fault log triggered when MON5 is above/below the early threshold warning
		[5]	1 = Fault log triggered when MON6 is above/below the early threshold warning
		[6]	1 = Fault log triggered when MON7 is above/below the early threshold warning
		[7]	1 = Fault log triggered when MON8 is above/below the early threshold warning
72h	272h	[0]	1 = Fault log triggered when MON9 is above/below the early threshold warning
		[1]	1 = Fault log triggered when MON10 is above/below the early threshold warning
		[2]	1 = Fault log triggered when MON11 is above/below the early threshold warning
		[3]	1 = Fault log triggered when MON12 is above/below the early threshold warning
		[4]	1 = Fault log triggered when overcurrent early threshold is exceeded
		[5]	1 = EXTFAULT pulled low externally causes sequencer to enter fault state, turning off all EN_OUT_s 0 = EXTFAULT pulled low externally does not cause sequencer to enter fault state
		[7:6]	Reserved

Table 19. Nonvolatile Fault Log Registers

FLASH ADDRESS	BIT RANGE	DESCRIPTION
200h	[4:0]	Sequencer state where the fault has happened (see Table 1 for state codes)
	[7:5]	Not used
201h	[0]	Fault log triggered on MON1
	[1]	Fault log triggered on MON2
	[2]	Fault log triggered on MON3
	[3]	Fault log triggered on MON4
	[4]	Fault log triggered on MON5
	[5]	Fault log triggered on MON6
	[6]	Fault log triggered on MON7
	[7]	Fault log triggered on MON8

Table 19. Nonvolatile Fault Log Registers (continued)

FLASH ADDRESS	BIT RANGE	DESCRIPTION
202h	[0]	Fault log triggered on MON9
	[1]	Fault log triggered on MON10
	[2]	Fault log triggered on MON11
	[3]	Fault log triggered on MON12
	[4]	Fault log triggered on overcurrent
	[5]	Fault log triggered on EXTFAULT
	[7:6]	Not used
203h	[7:0]	MON1 ADC output bits 9–2
204h	[7:0]	MON2 ADC output bits 9–2
205h	[7:0]	MON3 ADC output bits 9–2
206h	[7:0]	MON4 ADC output bits 9–2
207h	[7:0]	MON5 ADC output bits 9–2
208h	[7:0]	MON6 ADC output bits 9–2
209h	[7:0]	MON7 ADC output bits 9–2
20Ah	[7:0]	MON8 ADC output bits 9–2
20Bh	[7:0]	MON9 ADC output bits 9–2
20Ch	[7:0]	MON10 ADC output bits 9–2
20Dh	[7:0]	MON11 ADC output bits 9–2
20Eh	[7:0]	MON12 ADC output bits 9–2
20Fh	[7:0]	Current-sense ADC output bits 9–2

Table 20. Autoretry Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
74h	274h	[2:0]	Retry Delay: 000 = 20ms 001 = 40ms 010 = 80ms 011 = 150ms 100 = 280ms 101 = 540ms 110 = 1s 111 = 2s
		[4:3]	Autoretry/Latch Mode: 00 = Latch 01 = Retry 1 time 10 = Retry 3 times 11 = Always retry

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Set r74h[4:3] to a value other than '00' to select autoretry mode (see Table 20). In this configuration, the device shuts down after a critical fault event then restarts following a configurable delay. Use r74h[2:0] to select an autoretry delay from 20ms to 1.6s. See Table 20 for more information on setting the autoretry delay.

When fault information is stored in flash (see the *Critical Faults* section) and autoretry mode is selected, set an autoretry delay greater than the time required for the storing operation. When fault information is stored in flash and latch-on-fault mode is chosen, toggle EN or reset the software enable bit only after the completion of the storing operation. When saving information about the failed lines only, ensure a delay of at least 150ms before the restart procedure. Otherwise, ensure a minimum 280ms timeout, to ensure that ADC conversions are completed and values are stored correctly in flash.

Programmable Ouputs (EN_OUT1–EN_OUT12)

The MAX16065 includes twelve programmable outputs, and the MAX16066 includes eight programmable outputs. These outputs are capable of connecting to either the enable (EN) inputs of a DC-DC or LDO power supply, or to drive the gate of an n-channel MOSFET in charge-pump mode. Selectable output configurations include: active-low or active-high, open drain or push-pull. EN_OUT1–EN_OUT8 can act as charge-pump outputs, EN_OUT9–EN_OUT12 can be configured as general-purpose inputs or general-purpose outputs. Use registers r30h to r33h to configure outputs. See Table 21 for detailed information on configuring EN_OUT1–EN_OUT12.

In charge-pump configuration, EN_OUT1–EN_OUT8 act as high-voltage charge-pump outputs to drive up to eight external n-channel MOSFETs. During sequencing, an EN_OUT_ output set to the charge-pump configuration outputs 11V relative to GND. See the *Sequencing* section for more detailed information on power-supply sequencing.

In open-drain output configuration, connect an external pullup resistor from the output to an external voltage up to 5.5V (EN_OUT9–EN_OUT12) or 14V (EN_OUT1–EN_OUT8). Choose the pullup resistor depending on the number of devices connected to the open-drain output and the allowable current consumption. The open-drain output configuration allows wire-ORed connection.

In push-pull configuration, the MAX16065/MAX16066's programmable outputs are referenced to V_{DBP}.

Table 21. EN_OUT1–EN_OUT12 Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
30h	230h	[1:0]	EN_OUT1 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[3:2]	EN_OUT2 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[5:4]	EN_OUT3 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[7:6]	EN_OUT4 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull

Table 21. EN_OUT1–EN_OUT12 Configuration (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
31h	231h	[1:0]	EN_OUT5 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[3:2]	EN_OUT6 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[5:4]	EN_OUT7 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[7:6]	EN_OUT8 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
32h (MAX16065 Only)	232h	[1:0]	EN_OUT9 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[3:2]	EN_OUT10 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[5:4]	EN_OUT11 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[7:6]	EN_OUT12 Configuration: 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull

Table 21. EN_OUT1–EN_OUT12 Configuration (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
33h	233h	[0]	EN_OUT1 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[1]	EN_OUT2 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[2]	EN_OUT3 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[3]	EN_OUT4 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[4]	EN_OUT5 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[5]	EN_OUT6 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[6]	EN_OUT7 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[7]	EN_OUT8 Charge-Pump Output Configuration: 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)

EN_OUT_s as GPIO_ (MAX16065 Only)

EN_OUT9 to EN_OUT12 can be configured as GPIO_ by setting the sequencing slot assignments in r88h and r89h to '1101' and '1110', see Tables 5 and 6. If an EN_OUT_ is configured as a general-purpose input, the state of the pin can be read from r1Fh (see Table 22). If an EN_OUT_ is configured as a general-purpose output, it is controlled by r34h.

EN_OUT_ State During Power-Up

When V_{CC} is ramped from 0 to the operating supply voltage, the EN_OUT_ output is high impedance until V_{CC} reaches UVLO and then EN_OUT_ goes into the configured deasserted state after the boot-up relay. See Figures 6 and 7. Configure RESET as an active-low push-pull or open-drain output pulled up to V_{CC} through a 10kΩ resistor for Figures 6 and 7.

Reset Output

The reset output, RESET, indicates the status of the primary sequence. It asserts during power-up/power-down and deasserts following the reset timeout period once the power-up sequence is complete. The power-up sequence is complete when any MON_ inputs assigned to the final slot exceed the undervoltage thresholds and final sequence delay expires. When no MON_ inputs are assigned to the final slot, the power-up sequence is complete after the slot sequence delay expires.

During normal monitoring, RESET can be configured to assert when any combination of MON_ inputs violates configurable combinations of thresholds: undervoltage, overvoltage, or early warning. Select the combination of thresholds using r3Bh[1:0], and select the combination of MON_ inputs using r3Ch[7:1] and r3Dh[4:0]. Note that MON_ inputs configured as critical faults will always cause RESET to assert regardless of these configuration bits.

RESET can be configured as push-pull or open drain using r3Bh[3], and active-high or active-low using r3Bh[2]. Select the reset timeout by loading a value from Table 23 into r3Bh[7:4]. RESET can be forced to assert by writing a '1' into r3Ch[0]. RESET remains asserted for the reset timeout period after a '0' is written into r3Ch[0]. See Table 23. The current state of RESET can be checked by reading r20h[0].

Table 22. EN_OUT_ GPIO_ State Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
1Fh	—	[0]	EN_OUT9 input state
		[1]	EN_OUT10 input state
		[2]	EN_OUT11 input state
		[3]	EN_OUT12 input state
34h	234h	[0]	1 = Assert EN_OUT9
		[1]	1 = Assert EN_OUT10
		[2]	1 = Assert EN_OUT11
		[3]	1 = Assert EN_OUT12

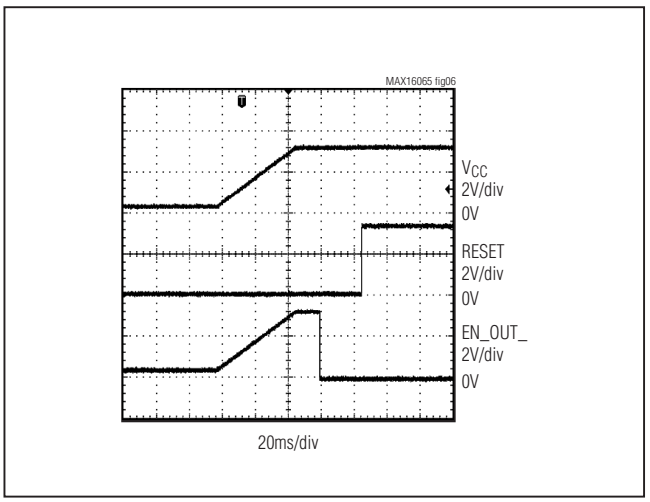

Figure 6. RESET and EN_OUT_ During Power-Up, EN_OUT_ in Open-Drain Active-Low Configuration

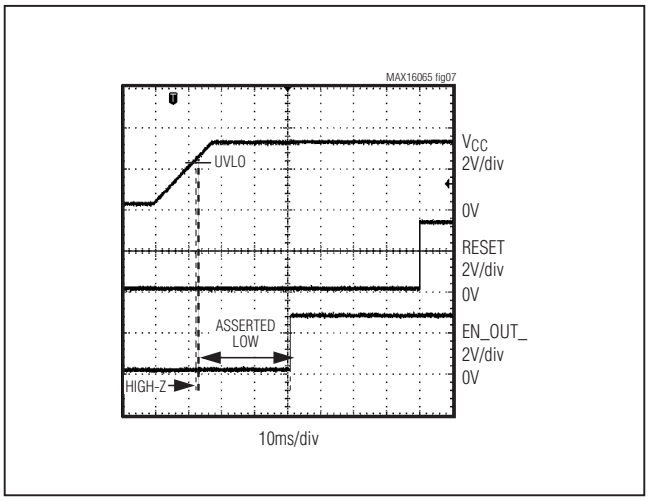

Figure 7. RESET and EN_OUT_ During Power-Up, EN_OUT_ in Push-Pull Active-High Configuration

Watchdog Timer

The watchdog timer operates together with or independently of the MAX16065/MAX16066. When operating in dependent mode, the watchdog is not activated until the sequencing is complete and RESET is deasserted. When operating in independent mode, the watchdog timer is independent of the sequencing operation and activates immediately after V_{CC} exceeds the UVLO threshold and the boot phase is complete. Set r73h[4] to '0' to configure the watchdog in dependent mode. Set r73h[4] to '1' to configure the watchdog in independent mode. See Table 24 for more information on configuring the watchdog timer in dependent or independent mode.

Dependent Watchdog Timer Operation

Use the watchdog timer to monitor µP activity in two modes. Flexible timeout architecture provides an adjustable watchdog startup delay of up to 300s, allowing complicated systems to complete lengthy boot-up routines. An adjustable watchdog timeout allows the supervisor to provide quick alerts when processor activity fails. After each reset event (V_{CC} drops below UVLO then returns above UVLO, software reboot, manual reset ($\overline{MR}$), EN input going low then high, or watchdog reset) and once sequencing is complete, the watchdog startup delay provides an extended time for the system to power up and fully initialize all µP and system components before assuming responsibility for routine watchdog updates. Set r76h[6:4] to a value other than '000' to enable the watchdog startup delay. Set r76h[6:4] to '000' to disable the watchdog startup delay.

Table 23. Reset Output Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
3Bh	23Bh	[1:0]	Reset Output Depends On: 00 = Undervoltage threshold violations 01 = Early warning threshold violations 10 = Overvoltage threshold violations 11 = Undervoltage or overvoltage threshold violations
		[2]	0 = Active-low 1 = Active-high
		[3]	0 = Push-pull 1 = Open drain
		[7:4]	Reset Timeout Period: 0000 = 25µs 0001 = 1.5ms 0010 = 2.5ms 0011 = 4ms 0100 = 6ms 0101 = 10ms 0110 = 15ms 0111 = 25ms 1000 = 40ms 1001 = 60ms 1010 = 100ms 1011 = 150ms 1100 = 250ms 1101 = 400ms 1110 = 600ms 1111 = 1s
3Ch	23Ch	[0]	Reset Soft Trigger: 0 = Normal RESET behavior 1 = Force RESET to assert
		[1]	1 = RESET depends on MON1
		[2]	1 = RESET depends on MON2
		[3]	1 = RESET depends on MON3
		[4]	1 = RESET depends on MON4
		[5]	1 = RESET depends on MON5
		[6]	1 = RESET depends on MON6
		[7]	1 = RESET depends on MON7
3Dh	23Dh	[0]	1 = RESET depends on MON8
		[1]	1 = RESET depends on MON9
		[2]	1 = RESET depends on MON10
		[3]	1 = RESET depends on MON11
		[4]	1 = RESET depends on MON12
		[7:5]	Reserved

The normal watchdog timeout period, t_{WDI}, begins after the first transition on WDI before the conclusion of the long startup watchdog period, $t_{WDI\_STARTUP}$ (Figures 7 and 8). During the normal operating mode, $\overline{WDO}$ asserts if the µP does not toggle WDI with a valid transition (high-to-low or low-to-high) within the standard timeout period, t_{WDI}. $\overline{WDO}$ remains asserted until WDI is toggled or RESET is asserted (Figure 9).

While EN is low, the watchdog timer is in reset. The watchdog timer does not begin counting until the power-on mode is reached and $\overline{RESET}$ is deasserted. The watchdog timer is reset and $\overline{WDO}$ deasserts any time RESET is asserted (Figure 10). The watchdog timer will be held in reset while RESET is asserted.

The watchdog can be configured to control the RESET output as well as the $\overline{WDO}$ output. RESET asserts for the reset timeout, t_{RP}, when the watchdog timer expires and the Watchdog Reset Output Enable bit (r76h[7]) is set to '1.' When $\overline{RESET}$ is asserted, the watchdog timer is cleared and $\overline{WDO}$ is deasserted, therefore, $\overline{WDO}$ pulses low for a short time (approximately 1µs) when the watchdog timer expires. RESET is not affected by the watchdog timer when the Watchdog Reset Output Enable bit (r76h[7]) is set to '0.' If a RESET is asserted by the watchdog timeout, the WDRESET bit is set to '1.' A connected processor can check this bit to see the reset was due to a watchdog timeout. See Table 24 for more information on configuring watchdog functionality.

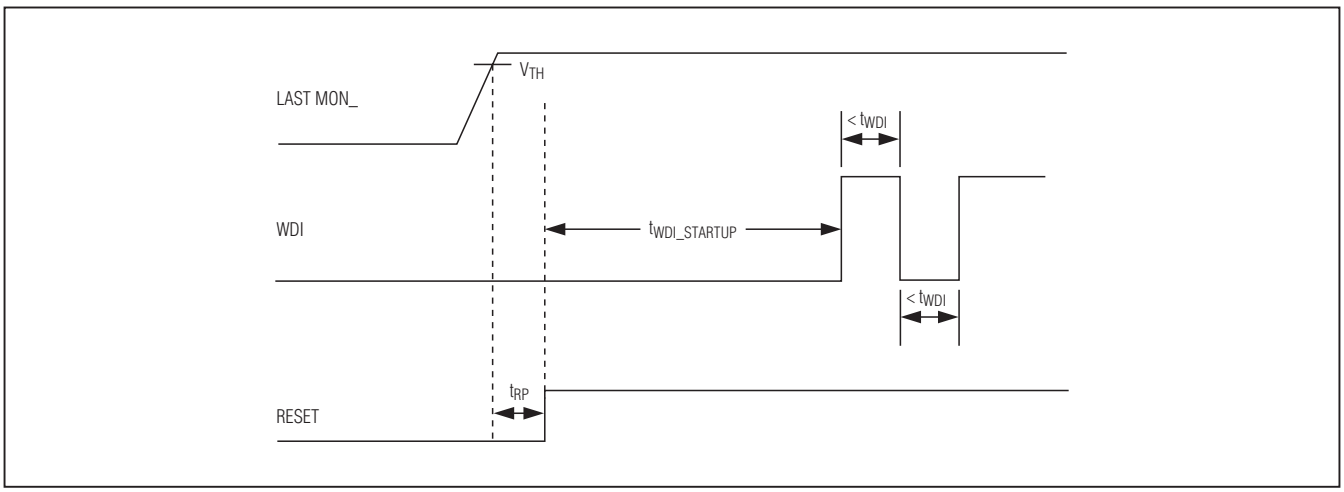

Figure 8. Normal Watchdog Startup Sequence

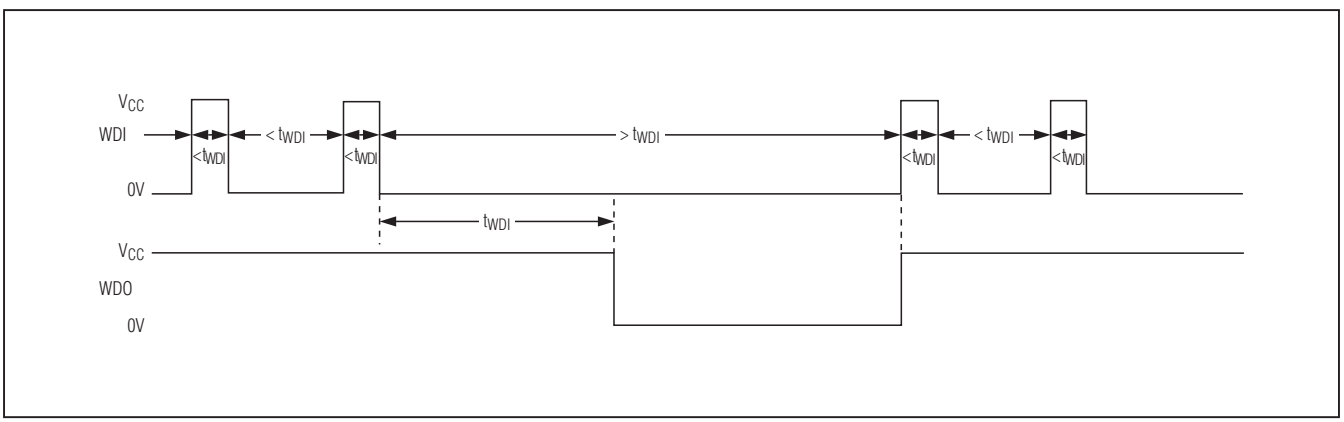

Figure 9. Watchdog Timer Operation

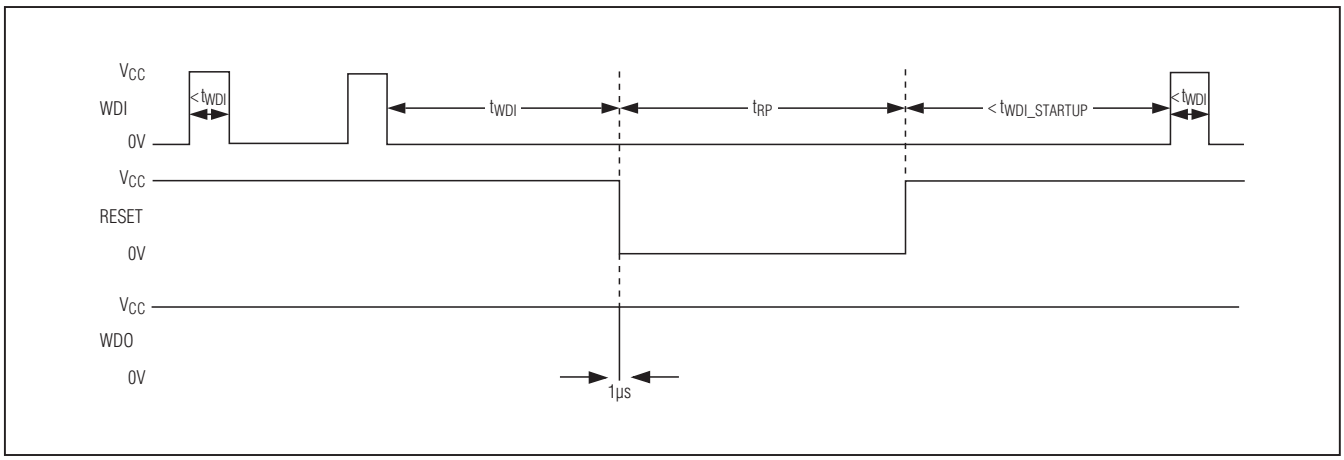

Figure 10. Watchdog Startup Sequence with Watchdog Reset Enable Bit Set to '1'

Table 24. Watchdog Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[4]	1 = Independent mode 0 = Dependent mode
76h	276h	[7]	1 = Watchdog affects RESET output 0 = Watchdog does not affect RESET output
		[6:4]	Watchdog Startup Delay: 000 = No initial timeout 001 = 30s 010 = 40s 011 = 80s 100 = 120s 101 = 160s 110 = 220s 111 = 300s
		[3:0]	Watchdog Timeout: 0000 = Watchdog disabled 0001 = 1ms 0010 = 2ms 0011 = 4ms 0100 = 8ms 0101 = 14ms 0110 = 27ms 0111 = 50ms 1000 = 100ms 1001 = 200ms 1010 = 400ms 1011 = 750ms 1100 = 1.4s 1101 = 2.7s 1110 = 5s 1111 = 10s

Table 25. Memory Lock Bits

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
8Ch	28Ch	0	Configuration Register Lock: 1 = Locked 0 = Unlocked
		1	Flash Fault Register Lock: 1 = Locked 0 = Unlocked
		2	Flash Configuration Lock: 1 = Locked 0 = Unlocked
		3	User Flash Lock: 1 = Locked 0 = Unlocked

Independent Watchdog Timer Operation

When r73h[3] is '1' the watchdog timer operates in independent mode. In independent mode, the watchdog timer operates as if it were a separate device. The watchdog timer is activated immediately upon V_{CC} exceeding UVLO and once the boot-up sequence is finished. When RESET is asserted by the sequencer state machine, the watchdog timer and $\overline{WDO}$ are not affected.

There will be a startup delay if r76h[6:4] is set to a value different than '000.' If r76h[6:4] is set to '000,' there will not be a startup delay. See Table 24 for delay times.

In independent mode, if the Watchdog Reset Output Enable bit r76h[7] is set to '1,' when the watchdog timer expires, $\overline{WDO}$ asserts then RESET asserts. $\overline{WDO}$ will then deassert. $\overline{WDO}$ will be low for approximately 1µs. If the Watchdog Reset Output Enable bit (r76h[7]) is set to '0,' when the WDT expires, $\overline{WDO}$ asserts but RESET is not affected.

User-Defined Register

Register r8Ah provides storage space for a user-defined configuration or firmware version number. Note that this register controls the contents of the JTAG USERCODE register bits 7:0. The user-defined register is stored at r28Ah in the flash memory.

Memory Lock Bits

Register r8Ch contains the lock bits for the configuration registers, configuration flash, user flash and fault register lock. See Table 25 for details.

SMBus-Compatible Interface

The MAX16065/MAX16066 feature an SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX16065/MAX16066 and the master device at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX16065/MAX16066 are transmit/receive slave-only devices, relying upon a master device to generate a clock signal. The master device (typically a microcontroller) initiates a data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX16065/MAX16066 by transmitting the proper address followed by a command and/or data words. The slave address input, A0, is capable of detecting four different states, allowing multiple identical devices to share the same serial bus. The slave address is described further in the *Slave Address* section. Each transmit sequence is framed by a START (S) or REPEATED START (SR) condition and a STOP (P) condition. Each word transmitted

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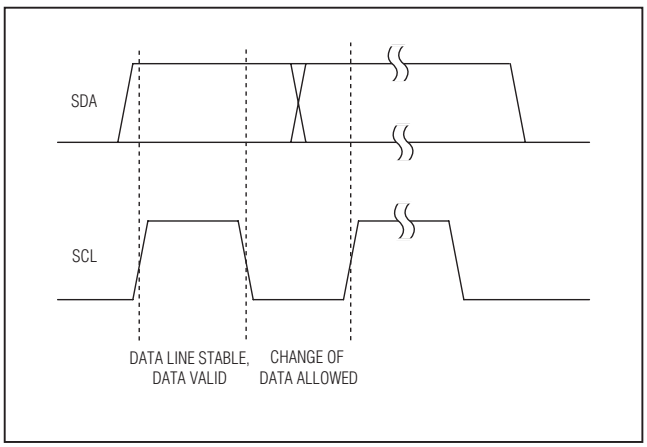

Figure 11. Bit Transfer

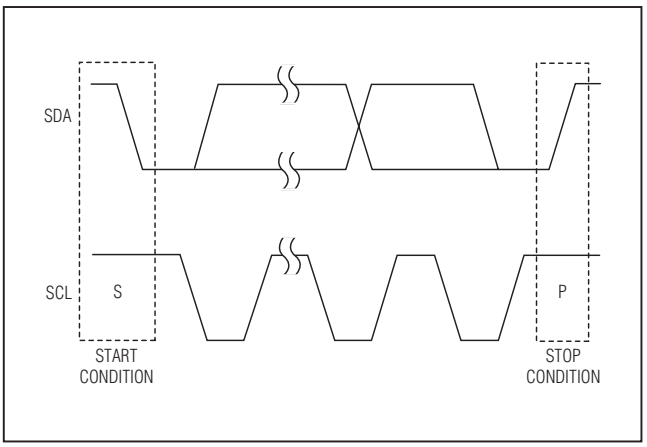

Figure 12. START and STOP Conditions

over the bus is 8 bits long and is always followed by an acknowledge pulse. SCL is a logic input, while SDA is an open-drain input/output. SCL and SDA both require external pullup resistors to generate the logic-high voltage. Use 4.7kΩ for most applications.

Bit Transfer

Each clock pulse transfers one data bit. The data on SDA must remain stable while SCL is high (Figure 11); otherwise the MAX16065/MAX16066 register a START or STOP condition (Figure 12) from the master. SDA and SCL idle high when the bus is not busy.

START and STOP Conditions

Both SCL and SDA idle high when the bus is not busy. A master device signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. The master device issues a STOP condition by transitioning SDA from low to high while SCL is high. A STOP condition frees the bus for another transmission. The bus remains active if a REPEATED START condition is generated, such as in the block read protocol (see Figure 1).

Early STOP Conditions

The MAX16065/MAX16066 recognize a STOP condition at any point during transmission except if a STOP condition occurs in the same high pulse as a START condition. This condition is not a legal SMBus format; at least one clock pulse must separate any START and STOP condition.

REPEATED START Conditions

A REPEATED START can be sent instead of a STOP condition to maintain control of the bus during a read operation. The START and REPEATED START conditions are functionally identical.

Acknowledge

The acknowledge bit (ACK) is the 9th bit attached to any 8-bit data word. The receiving device always generates an ACK. The MAX16065/MAX16066 generate an ACK when receiving an address or data by pulling SDA low during the 9th clock period (Figure 14). When transmitting data, such as when the master device reads data back from the MAX16065/MAX16066, the device waits for the master device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if the receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication at a later time. The MAX16065/MAX16066 generate a NACK after the command byte received during a software reboot, while writing to the flash, or when receiving an illegal memory address.

Slave Address

Use the slave address input, A0, to allow multiple identical devices to share the same serial bus. Connect A0 to GND, DBP (or an external supply voltage greater than 2V), SCL, or SDA to set the device address on the bus. See Table 27 for a listing of all possible 7-bit addresses.

The slave address can also be set to a custom value by loading the address into register r8Bh[6:0]. See Table 26. If r8Bh[6:0] is loaded with 00h, the address is set by input A0. Do not set the address to 09h or 7Fh to avoid address conflicts. The slave address setting takes effect immediately after writing to the register.

Packet Error Checking (PEC)

The MAX16065/MAX16066 feature a PEC mode that is useful for improving the reliability of the communication bus by detecting bit errors. By enabling PEC, an extra

Table 26. SMBus Settings Register

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
8Bh	28Bh	[6:0]	SMBus Slave Address Register. Set to 00h to use A0 pin address setting.
		[7]	1 = Enable PEC (packet error check).

Table 27. Setting the SMBus Slave Address

SLAVE ADDRESSES	
A0	**SLAVE ADDRESS**
0	1010 000R
1	1010 001R
SCL	1010 010R
SDA	1010 011R

R = Read/Write select bit.

Table 28. Command codes

COMMAND CODE	ACTION
A5h	Block write
A6h	Block read
A7h	Reboot flash in register file
A8h	Trigger emergency save to flash
A9h	Flash page access ON
AAh	Flash page access OFF
ABh	User flash access ON (must be in flash page already)
ACh	User flash access OFF (return to flash page)

CRC-8 error check byte is added in the data string during each read and/or write sequence. Enable PEC by writing a '1' to r8Bh[7].

The CRC-8 byte is calculated using the polynomial

$$C = X^8 + X^2 + X + 1$$

The PEC calculation includes all bytes in the transmission, including address, command, and data. The PEC calculation does not include ACK, NACK, START, STOP, or REPEATED START.

Command Codes

The MAX16065/MAX16066 use eight command codes for block read, block write, and other commands. See Table 28 for a list of command codes.

To initiate a software reboot, send A7h using the send byte format. A software-initiated reboot is functionally the same as a hardware-initiated power-on reset. During boot-up, flash configuration data in the range of 230h to 28Ch is copied to r30h to r8Ch registers in the default page.

Send command code A8h to trigger a fault store to flash. Configure the Critical Fault Log Control register (6Dh) to store ADC conversion results and/or fault flags.

While in the flash page, send command code A9h to access the flash page (addresses from 200h to 28Fh). Once command code A9h has been sent, all addresses are recognized as flash addresses only. Send command code AAh to return to the default page (addresses from 000h to 0FFh). Send command code ABh to access the user flash-page (addresses from 300h to 3A4h and 3ADh to 3FFh), and send command code ACh to return to the flash page.

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Restrictions When Writing to Flash

Flash must be written to 8 bytes at a time. The initial address must be aligned to 8-byte boundaries—the 3 LSBs of the initial address must be '000'. Write the 8 bytes using a single block-write command or using 8 successive Write Byte commands.

Send Byte

The send byte protocol allows the master device to send one byte of data to the slave device (see Figure 14). The send byte presets a register pointer address for a subsequent read or write. The slave sends a NACK instead of an ACK if the master tries to send a memory address or command code that is not allowed. If the master sends A5h or A6h, the data is ACK, because this could be the start of the write block or read block. If the master sends a STOP condition before the slave asserts an ACK, the internal address pointer does not change. If the master sends A7h, this signifies a software reboot. The send byte procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address or command code.
5) The addressed slave asserts an ACK (or NACK) on SDA.
6) The master sends a STOP condition.

Receive Byte

The receive byte protocol allows the master device to read the register content of the MAX16065/MAX16066 (see Figure 14). The flash or register address must be preset with a send byte or write word protocol first. Once the read is complete, the internal pointer increases by one. Repeating the receive byte protocol reads the contents of the next address. The receive byte procedure follows:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a read bit (high).
3) The addressed slave asserts an ACK on SDA.
4) The slave sends 8 data bits.
5 The master asserts a NACK on SDA.
6) The master generates a STOP condition.

Write Byte

The write byte protocol (see Figure 14) allows the master device to write a single byte in the default page, extended page, or flash page, depending on which

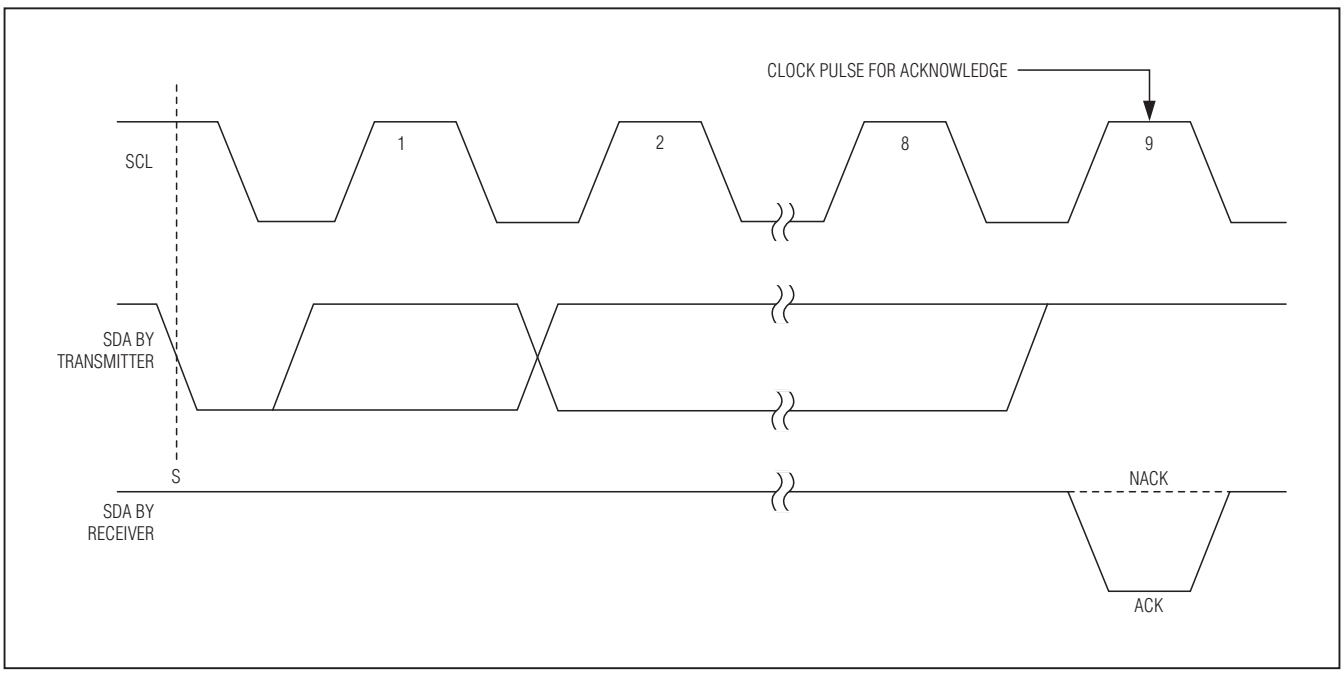

Figure 13. Acknowledge

page is currently selected. The write byte procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address.
5) The addressed slave asserts an ACK on SDA.
6) The master sends an 8-bit data byte.
7) The addressed slave asserts an ACK on SDA.
8) The master sends a STOP condition.

To write a single byte, only the 8-bit memory address and a single 8-bit data byte are sent. The data byte is written to the addressed location if the memory address is valid. The slave asserts a NACK at step 5 if the memory address is not valid.

When PEC is enabled, the Write Byte protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends an 8-bit command code.
5) The active slave asserts an ACK on the data line.
6) The master sends an 8-bit data byte.
7) The slave asserts an ACK on the data line.
8) The master sends an 8-bit PEC byte.
9) The slave asserts an ACK on the data line (if PEC is good, otherwise NACK).
10) The master generates a STOP condition.

Read Byte

The read byte protocol (see Figure 14) allows the master device to read a single byte located in the default page, extended page, or flash page depending on which page is currently selected. The read byte procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends an 8-bit memory address.
5) The addressed slave asserts an ACK on SDA.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The addressed slave asserts an ACK on SDA.
9) The slave sends an 8-bit data byte.
10) The master asserts a NACK on SDA.
11) The master sends a STOP condition.

If the memory address is not valid, it is NACKed by the slave at step 5 and the address pointer is not modified.

When PEC is enabled, the Read Byte protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends 8 data bits.
5) The active slave asserts an ACK on the data line.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave ID plus a read bit (high).
8) The addressed slave asserts an ACK on the data line.
9) The slave sends 8 data bits.
10) The master asserts an ACK on the data line.
11) The slave sends an 8-bit PEC byte.
12) The master asserts a NACK on the data line.
13) The master generates a STOP condition.

Block Write

The block write protocol (see Figure 14) allows the master device to write a block of data (1 byte to 16 bytes) to memory. Preload the destination address by a previous send byte command; otherwise the block write command begins to write at the current address pointer. After the last byte is written, the address pointer remains preset to the next valid address. If the number of bytes to be written causes the address pointer to exceed 8Fh for configuration registers or configuration flash or FFh for user flash, the address pointer stays at 8Fh or FFh, respectively, overwriting this memory address with the remaining bytes of data. The slave generates a NACK at step 5 if the command code is invalid or if the device is busy, and the address pointer is not altered.

The block write procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends the 8-bit command code for a block write (94h).
5) The addressed slave asserts an ACK on SDA.
6) The master sends the 8-bit byte count (1 byte to 16 bytes), n.
7) The addressed slave asserts an ACK on SDA.
8) The master sends 8 bits of data.
9) The addressed slave asserts an ACK on SDA.
10) Repeat steps 8 and 9 n - 1 times.
11) The master sends a STOP condition.

When PEC is enabled, the Block Write protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends 8 bits of the block write command code.
5) The slave asserts an ACK on the data line.
6) The master sends an 8-bit byte count (min 1, max 16) N.
7) The slave asserts an ACK on the data line.
8) The master sends 8 bits of data.
9) The slave asserts an ACK on the data line.
10) Repeat 8 and 9 n - 1 times.
11) The master sends an 8-bit PEC byte.
12) The slave asserts an ACK on the data line (if PEC is good, otherwise NACK).
13) The master generates a STOP condition.

Block Read

The block read protocol (see Figure 14) allows the master device to read a block of up to 16 bytes from memory. Read fewer than 16 bytes of data by issuing an early STOP condition from the master, or by generating a NACK with the master. The destination address should be preloaded by a previous send byte command; otherwise the block read command begins to read at the current address pointer. If the number of bytes to be read causes the address pointer to exceed 8Fh for the configuration register or configuration flash or FFh in user flash, the address pointer stays at 8Fh or FFh, respectively. The block read procedure is the following:

1) The master sends a START condition.
2) The master sends the 7-bit slave address and a write bit (low).
3) The addressed slave asserts an ACK on SDA.
4) The master sends 8 bits of the block read command (95h).
5) The slave asserts an ACK on SDA, unless busy.
6) The master generates a REPEATED START condition.
7) The master sends the 7-bit slave address and a read bit (high).
8) The slave asserts an ACK on SDA.
9) The slave sends the 8-bit byte count (16).
10) The master asserts an ACK on SDA.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on SDA.
13) Repeat steps 11 and 12 up to fifteen times.
14) The master asserts a NACK on SDA.
15) The master sends a STOP condition.

When PEC is enabled, the Block Read protocol becomes:

1) The master sends a START condition.
2) The master sends the 7-bit slave ID plus a write bit (low).
3) The addressed slave asserts an ACK on the data line.
4) The master sends 8 bits of the block read command code.
5) The slave asserts an ACK on the data line unless busy.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave ID plus a read bit (high).
8) The slave asserts an ACK on the data line.
9) The slave sends an 8-bit byte count (16).
10) The master asserts an ACK on the data line.
11) The slave sends 8 bits of data.
12) The master asserts an ACK on the data line.
13) Repeat 11 and 12 up to 15 times.
14) The slave sends an 8-bit PEC byte.
15) The master asserts a NACK on the data line.
16) The master generates a STOP condition.

SMBALERT

The MAX16065/MAX16066 support the SMBus alert protocol. To enable the SMBus alert output, set r35h[1:0] according to Table 29, which configures a Fault1, Fault2, or Any_Fault output to act as the SMBus alert. This output is open-drain and uses the wired-OR configuration with other devices on the SMBus. During a fault, the MAX16065/MAX16066 assert ALERT low, signaling the master that an interrupt has occurred. The master responds by sending the ARA (Alert Response Address) protocol on the SMBus. This protocol is a read byte with 09h as the slave address. The slave acknowledges the ARA (09h) address and sends its own SMBus address to the master. The slave then deasserts ALERT. The master can then query the slave and determine the cause of the fault. By checking r1C[6], the master can confirm that the MAX16065/MAX16066 triggered the SMBus alert. The master must send the ARA before clearing r1Ch[6]. Clear r1Ch[6] by writing a '1.'

JTAG Serial Interface

The MAX16065/MAX16066 feature a JTAG port that complies with a subset of the IEEE 1149.1 specification. Either the SMBus or the JTAG interface can be used to access internal memory; however, only one interface is allowed to run at a time. The MAX16065/MAX16066 do not support IEEE 1149.1 boundary-scan functionality. The MAX16065/MAX16066 contain extra JTAG instructions and registers not included in the JTAG specification that provide access to internal memory. The extra instructions include LOAD ADDRESS, WRITE, READ, REBOOT, SAVE.

Test Access Port (TAP)

Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at TMS on the rising edge of TCK. See Figure 16 for a diagram of the finite state machine. The possible states are described in the following:

Test-Logic-Reset: At power-up, the TAP controller is in the test-logic-reset state. The instruction register contains the IDCODE instruction. All system logic of the device operates normally. This state can be reached from any state by driving TMS high for five clock cycles.

Run-Test/Idle: The run-test/idle state is used between scan operations or during specific tests. The instruction register and test data registers remain idle.

Select-DR-Scan: All test data registers retain their previous state. With TMS low, a rising edge of TCK moves the controller into the capture-DR state and initiates a scan sequence. TMS high during a rising edge on TCK moves the controller to the select-IR-scan state.

Capture-DR: Data can be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected test data register does not allow parallel loads, the test data register remains at its current value. On the rising edge of TCK, the controller goes to the shift-DR state if TMS is low or it goes to the exit1-DR state if TMS is high.

Shift-DR: The test data register selected by the current instruction connects between TDI and TDO and shifts data one stage toward its serial output on each rising edge of TCK while TMS is low. On the rising edge of TCK, the controller goes to the exit1-DR state if TMS is high.

Exit1-DR: While in this state, a rising edge on TCK puts the controller in the update-DR state. A rising edge on TCK with TMS low puts the controller in the pause-DR state.

Table 29. SMBus Alert Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
35h	235h	[1:0]	SMBus Alert Configuration: 00 = Disabled 01 = Fault1 is SMBus ALERT 10 = Fault2 is SMBus ALERT 11 = Any_Fault is SMBus ALERT

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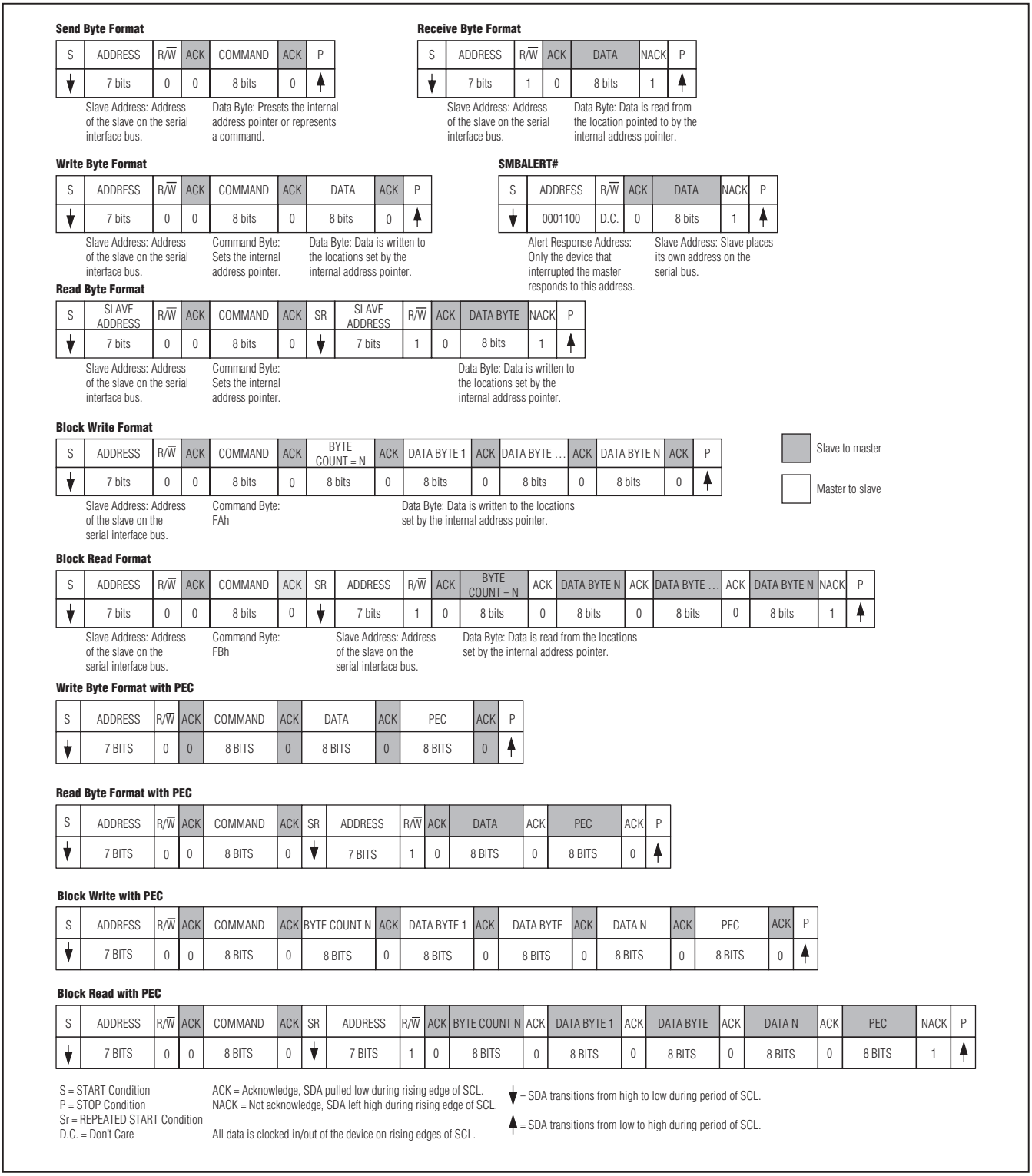

Figure 14. SMBus Protocols

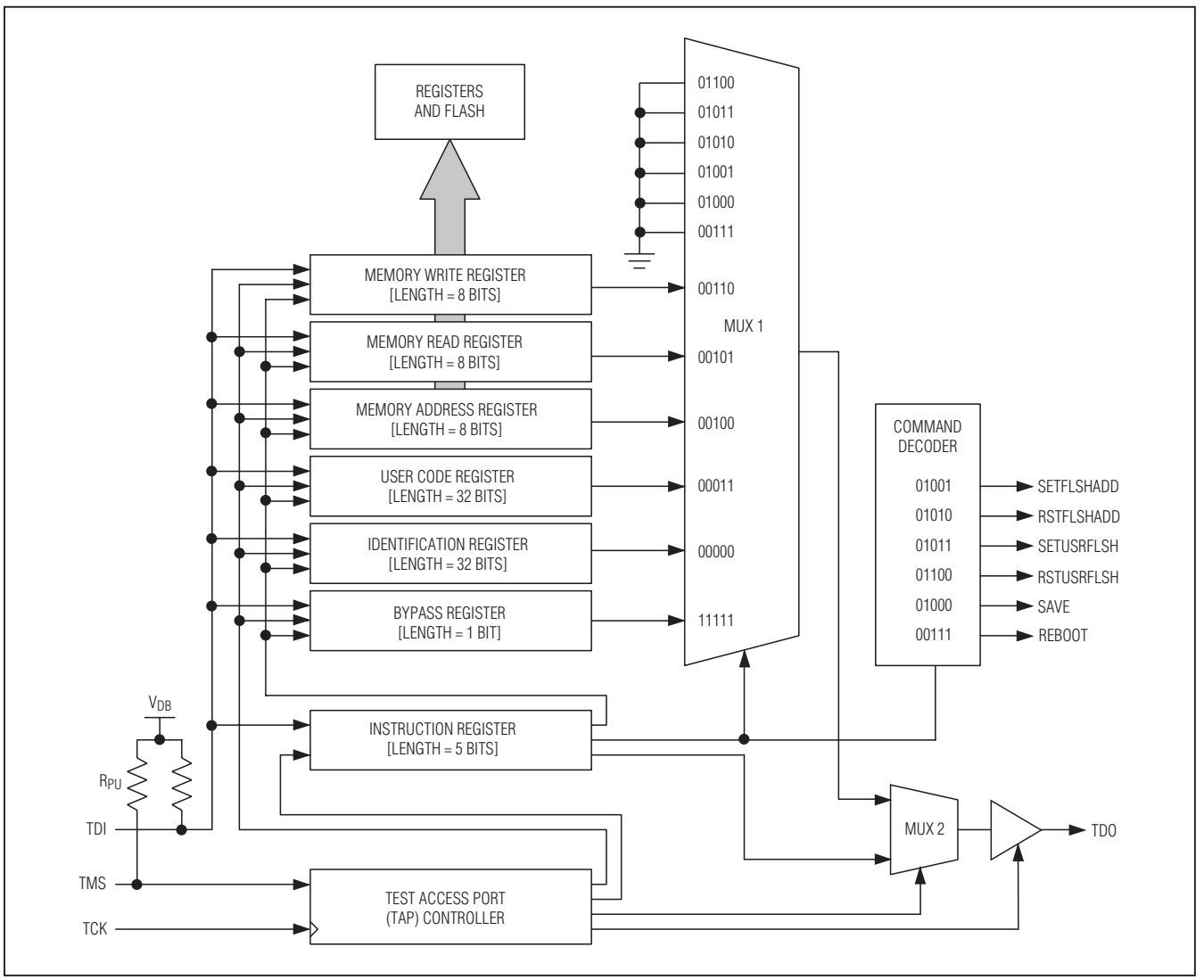

Figure 15. JTAG Block Diagram

Pause-DR: Shifting of the test data registers halts while in this state. All test data registers retain their previous state. The controller remains in this state while TMS is low. A rising edge on TCK with TMS high puts the controller in the exit2-DR state.

Exit2-DR: A rising edge on TCK with TMS high while in this state puts the controller in the update-DR state. A rising edge on TCK with TMS low enters the shift-DR state.

Update-DR: A falling edge on TCK while in the update-DR state latches the data from the shift register path of the test data registers into a set of output latches. This prevents changes at the parallel output because of changes in the shift register. On the rising edge of TCK, the controller goes to the run-test/idle state if TMS is low or goes to the select-DR-scan state if TMS is high.

Select-IR-Scan: All test data registers retain the previous states. The instruction register remains unchanged during this state. With TMS low, a rising edge on TCK moves the controller into the capture-IR state. TMS high during a rising edge on TCK puts the controller back into the test-logic-reset state.

Capture-IR: Use the capture-IR state to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of TCK. If TMS is high on the rising edge of TCK, the controller enters the

exit1-IR state. If TMS is low on the rising edge of TCK, the controller enters the shift-IR state.

Shift-IR: In this state, the shift register in the instruction register connects between TDI and TDO and shifts data one stage for every rising edge of TCK toward the TDO serial output while TMS is low. The parallel outputs of the instruction register as well as all test data registers remain at the previous states. A rising edge on TCK with TMS high moves the controller to the exit1-IR state. A rising edge on TCK with TMS low keeps the controller in the shift-IR state while moving data one stage through the instruction shift register.

Exit1-IR: A rising edge on TCK with TMS low puts the controller in the pause-IR state. If TMS is high on the rising edge of TCK, the controller enters the update-IR state.

Pause-IR: Shifting of the instruction shift register halts temporarily. With TMS high, a rising edge on TCK puts the controller in the exit2-IR state. The controller remains in the pause-IR state if TMS is low during a rising edge on TCK.

Exit2-IR: A rising edge on TCK with TMS high puts the controller in the update-IR state. The controller loops back to shift-IR if TMS is low during a rising edge of TCK in this state.

Update-IR: The instruction code that has been shifted into the instruction shift register latches to the parallel outputs of the instruction register on the falling edge of TCK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on TCK with TMS low puts the controller in the run-test/idle state. With TMS high, the controller enters the select-DR-scan state.

Instruction Register

The instruction register contains a shift register as well as a latched 5-bit wide parallel output. When the TAP controller enters the shift-IR state, the instruction shift register connects between TDI and TDO. While in the shift-IR state, a rising edge on TCK with TMS low shifts the data one stage toward the serial output at TDO. A rising edge on TCK in the exit1-IR state or the exit2-IR state with TMS high moves the controller to the update-IR state. The falling edge of that same TCK latches the data in the instruction shift register to the instruction register parallel output. Table 30 shows the instructions supported by the MAX16065/MAX16066 and the respective operational binary codes.

BYPASS: When the BYPASS instruction is latched into the instruction register, TDI connects to TDO through the 1-bit bypass test data register. This allows data to pass from TDI to TDO without affecting the device's operation.

IDCODE: When the IDCODE instruction is latched into the parallel instruction register, the identification data register is selected. The device identification code is loaded into the identification data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR can be used to shift the identification code out serially through TDO. During test-logic-reset, the IDCODE instruction is forced into the instruction register. The identification code always has a '1' in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. See Table 31.

USERCODE: When the USERCODE instruction latches into the parallel instruction register, the user-code data register is selected. The device user-code loads into the user-code data register on the rising edge of TCK following entry into the capture-DR state. Shift-DR can be used to shift the user-code out serially through TDO. See Table 32. This instruction can be used to help identify multiple MAX16065/MAX16066 devices connected in a JTAG chain.

LOAD ADDRESS: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16065/MAX16066. When the LOAD ADDRESS instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory address test data register during the shift-DR state.

READ DATA: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16065/MAX16066. When the READ instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory read test data register during the shift-DR state.

WRITE DATA: This is an extension to the standard IEEE 1149.1 instruction set to support access to the memory in the MAX16065/MAX16066. When the WRITE instruction latches into the instruction register, TDI connects to TDO through the 8-bit memory write test data register during the shift-DR state.

REBOOT: This is an extension to the standard IEEE 1149.1 instruction set to initiate a software-controlled reset to the MAX16065/MAX16066. When the REBOOT instruction latches into the instruction register, the MAX16065/MAX16066 resets and immediately begins the boot-up sequence.

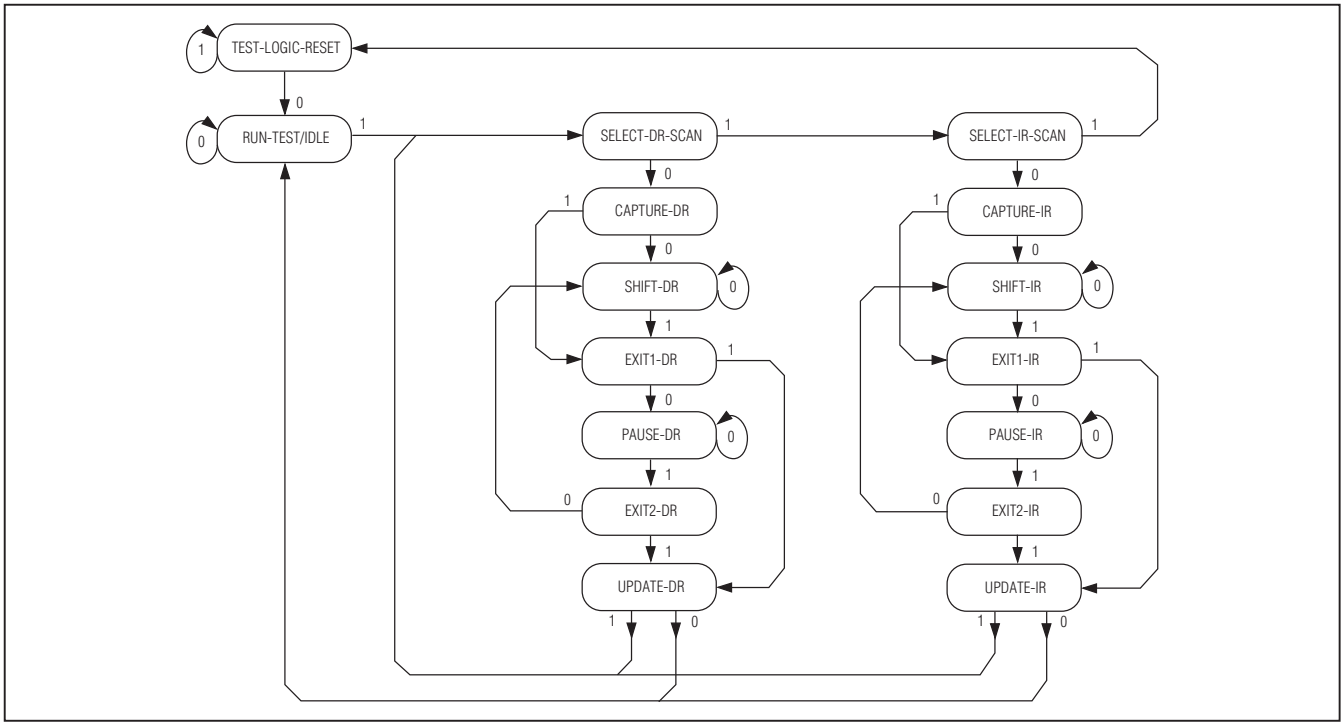

Figure 16. Tap Controller State Diagram

Table 30. JTAG Instruction Set

INSTRUCTION	CODE	NOTES
BYPASS	0x1F	Mandatory instruction code
IDCODE	0x00	Load manufacturer ID code/part number
USERCODE	0x03	Load user code
LOAD ADDRESS	0x04	Load address register content
READ DATA	0x05	Read data pointed by current address
WRITE DATA	0x06	Write data pointed by current address
REBOOT	0x07	Reboot FLASH data content into register file
SAVE	0x08	Trigger emergency save to flash
SETFLSHADD	0x09	Flash page access ON
RSTFLSHADD	0x0A	Flash page access OFF
SETUSRFLSH	0x0B	User flash access ON (must be in flash page already)
RSTUSRFLSH	0x0C	User flash access OFF (return to flash page)

Table 31. 32-Bit Identification Code

MSB			LSB
Version (4 bits)	Part number (16 bits)	Manufacturer (11 bits)	Fixed value (1 bit)
0001	1000000000000001	00011001011	1

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Table 32. 32-Bit User-Code Data

MSB																LSB
Don't Care								SMBus slave id								User ID (r8A[7:0])
00000000000000000								See Table 27								

SAVE: This is an extension to the standard IEEE 1149.1 instruction set that triggers a fault log. The current ADC conversion results along with fault information are saved to flash depending on the configuration of the Critical Fault Log Control register (r6Dh).

SETFLSHADD: This is an extension to the standard IEEE 1149.1 instruction set that allows access to the flash page. Flash registers include ADC conversion results, DACOUT enables, and GPIO_ input/output data. Use this page to access registers 200h to 2FFh

RSTFLSHADD: This is an extension to the standard IEEE 1149.1 instruction set. Use RSTFLSHADD to return to the default page and disable access to the flash page.

SETUSRFLSH: This is an extension to the standard IEEE 1149.1 instruction set that allows access to the user flash page. When on the configuration flash page, send the SETUSRFLSH command, all addresses are recognized as flash addresses only. Use this page to access registers 300h to 3FFh.

RSTUSRFLSH: This is an extension to the standard IEEE 1149.1 instruction set. Use RSTUSRFLSH to return to the configuration flash page and disable access to the user flash.

Restrictions When Writing to Flash

Flash must be written to 8 bytes at a time. The initial address must be aligned to 8-byte boundaries—the 3 LSBs of the initial address must be '000'. Write the 8 bytes using eight successive Write Data commands.

Applications Information

Unprogrammed Device Behavior

When the flash has not been programmed using the JTAG or SMBus interface, the default configuration of the EN_OUT_ outputs is open-drain active-low. This means that the EN_OUT_ outputs are high impedance. When it is necessary to hold an EN_OUT_ high or low to prevent premature startup of a power supply before the flash is programmed, connect a resistor from EN_OUT_ to ground or the supply voltage. Avoid connecting a resistor to ground when the output is to be configured as open-drain with a separate pullup resistor.

Device Behavior at Power-Up

When V_{CC} is ramped from 0, the RESET output is high impedance until V_{CC} reaches 1.4V, at which point RESET goes low. All other outputs are high impedance until V_{CC} reaches 2.7V, when the flash contents are copied into register memory. This takes 150µs (max), after which the outputs assume their programmed states.

Programming the MAX16065/MAX16066 in Circuit

The MAX16065/MAX16066 can be programmed in the application circuit by taking into account the following points during circuit design:

- The MAX16065/MAX16066 needs to be powered from an intermediate voltage bus or auxiliary voltage supply so programming can occur even when the board's power supplies are off. This could also be achieved by using ORing diodes so that power can be provided through the programming connector.
- The SMBus or JTAG bus lines should not connect through a bus multiplexer powered from a voltage rail controlled by the MAX16065/MAX16066. If the device needs to be controlled by an on-board µP, consider connecting the µP to one bus (such as SMBus) and use the other bus for in-circuit programming.
- An unprogrammed MAX16065/MAX16066's EN_OUT_s go high impedance. Ensure that this does not cause undesired circuit behavior. If necessary, connect pull-down resistors to prevent power supplies from turning on.

Maintaining Power During a Fault Condition

Power to the MAX16065/MAX16066 must be maintained for a specific period of time to ensure a successful flash fault log operation during a fault that removes power to the circuit. Table 33 shows the amount of time required depends on the settings in the fault control register (r6Dh[1:0]).

Maintain power for shutdown during fault conditions in applications where the always-on power supply cannot be relied upon by placing a diode and a large capacitor between the voltage source, V_{IN}, and V_{CC} (Figure 17). The capacitor value depends on V_{IN} and the time delay

Table 33. Maximum Write Time

R6Dh[1:0] VALUE	DESCRIPTION	MAXIMUM WRITE TIME (ms)
00	Save flags and ADC readings	244
01	Save flags	77
10	Save ADC readings	153
11	Do not save anything	—

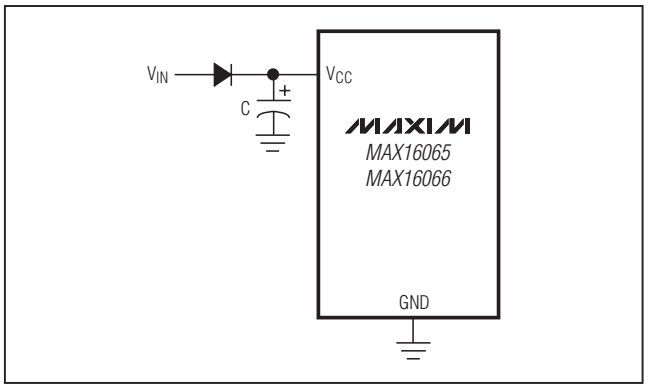

Figure 17. Power Circuit for Shutdown During Fault Conditions

required, t_{FAULT_SAVE}. Use the following formula to calculate the capacitor size:

$$C = (t_{FAULT\_SAVE} \times I_{CC(MAX)})/(V_{IN} - V_{DIODE} - V_{UVLO})$$

where the capacitance is in Farads and t_{FAULT_SAVE} is in seconds, $I_{CC(MAX)}$ is 14mA, V_{DIODE} is the voltage drop across the diode, and V_{UVLO} is 2.7V. For example, with a V_{IN} of 14V, a diode drop of 0.7V, and a t_{FAULT_SAVE} of 153ms, the minimum required capacitance is 202µF.

Driving High-Side MOSFET Switches

Up to eight of the programmable outputs (EN_OUT1–EN_OUT8) of the MAX16065/MAX16066 can be configured as charge-pump outputs to drive the gates of series-pass n-channel MOSFETS. When driving MOSFETs, these outputs act as simple power switches to turn on the voltage supply rails. Approximate the slew rate, SR, using the following formula:

$$SR = I_{CP}/(C_{GATE} + C_{EXT})$$

where I_{CP} is the 4µA (typ) charge-pump source current, C_{GATE} is the gate capacitance of the MOSFET, and C_{EXT} is the capacitance connected from the gate to ground. If more than eight series-pass MOSFETs are required for an application, additional series-pass p-channel MOSFETS can be connected to outputs configured as active-low open drain (Figure 18). Connect a pullup resistor from the gate to the source of the MOSFET, and ensure the absolute maximum ratings of the MAX16065/MAX16066 are not exceeded.

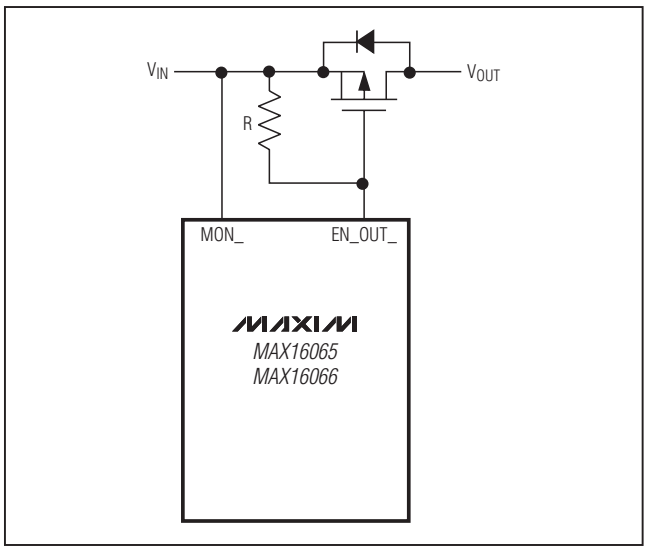

Figure 18. Connection for a p-Channel Series-Pass MOSFET

Configuring the Device

An evaluation kit and a graphical user interface (GUI) is available to create a custom configuration for the device. Refer to the MAX16065/MAX16066 Evaluation Kit for configuration.

Cascading Multiple MAX16065/MAX16066s

Multiple MAX16065/MAX16066s can be cascaded to increase the number of rails controlled for sequencing and monitoring. There are many ways to cascade the devices depending on the desired behavior. In general, there are several techniques:

- Configure a GPIO_ on each device to be EXTFAULT (open drain). Externally wire them together with a single pullup resistor. Set register bits r72h[5] and r6Dh[2] to '1' so that all faults will propagate between devices. If a critical fault occurs on one device, EXTFAULT will assert, triggering the nonvolatile fault logger in all cascaded devices and recording a snapshot of all system voltages.
- Connect open-drain RESET outputs together to obtain a master system reset signal.
- Connect all EN inputs together for a master enable signal. Since the internal timings of each cascaded device are not synchronized, EN_OUT_s placed in the same

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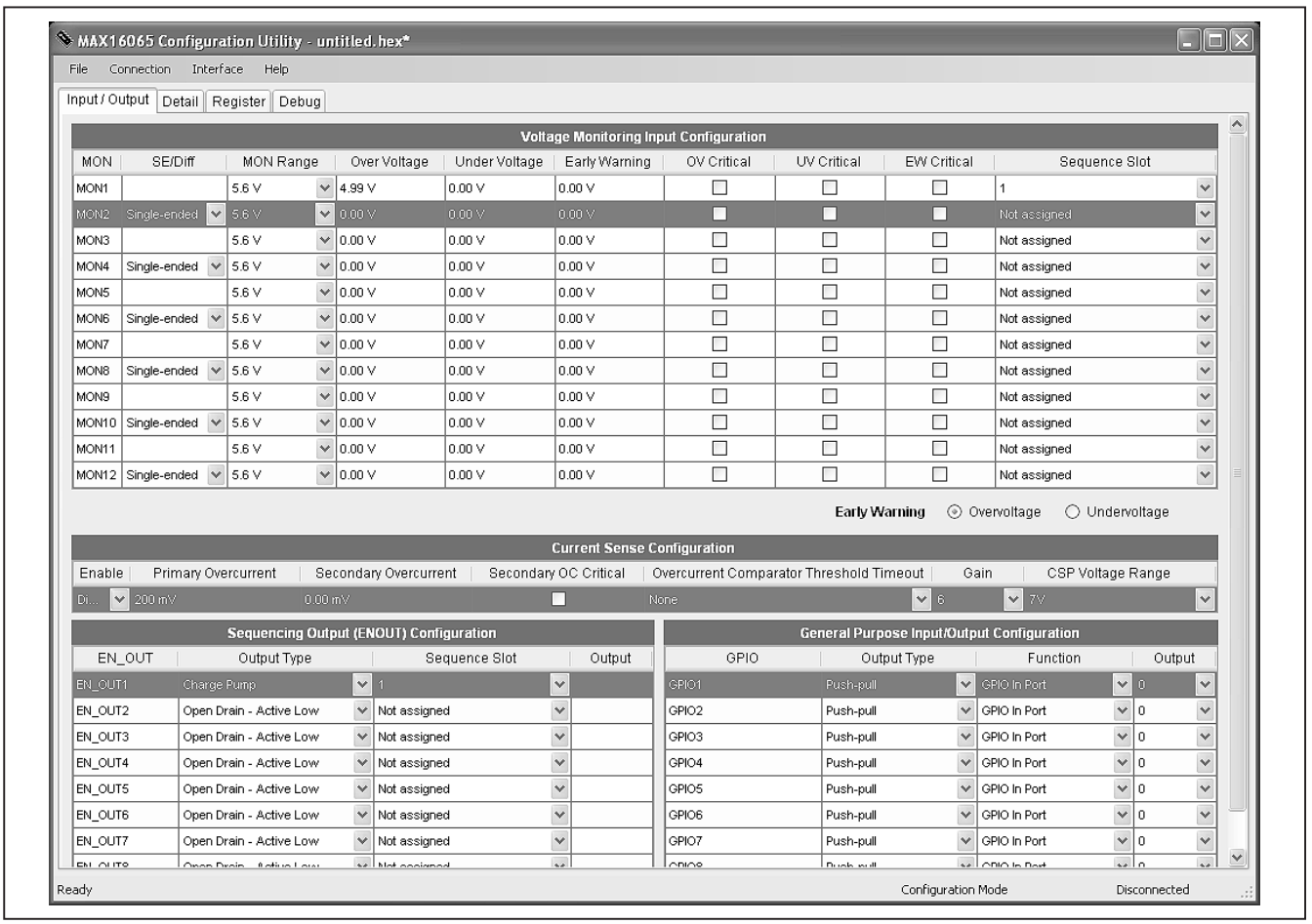

Figure 19. Graphical User Interface Screenshot

slot on different devices will not come up in the desired order even if the sequence delays are identical.

- Consider using an external µP to control the EN inputs or the software enable bits of cascaded devices, monitoring the RESET outputs as a power-good signal.
- For a large number of voltage rails, the MAX16065/MAX16066s can be cascaded hierarchically by using one master device's EN_OUT_s to control the EN inputs of several slave devices.

Controlling Power Supplies Without Using the Sequencer

A µP may control power supplies manually without involving the sequencing slot system by controlling EN_OUT_s configured as GPIO_. The output of a power supply controlled this way can be monitored using a MON_ input configured as "Monitoring Only(Primary Sequence)" or "Monitoring Only(Secondary Sequence)" (see the *Monitoring Inputs while Sequencing* section). To monitor the supply for critical faults, the µP will need to manually set the critical fault enable bit in r6Eh to r72h after turning on the EN_OUT_, and manually clear the critical fault enable bit before turning off the EN_OUT_.

Monitoring Current Using the Differential Inputs

The MAX16065/MAX16066 can monitor up to seven currents using the dedicated current-sense amplifier as well as up to six pairs of inputs configured in differential mode. The accuracy of the differential pairs is limited by the voltage range and the 10-bit conversions. Each input pair uses an odd-numbered MON_ input in combination with an even-numbered MON_ input to monitor both the voltage from the odd-numbered MON_ to ground and the voltage difference between the two MON_ inputs.

This way a single pair of inputs can monitor the voltage and the current of a power-supply rail. The overvoltage threshold on the even-numbered MON_ inputs can be used as an overcurrent flag.

Figure 20 shows how to connect a current-sense resistor to a pair of MON_ inputs for monitoring both current and voltage.

For best accuracy, set the voltage range on the even-numbered MON_ to 1.4V. Since the ADC conversion results are 10 bits, the monitoring precision is 1.4/1024 = 1.4mV. For more accurate current measurements, use larger current-sense resistors. The application requirements should determine the balance between accuracy and voltage drop across the current-sense resistor.

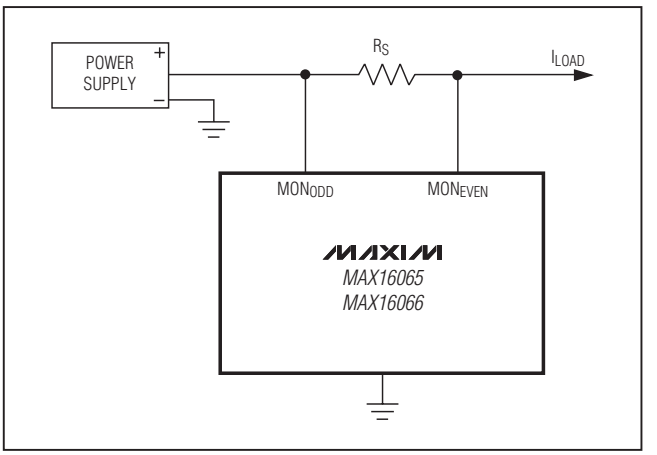

Figure 20. Current Monitoring Connection

Layout and Bypassing

Bypass DBP and ABP each with a 1µF ceramic capacitor to GND. Bypass V_{CC} with a 10µF capacitor to ground. Avoid routing digital return currents through a sensitive analog area, such as an analog supply input return path or ABP's bypass capacitor ground connection. Use dedicated analog and digital ground planes. Connect the capacitors as close as possible to the device.

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Register Map

FLASH ADDRESS	REGISTER ADDRESS	READ/ WRITE	DESCRIPTION
ADC VALUES, FAULT REGISTERS, GPIO_s AS INPUT PORTS—NOT IN FLASH			
—	000	R	MON1 ADC output, MSBs
—	001	R	MON1 ADC output, LSBs
—	002	R	MON2 ADC output, MSBs
—	003	R	MON2 ADC output, LSBs
—	004	R	MON3 ADC output, MSBs
—	005	R	MON3 ADC output, LSBs
—	006	R	MON4 ADC output, MSBs
—	007	R	MON4 ADC output, LSBs
—	008	R	MON5 ADC output, MSBs
—	009	R	MON5 ADC output, LSBs
—	00A	R	MON6 ADC output, MSBs
—	00B	R	MON6 ADC output, LSBs
—	00C	R	MON7 ADC output, MSBs
—	00D	R	MON7 ADC output, LSBs
—	00E	R	MON8 ADC output, MSBs
—	00F	R	MON8 ADC output, LSBs
—	010	R	MON9 ADC output, MSBs
—	011	R	MON9 ADC output, LSBs
—	012	R	MON10 ADC output, MSBs
—	013	R	MON10 ADC output, LSBs
—	014	R	MON11 ADC output, MSBs
—	015	R	MON11 ADC output, LSBs
—	016	R	MON12 ADC output, MSBs
—	017	R	MON12 ADC output, LSBs
—	018	R	Current-sense ADC output
—	019	R	CSP ADC output, MSBs
—	01A	R	CSP ADC output, LSBs
—	01B	R/W	Fault register—failed line flags
—	01C	R/W	Fault register—failed line flags/overcurrent
—	01D	R	Failing slot during secondary sequence
—	01E	R	GPIO data in (read only)
—	01F	R	EN_OUT_ as GPIO data in (read only)
—	020	R/W	Flash status/reset output monitor
—	021	R	Current state of the FSM

Register Map (continued)

FLASH ADDRESS	REGISTER ADDRESS	READ/ WRITE	DESCRIPTION
GPIO AND OUTPUT DEPENDENCIES/CONFIGURATIONS			
230	030	R/W	OUT configuration
231	031	R/W	OUT configuration
232	032	R/W	OUT configuration
233	033	R/W	Charge-pump configuration, bits
234	034	R/W	EN_OUT_ as GPIO data out
235	035	R/W	SMBALERT pin configuration
236	036	R/W	Fault1 dependencies
237	037	R/W	Fault1 dependencies
238	038	R/W	Fault2 dependencies
239	039	R/W	Fault2 dependencies
23A	03A	R/W	Fault1/Fault2 secondary overcurrent dependencies
23B	03B	R/W	RESET output configuration
23C	03C	R/W	RESET output dependencies
23D	03D	R/W	RESET output dependencies
23E	03E	R/W	GPIO data out
23F	03F	R/W	GPIO configuration
240	040	R/W	GPIO configuration
241	041	R/W	GPIO configuration
242	042	R/W	GPIO push-pull/open drain
ADC—CONVERSIONS			
243	043	R/W	ADCs voltage ranges—MON_ monitoring
244	044	R/W	ADCs voltage ranges—MON_ monitoring
245	045	R/W	ADCs voltage ranges—MON_ monitoring
246	046	R/W	Differential pairs enables
247	047	R/W	Current-sense gain-setting (CSP, HV, or LV)
INPUT THRESHOLDS			
248	048	R/W	MON1 secondary selectable UV/OV
249	049	R/W	MON1 primary OV
24A	04A	R/W	MON1 primary UV
24B	04B	R/W	MON2 secondary selectable UV/OV
24C	04C	R/W	MON2 primary OV
24D	04D	R/W	MON2 primary UV
24E	04E	R/W	MON3 secondary selectable UV/OV
24F	04F	R/W	MON3 primary OV
250	050	R/W	MON3 primary UV
251	051	R/W	MON4 secondary selectable UV/OV
252	052	R/W	MON4 primary OV
253	053	R/W	MON4 primary UV

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Register Map (continued)

FLASH ADDRESS	REGISTER ADDRESS	READ/ WRITE	DESCRIPTION
254	054	R/W	MON5 secondary selectable UV/OV
255	055	R/W	MON5 primary OV
256	056	R/W	MON5 primary UV
257	057	R/W	MON6 secondary selectable UV/OV
258	058	R/W	MON6 primary OV
259	059	R/W	MON6 primary UV
25A	05A	R/W	MON7 secondary selectable UV/OV
25B	05B	R/W	MON7 primary OV
25C	05C	R/W	MON7 primary UV
25D	05D	R/W	MON8 secondary selectable UV/OV
25E	05E	R/W	MON8 primary OV
25F	05F	R/W	MON8 primary UV
260	060	R/W	MON9 secondary selectable UV/OV
261	061	R/W	MON9 primary OV
262	062	R/W	MON9 primary UV
263	063	R/W	MON10 secondary selectable UV/OV
264	064	R/W	MON10 primary OV
265	065	R/W	MON10 primary UV
266	066	R/W	MON11 secondary selectable UV/OV
267	067	R/W	MON11 primary OV
268	068	R/W	MON11 primary UV
269	069	R/W	MON12 secondary selectable UV/OV
26A	06A	R/W	MON12 primary OV
26B	06B	R/W	MON12 primary UV
26C	06C	R/W	Secondary overcurrent threshold
FAULT SETUP			
26D	06D	R/W	Save after $\overline{\text{EXTFAULT}}$ fault control
26E	06E	R/W	Faults causing store in flash
26F	06F	R/W	Faults causing store in flash
270	070	R/W	Faults causing store in flash
271	071	R/W	Faults causing store in flash
272	072	R/W	Faults causing store in flash
TIMEOUTS			
273	073	R/W	Overcurrent debounce, watchdog mode, secondary threshold type, software enables
274	074	R/W	ADC fault deglitch/autoretry configuration
275	075	R/W	WDI toggle, power-up fault timer, reverse sequence
276	076	R/W	Watchdog reset output enable, watchdog timers
277	077	R/W	Sequence delay for Slot 0 and Slot 1

Register Map (continued)

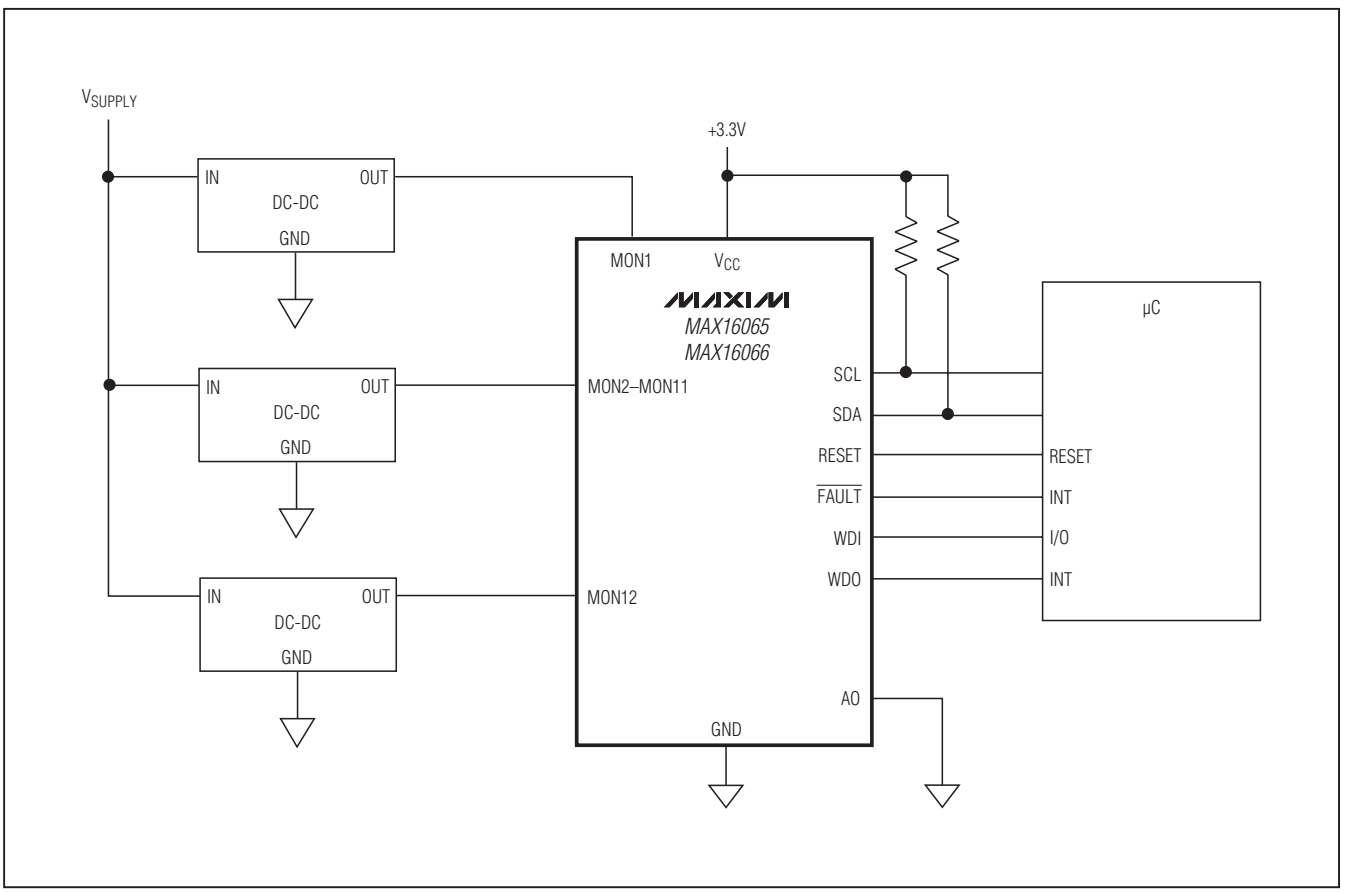
FLASH ADDRESS	REGISTER ADDRESS	READ/ WRITE	DESCRIPTION
278	078	R/W	Sequence delay for Slot 2 and Slot 3
279	079	R/W	Sequence delay for Slot 4 and Slot 5
27A	07A	R/W	Sequence delay for Slot 6 and Slot 7
27B	07B	R/W	Sequence delay for Slot 8 and Slot 9
27C	07C	R/W	Sequence delay for Slot 10 and Slot 11
27D	07D	R/W	Primary sequence final slot, sequence delay for Slot 12
MISCELLANEOUS			
27E	07E	R/W	MON1/MON2 slot assignment
27F	07F	R/W	MON3/MON4 slot assignment
280	080	R/W	MON5/MON6 slot assignment
281	081	R/W	MON7/MON8 slot assignment
282	082	R/W	MON9/MON10 slot assignment
283	083	R/W	MON11/MON12 slot assignment
284	084	R/W	EN_OUT1/EN_OUT2 slot assignment
285	085	R/W	EN_OUT3/EN_OUT4 slot assignment
286	086	R/W	EN_OUT5/EN_OUT6 slot assignment
287	087	R/W	EN_OUT7/EN_OUT8 slot assignment
288	088	R/W	EN_OUT9/EN_OUT10 slot assignment
289	089	R/W	EN_OUT11/EN_OUT12 slot assignment
28A	08A	R/W	Customer use (version)
28B	08B	R/W	PEC enable/SMBus address
28C	08C	R/W	Lock bits
28D	08D	R	Revision code
NONVOLATILE FAULT LOG			
200	—	R/W	Sequence state
201	—	R/W	Fault flags, MON1–MON8
202	—	R/W	Fault flags, MON9–MON12, OC, EXTFAULT
203	—	R/W	MON1 ADC output
204	—	R/W	MON2 ADC output
205	—	R/W	MON3 ADC output
206	—	R/W	MON4 ADC output
207	—	R/W	MON5 ADC output
208	—	R/W	MON6 ADC output
209	—	R/W	MON7 ADC output
20A	—	R/W	MON8 ADC output
20B	—	R/W	MON9 ADC output
20C	—	R/W	MON10 ADC output
20D	—	R/W	MON11ADC output
20E	—	R/W	MON12 ADC output
20F	—	R/W	Current-sense ADC output

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

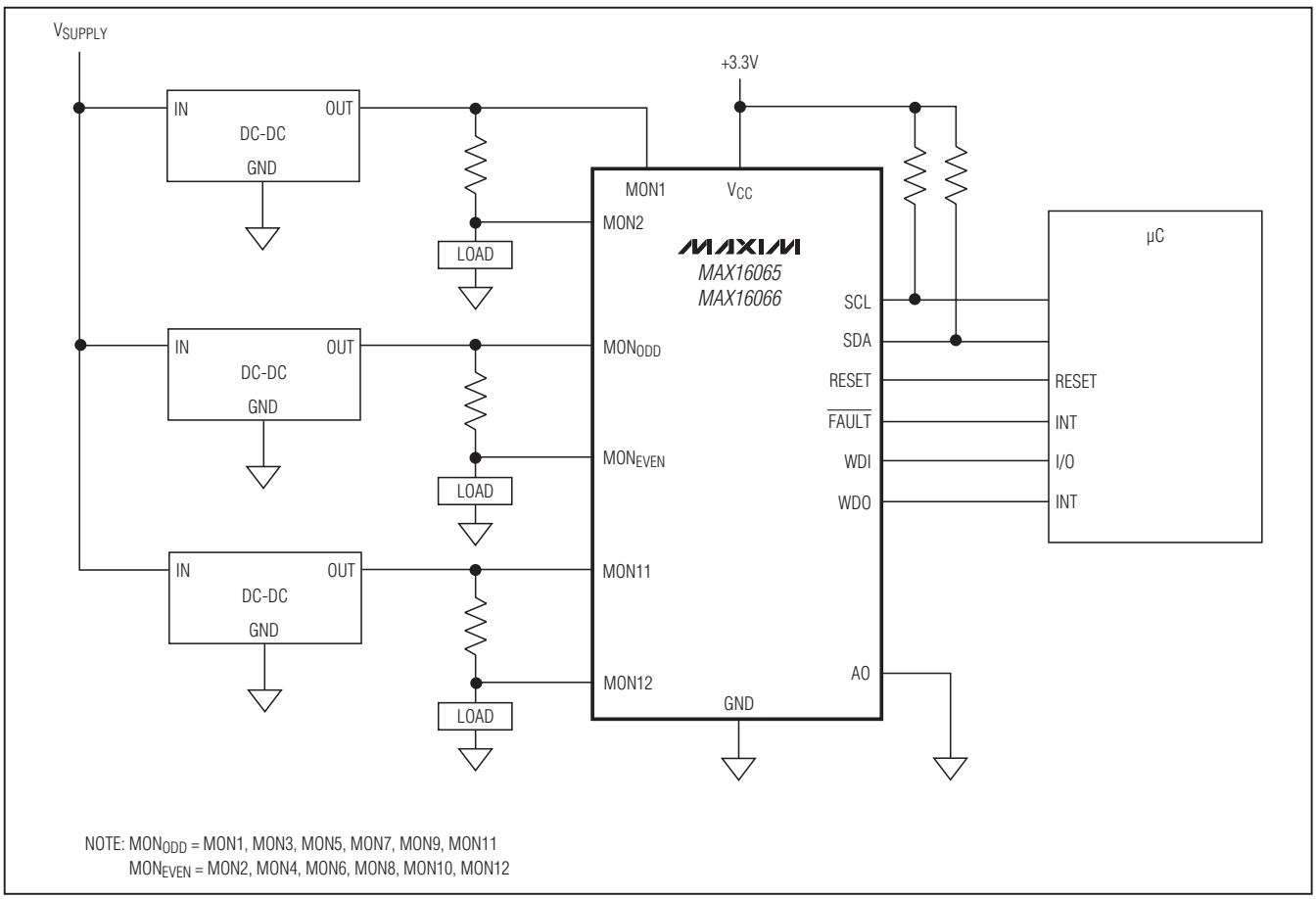
Register Map (continued)

USER FLASH			
300	39F	R/W	User flash
3A0	3AF	—	Reserved
3B0	3FF	R/W	User flash

Typical Operating Circuits



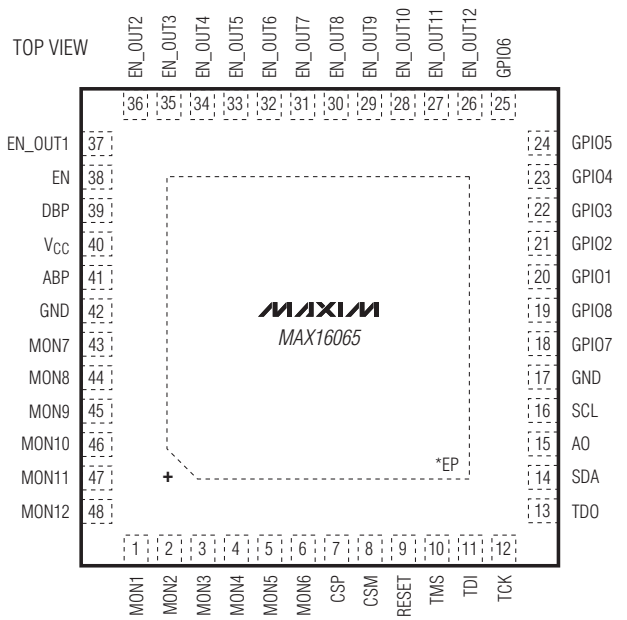
Typical Operating Circuits (continued)



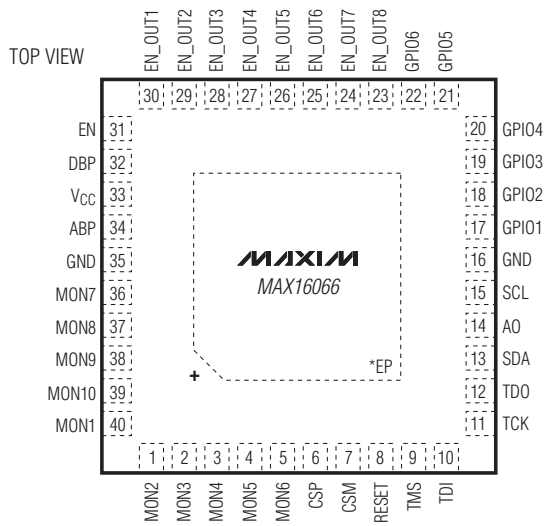
NOTE: MON_{ODD} = MON1, MON3, MON5, MON7, MON9, MON11
MON_{EVEN} = MON2, MON4, MON6, MON8, MON10, MON12

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

Pin Configurations



THIN QFN
(7mm x 7mm)



THIN QFN
(6mm x 6mm)

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 TQFN-EP*	T4877-6	21-0144
40 TQFN-EP*	T4066-5	21-0141