

LTM4632EV

Ultrathin μ Module Regulator for DDR-QDR4 Memory VDDQ, VTT and VREF

DESCRIPTION

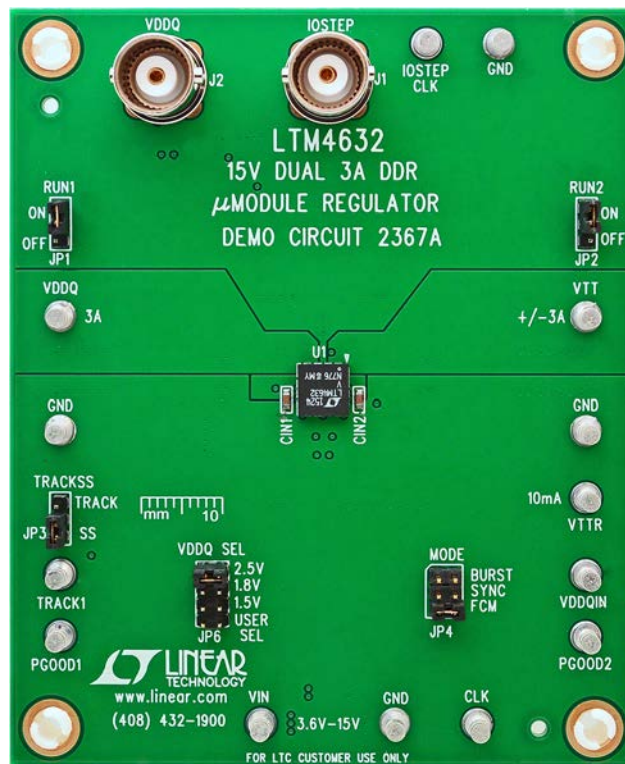
Demonstration circuit DC2367A features the [LTM[®]4632EV](#) μ Module[®] regulator, a tiny low-profile high-performance high efficiency dual step-down regulator for DDR power. LTM4632 has an operating input voltage range of 3.6V to 15V. The output voltage of channel 1 (VDDQ) is resistor programmable from 0.6V to 2.5V and is capable of delivering up to 3A of output current. The output voltage of channel 2 (VTT) is set to regulate $\frac{1}{2}$ of the voltage on the VDDQIN pin which can be provided by either the channel 1 output or an external reference voltage. It can source or sink up to 3A of output current. A 10mA buffered output of VDDQIN/2 is also provided for supplying VREF voltage for DDR memory. DC2367A also provides the option for paralleling channels 1 and 2 together for up to 6A capable VTT rail. LTM4632 is a complete DC/DC DDR dual point

of load regulator in a low-profile thermally enhanced 6.25mm \times 6.25mm \times 1.82mm LGA package requiring only a few input and output capacitors. Output voltage tracking is available through the TRACK/SS pin for supply rail sequencing. External clock synchronization is available through the SYNC/MODE pin. For high efficiency at low load currents the MODE pin jumper (JP4) selects the Burst Mode[®] option for operation in less noise sensitive applications. The LTM4632 data sheet must be read in conjunction with this demo manual for working on or modifying demo circuit 2367A.

Design files for this circuit board are available at <http://www.linear.com/demo/DC2367A>

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BOARD PHOTO



dc2367af

DEMO MANUAL DC2367A

PERFORMANCE SUMMARY Specifications are at $T_A = 25^\circ\text{C}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		3.6		15	V
Output Voltage V_{OUT1} (VDDQ)	Resistor Programmable, Jumper Selectable		1.5 ($\pm 1.5\%$) 1.8 ($\pm 1.5\%$) 2.5 ($\pm 1.5\%$)		V V V
Maximum Continuous Output Current I_{OUT1}	Derating Is Necessary for Certain Operating Conditions. See Data Sheet for Details		3		A
Output Voltage V_{OUT2} (VTT)	$V_{OUT1} = 1.5\text{V}$ $V_{OUT1} = 1.8\text{V}$ $V_{OUT1} = 2.5\text{V}$		0.75 0.9 1.25		V V V
Maximum Continuous Output Current I_{OUT2}	Derating Is Necessary for Certain Operating Conditions. See Data Sheet for Details		± 3		A
Default Operating Frequency			1		MHz
Efficiency	$V_{IN} = 12\text{V}, V_{OUT1} = 2.5\text{V}, I_{OUT} = 3\text{A}, f_{SW} = 1\text{MHz}$ $V_{IN} = 12\text{V}, V_{OUT2} = 1.25\text{V}, I_{OUT} = 3\text{A}, f_{SW} = 1\text{MHz}$		83.9 (See Figure 2) 72.3 (See Figure 3)		% %

QUICK START PROCEDURE

Demonstration circuit DC2367A is an easy way to evaluate the performance of the LTM4632. Please refer to Figure 1 for test setup connections and follow the procedure below.

1. With power off, place the jumpers in the following positions for a typical application for $2.5V_{OUT1}$ and $1.25V_{OUT2}$ rails:

JP1	JP2	JP3	JP4	JP6
RUN1	RUN2	TRACK/SS	MODE	VDDQ SEL
ON	ON	SS	CCM	2.5V

2. Before powering up the input supply and loads, preset the input voltage supply to be between 3.6V to 15V. Preset the load current for each output rail to 0A.

3. With power off, connect the loads, input voltage supply and meters as shown in Figure 1.
4. Turn on the input power supply. The output voltage meters for each output rail should display the programmed output voltage $\pm 1.5\%$.
5. Once the proper output voltages are established, adjust the load current on each rail within the 0A to 3A range and observe each output rail's load regulation, efficiency, and other parameters.
6. To observe increased light load efficiency place the mode pin jumper (JP4) in the BURST MODE position.

QUICK START PROCEDURE

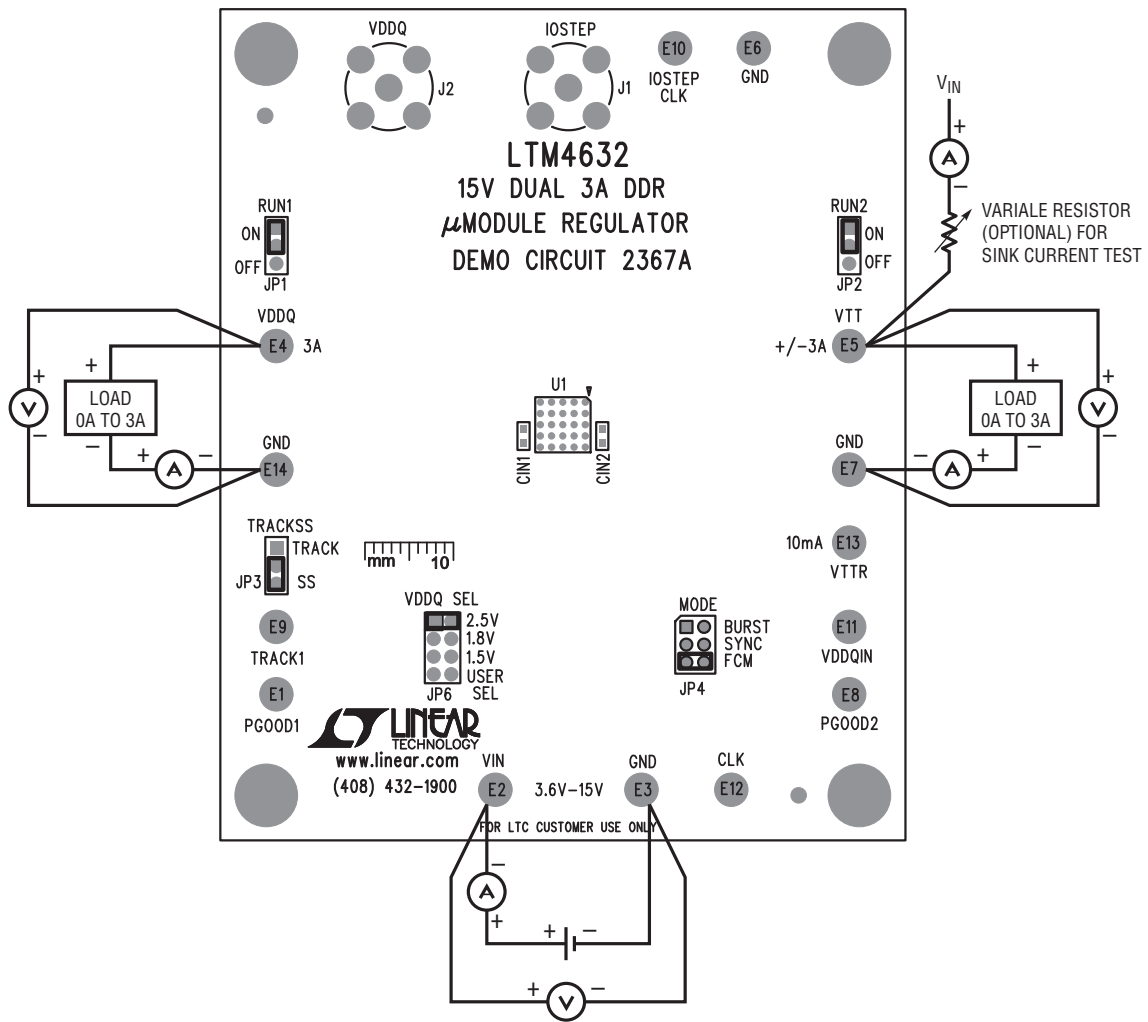


Figure 1. Test Setup

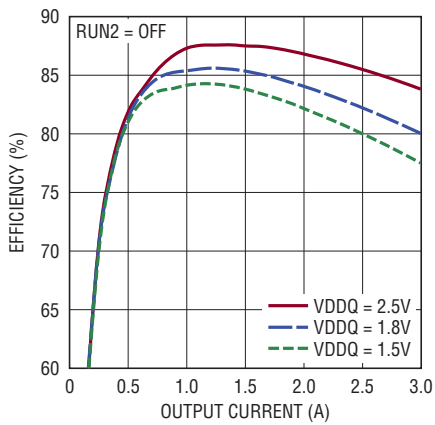


Figure 2. VDDQ 12VIN Efficiency

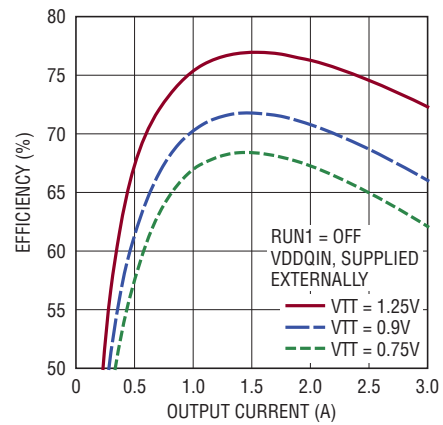


Figure 3. VTT 12VIN Efficiency

QUICK START PROCEDURE

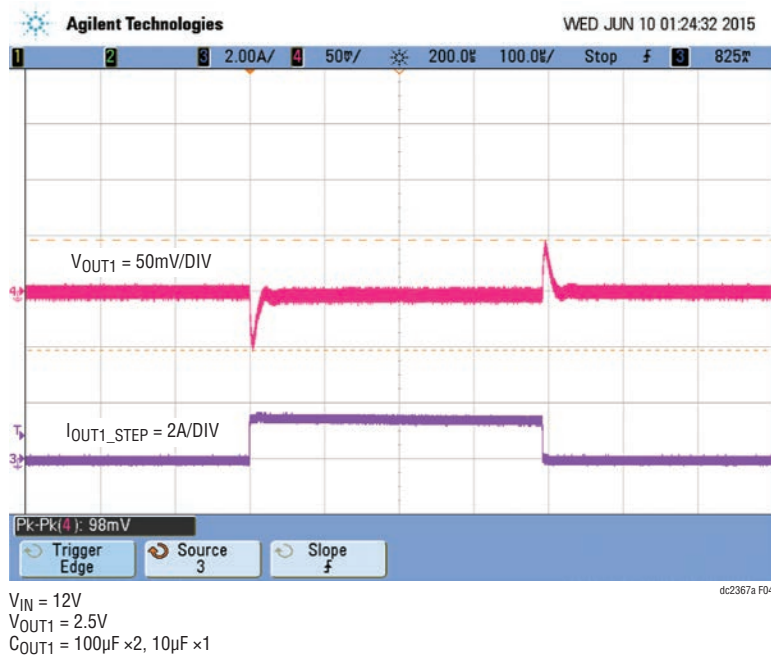


Figure 4. VDDQ Load Transient Response (0A to 1.5A Load Step)

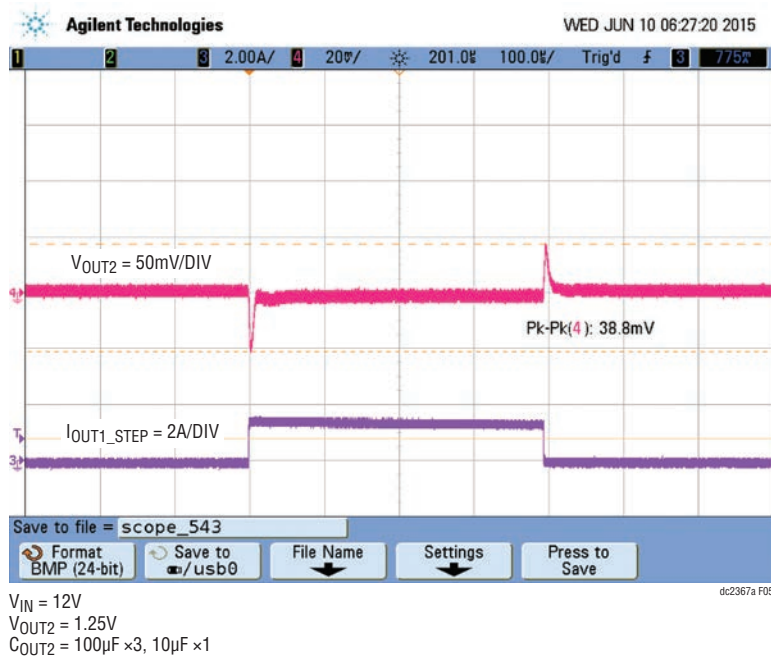
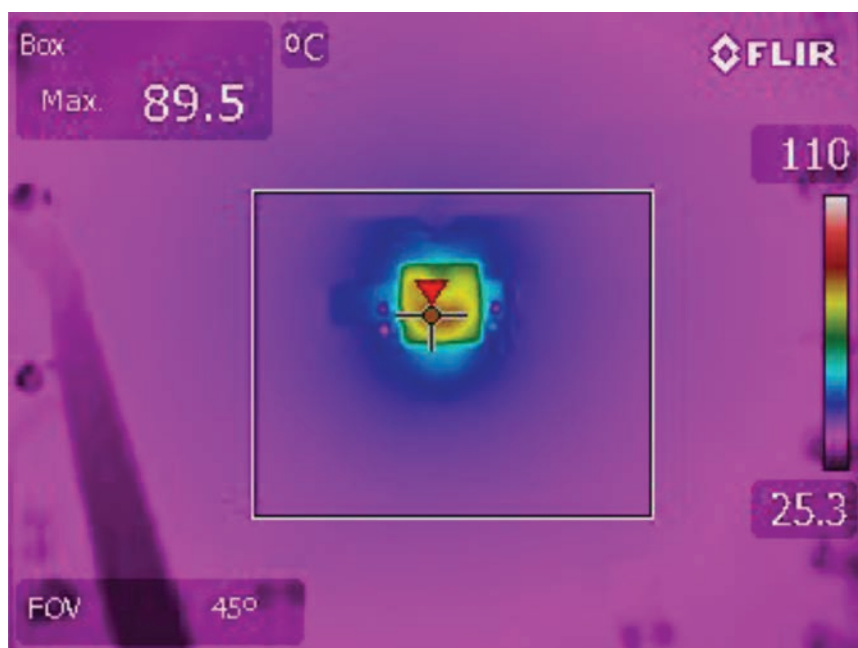


Figure 5. VTT Load Transient Response (0A to 1.5A Load Step)

QUICK START PROCEDURE



$V_{IN} = 12V$
 $V_{OUT1} = 2.5V$
 $I_{OUT1} = 3A$
 $V_{OUT2} = 1.25V$
 $I_{OUT2} = 3A$
 $f_{SW} = 1MHz$
 $T_A = 25^{\circ}C$, NO FORCED AIRFLOW

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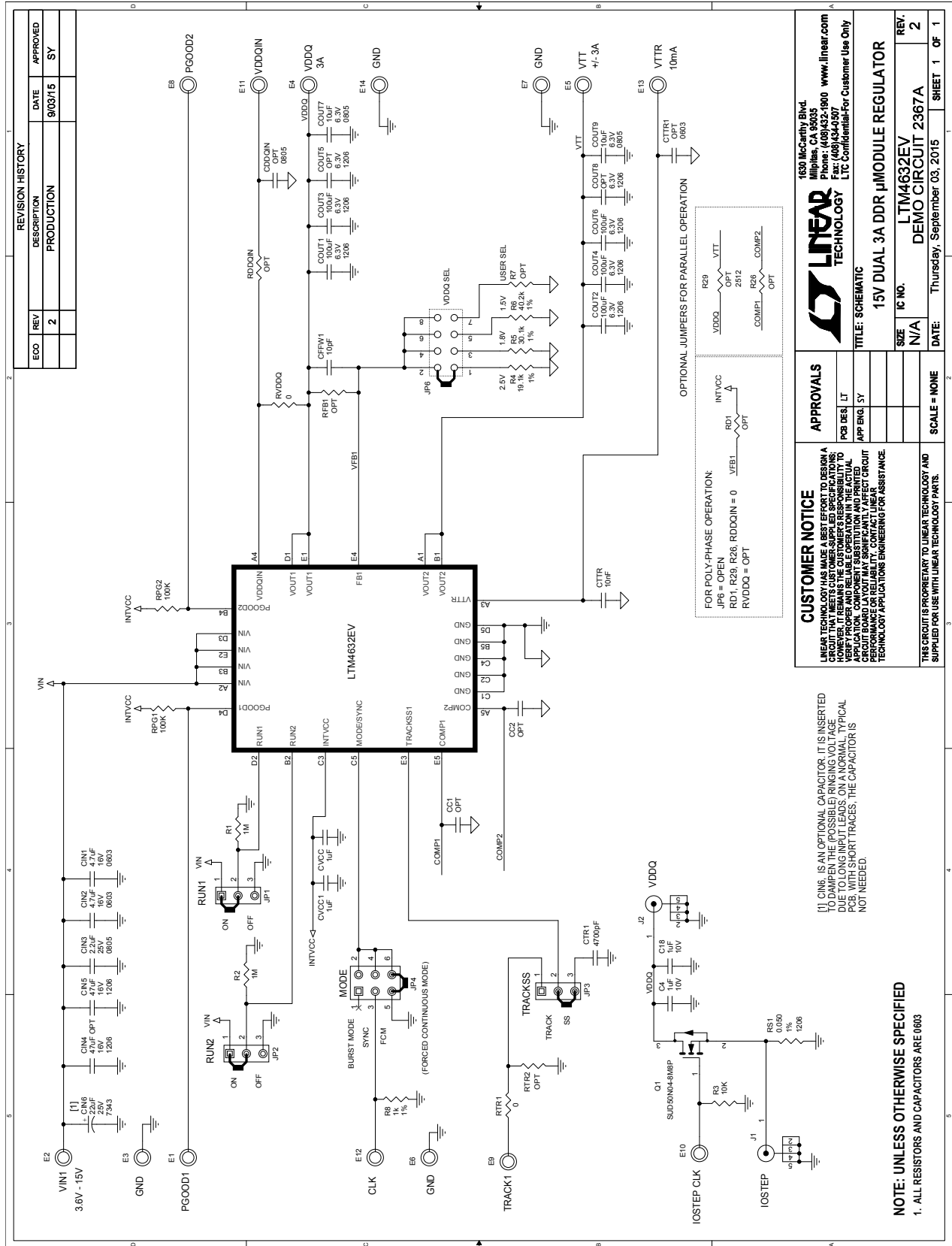
Figure 6. 12V_{IN} Full Load Thermal Capture

DEMO MANUAL DC2367A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	CIN1, CIN2	CAP, 4.7 μ F, X5R, 16V, 10%, 0603	TDK - C1608X5R1C475K080AC
2	2	COUT7, COUT9	CAP, 10 μ F, X5R, 6.3V, 10%, 0805	MURATA, GRM219R60J106KE19D
3	5	COUT1, COUT2, COUT3, COUT4, COUT6	CAP, 100 μ F, X5R, 6.3V, 20%, 1206	MURATA, GRM31CR60J107ME39L
4	1	R4	RES., 19.1k, 1/10W, 1%, 0603	VISHAY, CRCW060319K1FKEA
5	1	U1	I.C., LTM4632EV, LGA 25-6.25X6.25	LINEAR TECH., LTM4632EV#PBF
Additional Demo Board Circuit Components				
1	0	CIN4, COUT5, COUT8	CAP, OPTION, 1206	OPT
2	1	CIN5	CAP, 47 μ F, X5R, 16V, 20%, 1206	TDK, C3216X5R1C476M160AB
3	1	CIN3	CAP, 2.2 μ F, X7R, 25V, 10%, 0805	TAIYO YUDEN, TMK212B7225KGHT
4	1	CIN6	CAP, POSCAP, 22 μ F, X5R, 25V, 20%, 7343	PANASONIC, 25TQC22MV
5	4	CVCC1, C4, C18, CVCC	CAP, 1 μ F, X5R, 10V, 10%, 0603	MURATA, GRM188R61A105KA61D
6	0	CDDQIN	CAP, OPTION, 0805	OPT
7	1	CTR1	CAP, 4700pF, X7R, 50V, 10%, 0603	KEMET, C0603C472K5RACTU
8	1	CTTR	CAP, 0.01 μ F, X7R, 50V, 10%, 0603	KEMET, C0603C103K5RACTU
9	1	CFFW1	CAP, 10pF, C0G, 50V, 5%, 0603	MURATA, GRM1885C1H100JA01D
10	0	CC1, CC2, CTTR1	CAP, OPTION, 0603	OPT
11	0	RFB1, RTR2, R7, R26, RD1, RDDQIN	RES, OPTION, 0603	OPT
12	1	R5	RES., 30.1k, 1/10W, 1%, 0603	VISHAY, CRCW060330K1FKEA
13	1	R6	RES., 40.2k, 1/10W, 1%, 0603	VISHAY, CRCW060340K2FKEA
14	1	R3	RES., 10k, 1/10W, 1%, 0603	VISHAY, CRCW060310K0FKEA
15	2	RPG1, RPG2	RES., 100k, 1/10W, 1%, 0603	VISHAY, CRCW0603100KFKEA
16	1	R8	RES., 1k, 1/10W, 1%, 0603	VISHAY, CRCW06031K00FKEA
17	2	R1, R2	RES., 1M, 1/10W, 1%, 0603	VISHAY, CRCW06031M00FKEA
18	2	RTR1, RVDDQ	RES., 0 Ω , 1/10W, 0603	VISHAY, CRCW06030000Z0EA
19	1	RS1	RES., 0.05 Ω , 1/4W, 1%, 1206	VISHAY, WSL1206R0500FEA
20	0	R29	RES, OPTION, 2512	OPT
21	1	Q1	XSTR., MOSFET, N-CH, 40V, 14A, TO-252	VISHAY, SUD50N04-8M8P-4GE3
Hardware: For Demo Board Only				
1	14	E1-E14	TESTPOINT, TURRET, 0.094" MTG. HOLE	MILL-MAX, 2501-2-00-80-00-00-07-0
2	3	JP1, JP2, JP3	CONN., HEADER, 1X3, 2mm	SULLINS, NRPNO31PAEN-RC
3	1	JP4	CONN., HEADER, 2X3, 2mm	SULLINS, NRPNO32PAEN-RC
4	1	JP6	CONN., HEADER, 2X4, 2mm	SULLINS, NRPNO42PAEN-RC
5	5	XJP1, XJP2, XJP3, XJP4, XJP6	SHUNT, 2mm	SAMTEC 2SN-BK-G
6	2	J1, J2	CONN, BNC, 5PINS	CONNEX, 112404
7	4	STAND OFF	STAND OFF, NYLON, SNAP-ON, 0.375"	KEYSTONE_8832

SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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