LTM4603/LTM4603-1

6A DC/DC µModule with PLL, Output Tracking and Margining

FEATURES

- **Complete Switch Mode Power Supply**
- **Wide Input Voltage Range: 4.5V to 20V**
- **6A DC Typical, 8A Peak Output Current**
- **0.6V to 5V Output Voltage**
- **Output Voltage Tracking and Margining**
- **Remote Sensing for Precision Regulation (LTM4603 Only)**
- **Typical Operating Frequency: 1MHz**
- **PLL Frequency Synchronization**
- **1.5% Regulation**
- **Current Foldback Protection (Disabled at Start-Up)**
- Pin Compatible with the LTM4601
- Pb-Free (e4) RoHS Compliant Package with Gold Finish Pads
- Ultrafast Transient Response
- Current Mode Control
- Up to 93% Efficiency at $5V_{IN}$, $3.3V_{OUT}$
- Programmable Soft-Start
- Output Overvoltage Protection
- Small Footprint, Low Profile (15mm × 15mm × 2.8mm) Surface Mount LGA Package

APPLICATIONS

- Telecom and Networking Equipment
- Servers
- Industrial Equipment
- Point of Load Regulation

DESCRIPTION

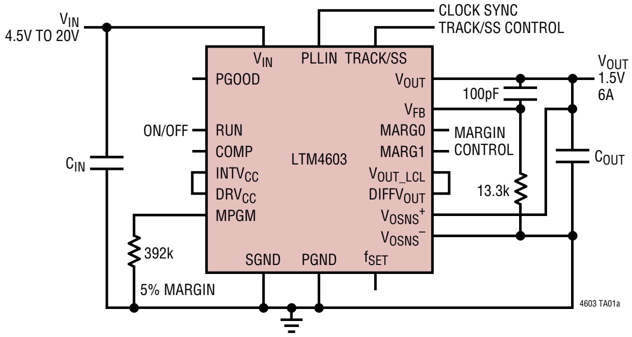
The LTM®4603 is a complete 6A step-down switch mode DC/DC power supply with onboard switching controller, MOSFETs, inductor and all support components. The µModule™ is housed in a small surface mount 15mm × 15mm × 2.8mm LGA package. Operating over an input voltage range of 4.5 to 20V, the LTM4603 supports an output voltage range of 0.6V to 5V as well as output voltage tracking and margining. The high efficiency design delivers 6A continuous current (8A peak). Only bulk input and output capacitors are needed to complete the design.

The low profile (2.8mm) and light weight (1.73g) package easily mounts on the unused space on the back side of PC boards for high density point of load regulation. The µModule can be synchronized with an external clock for reducing undesirable frequency harmonics and allows PolyPhase® operation for high load currents.

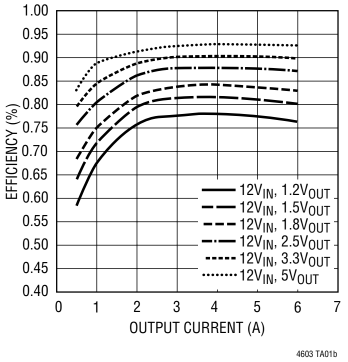
A high switching frequency and adaptive on-time current mode architecture deliver a very fast transient response to line and load changes without sacrificing stability. An onboard remote sense amplifier can be used to accurately regulate an output voltage independent of load current. The onboard remote sense amplifier is not available in the LTM4603-1. The LTM4603/LTM4603-1 are pin compatible with the 12A LTM4601/LTM4601-1.

TYPICAL APPLICATION

1.5V/6A Power Supply with 4.5V to 20V Input



Efficiency vs Load Current with $12V_{IN}$

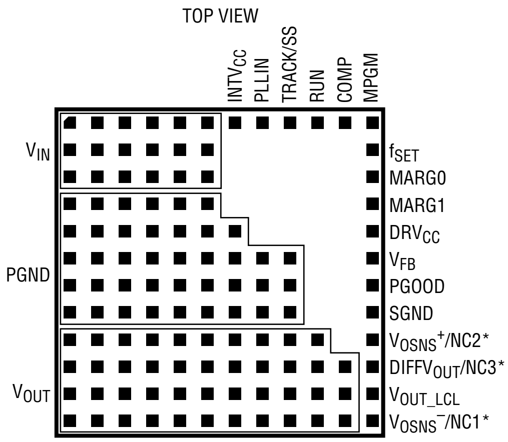


ABSOLUTE MAXIMUM RATINGS

(Note 1)

$INTV_{CC}$, DRV_{CC}, V_{OUT_LCL}, V_{OUT} ($V_{OUT} \leq 3.3V$ with Remote Sense Amp) .... –0.3V to 6V
PLLIN, TRACK/SS, MPGM, MARG0, MARG1, PGOOD, f_{SET} .... –0.3V to $INTV_{CC}$ + 0.3V
RUN .... –0.3V to 5V
V_{FB}, COMP .... –0.3V to 2.7V
V_{IN} .... –0.3V to 20V
V_{OSNS}^+, V_{OSNS}^- .... 0V to $INTV_{CC}$ – 1V
Operating Temperature Range (Note 2) ... –40°C to 85°C
Junction Temperature .... 125°C
Storage Temperature Range.................... –55°C to 125°C

PACKAGE/ORDER INFORMATION



LGA PACKAGE
118-LEAD (15mm × 15mm × 2.8mm)
T_{JMAX} = 125°C, θ_{JA} = 15°C/W, θ_{JC} = 6°C/W,
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS, WEIGHT = 1.7g
*LTM4603-1 Only

ORDER PART NUMBER	LGA PART MARKING*
LTM4603EV#PBF	LTM4603V
LTM4603IV#PBF	LTM4603V
LTM4603EV-1#PBF	LTM4603V-1
LTM4603IV-1#PBF	LTM4603V-1

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 85°C temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	4.5		20	V
$V_{OUT(DC)}$	Output Voltage	C_{IN} = 10µF ×2, C_{OUT} = 2×, 100µF/X5R/ Ceramic V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 0A V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A	 ● ●	 1.478 1.478	 1.5 1.5	 1.522 1.522	 V V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	I_{OUT} = 0A			3.2	4	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Startup	I_{OUT} = 0A. V_{OUT} = 1.5V V_{IN} = 5V V_{IN} = 12V			 0.6 0.7		 A A
$I_{Q(VIN,NOLOAD)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, No Switching V_{IN} = 12V, V_{OUT} = 1.5V, Switching Continuous V_{IN} = 5V, V_{OUT} = 1.5V, No Switching V_{IN} = 5V, V_{OUT} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			3.8 25 2.5 43 22		mA mA mA mA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 85°C temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 6A V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 6A V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 6A			0.85 1.78 2.034		A A A
$INTV_{CC}$	V_{IN} = 12V, RUN > 2V	No Load		4.7	5	5.3	V
Output Specifications							
I_{OUTDC}	Output Continuous Current Range (See Output Current Derating Curves for Different V_{IN}, V_{OUT} and T_A)	V_{IN} = 12V, V_{OUT} = 1.5V		0		6	A
$\frac{V_{OUT(NOM)} - V_{OUT(\Delta LINE)}}{V_{OUT(NOM)}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} = 4.5V to 20V	●			0.3	%
$\frac{V_{OUT(NOM)} - V_{OUT(\Delta LOAD)}}{V_{OUT(NOM)}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 6A V_{IN} = 12V, with Remote Sense Amp V_{IN} = 12V, LTM4603-1	 ● ●			 0.25 0.5	 % %
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 2×, 100µF/X5R/Ceramic V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			 10 10		 mV_{P-P} mV_{P-P}
f_S	Output Ripple Voltage Frequency	I_{OUT} = 3A, V_{IN} = 12V, V_{OUT} = 1.5V			1000		kHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot, TRACK/SS = 10nF	C_{OUT} = 2×, 100µF/X5R/Ceramic, V_{OUT} = 1.5V, I_{OUT} = 0A V_{IN} = 12V V_{IN} = 5V			 20 20		 mV mV
t_{START}	Turn-On Time, TRACK/SS = Open	C_{OUT} = 2×, 100µF/X5R/Ceramic, V_{OUT} = 1.5V, I_{OUT} = 1A Resisitive Load V_{IN} = 12V V_{IN} = 5V			 0.5 0.7		 ms ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 2 × 22µF/Ceramic, 470µF, 4V Sanyo POSCAP V_{IN} = 12V V_{IN} = 5V			 35 35		 mV mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 10% of Full Load V_{IN} = 12V			 25		 µs
I_{OUTPK}	Output Current Limit	C_{OUT} = 2×, 100µF/X5R/Ceramic V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			 8 8		 A A
Remote Sense Amp (LTM4603 Only, Not Supported in the LTM4603-1) (Note 3)							
V_{OSNS}^+, V_{OSNS}^- CM Range	Common Mode Input Voltage Range	V_{IN} = 12V, RUN > 2V		0		$INTV_{CC}$ – 1	V
$DIFFV_{OUT}$ Range	Output Voltage Range	V_{IN} = 12V, DIFF OUT Load = 100k		0		$INTV_{CC}$	V
V_{OS}	Input Offset Voltage Magnitude					1.25	mV
AV	Differential Gain				1		V/V
GBP	Gain Bandwidth Product				3		MHz
SR	Slew Rate				2		V/µs
R_{IN}	Input Resistance	V_{OSNS}^+ to GND			20		kΩ
CMRR	Common Mode Rejection Ratio				100		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 85°C temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Stage							
V_{FB}	Error Amplifier Input Voltage Accuracy	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.594	0.6	0.606	V
V_{RUN}	RUN Pin On/Off Threshold			1	1.5	1.9	V
$I_{SS/TRACK}$	Soft-Start Charging Current	$V_{SS/TRACK}$ = 0V		–1	–1.5	–2	µA
$t_{ON(MIN)}$	Minimum On Time	(Note 4)			50	100	ns
$t_{OFF(MIN)}$	Minimum Off Time	(Note 4)			250	400	ns
R_{PLLIN}	PLLIN Input Resistance				50		kΩ
I_{DRVCC}	Current into DRV_{CC} Pin	V_{OUT} = 1.5V, I_{OUT} = 1A, Frequency = 1MHz, DRV_{CC} = 5V			18	25	mA
R_{FBHI}	Resistor Between V_{OUT} and V_{FB}			60.098	60.4	60.702	kΩ
V_{MPGM}	Margin Reference Voltage				1.18		V
V_{MARG0}, V_{MARG1}	MARG0, MARG1 Voltage Thresholds				1.4		V
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		7	10	13	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–7	–10	–13	%
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			1.5	3	%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

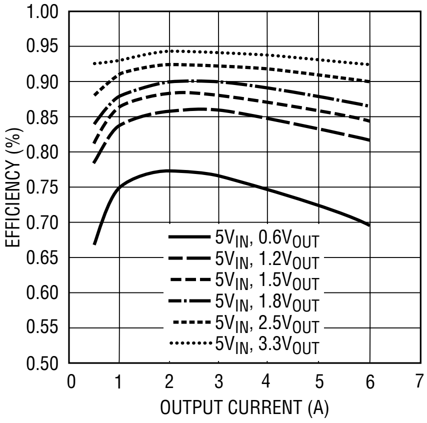
Note 2: The LTM4603E/LTM4603-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4603E/LTM4603-1 are guaranteed and tested over the –40°C to 85°C temperature range.

Note 3: Remote sense amplifier recommended for ≤3.3V output.

Note 4: 100% tested at wafer level only.

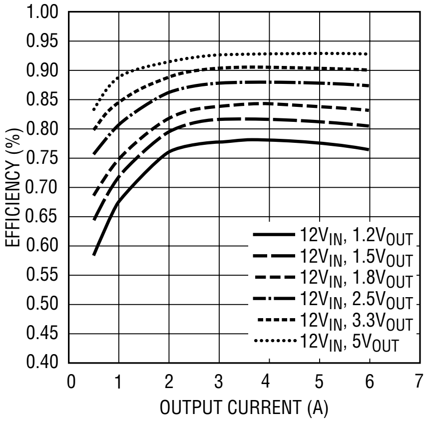
TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 18 for all curves)

Efficiency vs Load Current with $5V_{IN}$



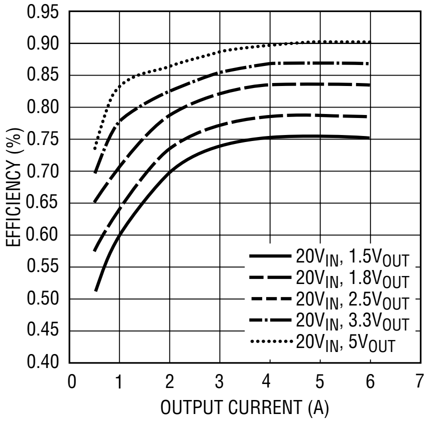
4603 G01

Efficiency vs Load Current with $12V_{IN}$



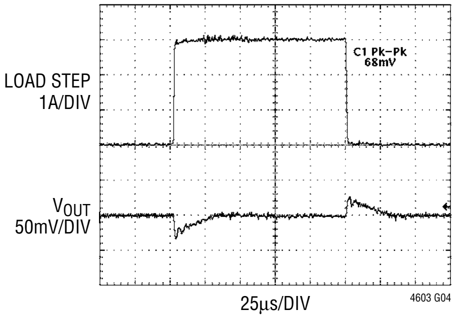
4603 G02

Efficiency vs Load Current with $20V_{IN}$



4603 G03

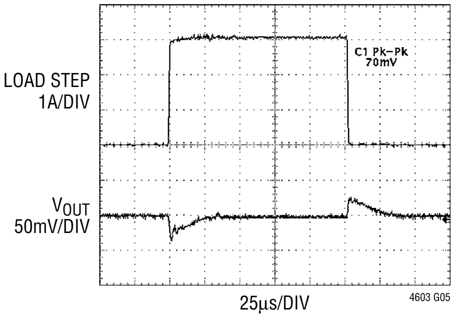
1.2V Transient Response



4603 G04

1.2V AT 3A/µs LOAD STEP
C_{OUT}: 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP

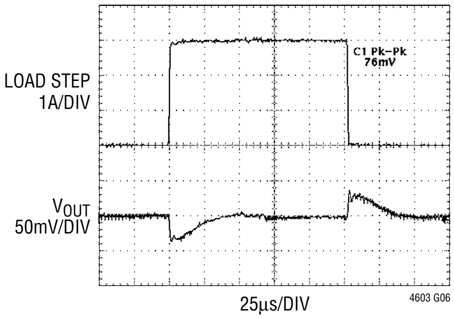
1.5V Transient Response



4603 G05

1.5V AT 3A/µs LOAD STEP
C_{OUT}: 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP

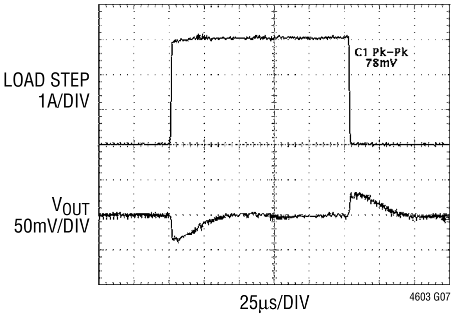
1.8V Transient Response



4603 G06

1.8V AT 3A/µs LOAD STEP
C_{OUT}: 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP

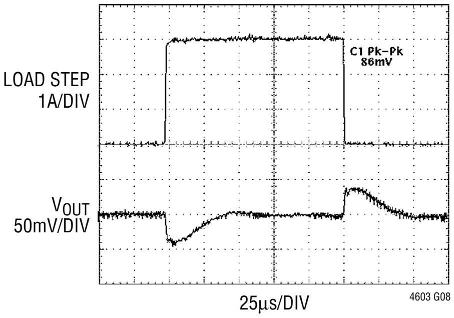
2.5V Transient Response



4603 G07

2.5V AT 3A/µs LOAD STEP
C_{OUT}: 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP

3.3V Transient Response

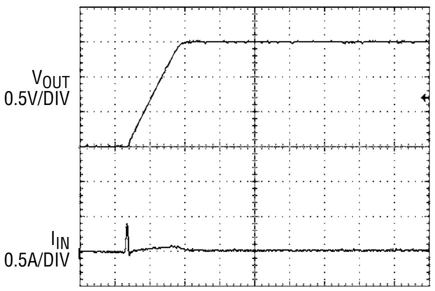


4603 G08

3.3V AT 3A/µs LOAD STEP
C_{OUT}: 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP

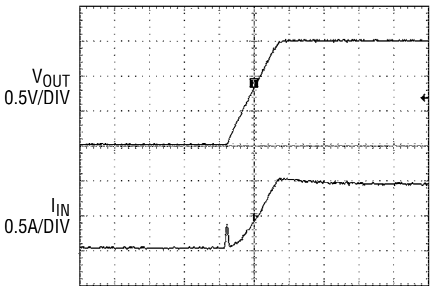
TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 18 for all curves)

Start-Up, I_{OUT} = 0A



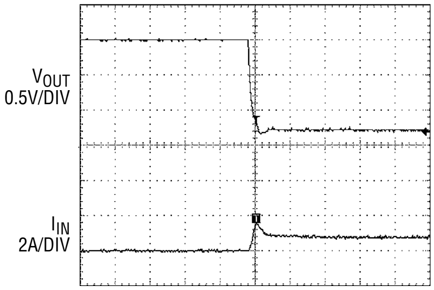
V_{IN} = 12V 1ms/DIV
V_{OUT} = 1.5V
C_{OUT} = 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP
SOFT-START = 3.9nF

Start-Up, I_{OUT} = 6A (Resistive Load)



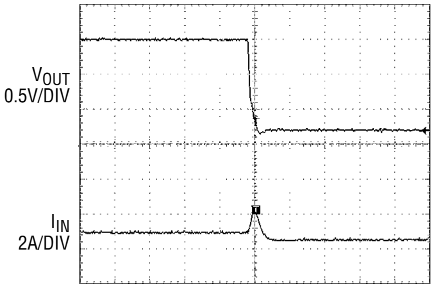
V_{IN} = 12V 1ms/DIV
V_{OUT} = 1.5V
C_{OUT} = 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP
SOFT-START = 3.9nF

Short-Circuit Protection, I_{OUT} = 0A



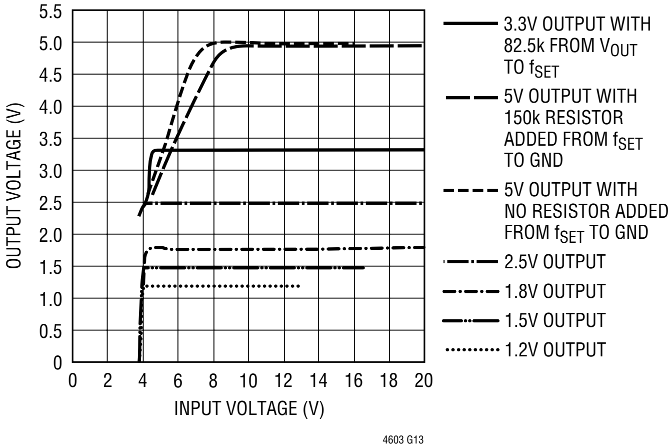
V_{IN} = 12V 100µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP
SOFT-START = 3.9nF

Short-Circuit Protection, I_{OUT} = 6A



V_{IN} = 12V 100µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 1x 22µF, 6.3V CERAMIC
1x 330µF, 4V SANYO POSCAP
SOFT-START = 3.9nF

V_{IN} to V_{OUT} Step-Down Ratio



PIN FUNCTIONS (See Package Description for Pin Assignment)

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

V_{OUT} (Bank 3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing output decoupling capacitance directly between these pins and PGND pins. Review the figure below.

PGND (Bank 2): Power ground pins for both input and output returns.

V_{OSNS}^- (Pin M12): (–) Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.3V$.

NC1 (Pin M12): No Connect on the LTM4603-1.

V_{OSNS}^+ (Pin J12): (+) Input to the Remote Sense Amplifier. This pin connects to the output remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.3V$.

NC2 (Pin J12): No Connect on the LTM4603-1.

$DIFFV_{OUT}$ (Pin K12): Output of the Remote Sense Amplifier. This pin connects to the V_{OUT_LCL} pin.

NC3 (Pin K12): No Connect on the LTM4603-1.

DRV_{CC} (Pin E12): This pin normally connects to $INTV_{CC}$ for powering the internal MOSFET drivers. This pin can be biased up to 6V from an external supply with about 50mA capability, or an external circuit shown in Figure 16. This improves efficiency at the higher input voltages by reducing power dissipation in the modules.

$INTV_{CC}$ (Pin A7): This pin is for additional decoupling of the 5V internal regulator.

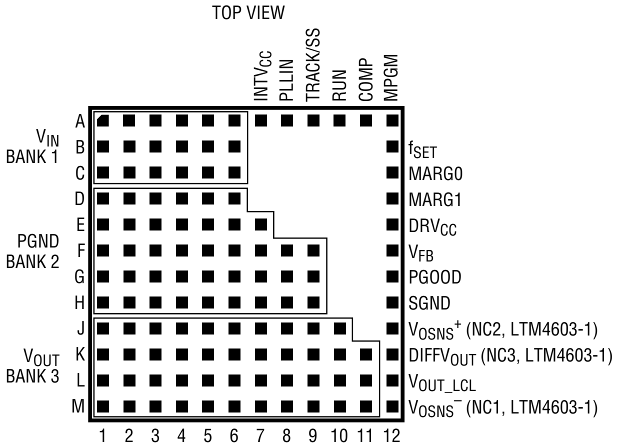
PLLIN (Pin A8): External Clock Synchronization Input to the Phase Detector. This pin is internally terminated to SGND with a 50k resistor. Apply a clock above 2V and below $INTV_{CC}$. See Applications Information.

TRACK/SS (Pin A9): Output Voltage Tracking and Soft-Start Pin. When the module is configured as a master output, then a soft-start capacitor is placed on this pin to ground to control the master ramp rate. A soft-start capacitor can be used for soft-start turn on as a stand alone regulator. Slave operation is performed by putting a resistor divider from the master output to the ground, and connecting the center point of the divider to this pin. See Applications Information.

MPGM (Pin A12): Programmable Margining Input. A resistor from this pin to ground sets a current that is equal to 1.18V/R. This current multiplied by 10kΩ will equal a value in millivolts that is a percentage of the 0.6V reference voltage. See Applications Information. To parallel LTM4603s, each requires an individual MPGM resistor. Do not tie MPGM pins together.

f_{SET} (Pin B12): Frequency Set Internally to 1MHz. An external resistor can be placed from this pin to ground to increase frequency. This pin can be decoupled with a 1000pF capacitor. See Applications Information for frequency adjustment.

V_{FB} (Pin F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT_LCL} with a 60.4k precision resistor. Different output voltages can be



PIN FUNCTIONS (See Package Description for Pin Assignment)

programmed with an additional resistor between V_{FB} and SGND pins. See Applications Information.

MARG0 (Pin C12): This pin is the LSB logic input for the margining function. Together with the MARG1 pin will determine if margin high, margin low or no margin state is applied. The pin has an internal pull-down resistor of 50k. See Applications Information.

MARG1 (Pin D12): This pin is the MSB logic input for the margining function. Together with the MARG0 pin will determine if margin high, margin low or no margin state is applied. The pin has an internal pull-down resistor of 50k. See Applications Information.

SGND (Pin H12): Signal Ground. This pin connects to PGND at output capacitor point.

COMP (Pin A11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.7V corresponding to zero sense voltage (zero current).

PGOOD (Pin G12): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point, after a 25µs power bad mask timer expires.

RUN (Pin A10): Run Control Pin. A voltage above 1.9V will turn on the module, and when below 1.9V, will turn off the module. A programmable UVLO function can be accomplished with a resistor from V_{IN} to this pin that has a 5.1V zener to ground. Maximum pin voltage is 5V.

V_{OUT_LCL} (Pin L12): V_{OUT} connects directly to this pin to bypass the remote sense amplifier, or $DIFFV_{OUT}$ connects to this pin when remote sense amplifier is used. V_{OUT_LCL} can be connected to V_{OUT} on the LTM4603-1. V_{OUT} is internally connected to V_{OUT_LCL} through 50Ω in the LTM4603-1.

SIMPLIFIED BLOCK DIAGRAM

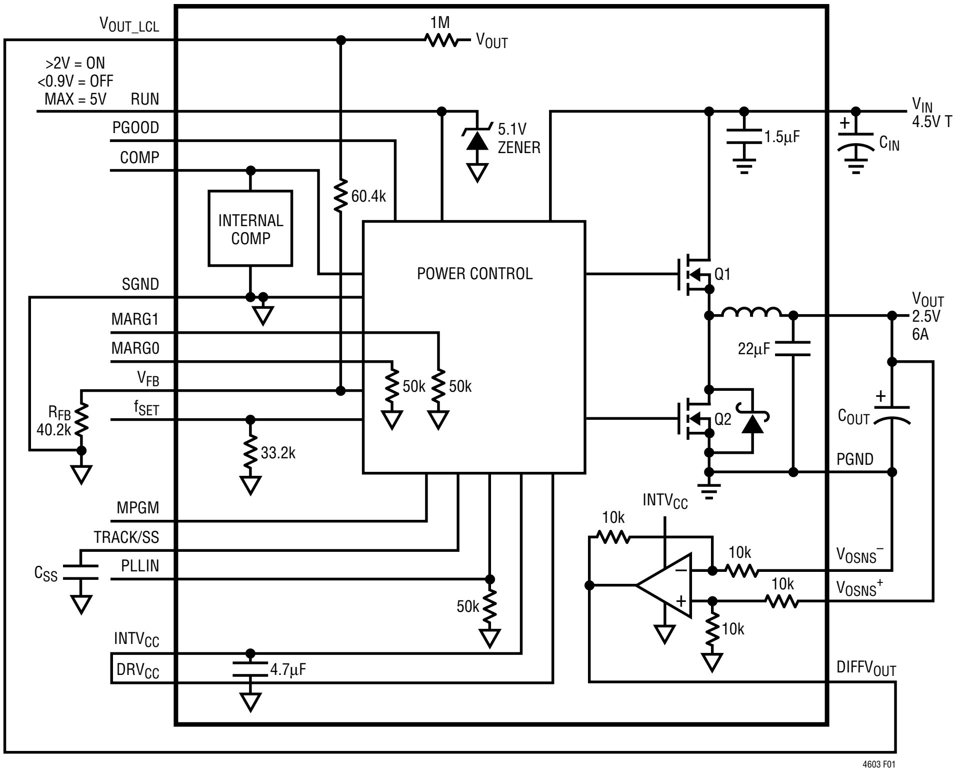


Figure 1. Simplified LTM4603/LTM4603-1 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C, V_{IN} = 12V. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 6A		20			μF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 6A		100	200		μF

OPERATION

Power Module Description

The LTM4603 is a standalone nonisolated switching mode DC/DC power supply. It can deliver up to 6A of DC output current with few external input and output capacitors. This module provides precisely regulated output voltage programmable via one external resistor from 0.6V_{DC} to 5.0V_{DC} over a 4.5V to 20V wide input voltage. The typical application schematic is shown in Figure 18.

The LTM4603 has an integrated constant on-time current mode regulator, ultralow $R_{DS(ON)}$ FETs with fast switching speed and integrated Schottky diodes. The typical switching frequency is 1MHz at full load. With current mode control and internal feedback loop compensation, the LTM4603 module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit. Besides, foldback current limiting is provided in an overcurrent condition while V_{FB} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET Q1 is turned off and bottom FET Q2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN pin below 1V forces the controller into its shutdown state, turning off both Q1 and Q2. At low load current, the module works in continuous current mode by default to achieve minimum output voltage ripple.

When DRV_{CC} pin is connected to $INTV_{CC}$ an integrated 5V linear regulator powers the internal gate drivers. If a 5V external bias supply is applied on the DRV_{CC} pin, then an efficiency improvement will occur due to the reduced power loss in the internal linear regulator. This is especially true at the higher input voltage range.

The LTM4603 has a very accurate differential remote sense amplifier with very low offset. This provides for very accurate remote sense voltage measurement. The MPGM pin, MARG0 pin and MARG1 pin are used to support voltage margining, where the percentage of margin is programmed by the MPGM pin, and the MARG0 and MARG1 select margining.

The PLLIN pin provides frequency synchronization of the device to an external clock. The TRACK/SS pin is used for power supply tracking and soft-start programming.

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The typical LTM4603 application circuit is shown in Figure 18. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 2 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step down ratio that can be achieved for a given input voltage. These constraints are shown in the Typical Performance Characteristics curves labeled V_{IN} to V_{OUT} Step-Down Ratio. Note that additional thermal derating may apply. See the Thermal Considerations and Output Current Derating section of this data sheet.

Output Voltage Programming and Margining

The PWM controller has an internal 0.6V reference voltage. As shown in the Block Diagram, a 1M and a 60.4k 0.5% internal feedback resistor connects V_{OUT} and FB pins together. The V_{OUT_LCL} pin is connected between the 1M and the 60.4k resistor. The 1M resistor is used to protect against an output overvoltage condition if the V_{OUT_LCL} pin is not connected to the output, or if the remote sense amplifier output is not connected to V_{OUT_LCL}. The output voltage will default to 0.6V. Adding a resistor R_{SET} from the FB pin to SGND pin programs the output voltage:

$$V_{OUT} = 0.6V\frac{60.4k + R_{SET}}{R_{SET}}$$

Table 1. Standard 1% Resistor Values

R_{SET} (kΩ)	Open	60.4	40.2	30.1	25.5	19.1	13.3	8.25
V_{OUT} (V)	0.6	1.2	1.5	1.8	2	2.5	3.3	5

The MPGM pin programs a current that when multiplied by an internal 10k resistor sets up the 0.6V reference ± offset for margining. A 1.18V reference divided by the RPGM resistor on the MPGM pin programs the current. Calculate $V_{OUT(MARGIN)}$:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \bullet V_{OUT}$$

where $\%V_{OUT}$ is the percentage of V_{OUT} you want to margin, and $V_{OUT(MARGIN)}$ is the margin quantity in volts:

$$R_{PGM} = \frac{V_{OUT}}{0.6V} \bullet \frac{1.18V}{V_{OUT(MARGIN)}} \bullet 10k$$

where RPGM is the resistor value to place on the MPGM pin to ground.

The output margining will be ± margining of the value. This is controlled by the MARG0 and MARG1 pins. See the truth table below:

MARG0	MARG1	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

Input Capacitors

LTM4603 module should be connected to a low AC impedance DC source. Input capacitors are required to be placed adjacent to the module. In Figure 18, the 10µF ceramic input capacitors are selected for their ability to handle the large RMS current into the converter. An input bulk capacitor of 100µF is optional. This 100µF capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1 - D)}$$

In the above equation, η% is the estimated efficiency of the power module. C_{IN} can be a switcher-rated electrolytic aluminum capacitor, OS-CON capacitor or high volume ceramic capacitor. Note the capacitor ripple current ratings are often based on temperature and hours of life. This makes it advisable to properly derate the input capacitor,

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or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

In Figure 18, the 10µF ceramic capacitors are together used as a high frequency input decoupling capacitor. In a typical 6A output application, two very low ESR, X5R or X7R, 10µF ceramic capacitors are recommended. These decoupling capacitors should be placed directly adjacent to the module input pins in the PCB layout to minimize the trace inductance and high frequency AC noise. Each 10µF ceramic is typically good for 2A to 3A of RMS ripple current. Refer to your ceramics capacitor catalog for the RMS current ratings.

Multiphase operation with multiple LTM4603 devices in parallel will lower the effective input RMS ripple current due to the interleaving operation of the regulators. Application Note 77 provides a detailed explanation. Refer to Figure 2 for the input capacitor ripple current requirement as a function of the number of phases. The figure provides a ratio of RMS ripple current to DC load current as a function of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to arrive at the correct ripple current value. For example, the 2-phase parallel LTM4603 design provides 10A at 2.5V output from a 12V input. The duty cycle is DC = 2.5V/12V = 0.21. The 2-phase curve has a ratio of ~0.25 for a duty cycle of 0.21. This 0.25 ratio of RMS ripple current to a DC load current of 10A equals ~2.5A of input RMS ripple current for the external input capacitors.

Output Capacitors

The LTM4603 is designed for low output voltage ripple. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical capacitance is 200µF if all ceramic output capacitors are used. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. Table 2 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2.5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to maximize transient performance.

Multiphase operation with multiple LTM4603 devices in parallel will lower the effective output ripple current due to the interleaving operation of the regulators. For example, each LTM4603's inductor current of a 12V to 2.5V multiphase design can be read from the "Inductor Ripple versus Duty Cycle" (Figure 3). The large ripple current at low duty cycle and high output voltage can be reduced by adding an external resistor from f_{SET} to ground which increases the frequency. If we choose the duty cycle of DC = 2.5V/12V = 0.21, the inductor ripple current for 2.5V output at 21% duty cycle is ~2.5A in Figure 3.

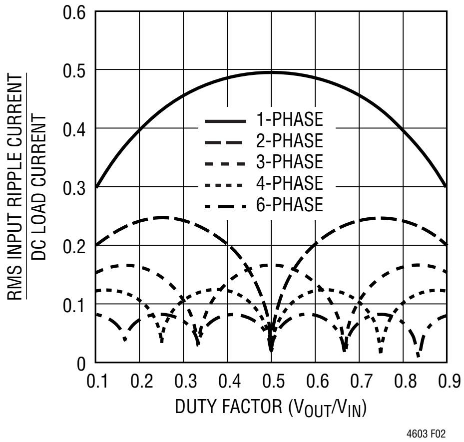

Figure 2. Normalized Input RMS Ripple Current vs Duty Factor for One to Six Modules (Phases)

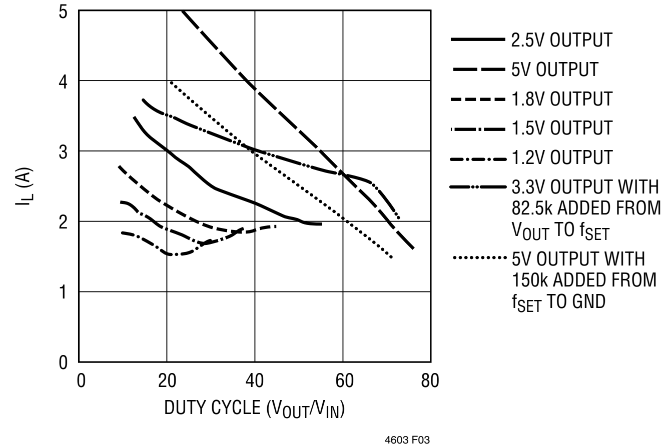

Figure 3. Inductor Ripple Current vs Duty Cycle

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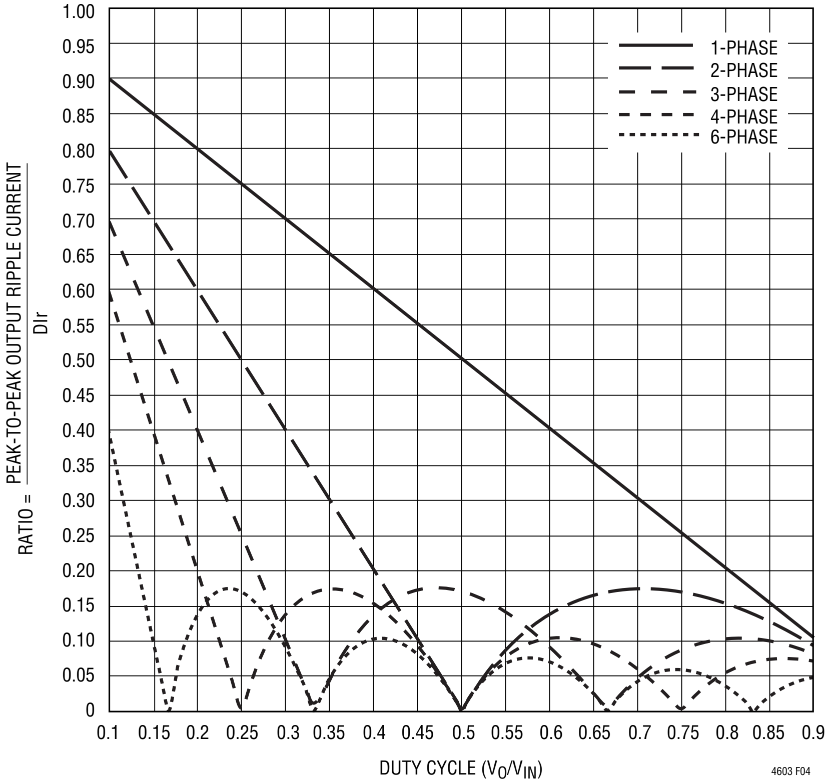

Figure 4. Normalized Output Ripple Current vs Duty Cycle, DIr = V_OT/L_I

Figure 4 provides a ratio of peak-to-peak output ripple current to the inductor current as a function of duty cycle and the number of paralleled phases. Pick the corresponding duty cycle and the number of phases to arrive at the correct output ripple current ratio value. If a 2-phase operation is chosen at a duty cycle of 21%, then 0.6 is the ratio. This 0.6 ratio of output ripple current to inductor ripple of 2.5A equals 1.5A of effective output ripple current. Refer to Application Note 77 for a detailed explanation of output ripple current reduction as a function of paralleled phases.

The output voltage ripple has two components that are related to the amount of bulk capacitance and effective series resistance (ESR) of the output bulk capacitance. Therefore, the output voltage ripple can be calulated with the known effective output ripple current. The equation: $\Delta V_{OUT(P-P)} \approx (\Delta I_L/(8 \bullet f \bullet m \bullet C_{OUT}) + ESR \bullet \Delta I_L)$, where f is frequency and m is the number of parallel phases. This calclation process can be easily fulfilled using our Excel tool (refer to??).

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4603 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

To further limit current in the event of an overload condition, the LTM4603 provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to about one sixth of its full current limit value.

Soft-Start and Tracking

The TRACK/SS pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on this pin will program the ramp rate of the output voltage. A 1.4μA current source will charge up the external soft-start capacitor to 80% of the 0.6V internal voltage reference minus any margin delta. This will control

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the ramp of the internal reference and the output voltage. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.8V \bullet \left(0.6V - V_{OUT(MARGIN)}\right) \bullet \frac{C_{SS}}{1.5\mu A}$$

When the RUN pin falls below 1.5V, then the SS pin is reset to allow for proper soft-start control when the regulator is enabled again. Current foldback and force continuous mode are disabled during the soft-start process. The soft-start function can also be used to control the output ramp up time, so that another regulator can be easily tracked to it.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider. Figure 5 shows an example of coincident tracking. Ratiometric modes of tracking can be achieved by selecting different resistor values to change the output tracking ratio. The master output must be greater than the slave output for the tracking to work. Figure 6 shows the coincident output tracking characteristics.

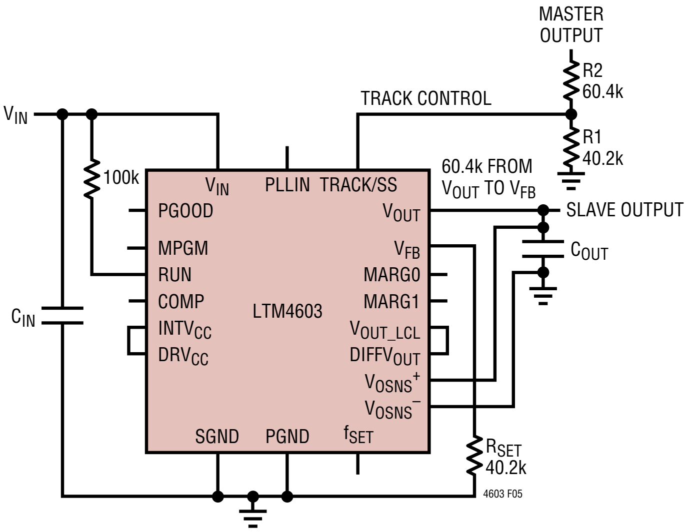

Figure 5

Run Enable

The RUN pin is used to enable the power module. The pin has an internal 5.1V zener to ground. The pin can be driven with a logic input not to exceed 5V.

The RUN pin can also be used as an undervoltage lock out (UVLO) function by connecting a resistor divider from the input supply to the RUN pin:

$$V_{UVLO} = \frac{R1 + R2}{R2} \bullet 1.5V$$

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point and tracks with margining.

COMP Pin

This pin is the external compensation pin. The module has already been internally compensated for most output voltages. Table 2 is provided for most application requirements. A spice model will be provided for other control loop optimization.

PLLIN

The power module has a phase-locked loop comprised of an internal voltage controlled oscillator and a phase detector. This allows the internal top MOSFET turn-on to be locked

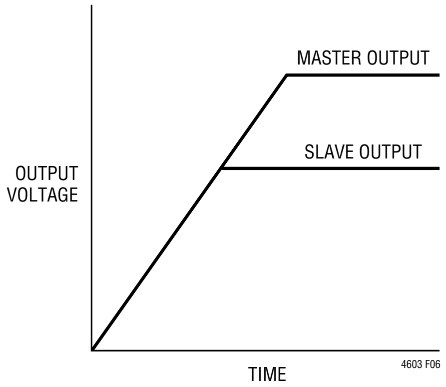

Figure 6

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to the rising edge of the external clock. The frequency range is ±30% around the operating frequency of 1MHz. A pulse detection circuit is used to detect a clock on the PLLIN pin to turn on the phase lock loop. The pulse width of the clock has to be at least 400ns and 2V in amplitude. During the start-up of the regulator, the phase-lock loop function is disabled.

INTV$_{CC}$ and DRV$_{CC}$ Connection

An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and DRV$_{CC}$ for driving the internal power MOSFETs. Therefore, if the system does not have a 5V power rail, the LTM4603 can be directly powered by Vin. The gate driver current through the LDO is about 20mA. The internal LDO power dissipation can be calculated as:

$$P_{LDO\_LOSS} = 20mA \bullet (V_{IN} - 5V)$$

The LTM4603 also provides the external gate driver voltage pin DRV$_{CC}$. If there is a 5V rail in the system, it is recommended to connect DRV$_{CC}$ pin to the external 5V rail. This is especially true for higher input voltages. Do not apply more than 6V to the DRV$_{CC}$ pin. A 5V output can be used to power the DRV$_{CC}$ pin with an external circuit as shown in Figure 16.

Parallel Operation of the Module

The LTM4603 device is an inherently current mode controlled device. Parallel modules will have very good current sharing. This will balance the thermals on the design. The voltage feedback equation changes with the variable η as modules are paralleled:

$$V_{OUT} = 0.6V \frac{\frac{60.4k}{\eta} + R_{FB}}{R_{FB}}$$

η is the number of paralleled modules.

Thermal Considerations and Output Current Derating

The power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 12, and Figures 13 to 14 for calculating an approximate θ_{JA} for the module with various heat sinking methods. Thermal models are derived from several temperature measurements at the bench and thermal modeling analysis. Thermal Application Note 103 provides a detailed explanation of the analysis for the thermal models and the derating curves. Tables 3 and 4 provide a summary of the equivalent θ_{JA} for the noted conditions. These equivalent θ_{JA} parameters are correlated to the measured values, and are improved with air flow. The case temperature is maintained at 100°C or below for the derating curves. This allows for 4W maximum power dissipation in the total module with top and bottom heatsinking, and 2W power dissipation through the top of the module with an approximate θ_{JC} between 6°C/W to 9°C/W. This equates to a total of 124°C at the junction of the device.

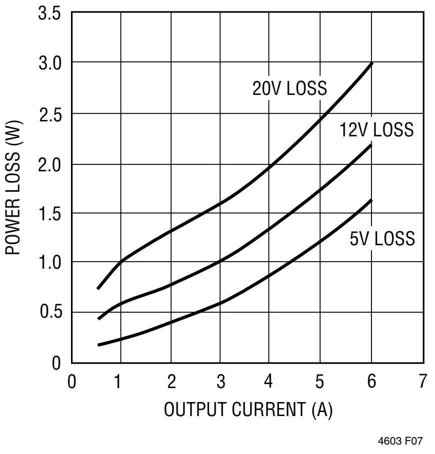

Figure 7. 1.5V Power Loss

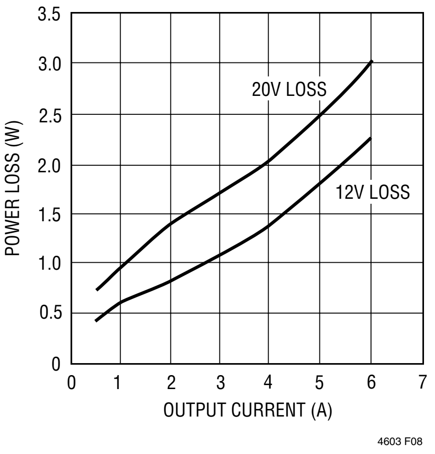

Figure 8. 3.3V Power Loss

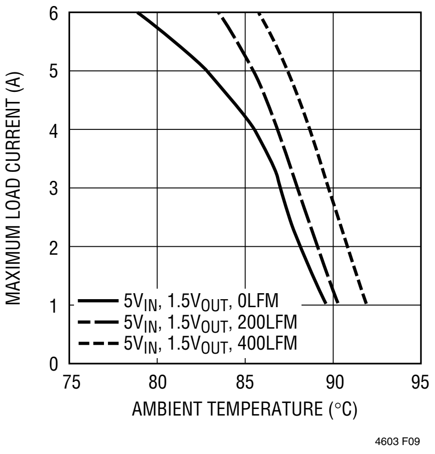

Figure 9. No Heat Sink

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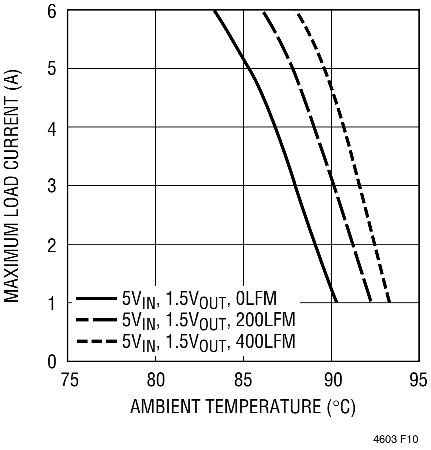

Figure 10. BGA Heat Sink

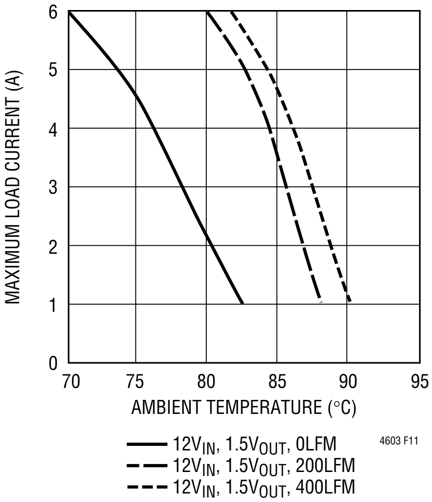

Figure 11. No Heat Sink

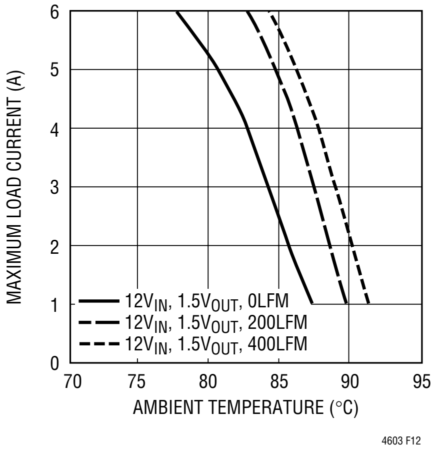

Figure 12. BGA Heat Sink

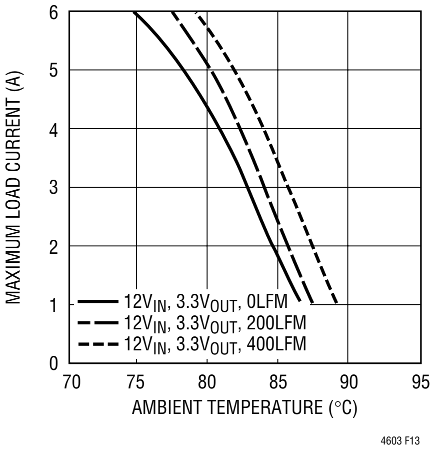

Figure 13. No Heat Sink

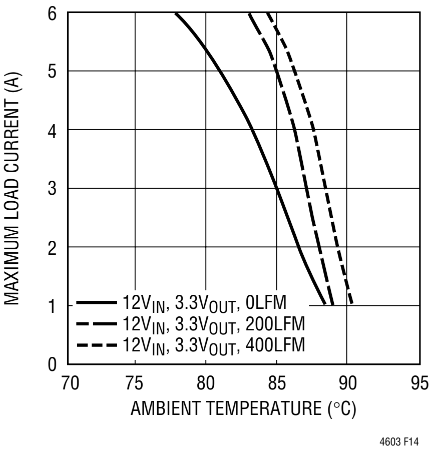

Figure 14. BGA Heat Sink

Table 2. Output Voltage Response Versus Component Matrix (Refer to Figure 18)

TYPICAL MEASURED VALUES

C_{OUT1} VENDORS	PART NUMBER	C_{OUT2} VENDORS	PART NUMBER
TAIYO YUDEN	JMK316BJ226ML-T501 (22µF, 6.3V)	SANYO POSCAP	6TPE220MIL (220µF, 6.3V)
TAIYO YUDEN	JMK325BJ476MM-T (47µF, 6.3V)	SANYO POSCAP	2R5TPE330M9 (330µF, 2.5V)
TDK	C3225X5R0J476M (47µF, 6.3V)	SANYO POSCAP	4TPE330MCL (330µF, 4V)

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	V_{IN} (V)	DROOP (mV)	PEAK TO PEAK (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{SET} (kΩ)
1.2	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	34	68	30	3	60.4
1.2	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	5	22	40	26	3	60.4
1.2	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	20	40	24	3	60.4
1.2	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	5	32	60	18	3	60.4
1.2	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	34	68	30	3	60.4
1.2	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	12	22	40	26	3	60.4
1.2	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	20	39	24	3	60.4
1.2	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	12	29.5	55	18	3	60.4
1.5	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	35	70	30	3	40.2
1.5	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	5	25	48	30	3	40.2
1.5	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	24	47.5	26	3	40.2
1.5	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	5	36	68	26	3	40.2
1.5	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	35	70	30	3	40.2
1.5	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	12	25	48	30	3	40.2
1.5	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	24	45	26	3	40.2
1.5	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	12	32.6	61.9	26	3	40.2
1.8	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	38	76	37	3	30.1
1.8	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	5	29.5	57.5	30	3	30.1
1.8	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	28	55	26	3	30.1
1.8	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	5	43	80	26	3	30.1
1.8	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	38	76	37	3	30.1
1.8	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 2.5V	12	28	55	30	3	30.1
1.8	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	27	52	26	3	30.1
1.8	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	12	36.4	70	26	3	30.1
2.5	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	5	38	78	40	3	19.1
2.5	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 4V	5	37.6	74	34	3	19.1
2.5	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	5	39.5	78.1	28	3	19.1
2.5	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	5	66	119	12	3	19.1
2.5	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	38	78	40	3	19.1
2.5	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 4V	12	34.5	66.3	34	3	19.1
2.5	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	35.8	68.8	28	3	19.1
2.5	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	12	50	98	18	3	19.1
3.3	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	7	42	86	40	3	13.3
3.3	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 4V	7	47	89	32	3	13.3
3.3	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	7	50	94	28	3	13.3
3.3	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	7	75	141	14	3	13.3
3.3	2 × 10µF 25V	150µF 35V	1 × 22µF 6.3V	330µF 4V	12	42	86	40	3	13.3
3.3	2 × 10µF 25V	150µF 35V	1 × 47µF 6.3V	330µF 4V	12	47	88	32	3	13.3
3.3	2 × 10µF 25V	150µF 35V	2 × 47µF 6.3V	220µF 6.3V	12	50	94	28	3	13.3
3.3	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	12	69	131	22	3	13.3
5	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	15	110	215	20	3	8.25
5	2 × 10µF 25V	150µF 35V	4 × 47µF 6.3V	NONE	20	110	217	20	3	8.25

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Table 3. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 9, 11	5, 12	Figure 7	0	None	15.2
Figures 9, 11	5, 12	Figure 7	200	None	14
Figures 9, 11	5, 12	Figure 7	400	None	12
Figures 10, 12	5, 12, 20	Figure 7	0	BGA Heat Sink	13.9
Figures 10, 12	5, 12, 20	Figure 7	200	BGA Heat Sink	11.3
Figures 10, 12	5, 12, 20	Figure 7	400	BGA Heat Sink	10.25

Table 4. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 13	12	Figure 8	0	None	15.2
Figure 13	12	Figure 8	200	None	14.6
Figure 13	12	Figure 8	400	None	13.4
Figure 14	12	Figure 8	0	BGA Heat Sink	13.9
Figure 14	12	Figure 8	200	BGA Heat Sink	11.1
Figure 14	12	Figure 8	400	BGA Heat Sink	10.5

Heat Sink Manufacturer

Wakefield Engineering	Part No: 20069	Phone: 603-635-2800

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Safety Considerations

The LTM4603 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4603 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, PGND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads.
- If vias are placed onto the pads, the the vias must be capped.
- Interstitial via placement can also be used if necessary.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.

Figure 15 gives a good example of the recommended layout.

Frequency Adjustment

The LTM4603 is designed to typically operate at 1MHz across most input conditions. The f_{SET} pin is typically left open or decoupled with an optional 1000pF capacitor. The switching frequency has been optimized for maintaining constant output ripple noise over most operating ranges. The 1MHz switching frequency and the 400ns minimum off time can limit operation at higher duty cycles like 5V to 3.3V, and produce excessive inductor ripple currents for lower duty cycle applications like 20V to 5V. The 5V and 3.3V drop out curves are modified by adding an external resistor on the f_{SET} pin to allow for lower input voltage operation, or higher input voltage operation.

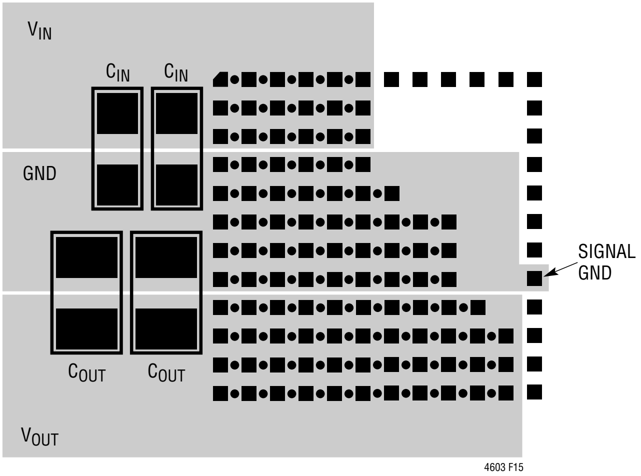


Figure 15. Recommended Layout

APPLICATIONS INFORMATION

Example for 5V Output

LTM4603 minimum on-time = 100ns;
t_{ON} = ((4.8 • 10pf)/I_{fSET})

LTM4603 minimum off-time = 400ns; t_{OFF} = t – t_{ON}, where t = 1/Frequency

Duty Cycle = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

I_{fSET} = (V_{IN}/(3 • R_{fSET})), for 20V operation, I_{SET} = 201µA, t_{ON} = ((4.8 • 10pF)/I_{fSET}), t_{ON} = 239ns, where the internal R_{fSET} is 33.2k. Frequency = (V_{OUT}/(V_{IN} • t_{ON})) = (5V/(20 • 239ns)) ~ 1MHz. The inductor ripple current begins to get high at the higher input voltages due to a larger voltage across the inductor. This is noted in the "Typical Inductor Ripple Current verses Duty Cycle graph" at ~4.5A at 25% duty cycle. The inductor ripple current can be lowered at the higher input voltages by adding an external resistor from f_{SET} to ground to increase the switching frequency. A 3A ripple current is chosen, and the total peak current is equal to 1/2 of the 3A ripple current plus the output current. The 5V output current is limited to 5A, so total peak current is less than 6.5A. This is below the 7A peak specified value. A 150k resistor is placed from f_{SET} to ground, and the parallel combination of 150k and 33.2k equates to 27.2k. The I_{fSET} calculation with 27.2k and 20V input voltage equals 245µA. This equates to a t_{ON} of 196ns. This will increase the switching frequency from 1MHz to ~1.28MHz for the 20V to 5V conversion. The minimum on time is above 100ns at 20V input. Since the switching frequency is approximately constant over input and output conditions, then the lower input voltage range is limited to 10V for the 1.28MHz operation due to the 400ns minimum off time. Equation: t_{ON} = (V_{OUT}/V_{IN}) • (1/Frequency) equates to a 382ns on time, and a 400ns off time. The "V_{IN} to V_{OUT} Step Ratio Curve" reflects an operating range of 10V to 20V for 1.28MHz operation with a 150k resistor to ground, and an 8V to 16V operation for f_{SET} floating. These modifications are made to provide wider input voltage ranges for the 5V output designs while limiting the inductor ripple current, and maintaining the 400ns minimum off time.

Example for 3.3V Output

LTM4603 minimum on-time = 100ns;
t_{ON} = ((3.3 • 10pF)/I_{fSET})

LTM4603 minimum off-time = 400ns;
t_{OFF} = t – t_{ON}, where t = 1/Frequency

Duty Cycle (DC) = t_{ON}/t or V_{OUT}/V_{IN}

Equations for setting frequency:

I_{fSET} = (V_{IN}/(3 • R_{fSET})), for 20V operation, I_{fSET} = 201µA, t_{ON} = ((3.3 • 10pf)/I_{fSET}), t_{ON} = 164ns, where the internal R_{fSET} is 33.2k. Frequency = (V_{OUT}/(V_{IN} • t_{ON})) = (3.3V/(20 • 164ns)) ~ 1MHz. The minimum on-time and minimum-off time are within specification at 164ns and 836ns. The 4.5V minimum input for converting 3.3V output will not meet the minimum off-time specification of 400ns. t_{ON} = 733ns, Frequency = 1MHz, t_{OFF} = 267ns.

Solution

Lower the switching frequency at lower input voltages to allow for higher duty cycles, and meet the 400ns minimum off-time at 4.5V input voltage. The off-time should be about 500ns with 100ns guard band. The duty cycle for (3.3V/4.5) = ~73%. Frequency = (1 – DC)/t_{OFF}, or (1 – 0.73)/500ns = 540kHz. The switching frequency needs to be lowered to 540kHz at 4.5V input. t_{ON} = DC/frequency, or 1.35µs. The f_{SET} pin voltage compliance is 1/3 of V_{IN}, and the I_{fSET} current equates to 45µA with the internal 33.2k. The I_{fSET} current needs to be 24µA for 540kHz operation. A resistor can be placed from V_{OUT} to f_{SET} to lower the effective I_{fSET} current out of the f_{SET} pin to 24µA. The f_{SET} pin is 4.5V/3 =1.5V and V_{OUT} = 3.3V, therefore 82.5k will source 21µA into the f_{SET} node and lower the I_{fSET} current to 24µA. This enables the 540kHz operation and the 4.5V to 20V input operation for down converting to 3.3V output. The frequency will scale from 540kHz to 1.2MHz over this input range. This provides for an effective output current of 5A over the input range.

APPLICATIONS INFORMATION

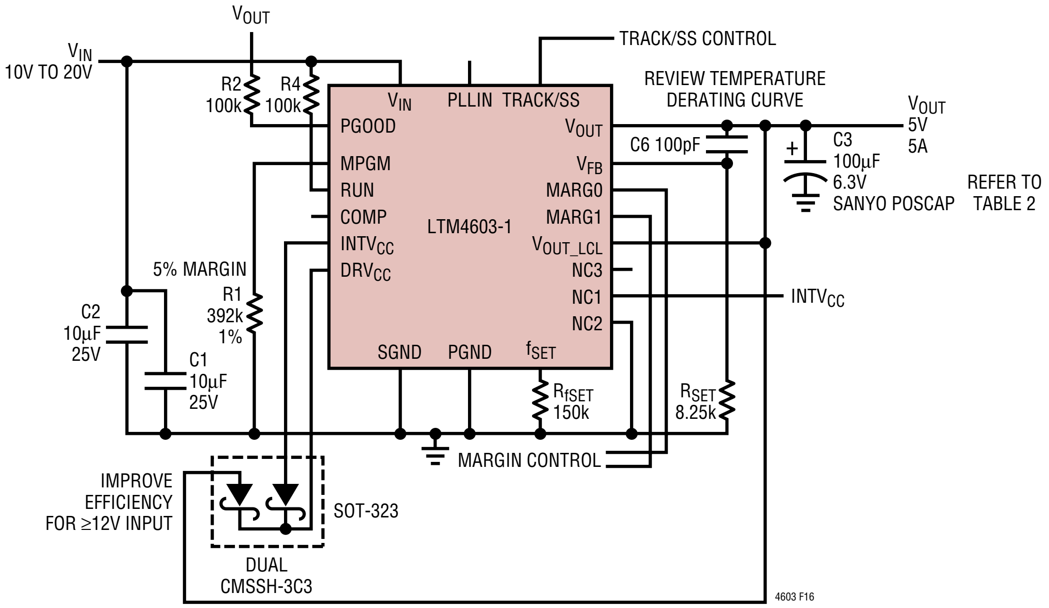


Figure 16. 5V at 5A Design Without Differential Amplifier

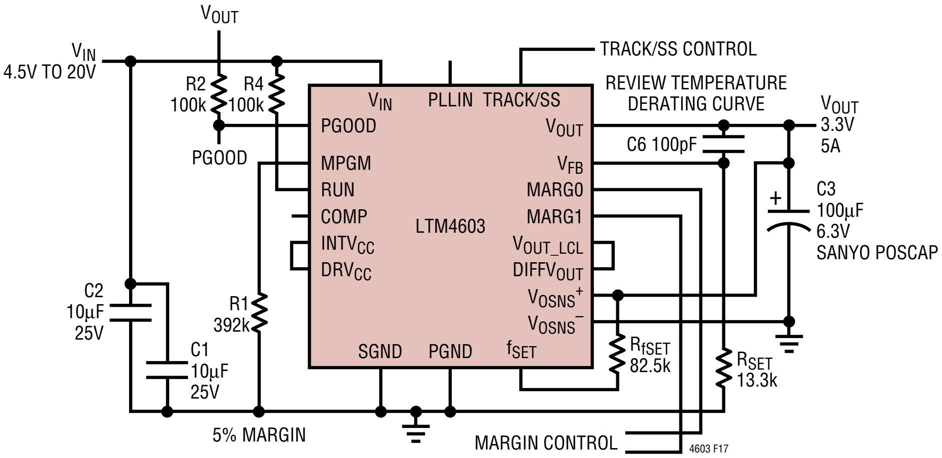


Figure 17. 3.3V at 5A Design

APPLICATIONS INFORMATION

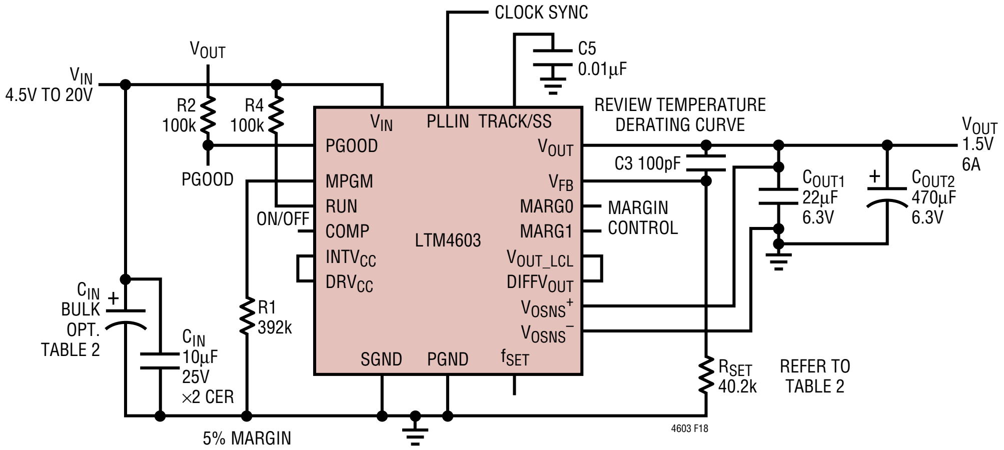
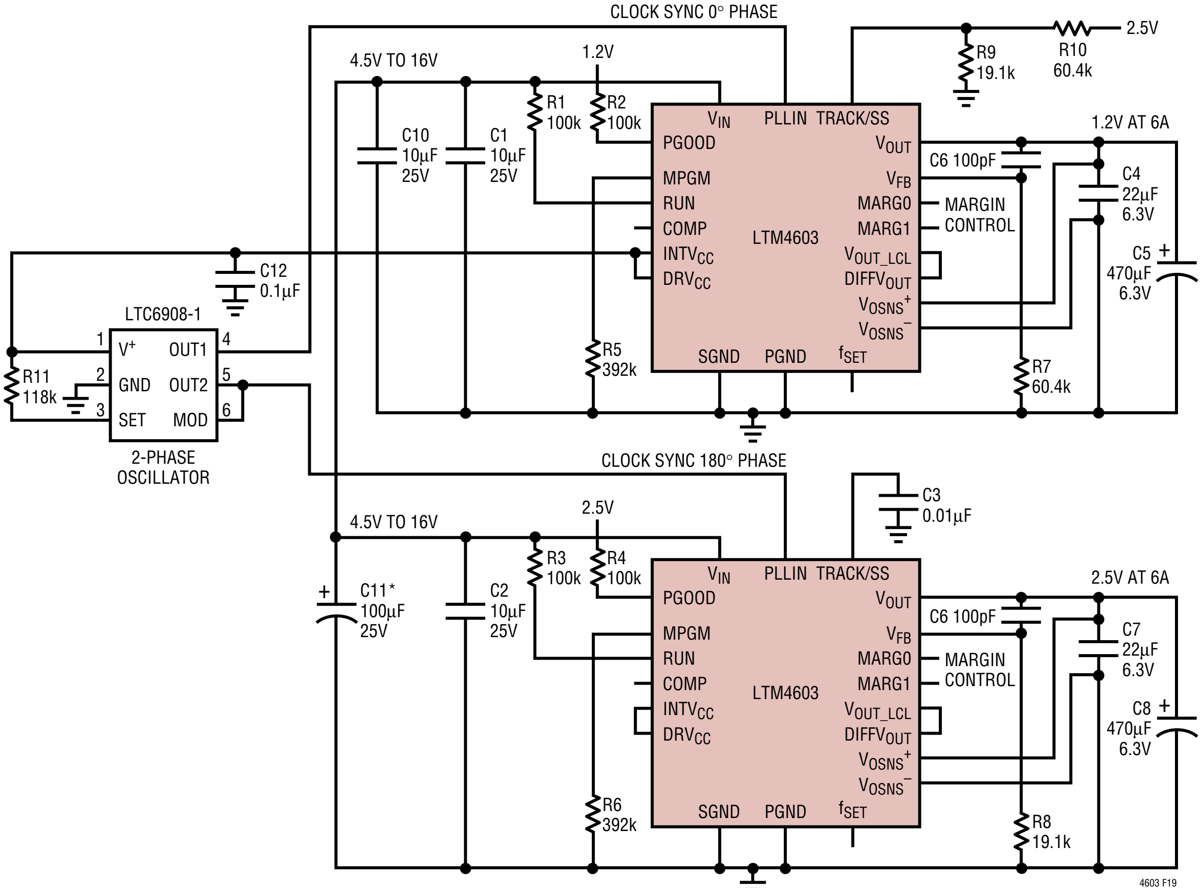


Figure 18. Typical 4.5V-20V_{IN}, 1.5V at 6A Design

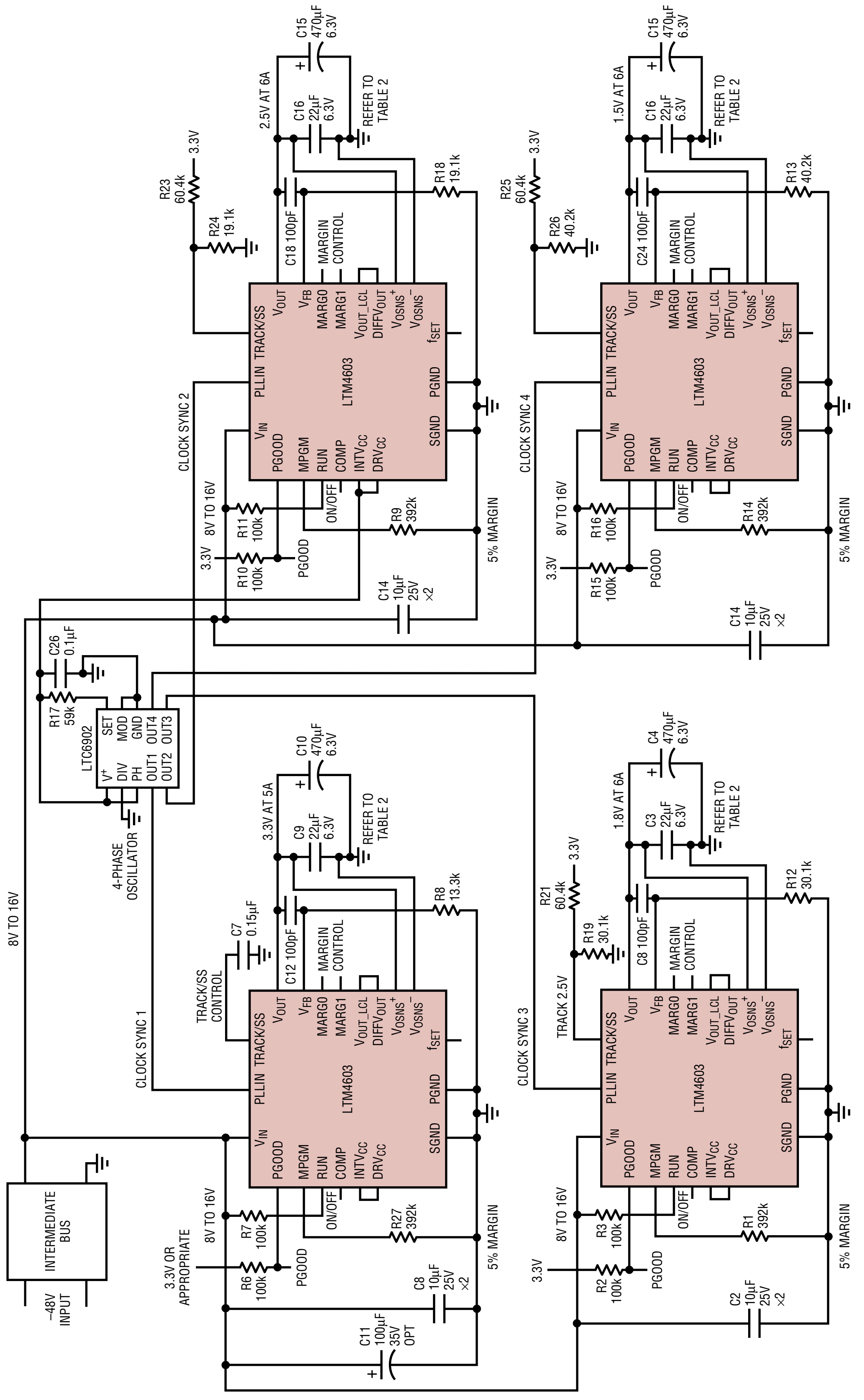


*C11 OPTIONAL TO REDUCE LC RINGING.
NOT NEEDED FOR LOW INDUCTANCE PLANE CONNECTIONS

Figure 19. 2-Phase, 2.5V and 1.2V at 6A with Tracking

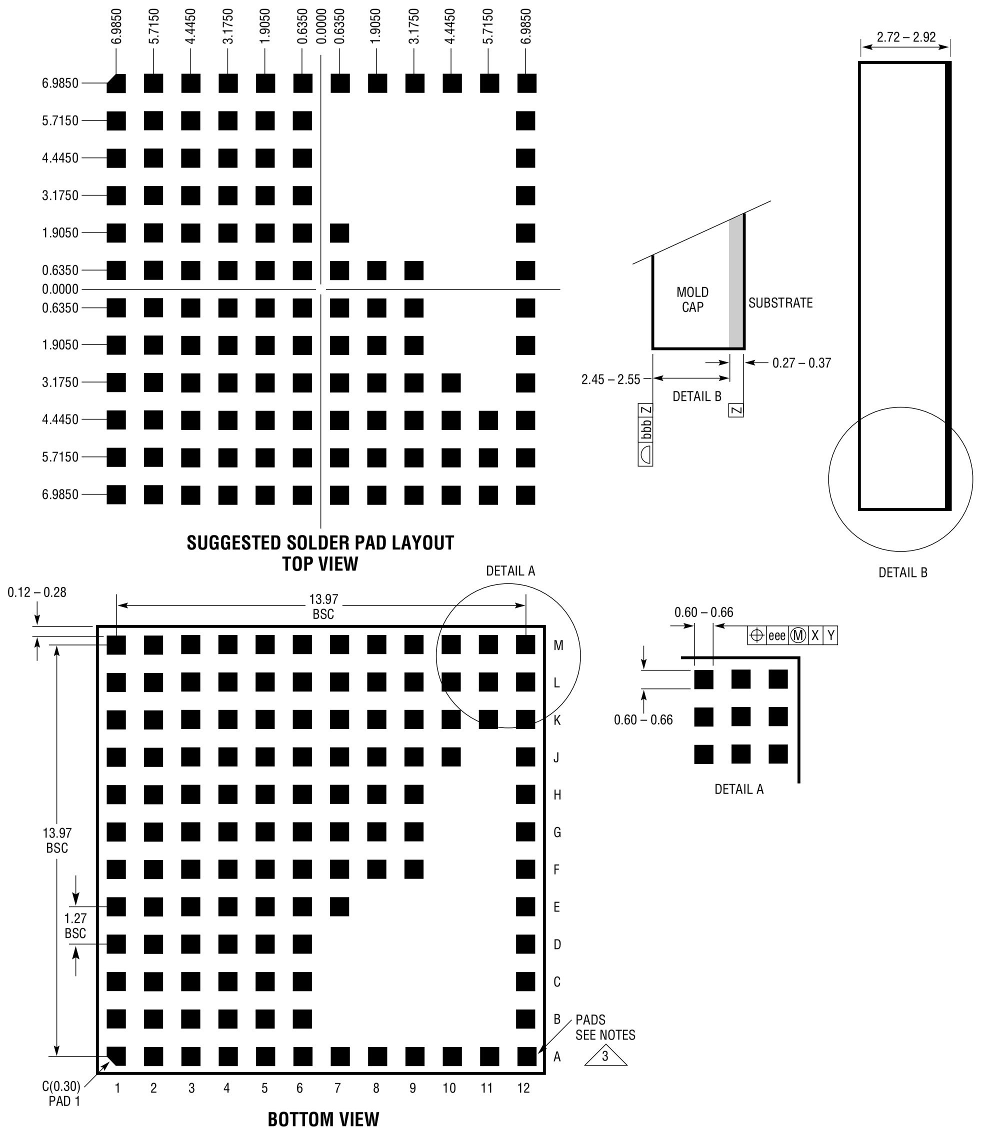
TYPICAL APPLICATION

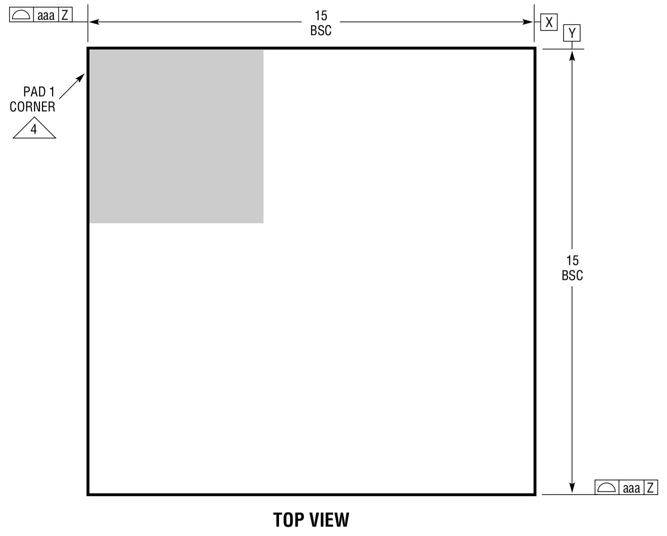
4-Phase, Four Outputs (3.3V, 2.5V, 1.8V and 1.5V) with Tracking



PACKAGE DESCRIPTION

LGA Package
118-Lead (15mm × 15mm)
(Reference LTM DWG # 05-05-1801 Rev Ø)





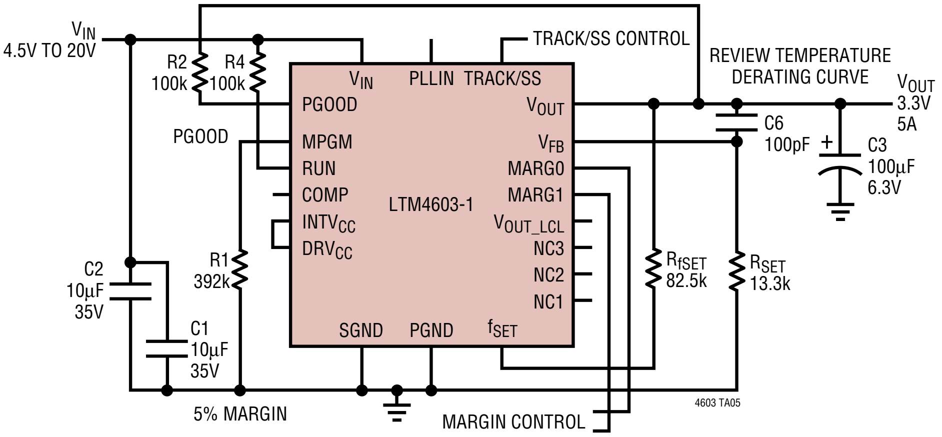
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 118

SYMBOL	TOLERANCE
aaa	0.10
bbb	0.10
eee	0.03

LGA 118 0306 REV Ø

TYPICAL APPLICATION

3.3V at 5A, LTM4603-1 (No Remote Sense Amplifier)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Quad Supply Monitor with Adjustable Reset Timer	Monitors Four Supplies; Adjustable Reset Timer
LTC2923	Power Supply Tracking Controller	Tracks Both Up and Down; Power Supply Sequencing
LT3825/LT3837	Synchronous Isolated Flyback Controllers	No Optocoupler Required; 3.3V, 12A Output; Simple Design
LTM4600	10A DC/DC µModule	Basic 10A Power Supply
LTM4601	12A DC/DC µModule	with PLL, Output Tracking and Margining, LTM4603 Pin Compatible
LTM4602	6A DC/DC µModule	Basic 6A Power Supply

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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