1.5GHz to 7GHz Dual Programmable Gain Downconverting Mixer

FEATURES

- **9dB Power Conversion Gain**
- **32dBm Output IP3**
- **15.5dB Range IF DVGA in 0.5dB Steps**
- **IF Frequency Range Up to 900MHz**
- **Reduced Power Mode**
- 3.3V Single Supply
- Simple SPI for Fast Development
- –40°C to 105°C Operation (T_C)
- Very Small Solution Size
- 32-Lead (5mm × 5mm) QFN Package

APPLICATIONS

- 4G and 5G MIMO Receivers
- 5.1GHz to 5.9GHz LTE-U
- Distributed Antenna Systems (DAS)
- Network Test/Monitoring Equipment
- Fixed Satellite Services

DESCRIPTION

The LTC®5556 dual programmable gain downconverting mixer is ideal for diversity and MIMO receivers that require precise gain setting. Each channel incorporates an active mixer and a digital IF VGA with 15.5dB gain control range. The IF gain of each channel is programmed in 0.5dB steps through the SPI.

Enable pins for each channel allow fast turn-on and shutdown. A reduced power mode is also available.

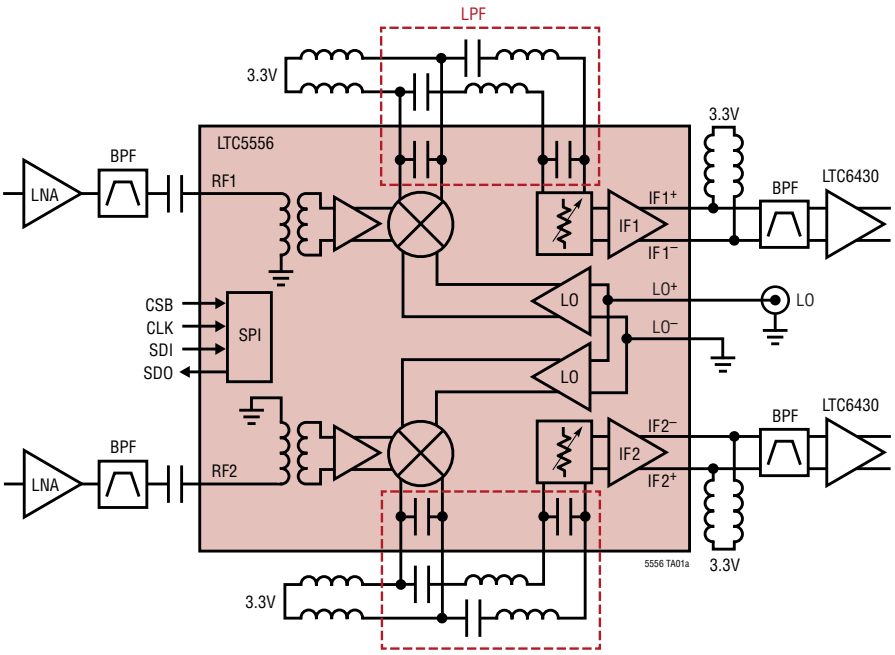
The device has the same functionality as the LTC5566, but the mixers are optimized for a higher 3GHz to 7GHz RF frequency range and the IF is optimized for use up to 900MHz. The mixers may be used down to 1.5GHz, or up to 8GHz with degraded performance.

Dual Programmable Gain Downconverting Mixers

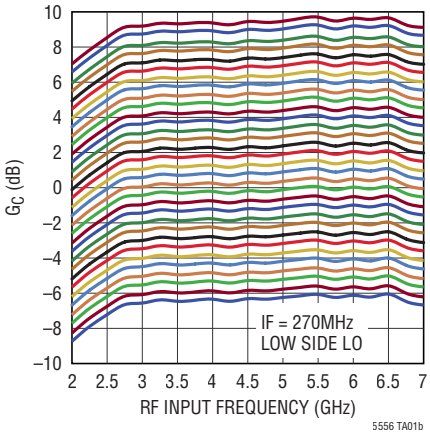
PART NUMBER	OPTIMUM RF RANGE	IF RANGE
LTC5556	3GHz to 7GHz	1MHz to 900MHz
LTC5566	300MHz to 4.5GHz	1MHz to 500MHz

TYPICAL APPLICATION

Dual Channel MIMO Receiver with Programmable 0.5dB Gain Steps



LTC5556 Conversion Gain vs RF Frequency and IF Attenuation (0.5dB Gain Steps)



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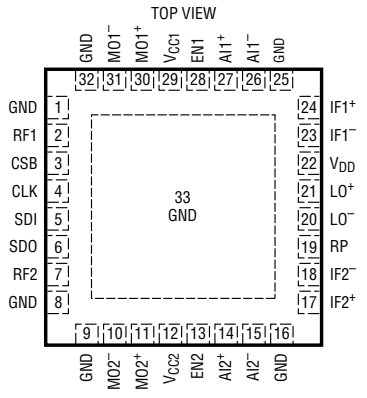
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}, V_{CC1}, V_{CC2}, $IF1^+$, $IF1^-$, $IF2^+$, $IF2^-$) 4V
EN1, EN2 Input Voltages ..... –0.3V to V_{CC} + 0.3V
LO^+, LO^- Input Power (500MHz to 8GHz) ..... +10dBm
RF1, RF2 Input Power (1.5GHz to 7GHz) ..... +20dBm
LO^+, LO^- DC Voltage ..... ±0.5V
IF DVGA Peak Differential Input Voltage ..... ±4V
SDI, CLK, CSB, RP Input Voltages .. –0.3V to V_{DD} + 0.3V
Operating Temperature Range (T_C) ..... –40°C to 105°C
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 7.7°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5556IUH#PBF	LTC5556IUH#TRPBF	5556	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 105°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		●	3.0	3.3	3.6	V
SPI Supply Voltage (V_{DD})		●	1.6		3.6	V
Supply Current (I_{CC})	One Channel, Full Power Mode Both Channels, Full Power Mode One Channel, Reduced Power Mode Both Channels, Reduced Power Mode Shutdown			190 380 145 290 1.2	225 450 1.9	mA mA mA mA mA
SPI Supply Current (I_{DD})	Operating: CSB = Low, f_{CLK} =20MHz Idle: CSB = High			0.3 50	1	mA µA
Enable Logic Inputs (EN1, EN2) Internal Pull-Down Resistors on Each Pin						
Input High Voltage (On)		●	1.4			V
Input Low Voltage (Off)		●			0.5	V
Input Current	V_{IN} = V_{CC} = 3.6V				100	µA
Enable Turn-On Time				0.3		µs
Enable Turn-Off Time				0.1		µs
Reduced Power Logic Input (RP) Internal Pull-Down Resistor						
Input High Voltage (Reduced Power, Both Channels)		●	0.7 • V_{DD}			V
Input Low Voltage		●			0.3 • V_{DD}	V
Input Current	V_{IN} = V_{DD} = 3.6V				50	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V. Test circuit shown in Figure 1. (Notes 3, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Port Logic Inputs (CSB, CLK, SDI)						
Input High Voltage		●	0.7 • V_{DD}			V
Input Low Voltage		●			0.3 • V_{DD}	V
Input Current	V_{IN} = V_{DD} = 3.6V				25	µA
Input Hysteresis				200		mV
SPI Port Logic Output (SDO)						
Output High Voltage	I_{SOURCE} = 3mA	●	V_{DD} – 0.4V			V
Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Output Leakage Current	V_{CSB} = V_{DD} = 3.6V				±20	µA
SPI Port Timing						
SDI Setup Time			5			ns
SDI Hold Time			10			ns
CLK Falling to SDO Valid Time	C_{SDO} = 20pF				15	ns
SDO Rise/Fall Time	C_{SDO} = 20pF			5		ns
SDO Enable Time					10	ns
SDO Disable Time					10	ns
CSB Setup Time			15			ns
CSB Hold Time			5			ns
CLK Frequency	C_{SDO} = 20pF				20	MHz

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN1, EN2 = High, P_{LO} = 0dBm. Test circuit shown in Figure 1. (Notes 3, 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Input Frequency Range	External Matching Required	●		1.5 to 7		GHz
LO Input Frequency Range		●		0.5 to 8		GHz
IF Output Frequency Range	External Matching Required	●		1 to 900		MHz
1dB IF Gain Rolloff	Wideband IF Match			700		MHz
IF Gain Error at 270MHz	Differential; Between Any Two 0.5dB Atten Steps Integral; Over Entire 15.5dB IF Atten Range			±0.04 0.3		dB dB
IF Phase Error	IF = 250MHz, Full 15.5dB Atten Range IF = 500MHz, Full 15.5dB Atten Range			3.6 5.1		Deg Deg
LO Input Return Loss	Single-Ended, Z_O = 50Ω, 500MHz to 8GHz			>9		dB
LO Input Power	Single-Ended or Differential	●	–6	0	6	dBm
Mixer IF Output Impedance	Differential, 10MHz to 1GHz			200Ω || 1pF		R || C
IF DVGA Input Impedance	Differential, 10MHz to 1GHz			200Ω || 1pF		R || C
IF DVGA Output Impedance	Differential, 10MHz to 1GHz			206Ω || 1pF		R || C
RF to LO Isolation	RF = 1.5GHz to 1.7GHz RF = 1.7GHz to 7GHz			>38 >43		dB dB
RF to Unbalanced IF Port Isolation	RF = 1.5GHz to 1.8GHz RF = 1.8GHz to 7GHz			>39 >46		dB dB
LO to Unbalanced IF Port Leakage	LO = 500MHz to 3GHz LO = 3GHz to 8GHz			<–30 <–40		dBm dBm

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN1, EN2 = High, P_{RF} = –6dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

2.6GHz to 6.4GHz RF Input Matching (See Figure 1): RF = 3.6GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 2.6GHz to 6.4GHz			>10		>10	dB
Power Conversion Gain	0dB IF ATTEN			9.1		8.8	dB
	3dB IF ATTEN		4.4	6.0		5.7	dB
	6dB IF ATTEN			3.0		2.7	dB
	9dB IF ATTEN			0.0		–0.3	dB
	12dB IF ATTEN			–3.0		–3.4	dB
	15dB IF ATTEN			–6.1		–6.4	dB
Conversion Gain Flatness	RF = 3.6GHz ±100MHz, LO = 3.33GHz			±0.25		±0.25	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.013		–0.013	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			22.2		17.8	dBm
	3dB IF ATTEN			23.0		18.2	dBm
	6dB IF ATTEN			23.6		18.5	dBm
	9dB IF ATTEN			23.9		18.7	dBm
	12dB IF ATTEN			24.1		18.8	dBm
	15dB IF ATTEN			24.2		18.8	dBm
Two-Tone Output 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			31.3		26.6	dBm
	3dB IF ATTEN			29.0		23.9	dBm
	6dB IF ATTEN			26.6		21.2	dBm
	9dB IF ATTEN			23.9		18.4	dBm
	12dB IF ATTEN			21.1		15.4	dBm
	15dB IF ATTEN			18.1		12.4	dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			52		50	dBm
SSB Noise Figure	0dB IF ATTEN			14.1		13.3	dB
	3dB IF ATTEN			15.2		14.7	dB
	6dB IF ATTEN			16.6		16.4	dB
	9dB IF ATTEN			18.6		18.6	dB
	12dB IF ATTEN			21.0		21.2	dB
	15dB IF ATTEN			23.5		24.1	dB
SSB Noise Figure Under Blocking (3.7GHz Blocker)	+2dBm BLOCKER, 3dB IF ATTEN			19.3		19.0	dB
	+5dBm BLOCKER, 3dB IF ATTEN			21.7		21.5	dB
LO to RF Leakage	LO = 1.5GHz to 7GHz			<–46		<–46	dBm
1/2 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 270MHz)	f_{RF} = 3465MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–59		–58	dBc
1/3 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 270MHz)	f_{RF} = 3420MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–64		–60	dBc
Input 1dB Compression	0dB IF ATTEN			8.7		7.7	dBm
	3dB IF ATTEN			10.9		9.5	dBm
	6dB IF ATTEN			11.5		10.0	dBm
	9dB IF ATTEN and Higher			11.6		10.0	dBm
Output 1dB Compression	0dB IF ATTEN			16.8		15.5	dBm
	3dB IF ATTEN			15.9		14.2	dBm
	6dB IF ATTEN			13.5		11.7	dBm
	9dB IF ATTEN			10.6		8.7	dBm
Channel-to-Channel Isolation	RF = 3.6GHz			44		44	dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN1, EN2 = High, P_{RF} = –6dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

2.6GHz to 6.4GHz RF Input Matching (See Figure 1): RF = 5.5GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			9.7 3.6 –2.5		9.1 3.0 –3.0	dB dB dB
Conversion Gain Flatness	RF = 5.5GHz ±200MHz, LO = 5.23GHz			±0.7		±0.7	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.014		–0.014	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			19.7 19.8 19.9		14.8 15.1 15.1	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			47		48	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			13.9 16.4 20.8		12.6 15.8 20.6	dB dB dB
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			7.6 9.2 9.4 9.5		7.2 8.8 9.2 9.3	dBm dBm dBm dBm
Channel-to-Channel Isolation	RF = 5.5GHz			38		38	dB

RF = 4.6GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			9.2 3.1 –2.9		8.7 2.6 –3.5	dB dB dB
Conversion Gain Flatness	RF = 4.6GHz ±200MHz, LO = 4.33GHz			±0.7		±0.7	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.013		–0.013	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			23.0 23.6 23.7		16.3 16.9 17.0	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			47		46	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			14.2 16.6 21.0		13.1 16.1 20.9	dB dB dB
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			8.4 10.2 10.7 10.8		7.7 9.6 10.0 10.1	dBm dBm dBm dBm
Channel-to-Channel Isolation	RF = 4.6GHz			40		40	dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN1, EN2 = High, P_{RF} = –6dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

2.2GHz to 3.2GHz RF Input Matching (See Figure 1): RF = 2.6GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 2.2GHz to 3.2GHz			>10		>10	
LO to RF Leakage	LO = 1.4GHz to 3.8GHz			<–50		<–50	
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			9.2 3.1 –2.9		8.7 2.6 –3.4	dB dB dB
Conversion Gain Flatness	RF = 2.6GHz ±100MHz, LO = 2.33GHz			±0.14		±0.14	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.012		–0.012	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			26.6 24.5 24.0		19.2 20.4 20.7	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 271MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			59		51	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			13.4 16.5 20.9		12.7 16.2 21.2	dB dB dB
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			9.3 11.4 12.3 12.5		8.2 10.3 10.9 11.0	dBm dBm dBm dBm
Channel-to-Channel Isolation	RF = 2.6GHz			43		43	dB

1.5GHz to 2.1GHz RF Input Matching (See Figure 1): RF = 1.8GHz, IF = 270MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 1.5GHz to 2.1GHz			>10		>10	dB
LO to RF Leakage	LO = 500MHz to 3GHz			<–55		≤–55	dBm
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			8.7 2.6 –3.4		8.3 2.2 –3.8	dB dB dB
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			12.6 16.1 21.0		12.1 16.0 21.2	dB dB dB
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			22.6 24.0 24.4		19.8 20.9 21.3	dBm dBm dBm
Channel-to-Channel Isolation	RF = 1.8GHz			46		46	dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The mixer output pins on this device are sensitive to ESD greater than 1kV (HBM). Proper ESD handling precautions must be observed. All other pins withstand 2kV.

Note 3: The LTC5556 is guaranteed functional over the –40°C to 105°C case temperature range.

Note 4: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 2dB matching pad on RF input, and bandpass filter on the LO input.

Note 5: Channel-to-channel isolation is defined as the relative IF output power of channel 2 to channel 1, with the RF input signal applied to RF1 while the RF2 input is 50Ω terminated. Both channels are enabled and programmed for 3dB IF attenuation.

Note 6: SPI timing guaranteed by design, not subject to test.

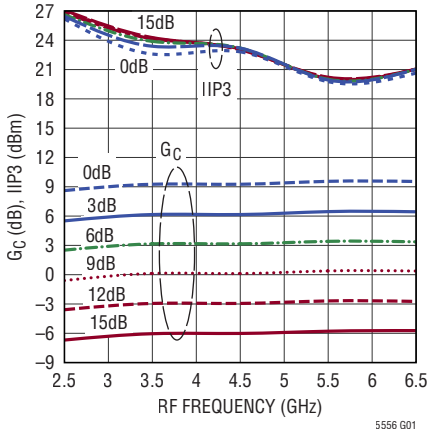
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

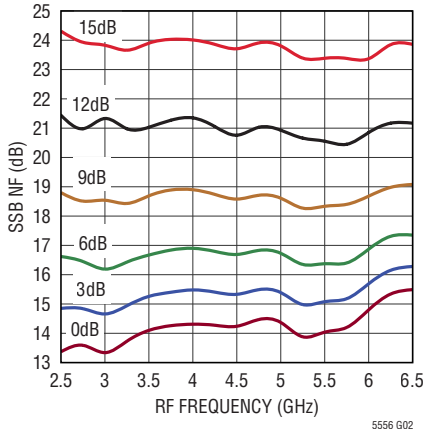
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.6GHz to 6.4GHz RF Input Matching: IF = 270MHz, Low Side LO

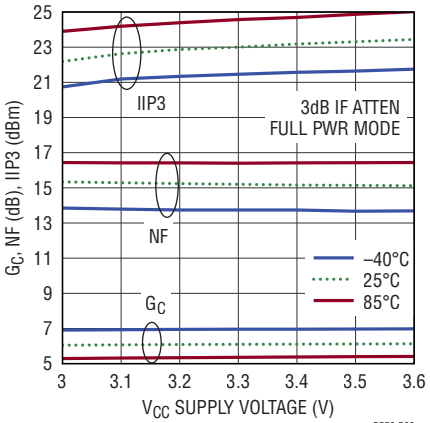
Conv Gain and IIP3 vs RF Frequency and IF Attenuation (3dB Steps)



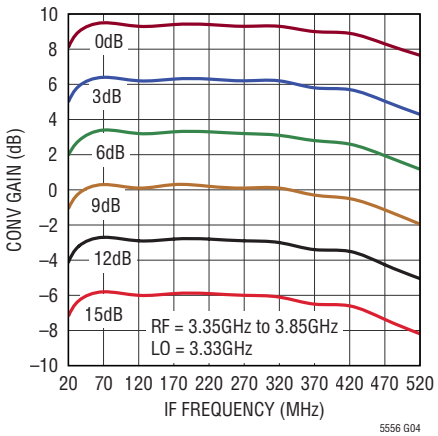
SSB NF vs RF Frequency and IF Attenuation (3dB Steps)



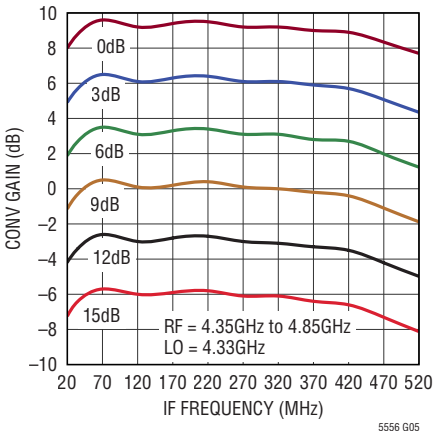
3.6GHz Conv Gain IIP3 and SSB NF vs V_{CC} and Case Temperature



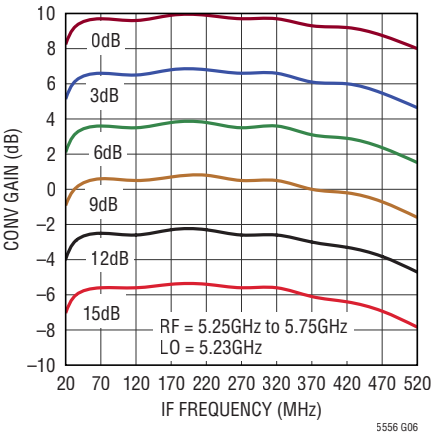
3.6GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



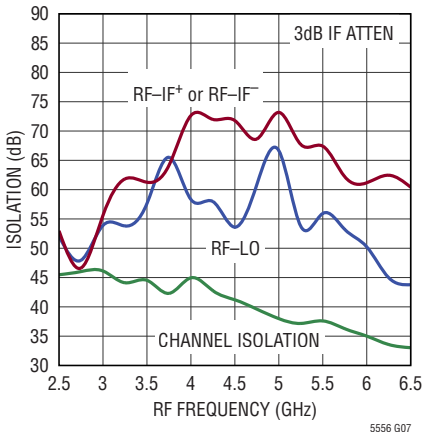
4.6GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



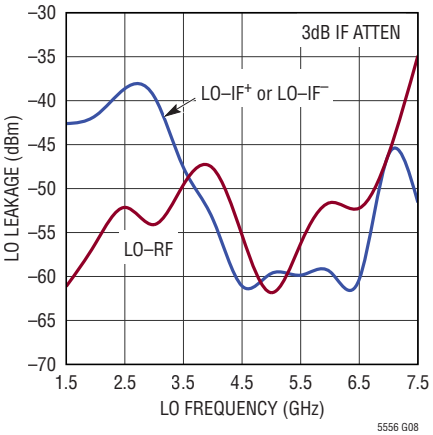
5.5GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



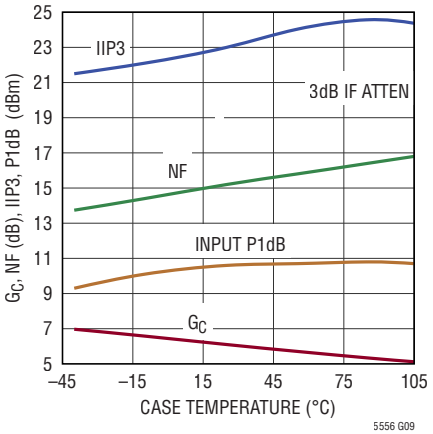
Isolation vs RF Frequency



LO Leakage vs LO Frequency



3.6GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



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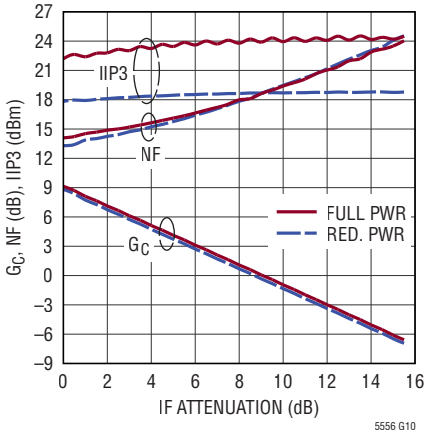
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

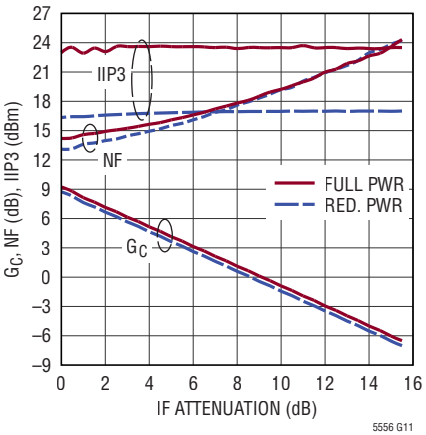
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.6GHz to 6.4GHz RF Input Matching: IF = 270MHz, Low Side LO

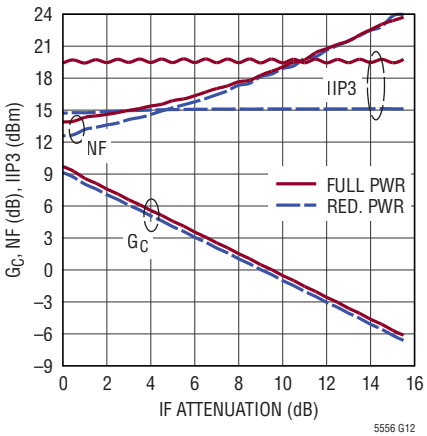
3.6GHz Conv Gain, IIP3, and SSB NF vs IF Attenuation (0.5dB Steps)



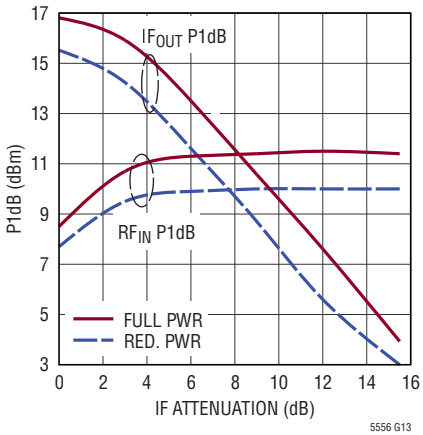
4.6GHz Conv Gain, IIP3, and SSB NF vs IF Attenuation (0.5dB Steps)



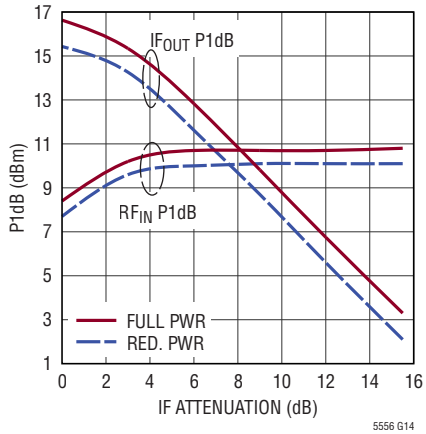
5.5GHz Conv Gain, IIP3, and SSB NF vs IF Attenuation (0.5dB Steps)



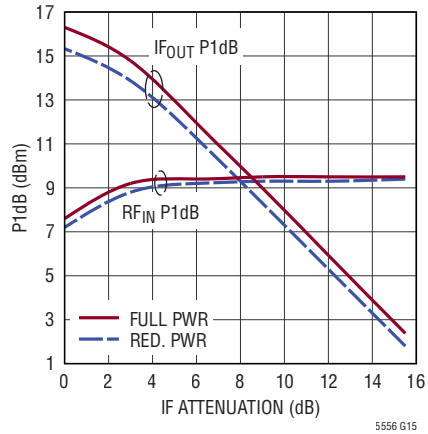
3.6GHz RF Input and IF Output P1dB vs IF Attenuation



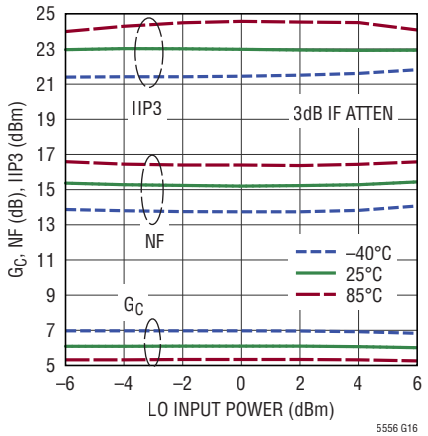
4.6GHz RF Input and IF Output P1dB vs IF Attenuation



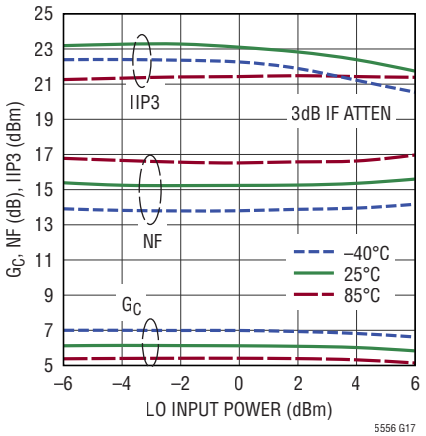
5.5GHz RF Input and IF Output P1dB vs IF Attenuation



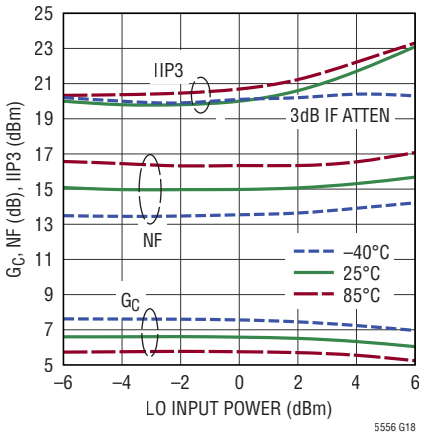
3.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



4.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



5.5GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



Rev 0

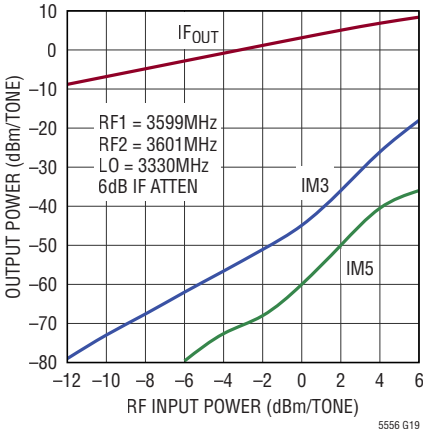
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

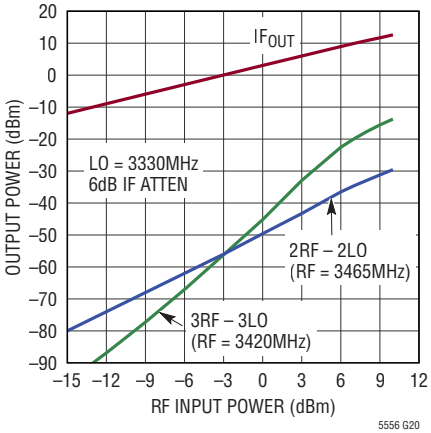
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.6GHz to 6.4GHz RF Input Matching: IF = 270MHz, Low Side LO

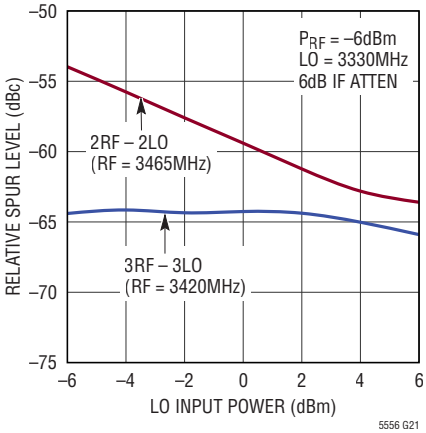
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



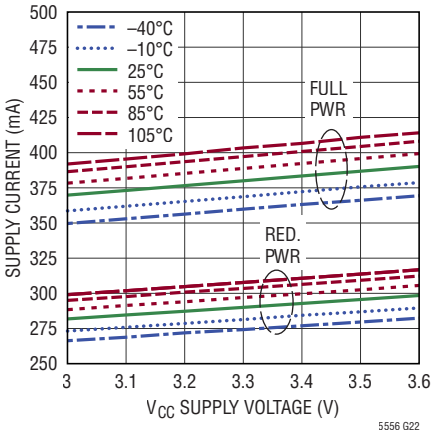
Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



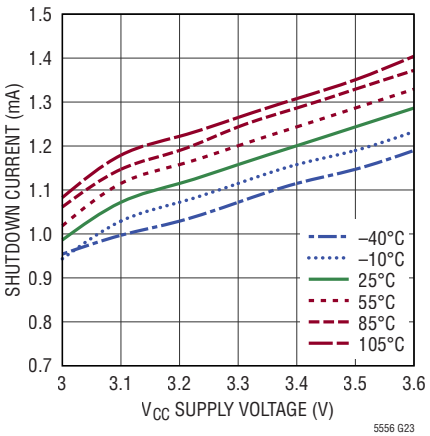
2 × 2 and 3 × 3 Spur Suppression vs LO Power



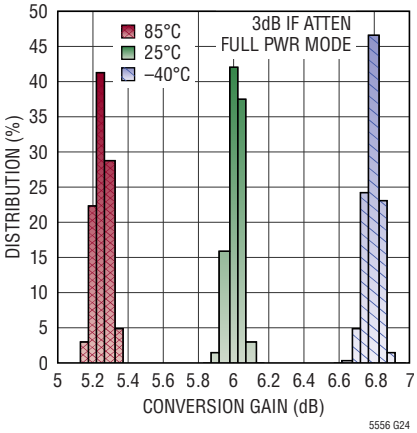
V_{CC} Supply Current vs Supply Voltage (Both Channels Enabled)



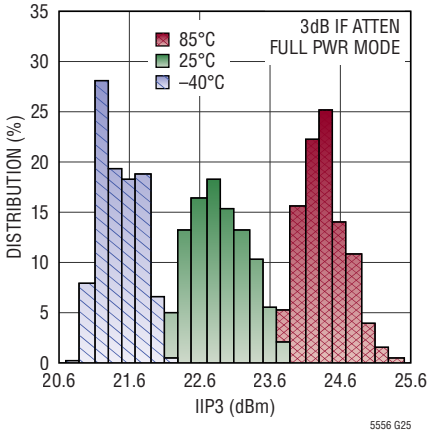
V_{CC} Shutdown Current vs Supply Voltage (Both Channels Disabled)



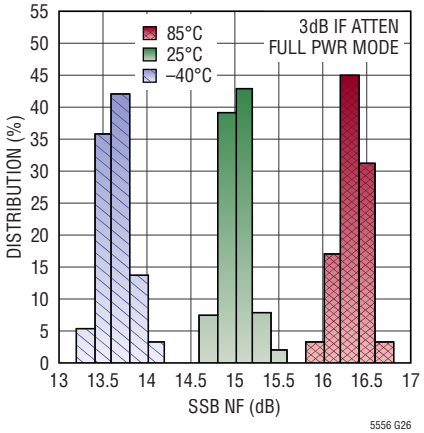
3.6GHz Conversion Gain Distribution



3.6GHz IIP3 Distribution



3.6GHz SSB NF Distribution



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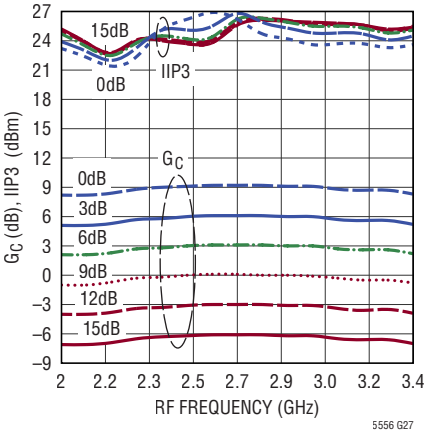
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

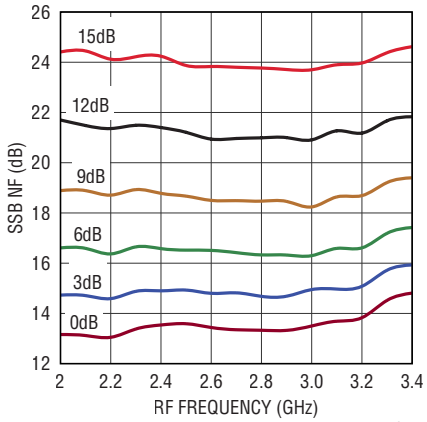
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

2.2GHz to 3.2GHz RF Input Matching: RF = 2.6GHz, IF = 270MHz, Low Side LO

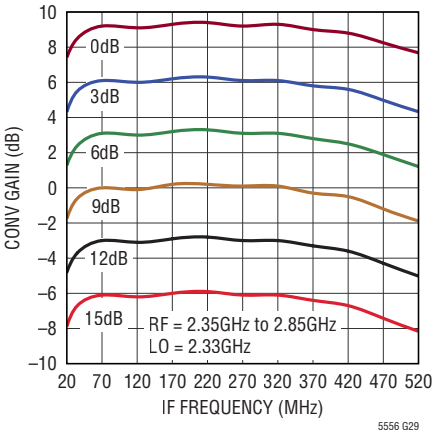
Conv Gain and IIP3 vs RF Frequency and IF Attenuation (3dB Steps)



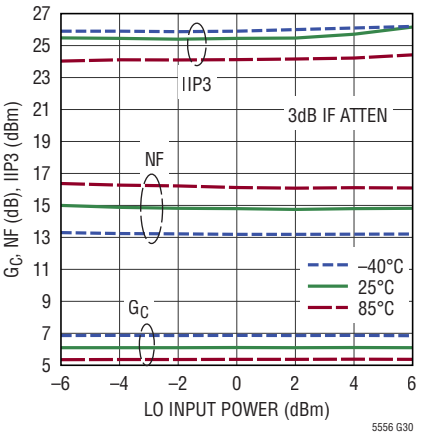
SSB NF vs RF Frequency and IF Attenuation (3dB Steps)



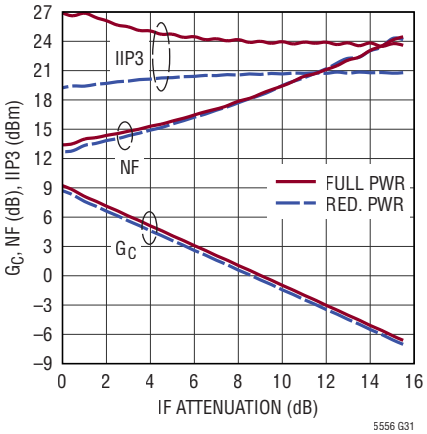
Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



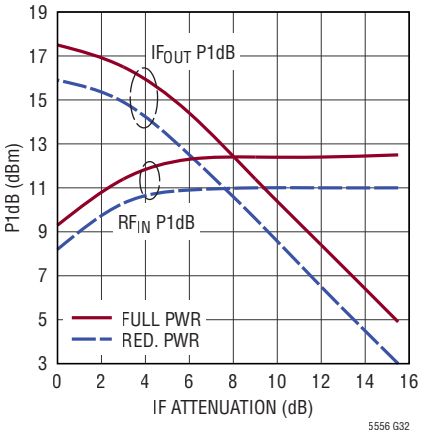
2.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



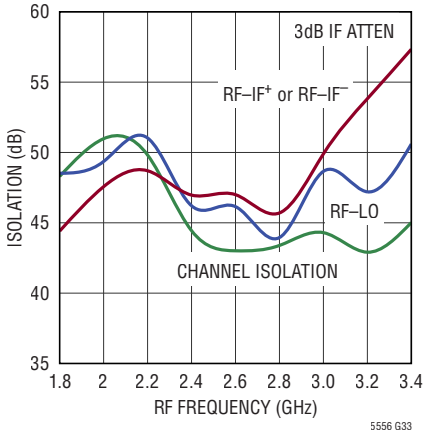
2.6GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation (0.5dB Steps)



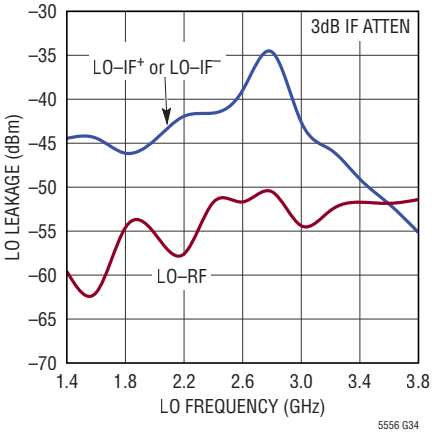
2.6GHz RF Input and IF Output P1dB vs IF Attenuation



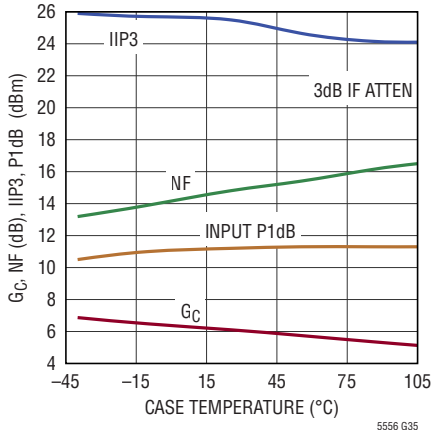
Isolation vs RF Frequency



LO Leakage vs LO Frequency



2.6GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



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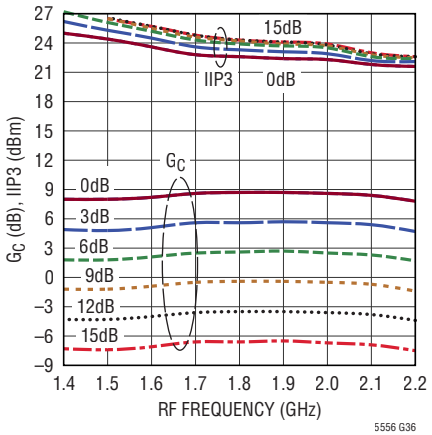
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

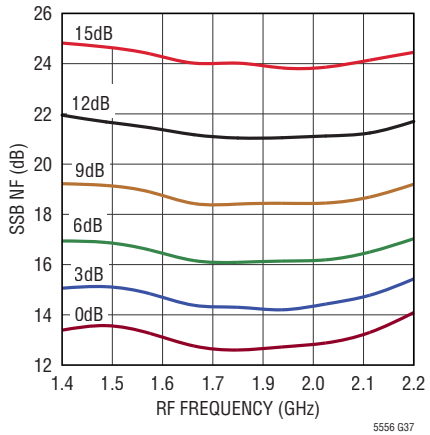
P_{RF} = –6dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, full power mode, unless otherwise noted.

1.5GHz to 2.1GHz RF Input Matching: RF = 1.8GHz, IF = 270MHz, Low Side LO

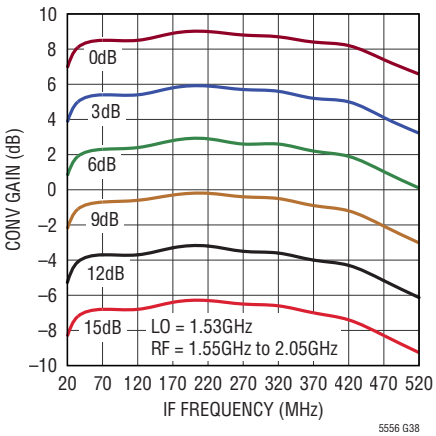
Conv Gain and IIP3 vs RF Frequency and IF Attenuation (3dB Steps)



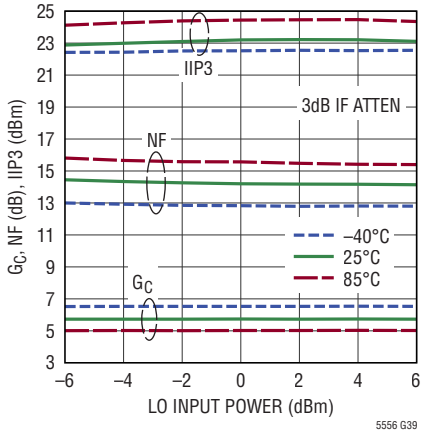
SSB NF vs RF Frequency and IF Attenuation (3dB Steps)



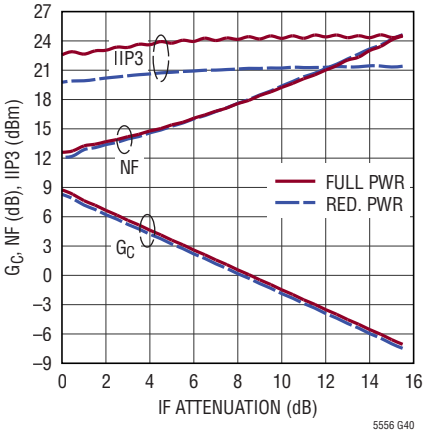
Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



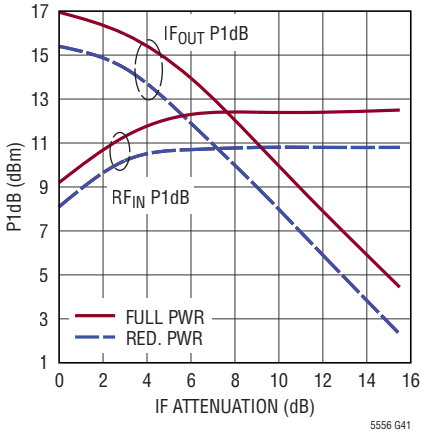
1.8GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



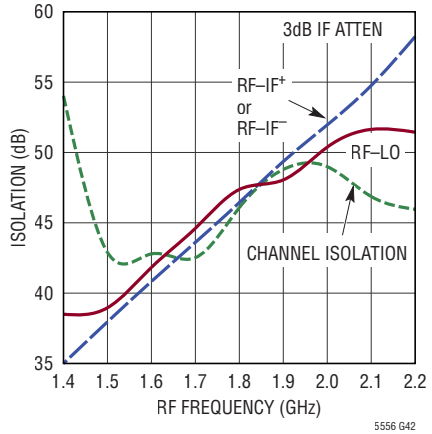
1.8GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation



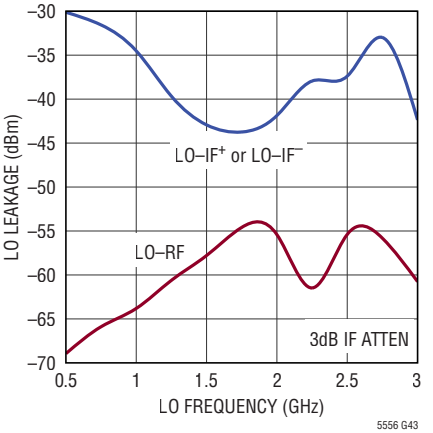
1.8GHz RF Input and IF Output P1dB vs IF Attenuation



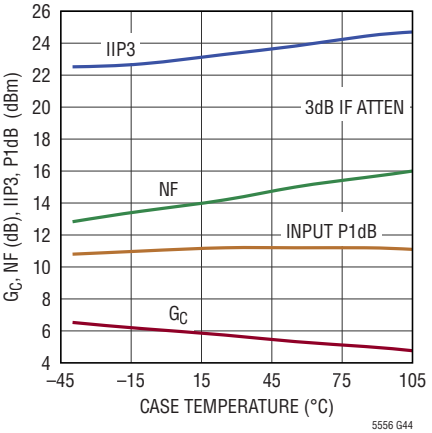
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



1.8GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



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PIN FUNCTIONS

GND (Pins 1, 8, 9, 16, 25, 32, Exposed Pad Pin 33): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad provides both electrical ground contact and thermal contact to the printed circuit board.

RF1, RF2 (Pins 2, 7): Single-Ended RF Inputs for Channels 1 and 2, Respectively. These pins are internally biased to $V_{CC}/2$ when V_{CC} is applied. Therefore, a series DC-blocking capacitor must be used.

CSB (Pin 3): Serial Port Chip Select. This CMOS input activates the SPI inputs when driven low. When driven high, the inputs are deactivated. See the Applications section for more details.

CLK (Pin 4): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Applications section for more details.

SDI (Pin 5): Serial Port Data Input. This CMOS input is used to load serial data into the 16-bit register. See the Applications section for more details.

SDO (Pin 6): Serial Port Data Output. This CMOS three-state output presents data from the serial port during a communication burst. Optionally, attach a resistor of >200k to GND to prevent a floating output. See the Applications section for more details.

$MO2^-$, $MO2^+$, $MO1^+$, $MO1^-$ (Pins 10, 11, 30, 31): Open-Collector Differential IF Outputs for Mixer 2 and Mixer 1, Respectively. These pins must be connected to V_{CC} through pull-up inductors. Typical DC current is 28mA into each pin.

V_{CC2}, V_{CC1} (Pins 12, 29): Power Supply Pins for Channels 2 and 1, Respectively. These pins must be connected to a regulated 3.3V supply, with a bypass capacitor located close to the pins. Typical DC current consumption is 40mA into each pin.

EN2, EN1 (Pins 13, 28): Enable Control Pins for Channels 2 and 1, Respectively. A CMOS logic high will enable each channel. These pins have internal 330k pull-down resistors, so if unconnected, both channels are shutdown.

$AI2^+$, $AI2^-$, $AI1^-$, $AI1^+$ (Pins 14, 15, 26, 27): Differential IF Attenuator Inputs for Channel 2 and Channel 1, Respectively. These pins are internally biased to $V_{CC}/2$ when V_{CC} is applied. Therefore, a series DC-blocking capacitor must be used.

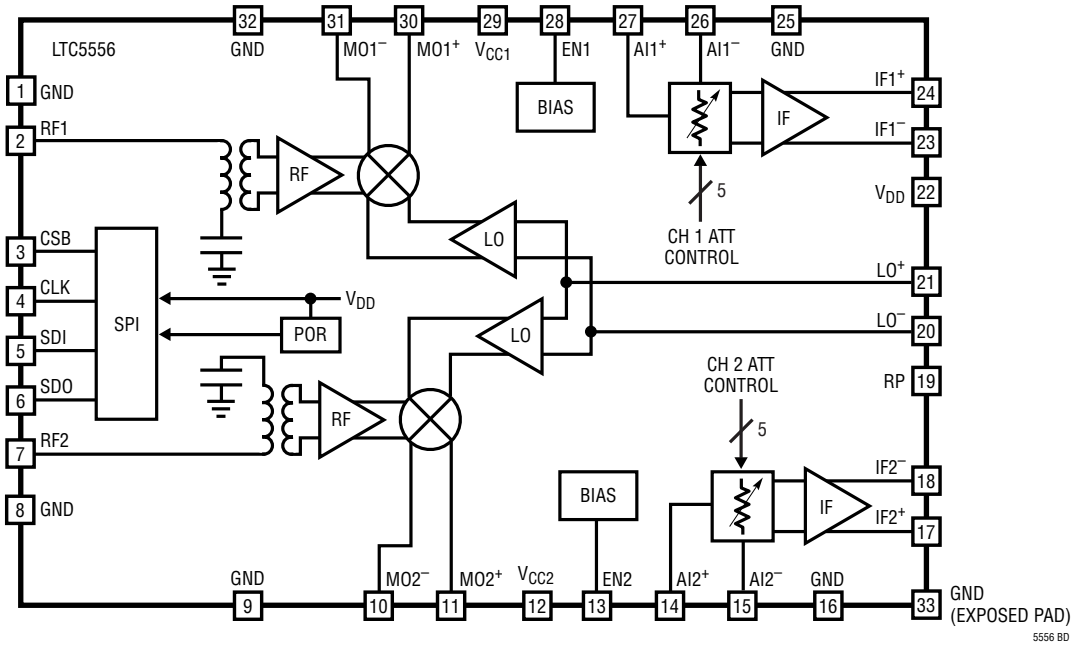
$IF2^+$, $IF2^-$, $IF1^-$, $IF1^+$ (Pins 17, 18, 23, 24): Open-Collector Differential IF Buffer Outputs for Channel 2 and Channel 1, Respectively. These pins must be connected to V_{CC} through pull-up inductors. Typical DC current is 47mA into each pin.

RP (Pin 19): Reduced Power Select Pin. A CMOS logic low on this pin commands both channels to full power mode, unless programmed to reduced power mode by the SPI. A CMOS logic high programs both channels to reduced power mode, independent of the SPI. This pin has an internal 330k pull-down resistor.

LO^-, LO^+ (Pins 20, 21): Differential Local Oscillator Input. These pins are internally connected to ESD diodes to ground. Therefore, series DC-blocking capacitors must be used if the LO source has a DC voltage present. Single-ended or differential drive may be used. Each pin is internally matched to 50Ω, even when the mixers are disabled.

V_{DD} (Pin 22): Power Supply Pin for Serial Interface Logic. This pin must be connected to a regulated 1.8V to 3.3V supply. Typical DC current consumption is less than 1mA with CSB low and the clock running at 10MHz. When idle, typical current consumption is less than 500µA. The supply voltage on this pin defines the logic levels for the SPI inputs (CSB, CLK and SDI), the SDO output, and the RP pin.

BLOCK DIAGRAM



TEST CIRCUIT

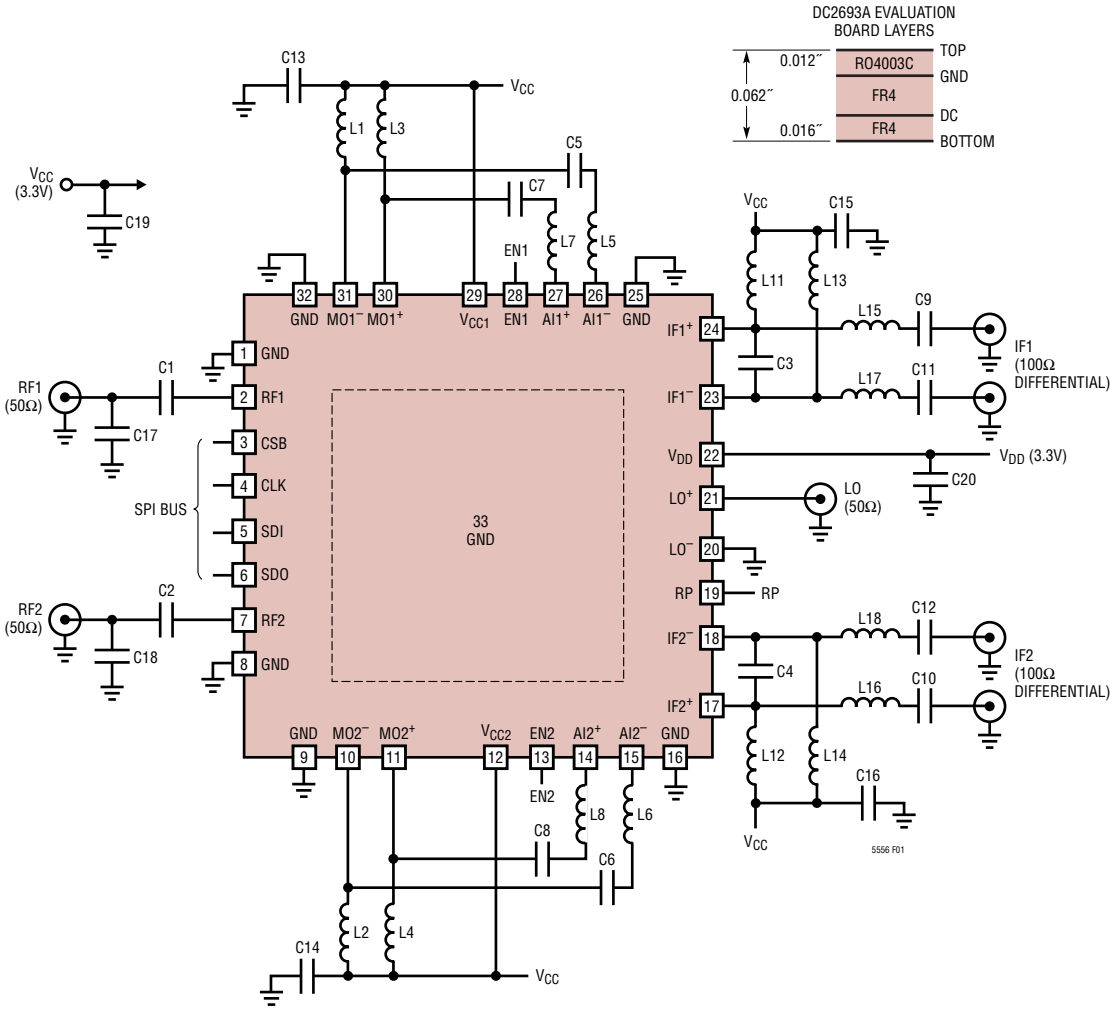


Figure 1. Test Circuit Schematic with 100Ω Matched Differential IF Outputs

RF INPUT MATCHING			
BAND	**RF RANGE (GHz)**	**C1, C2**	**C17, C18**
B1	1.5 to 2.1	7pF	2pF
B2	2.2 to 3.2	2pF	0.7pF
B3	2.6 to 6.4	1pF	—
B4	5.6 to 7.2	1.1pF	0.3pF

REF DES	VALUE	SIZE	VENDOR	REF DES	VALUE	SIZE	VENDOR
C19, C20	1µF	0603	Murata 50V X5R	C17, C18	see Table	0402	Murata 50V NPO
C1, C2	See Table	0402	Murata 50V NPO	L1 to L4, L11 to L14	680nH	0603	Coilcraft 0603AF
C3, C4	1.2pF	0402	Murata 50V NPO	L5 to L8	18nH	0201	Murata LQP03HQ
C5 to C8	1nF	0201	Murata 50V NPO				
C9 to C16	10nF	0402	Murata 50V X7R	L15 to L18	20nH	0402	Coilcraft 0402HP

APPLICATIONS INFORMATION

Introduction

The LTC5556 incorporates two identical RF-to-IF down-conversion mixers driven by a common LO input. The symmetry of the IC assures that both mixers are driven with an amplitude- and phase-coherent LO. Each channel includes an IF DVGA (digital variable gain amplifier) consisting of a programmable 15.5dB range digital IF attenuator with 0.5dB steps, and a fixed-gain IF buffer amplifier. The cascaded RF-to-IF conversion gain ranges from 9.5dB at maximum IF gain, to –6dB at minimum IF gain. The IF frequency response is flat within 1dB from 30MHz to 450MHz, and may be modified by changing the IF output match.

Each channel can be programmed to a reduced power mode via the SPI or the RP pin, resulting in a 24% power savings, with reduced linearity performance. The test circuit schematic in Figure 1 shows the external components used to characterize the IC. The evaluation board is shown in Figure 2.

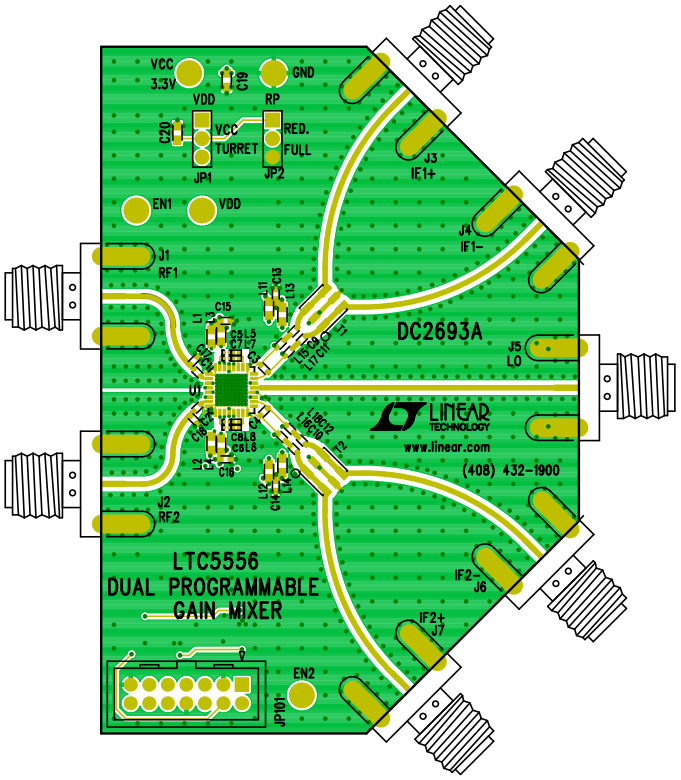


Figure 2. Evaluation Board

RF Inputs

A simplified schematic of the channel 1 RF input is shown in Figure 3 (channel 2 is identical and not shown). Each RF input includes an integrated transformer and a differential RF buffer amplifier. The transformer's primary winding is biased at 1.65V_{DC}, and therefore requires an external DC-blocking capacitor.

The RF inputs are 50Ω matched from 2.6GHz to 6.4GHz, requiring only a 1pF series capacitor (C1) for DC-blocking. Shunt reactance C17 is used to tune the inputs down to 1.5GHz, or up to 7GHz. Figure 1 summarizes the external matching component values for all bands. Measured RF input return loss for each band is shown in Figure 4.

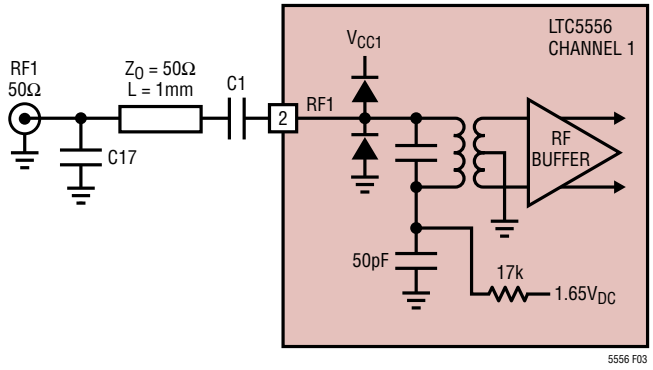


Figure 3. RF Input Schematic

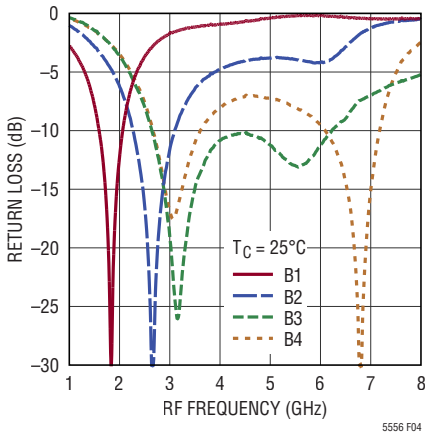


Figure 4. RF Input Return Loss for Each Band

APPLICATIONS INFORMATION

LO Input

A simplified schematic of the LO input is shown in Figure 5. As shown, each mixer has its own LO amplifier. A differential input is provided although the IC is characterized and production-tested with single-ended drive. Differential LO drive improves performance slightly, and is recommended if available. Each LO input is internally matched to 50Ω from 500MHz to 8GHz, requiring no external components. ESD protection diodes on each input limit the peak voltage swing to approximately ±700mV (+7dBm), although higher LO drive, up to 10dBm will not damage the input. An external DC-blocking capacitor is only needed if the LO source has DC voltage present. The measured LO input return loss is shown in Figure 6.

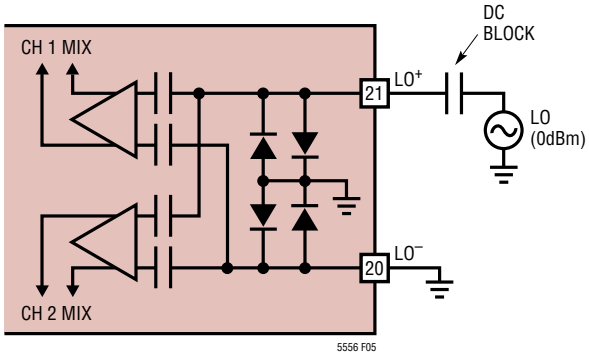


Figure 5. LO Input Schematic

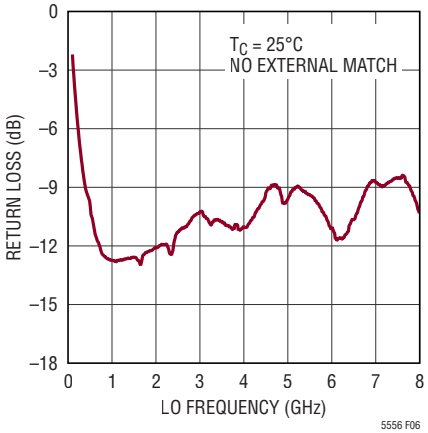


Figure 6. LO Input Return Loss

IF Outputs

A simplified IF output schematic for channel 1, with external matching components is shown in Figure 7 (channel 2 is identical, and not shown). The final output stage is differential, open-collector with integrated matching resistors, capacitors and ESD protection diodes. Each output pin must be biased at the supply voltage (V_{CC}) using external chokes (L11 and L13). Each pin draws approximately 47mA of DC supply current (94mA total). Therefore, inductors with low DC resistance (<1Ω), are required for the highest output IP3 and P1dB.

The integrated output resistors set the differential output resistance at 206Ω. C3, L15 and L17 form a 2:1 impedance transformer which transforms the output to 100Ω differential. If a 200Ω output is desired, C3 is not used and the values of L15 and L17 are reduced to the values shown in Table 1. C9 and C11 are DC-blocking capacitors, which may be omitted if the following stage is already DC-blocked.

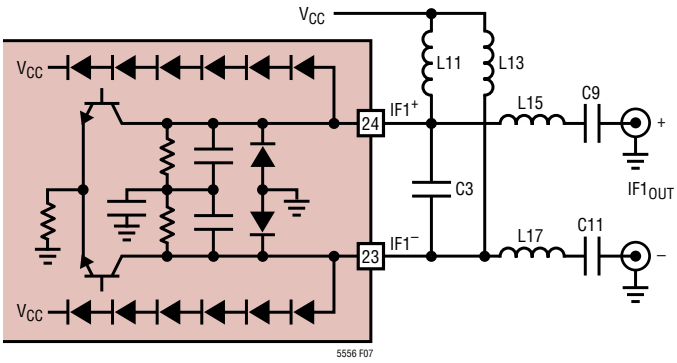


Figure 7. IF Output Schematic

APPLICATIONS INFORMATION

The standard evaluation board is built with 100Ω differential IF outputs, but also has pads which allow the use of IF transformers to provide 50Ω single-ended outputs. To implement this, it is recommended to use the 200Ω matching shown in Table 1 and 4:1 IF transformers. Figure 16 shows the circuit schematic and measured performance using this approach.

Table 1. IF Output Matching Element Values

DIFFERENTIAL Z_{OUT}	C3	L15, L17	9dB RETURN LOSS BANDWIDTH
200Ω*	—	10nH	23MHz to 440MHz
100Ω	3.9pF	47nH	70MHz to 242MHz
	2.2pF	33nH	87MHz to 352MHz
	1.2pF	20nH	115MHz to 495MHz
	0.6pF	16nH	155MHz to 610MHz
	—	12nH	190MHz to 810MHz

*200Ω differential output return loss measured with 4:1 transformer.

The differential IF output impedance vs frequency is listed in Table 2. The impedances are at the package pins with no external components. Measured IF output return loss vs frequency is shown in Figure 8.

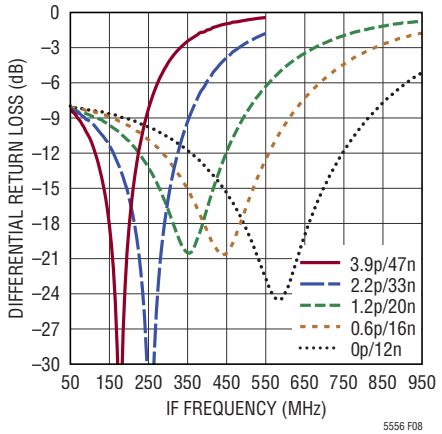


Figure 8. IF Output Return Loss (100Ω Differential)

Table 2. Differential IF Output Impedance vs Frequency

IF FREQUENCY (MHz)	DIFFERENTIAL IMPEDANCE (R_{IF} || C_{IF})
10	210 || 1.10pF
50	209 || 1.09pF
100	209 || 1.04pF
150	208 || 0.97pF
200	207 || 0.94pF
300	206 || 0.92pF
400	203 || 0.93pF
500	200 || 0.91pF
600	196 || 0.91pF
700	192 || 0.91pF
800	186 || 0.91pF
900	179 || 0.90pF
1000	172 || 0.89pF

Mixer Output to IF DVGA Interface

The mixer's 200Ω differential output impedance matches the IF DVGA's 200Ω differential input impedance, even over normal process variation due to the monolithic implementation. This assures minimal and repeatable DNL and INL over the full IF attenuation range. Furthermore, the mixer output and DVGA input include integrated matched capacitors, which simplify the realization of a lowpass filter between the mixer and DVGA. This filter attenuates undesired high frequency mixing products and LO leakage before entering the DVGA.

A simplified schematic of the interface for channel 1 is shown in Figure 9 (channel 2 is identical and not shown). L5 and L7 connect the mixer output to the DVGA input, while forming a 1GHz 3rd-order, 0.2dB ripple Chebyshev lowpass filter. L1 and L3 supply DC current to the mixer and C5 and C7 are DC-blocking capacitors.

APPLICATIONS INFORMATION

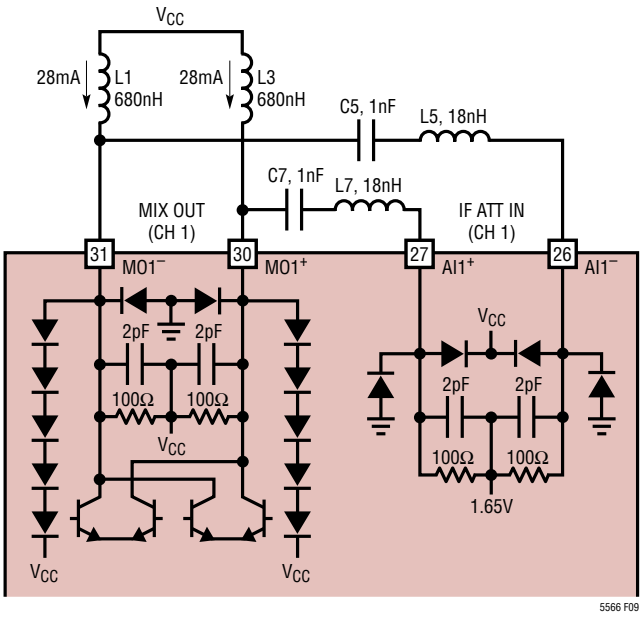


Figure 9. Mixer to IF DVGA Interface

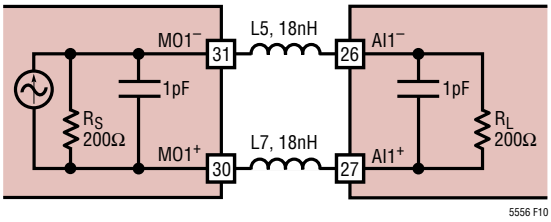


Figure 10. Equivalent Lowpass Filter Schematic

An equivalent AC schematic of the lowpass filter is shown in Figure 10, where the mixer output and DVGA input are modeled as 200Ω in parallel with 1pF. The mixer supply chokes and series DC blocking capacitors are ignored in this schematic.

It's also possible to implement a bandpass filter between the mixer and DVGA. An example is shown in Figure 11, where a 3rd-order bandpass filter is realized by changing the values of the reactive components and adding C21, C23 and L19. Figure 19 shows measured conversion gain vs IF output frequency using this bandpass topology.

IF DVGA Phase vs IF Attenuation

Ideally, the phase of the IF output would be constant over the full IF attenuation range. Practically, there is some phase shift due to circuit parasitics in the attenuator. The LTC5556's IF DVGA is optimized for the lowest possible phase variation (or phase error) over the full IF attenuation range. Phase error vs IF attenuation for the complete IF section is listed in Table 3.

Table 3. IF Phase Error vs IF Attenuation

ATT (dB)	250MHz	350MHz	500MHz
0	REF	REF	REF
3	–1.4°	–2.3°	–1.6°
6	–2.5°	–3.5°	–3.3°
9	–3.2°	–4.4°	–4.5°
12	–3.7°	–5.0°	–5.1°
15	–3.6°	–4.7°	–4.5°

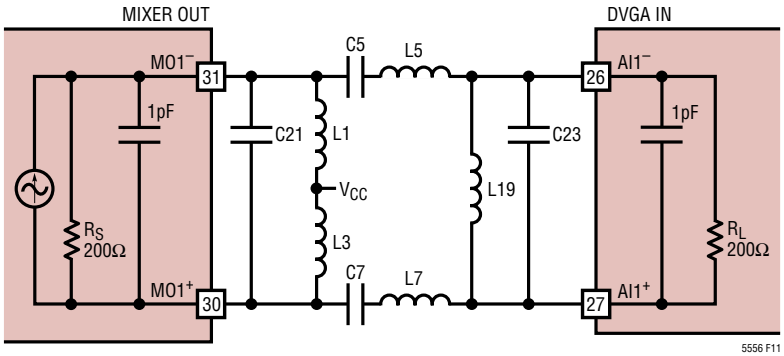


Figure 11. 3rd-Order Bandpass Filter Realization

APPLICATIONS INFORMATION

Downconverter Performance vs IF Attenuation

RF-IF conversion gain, IIP3, OIP3 and noise figure over the full 15.5dB attenuation range is shown in Figure 12. The same data is listed in Table 4 with the INL and DNL at each attenuator setting.

Table 4. Conversion Gain, IIP3, OIP3 and SSB NF vs IF Attenuation (RF = 3.6GHz, IF = 270MHz, Low Side LO)

A (dB)	IF1[4:0] IF2[4:0]	G_C (dB)	IIP3 (dBm)	OIP3 (dBm)	NF (dB)	DNL (dB)	INL (dB)
0	0	9.13	22.2	31.3	14.1	–	–
0.5	1	8.70	22.6	31.3	14.2	–0.07	–0.07
1.0	2	8.11	22.4	30.5	14.5	0.09	0.02
1.5	3	7.66	22.7	30.4	14.7	–0.05	–0.03
2.0	4	7.12	22.8	29.9	14.9	0.04	0.01
2.5	5	6.66	23.2	29.8	15.0	–0.04	–0.03
3.0	6	6.12	23.0	29.1	15.2	0.04	0.01
3.5	7	5.66	23.4	29.1	15.4	–0.04	–0.03
4.0	8	5.12	23.2	28.4	15.6	0.04	0.01
4.5	9	4.65	23.7	28.3	15.9	–0.03	–0.02
5.0	10	4.12	23.4	27.6	16.1	0.03	0.01
5.5	11	3.65	23.9	27.5	16.4	–0.03	–0.02
6.0	12	3.11	23.6	26.7	16.6	0.04	0.02
6.5	13	2.64	24.0	26.6	16.9	–0.03	–0.01
7.0	14	2.10	23.7	25.8	17.2	0.04	0.03
7.5	15	1.62	24.1	25.7	17.6	–0.02	0.01
8.0	16	1.08	23.8	24.9	18.0	0.04	0.05
8.5	17	0.61	24.2	24.8	18.2	–0.03	0.02
9.0	18	0.07	23.9	24.0	18.6	0.04	0.06
9.5	19	–0.41	24.3	23.9	19.0	–0.02	0.04
10.0	20	–0.95	23.9	23.0	19.4	0.04	0.08
10.5	21	–1.43	24.3	22.9	19.7	–0.02	0.06
11.0	22	–1.97	24.0	22.0	20.1	0.04	0.10
11.5	23	–2.46	24.3	21.9	20.5	–0.01	0.09
12.0	24	–2.99	24.1	21.1	21.0	0.03	0.12
12.5	25	–3.48	24.5	21.0	21.5	–0.01	0.11
13.0	26	–4.02	24.1	20.1	22.0	0.04	0.15
13.5	27	–4.50	24.5	20.0	22.4	–0.02	0.13
14.0	28	–5.05	24.2	19.1	22.9	0.05	0.18
14.5	29	–5.53	24.4	18.9	23.2	–0.02	0.16
15.0	30	–6.09	24.2	18.1	23.5	0.06	0.22
15.5	31	–6.57	24.5	17.9	24.0	–0.02	0.20

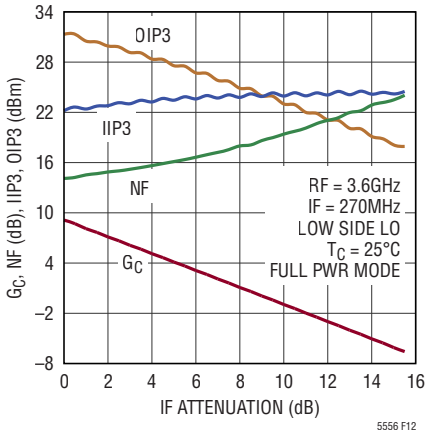


Figure 12. Downconverter RF-IF Conversion Gain, IIP3, OIP3 and Noise Figure vs IF Attenuation.

Individual Stage Performance

The LTC5556 is characterized, specified and production-tested as a complete downconverter, from the RF inputs to the final IF outputs. For some applications, it may be preferred to insert a higher selectivity IF filter between the mixer and IF DVGA. To help with system performance calculations, the nominal performance of the mixer is shown in Table 5 and the IF DVGA performance is listed in Table 6. This information is provided for reference only as these blocks are not production-tested independently.

Table 5. Mixer Power Conversion Gain, IIP3 and SSB NF (RF = 3.6GHz, IF = 270MHz, Low Side LO)

FULL PWR MODE			REDUCED PWR MODE		
G_P (dB)	IIP3 (dBm)	NF (dB)	G_P (dB)	IIP3 (dBm)	NF (dB)
–1	26	13	–1.3	21	11

Table 6. IF DVGA Power Gain, OIP3 and SSB NF (270MHz)

IF ATT (dB)	FULL PWR MODE			REDUCED PWR MODE		
	GAIN (dB)	OIP3 (dBm)	NF (dB)	GAIN (dB)	OIP3 (dBm)	NF (dB)
0	10.2	36.5	6.2	10.0	33.5	6.2
3	7.2	36.5	9.9	7.0	33.2	10.0
6	4.2	36.5	13.0	4.0	33.2	12.9
9	1.2	36.5	15.9	1.0	33.2	15.9
12	–1.8	36.2	18.9	–2.0	33.1	18.9
15	–4.8	36.0	21.9	–5.0	32.7	21.9

APPLICATIONS INFORMATION

Enable Inputs

Figure 13 shows a schematic of the Channel 1 enable interface. Channel 2 is identical and not shown. As shown, the positive ESD diodes for EN1 are connected to V_{CC1}. The positive ESD diodes for channel 2 are connected to V_{CC2} (not shown). To enable a channel, the applied voltage must be greater than 1.4V. An applied voltage less than 0.5V will disable the channel. If the enable function is not needed, the enable pin can be connected directly to the adjacent V_{CC} pin. If left floating, the internal 330kΩ pull-down resistor will disable the channel.

The voltage on the enable pins should never exceed V_{CC} by more than 0.3V, otherwise supply current may be sourced through the upper ESD diodes. Under no circumstances should voltage be applied to the enable pins before supply voltage is applied to the V_{CC} pins. If this occurs, damage to the IC may result.

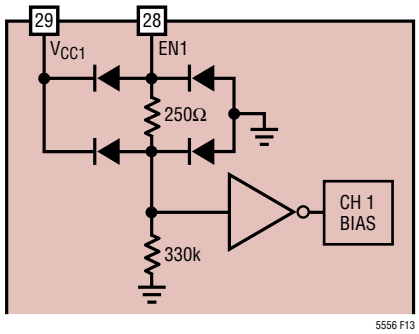


Figure 13. Channel 1 Enable Pin Interface

Supply Voltage Ramping

Fast ramping of the supply can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time greater than 1ms is recommended.

Supply voltage for V_{CC1}, V_{CC2} (Pins 29 and 21) and the IF amplifiers (Pins 17, 18, 23 and 24) are connected on the evaluation board, which assures that they all ramp up and down at the same rate. If they are powered independently in the final application circuit, care must be taken to assure that the IF amplifier supply pins go high before the V_{CC} pins, and go low after the V_{CC} pins.

SPI DESCRIPTION

IF DVGA attenuator control and reduced power mode for each downconverter channel is programmed through the 3-wire SPI consisting of CSB, CLK and SDI. A fourth pin, SDO, is a serial output available to read out the contents of the registers. The SDO pin may also be used to daisy-chain multiple SPI interfaces on a single bus. For example, in an 8-channel MIMO receiver application, all four LTC5556 dual downconverters can be programmed with a single, 64-bit load, while sharing a common CSB line.

A block diagram of the SPI is shown in Figure 14. As shown, it is a 16-bit double-buffered FIFO slave architecture, with 8-bits for each channel. Logic levels for the digital inputs and SDO output are 1.8V to 3.3V CMOS compatible, determined by the supply voltage on the V_{DD} pin. An internal POR (power-on-reset) connected to the V_{DD} pin, resets all 16 bits to logic 0 at power-up, or when V_{DD} drops below 0.5V and then rises back above 1.2V. The POR requires approximately 100µs to reset the registers.

SPI PROGRAMMING

Data transfers to the part are accomplished by first taking CSB low to enable the port. Then, serial input data on SDI is captured on the rising edge of CLK and shifted into a 16-bit shift register, MSB first. Serial data from the registers is driven out to SDO on the clock's falling edge. The communication burst is terminated by taking CSB high. The rising edge on CSB will then latch the shift-register's contents into a 16-bit buffer D-latch. The buffer latch prevents the downconverter's gain and power mode from changing while data is loaded. See Figure 15 for timing details.

When CSB is high, the clock and data inputs are internally gated off, minimizing current consumption when not selected, and the SDO output is high impedance. However, it is recommended that the serial interface signals should remain idle between data transfers to avoid digital noise coupling into the RF signal paths.

APPLICATIONS INFORMATION

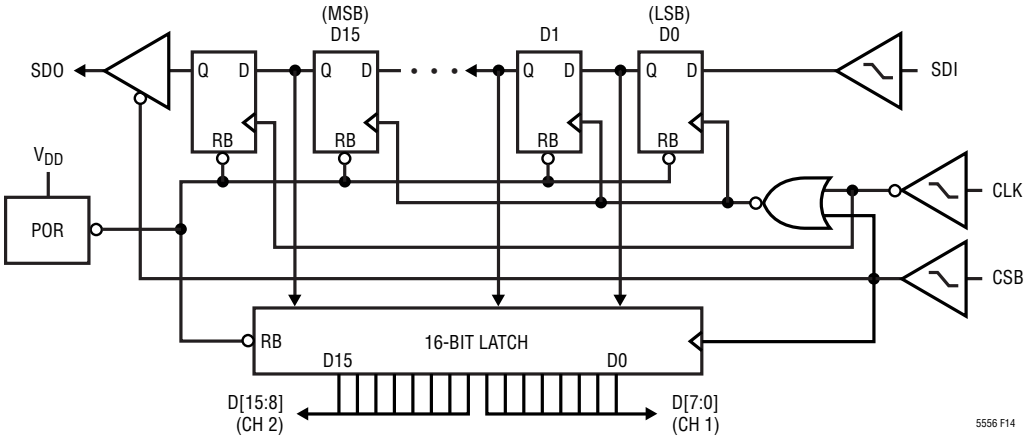


Figure 14. SPI Block Diagram

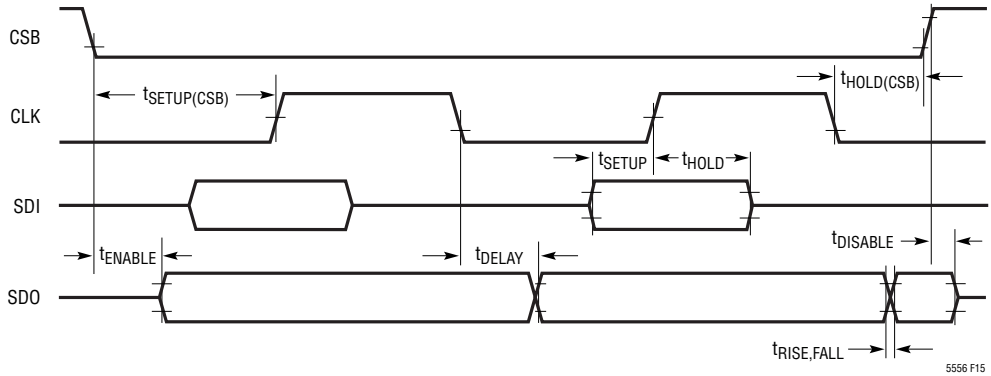


Figure 15. SPI Timing Diagram

APPLICATIONS INFORMATION

A memory map of the register contents is shown in Table 7, with detailed bit descriptions in Table 8. Each register's default power-up value is also shown in Table 8, which is:

- 0dB IF attenuation (maximum gain)
- Full power mode

When the logic level on RP (Pin 19) is low, each channel may be independently programmed to reduced power mode via the RP1 and RP2 bits in the SPI. When RP pin is driven high, both channels are commanded to reduced power mode and the RP1 and RP2 bits from the SPI are ignored.

Table 7. Serial Port Register Contents

CHANNEL 2 (8 bits)							
MSB D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
RP2	X	X	IF2[4]	IF2[3]	IF2[2]	IF2[1]	IF2[0]

CHANNEL 1 (8 bits)							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB D0**
RP1	X	X	IF1[4]	IF1[3]	IF1[2]	IF1[1]	IF1[0]

Table 8. Serial Port Register Bit Field Summary

BITS	DESCRIPTION	DEFAULT
IF1[4:0]	Ch. 1 IF Attenuator Control	00000 (Max Gain)
RP1	Ch. 1 Reduced Power	0 (Full Power)
IF2[4:0]	Ch. 2 IF Attenuator Control	00000 (Max Gain)
RP2	Ch. 2 Reduced Power	0 (Full Power)
X	Don't Care (Bits Not Used)	0

Spurious Output Levels

Spurious output levels vs harmonics of the RF and LO are tabulated in Table 9. The spur levels were measured using the test circuit shown in Figure 1, with an RF input power of –6dBm and 3dB of IF attenuation. Table 9a shows the relative spur levels in full power mode and Table 9b shows the relative spur levels in reduced power mode. The mixer spur levels are insensitive to the IF attenuation setting.

The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$$

Table 9. IF Output Spur Levels (dBc).
($RF = 3.6GHz$, $P_{RF} = -6dBm$, $IF = 270MHz$, Low Side LO, $P_{LO} = 0dBm$, 3dB IF Attenuation, $T_C = 25°C$)
Table 9a. Full Power Mode

		N					
		0	**1**	**2**	**3**	**4**	**5**
M	**0**		–47	–82	*	–82	–82
	1	–79	0	–77	*	*	*
	2	*	*	–64	*	*	*
	3	*	*	*	–71	*	*
	4	–83	*	*	*	*	*
	5	–84	–82	*	*	*	*

*Less than –85dBc

Table 9b. Reduced Power Mode

		N					
		0	**1**	**2**	**3**	**4**	**5**
M	**0**		–46	–82	*	–82	–82
	1	–78	0	–78	*	*	*
	2	–84	*	–64	*	*	*
	3	*	*	*	–70	*	*
	4	–82	*	*	*	*	*
	5	–83	–82	–84	*	*	*

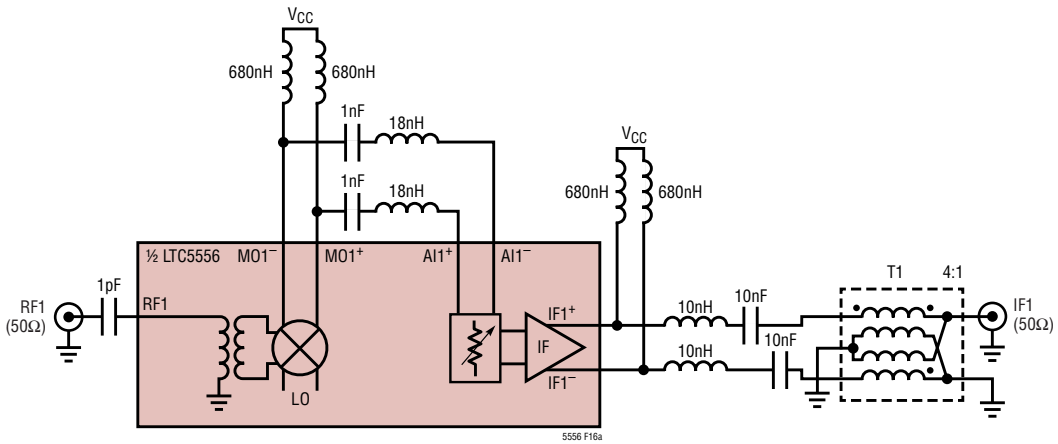
*Less than –85dBc

APPLICATIONS INFORMATION

Single-Ended IF Outputs Using a Balun

The LTC5556 evaluation board has differential IF outputs, but can be modified for single-ended operation by inserting a 4:1 balun, as shown in Figure 16. The 10nH series inductors at the differential IF output compensate for the IF amplifier's output capacitance, producing a 200Ω differential output up to approximately 500MHz. The 4:1 balun then converts the 200Ω differential output to 50Ω single-ended. For applications with IF frequency less than 250MHz, the series 10nH inductors are not needed.

Figure 16 shows the measured conversion gain vs IF output frequency, using a Mini-Circuits TCM4-19+ balun. The RF input was swept from 3.35GHz to 3.85GHz using a fixed 3.33GHz LO, producing an IF output ranging from 20MHz to 520MHz. Measured conversion gain for the standard 100Ω differential output matching is also shown on the same graph for comparison, highlighting the insertion loss of the balun.



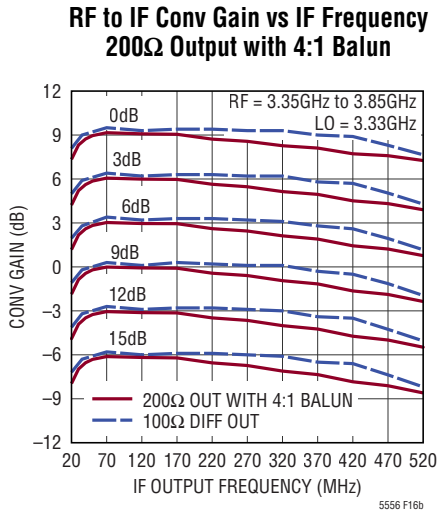


Figure 16. Test Circuit and Measured Conversion Gain Using 200Ω Output Matching with a 4:1 IF Transformer to Realize a 50Ω Single-Ended IF Output

APPLICATIONS INFORMATION

5.6GHz to 7.2GHz RF Application with Wideband IF

The LTC5556's RF inputs are optimized for operation up to 6GHz, but may be used up to 8GHz with degraded performance. Figure 17 shows an example where the RF input is matched from 5.6GHz to 7.2GHz and the IF output is matched for wideband operation up to 800MHz.

The measured performance is summarized in Figure 18, where the RF input is swept from 6.1GHz to 6.9GHz, with a fixed 6.03GHz LO, resulting in a wideband 70MHz to 870MHz IF output, centered at 470MHz.

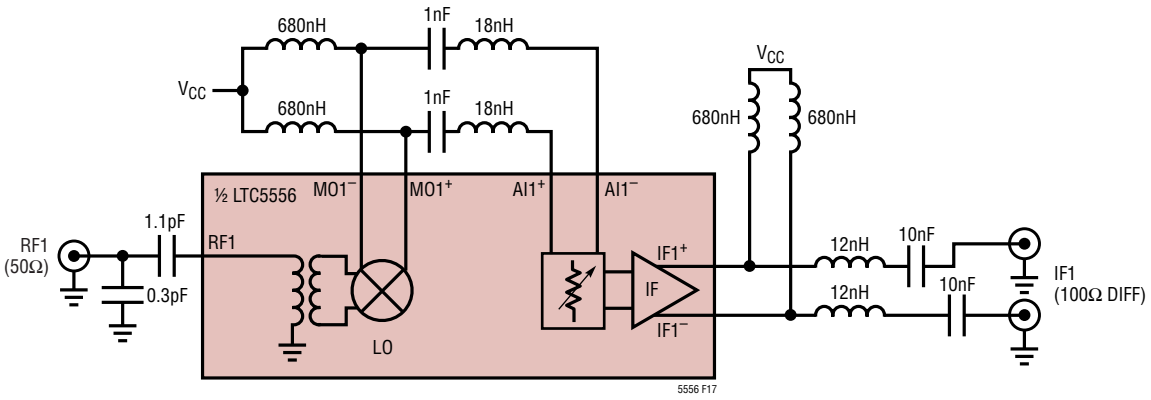


Figure 17. 5.6GHz to 7.2GHz Input Matching with Wideband IF Output Match

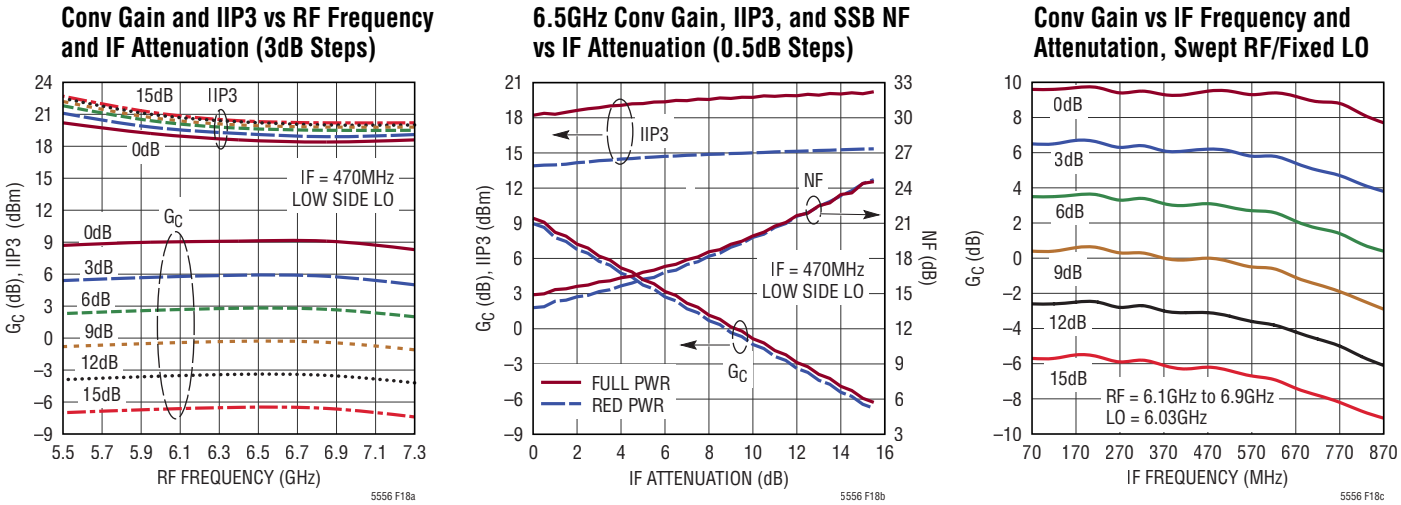
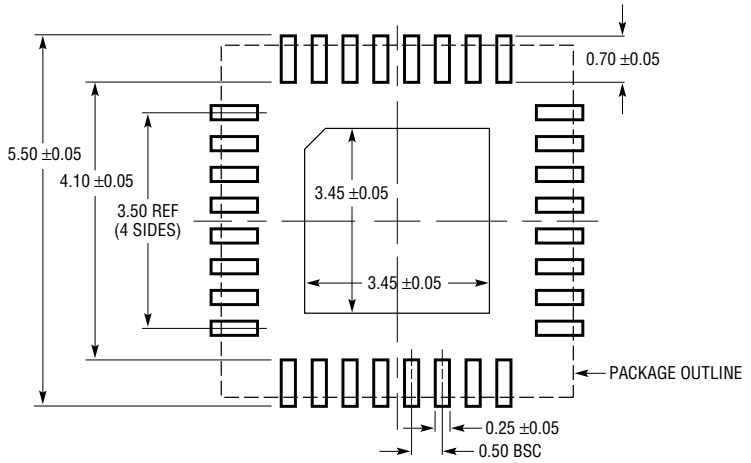


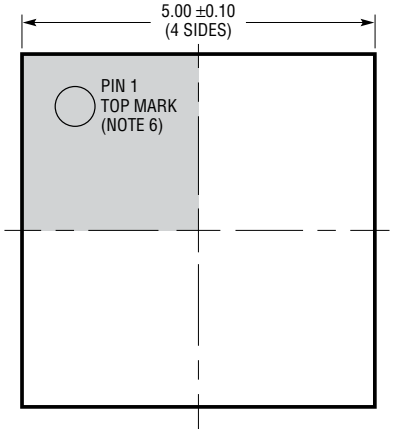
Figure 18. Measured Performance for 5.6GHz to 7.2GHz Downconverter with Wideband IF Output

PACKAGE DESCRIPTION

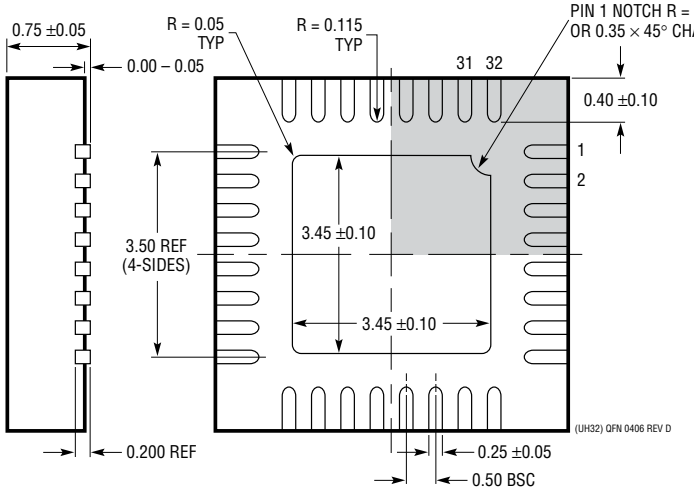
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

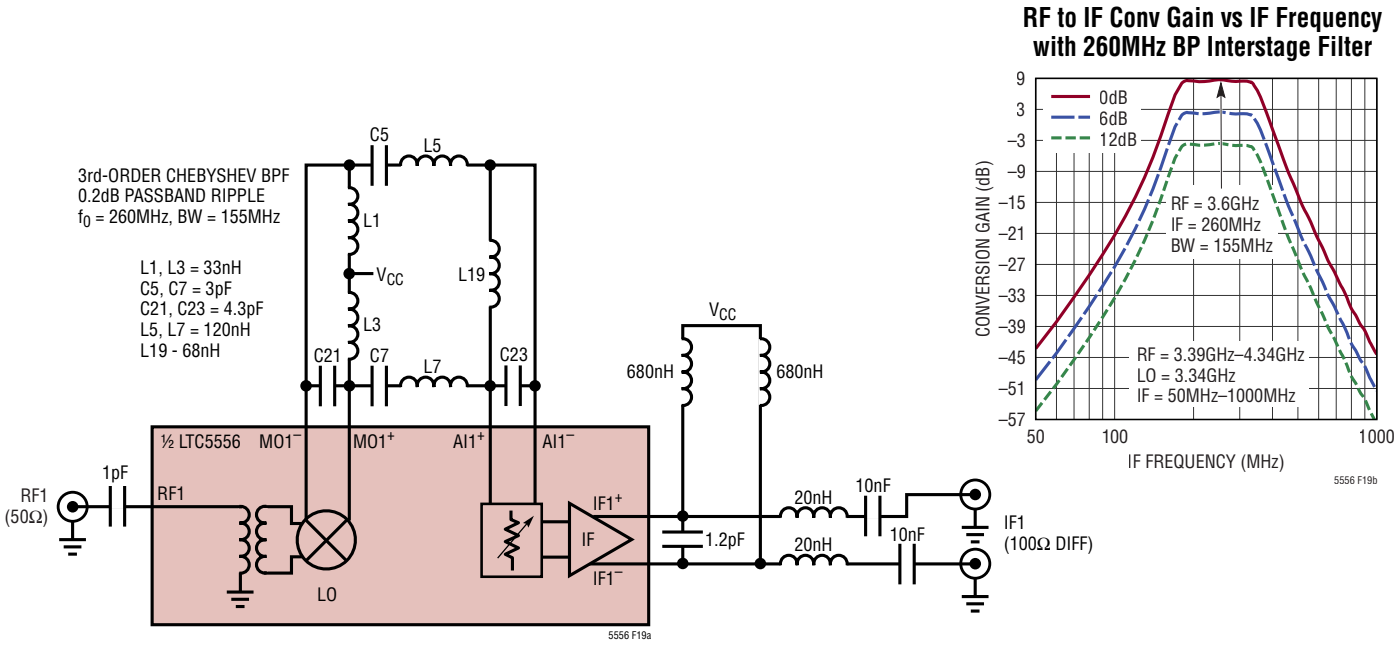


Figure 19. Test Circuit and Measured Conversion Gain with 3rd-Order Bandpass Interstage Filter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LTC5566	300MHz to 6GHz Dual Programmable Gain Downconverting Mixer	12dB Gain, 35dBm OIP3 and 13.3dB NF at 2.6GHz
LTC5569	300MHz to 4GHz Dual Active Downconverting Mixer	2dB Gain, 26.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/180mA Supply
LTC6430	High Linearity Differential RF/IF Amplifier	51dBm OIP3 at 240MHz, 100Ω Differential
LTC5544	4GHz to 6GHz Downconverting Mixer Family	7.4dB Gain, >25dBm IIP3, 11.3dB NF, 3.3V/200mA Supply
LT5554	Ultralow Distortion IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
LTC5576	3GHz to 8GHz Active Upconverting Mixer	25dBm OIP3, –0.6dB Gain, –154dBm/Hz Output Noise Floor, –36dBm LO Leakage
LTC5548	2GHz to 14GHz Wideband Microwave Mixer	Up- or Down-Conversion, 21.4dBm IIP3 at 9GHz, 0dBm LO Drive, IF Bandwidth DC to 6GHz
LTC5549	2GHz to 14GHz Wideband Microwave Mixer	Up- or Down-Conversion, 22.8dBm IIP3 at 12GHz, 0dBm LO Drive, Integrated Balun with IF BW = 500MHz to 6GHz
LTC5593	Dual 2.3GHz to 4.5GHz Downconverting Mixer	8.5dB Gain, 27.7dBm IIP3, 9.5dB Noise Figure
RF PLL/Synthesizer with VCO		
LTC6946	Low Noise, Low Spurious Integer-N PLL with Integrated VCO	373MHz to 5.79GHz, –157dBc/Hz WB Phase Noise Floor, –100dBc/Hz Closed-Loop Phase Noise
LTC6948	Low Noise, Low Spurious Frac-N PLL with Integrated VCO	373MHz to 6.39GHz, –157dBc/Hz WB Phase Noise Floor, –274dBc/Hz Normalized In-Band 1/f Noise
ADCs		
LTC2145-14	14-Bit, 125Msps 1.8V Dual ADC	73.1dB SNR, 90dB SFDR, 95mW/Ch Power Consumption
LTC2185	16-Bit, 125Msps 1.8V Dual ADC	76.8dB SNR, 90dB SFDR, 185mW/Channel Power Consumption
LTC2158-14	14-Bit, 310Msps 1.8V Dual ADC, 1.25GHz Full-Power Bandwidth	68.8dB SNR, 88dB SFDR, 362mW/Ch Power Consumption, 1.32V_{P-P} Input Range