UV, OV and Reverse Supply Protection Controller

FEATURES

- **Wide Operating Voltage Range: 2.5V to 34V**
- **Overvoltage Protection to 60V**
- **Reverse Supply Protection to –40V**
- **Blocks 50Hz and 60Hz AC Power**
- **No Input Capacitor or TVS Required for Most Applications**
- Adjustable Undervoltage and Overvoltage Protection Range
- Charge Pump Enhances External N-Channel MOSFET
- Low Operating Current: 125µA
- Low Shutdown Current: 10µA
- Fault Status Output
- Compact 8-Lead, 3mm × 2mm DFN and TSOT-23 (ThinSOT™) Packages

APPLICATIONS

- Portable Instrumentation
- Industrial Automation
- Laptops
- Automotive

DESCRIPTION

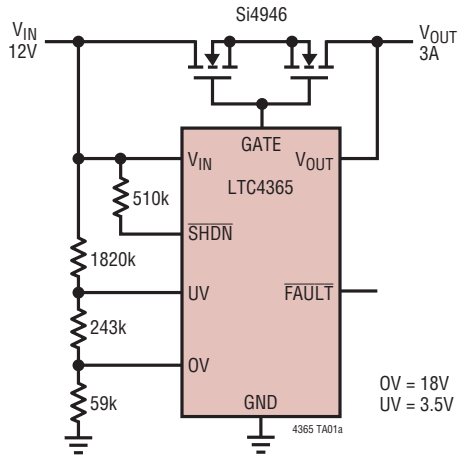
The LTC®4365 protects applications where power supply input voltages may be too high, too low or even negative. It does this by controlling the gate voltages of a pair of external N-channel MOSFETs to ensure that the output stays within a safe operating range.

The LTC4365 can withstand voltages between –40V and 60V and has an operating range of 2.5V to 34V, while consuming only 125µA in normal operation.

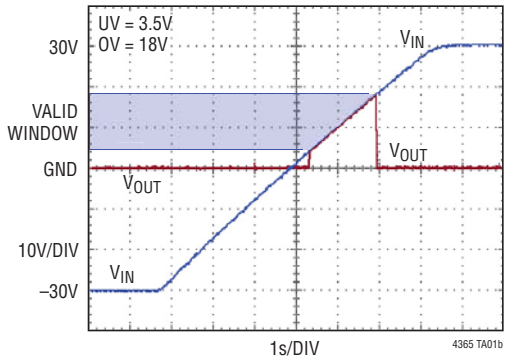
Two comparator inputs allow configuration of the overvoltage (OV) and undervoltage (UV) set points using an external resistive divider. A shutdown pin provides external control for enabling and disabling the MOSFETs as well as placing the device in a low current shutdown state. A fault output provides status of the gate pin pulling low. A fault is indicated when the part is in shutdown or the input voltage is outside the UV and OV set points.

TYPICAL APPLICATION

12V Automotive Application



Load Protected from Reverse and Overvoltage at V_{IN}



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)
- V_{IN} ..... –40V to 60V

Input Voltages (Note 3)
- UV, $\overline{SHDN}$ ..... –0.3V to 60V
- OV ..... –0.3V to 6V
- V_{OUT} ..... –0.3V to 40V

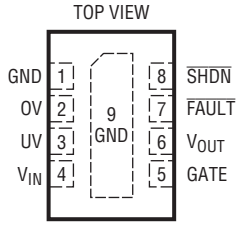
Output Voltages (Note 4)
- $\overline{FAULT}$ ..... –0.3V to 60V
- GATE ..... –40V to 45V

Operating Ambient Temperature Range
- LTC4365C ..... 0°C to 70°C
- LTC4365I ..... –40°C to 85°C
- LTC4365H ..... –40°C to 125°C

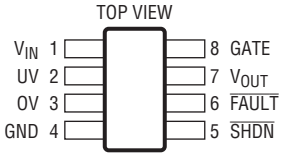
Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- for TSOT Only ..... 300°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) PCB GROUND CONNECTION OPTIONAL



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 195°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4365CDDB#TRMPBF	LTC4365CDDB#TRPBF	LFKS	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC4365IDDB#TRMPBF	LTC4365IDDB#TRPBF	LFKS	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC4365HDDB#TRMPBF	LTC4365HDDB#TRPBF	LFKS	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC4365CTS8#TRMPBF	LTC4365CTS8#TRPBF	LTFKT	8-Lead Plastic TSOT-23	0°C to 70°C
LTC4365ITS8#TRMPBF	LTC4365ITS8#TRPBF	LTFKT	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC4365HTS8#TRMPBF	LTC4365HTS8#TRPBF	LTFKT	8-Lead Plastic TSOT-23	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 2.5V to 34V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}, V_{OUT}							
V_{IN}	Input Voltage Range	Operating Range Protection Range	● ●	2.5 –40		34 60	V V
I_{VIN}	Input Supply Current	$\overline{SHDN}$ = 0V, V_{IN} = V_{OUT}, –40°C to 85°C $\overline{SHDN}$ = 0V, V_{IN} = V_{OUT}, –40°C to 125°C $\overline{SHDN}$ = 2.5V	● ● ●		10 10 25	50 100 150	µA µA µA
$I_{VIN(R)}$	Reverse Input Supply Current	V_{IN} = –40V, V_{OUT} = 0V	●		–1.2	–1.8	mA
$V_{IN(UVLO)}$	Input Supply Undervoltage Lockout	V_{IN} Rising	●	1.8	2.2	2.4	V
I_{VOUT}	V_{OUT} Input Current	$\overline{SHDN}$ = 0V, V_{IN} = V_{OUT} $\overline{SHDN}$ = 2.5V, V_{IN} = V_{OUT} V_{IN} = –40V, V_{OUT} = 0V	● ● ●		6 100 20	30 250 50	µA µA µA
GATE							
ΔV_{GATE}	N-Channel Gate Drive (GATE-V_{OUT})	V_{IN} = V_{OUT} = 5.0V, I_{GATE} = –1µA V_{IN} = V_{OUT} = 12V to 34V, I_{GATE} = –1µA	● ●	3 7.4	3.6 8.4	4.2 9.8	V V
$I_{GATE(UP)}$	N-Channel Gate Pull Up Current	GATE = V_{IN} = V_{OUT} = 12V	●	–12	–20	–30	µA
$I_{GATE(FAST)}$	N-Channel Gate Fast Pull Down Current	Fast Shutdown, GATE = 20V, V_{IN} = V_{OUT} = 12V	●	31	50	72	mA
$I_{GATE(SLOW)}$	N-Channel Gate Gentle Pull Down Current	Gentle Shutdown, GATE = 20V, V_{IN} = V_{OUT} = 12V	●	50	90	150	µA
$t_{GATE(FAST)}$	N-Channel Gate Fast Turn Off Delay	C_{GATE} = 2.2nF, UV or OV Fault	●		2	4	µs
$t_{GATE(SLOW)}$	N-Channel Gentle Turn Off Delay	C_{GATE} = 2.2nF, $\overline{SHDN}$ Falling, V_{IN} = V_{OUT} = 12V	●	150	250	350	µs
$t_{RECOVERY}$	GATE Recovery Delay Time	V_{IN} = 12V, Power Good to ΔV_{GATE} > 0V	●	26	36	49	ms
UV, OV							
V_{UV}	UV Input Threshold Voltage	UV Falling → ΔV_{GATE} = 0V	●	492.5	500	507.5	mV
V_{OV}	OV Input Threshold Voltage	OV Rising → ΔV_{GATE} = 0V	●	492.5	500	507.5	mV
V_{UVHYST}	UV Input Hysteresis		●	20	25	32	mV
V_{OVHYST}	OV Input Hysteresis		●	20	25	32	mV
I_{LEAK}	UV, OV Leakage Current	V = 0.5V, V_{IN} = 34V	●			±10	nA
t_{FAULT}	UV, OV Fault Propagation Delay	Overdrive = 50mV V_{IN} = V_{OUT} = 12V	●		1	2	µs
$\overline{SHDN}$							
V_{SHDN}	$\overline{SHDN}$ Input Threshold	$\overline{SHDN}$ Falling to ΔV_{GATE} = 0V	●	0.4	0.75	1.2	V
I_{SHDN}	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 0.75V, V_{IN} = 34V	●			±10	nA
t_{START}	Delay Coming Out of Shutdown Mode	$\overline{SHDN}$ Rising to ΔV_{GATE} > 0V, V_{IN} = V_{OUT} = 12V	●	400	800	1200	µs
$t_{SHDN(F)}$	$\overline{SHDN}$ to $\overline{FAULT}$ Asserted	V_{IN} = V_{OUT} = 12V	●		1.5	3	µs
t_{LOWPWR}	Delay from Turn Off to Low Power Operation	V_{IN} = V_{OUT} = 12V	●	26	36	55	ms
$\overline{FAULT}$							
V_{OL}	$\overline{FAULT}$ Output Voltage Low	I_{FAULT} = 500µA	●		0.15	0.4	V
I_{FAULT}	$\overline{FAULT}$ Leakage Current	$\overline{FAULT}$ = 5V, V_{IN} = 34V	●		±20		nA

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

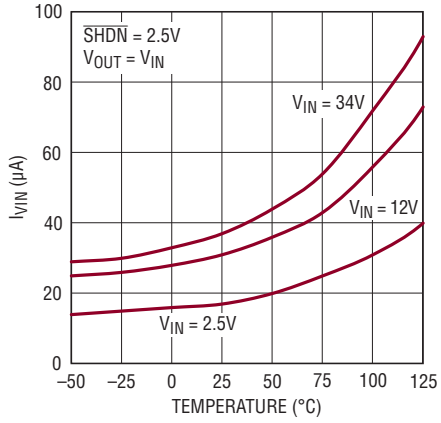
Note 2. All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3. These pins can be tied to voltages below –0.3V through a resistor that limits the current below 1mA.

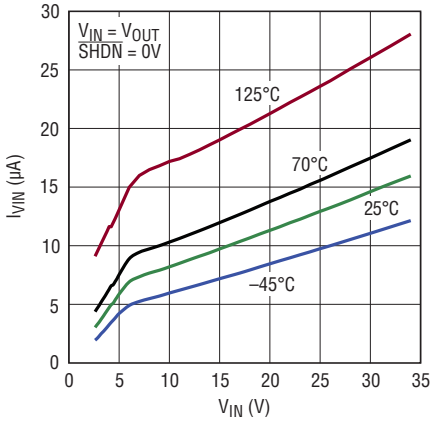
Note 4. The GATE pin is referenced to V_{OUT} and does not exceed 44V for the entire operating range.

TYPICAL PERFORMANCE CHARACTERISTICS

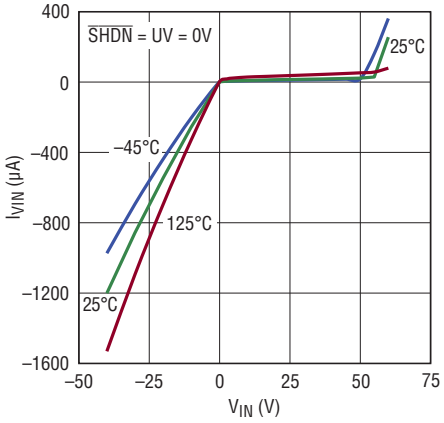
V_{IN} Operating Current vs Temperature



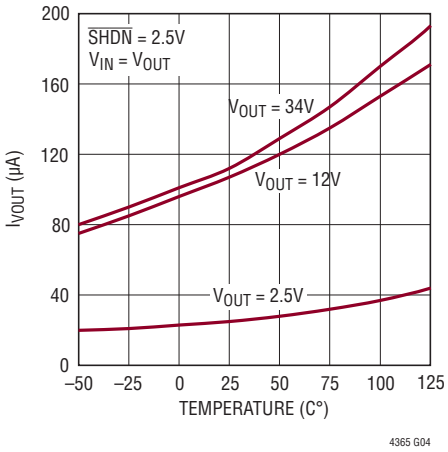
V_{IN} Shutdown Current vs V_{IN}



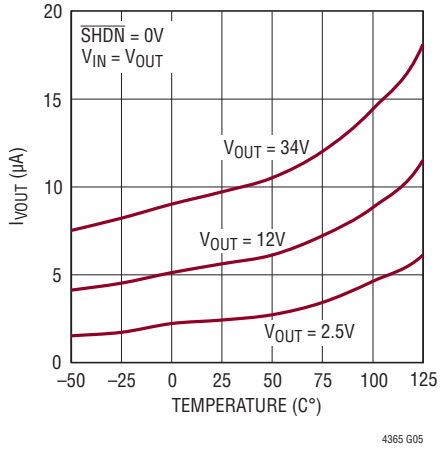
V_{IN} Current vs V_{IN} (–40 to 60V)



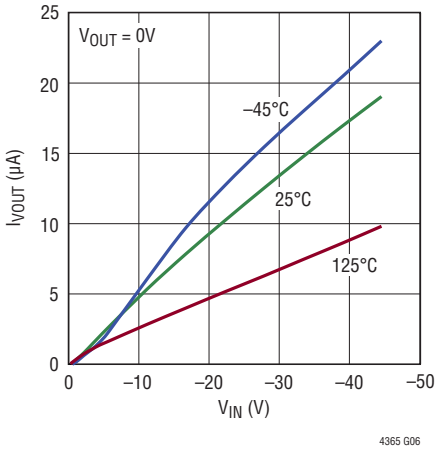
V_{OUT} Operating Current vs Temperature



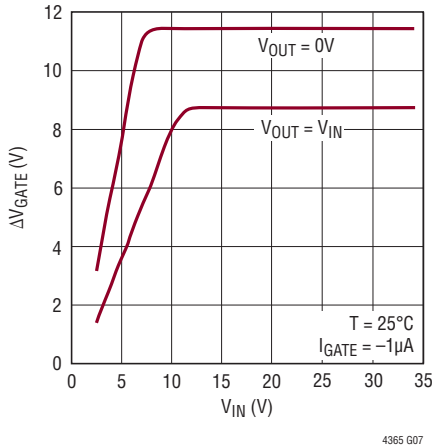
V_{OUT} Shutdown Current vs Temperature



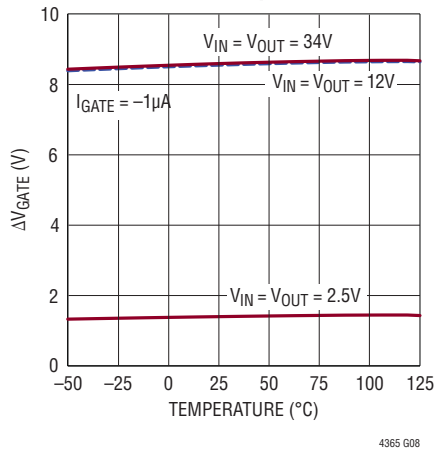
V_{OUT} Current vs Reverse V_{IN}



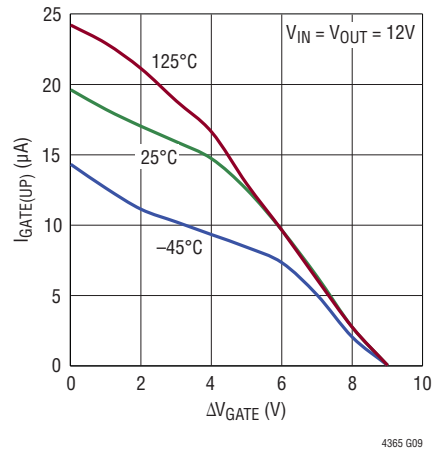
GATE Drive vs V_{IN}



GATE Drive vs Temperature

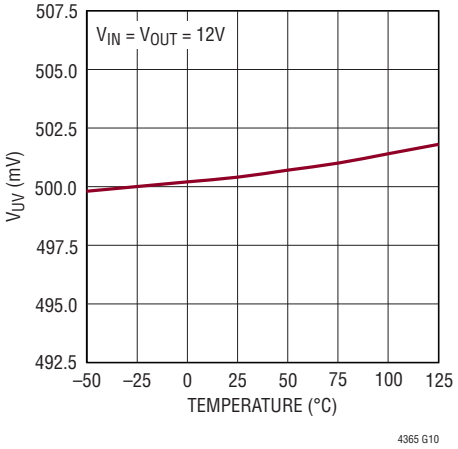


GATE Current vs GATE Drive

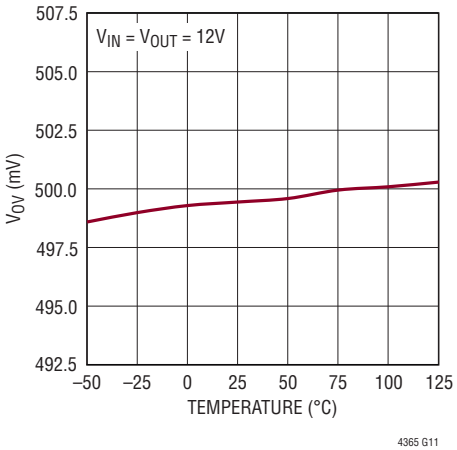


TYPICAL PERFORMANCE CHARACTERISTICS

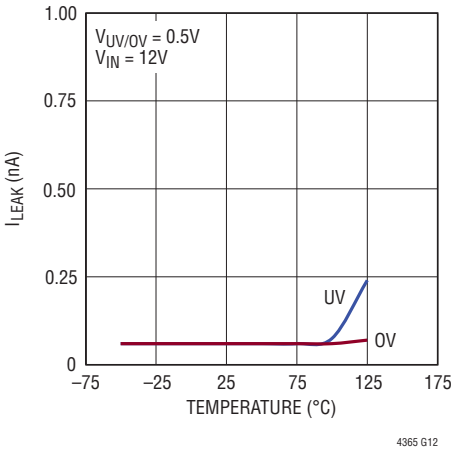
UV Threshold vs Temperature



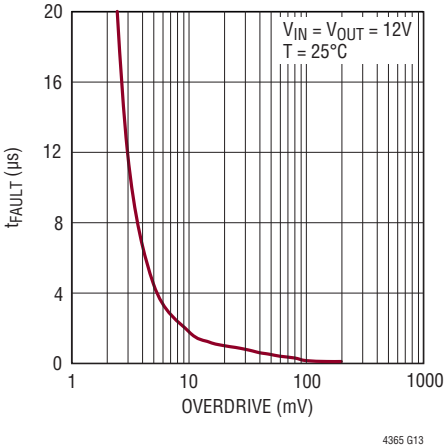
OV Threshold vs Temperature



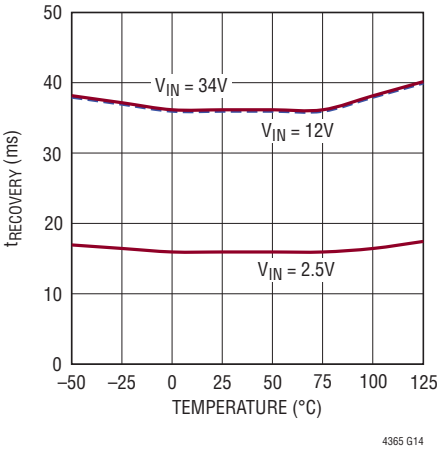
UV/OV Leakage vs Temperature



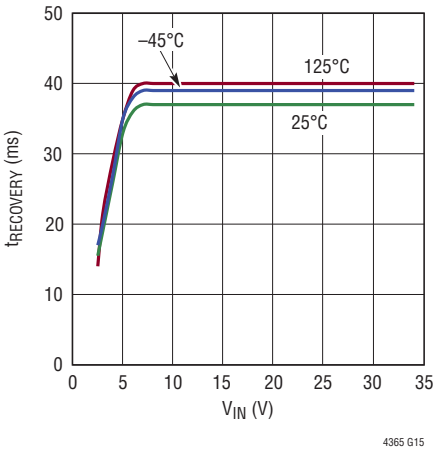
UV/OV Propagation Delay vs Overdrive



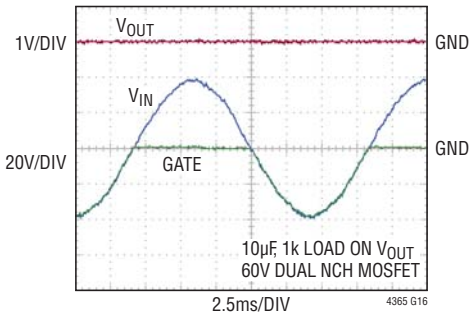
Recovery Delay Time vs Temperature



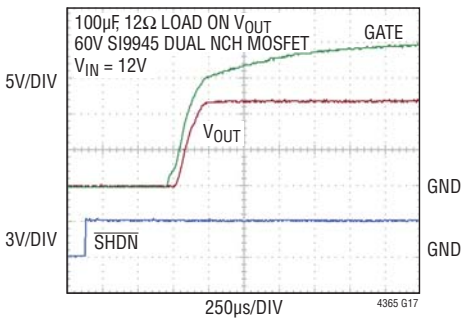
Recovery Delay Time vs V_{IN}



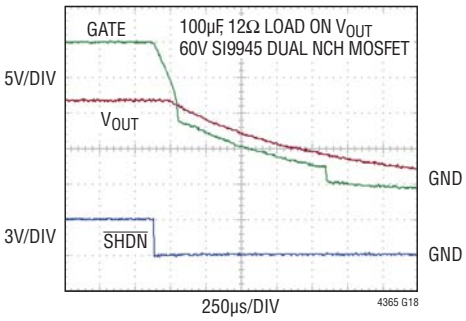
AC Blocking



Turn-On Timing



Turn-Off Timing



PIN FUNCTIONS

Exposed Pad: Connect to device ground.

$\overline{\text{FAULT}}$: Fault Indication Output. This high voltage open drain output is pulled low if UV is below its monitor threshold, if OV is above its monitor threshold, if $\overline{\text{SHDN}}$ is low, or if V_{IN} has not risen above $V_{IN(UVLO)}$.

GATE: Gate Drive Output for External N-channel MOSFETs. An internal charge pump provides 20µA of pull-up current and up to 9.8V of enhancement to the gate of an external N-channel MOSFET.

When turned off, GATE is pulled just below the lower of V_{IN} or V_{OUT}. When V_{IN} goes negative, GATE is automatically connected to V_{IN}.

GND: Device Ground.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider to set the desired V_{IN} overvoltage fault threshold. Input to an accurate, fast (1µs) comparator with a 0.5V rising threshold and 25mV of hysteresis. When OV rises above its threshold, a 50mA current sink pulls down on the GATE output. When OV falls back below 0.475V, and after a 36ms recovery delay waiting period, the GATE charge pump is enabled. The low leakage current of the OV input allows the use of large valued resistors for the external resistive divider. Connect to GND if unused.

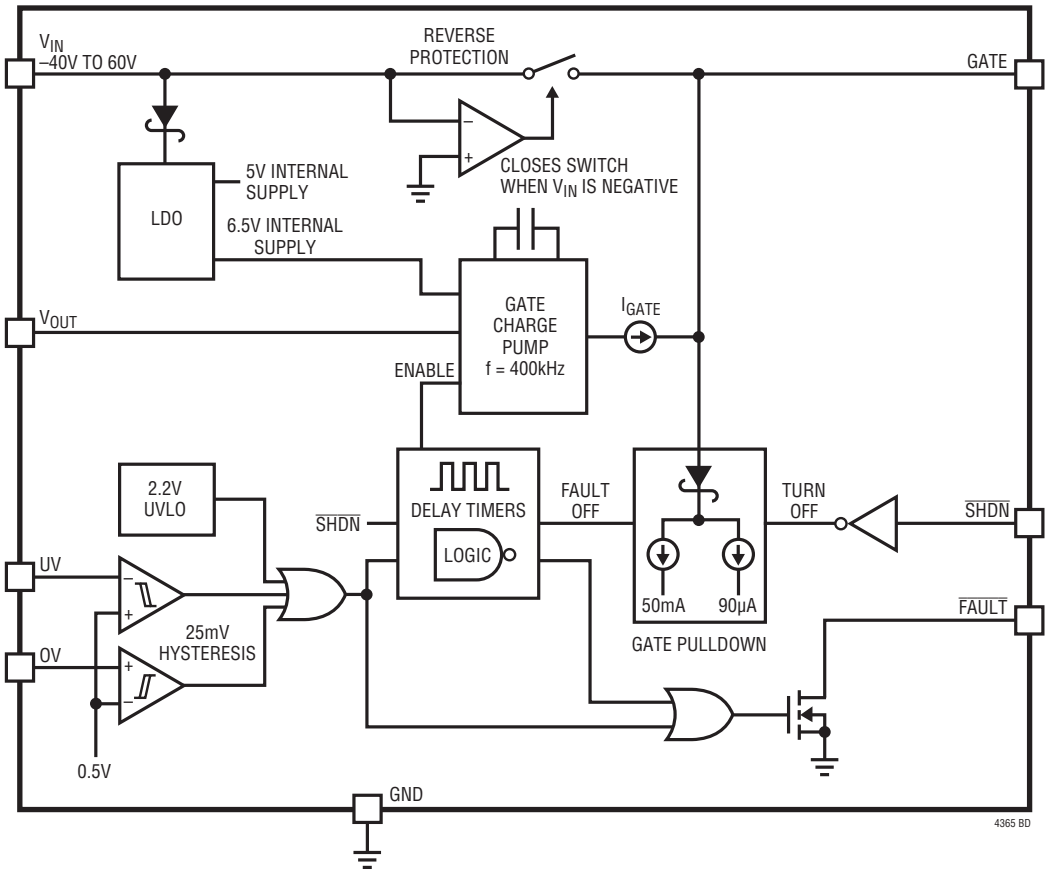
$\overline{\text{SHDN}}$: Shutdown Control Input. $\overline{\text{SHDN}}$ high enables the GATE charge pump which in turn enhances the gate of an external N-channel MOSFET. A low on $\overline{\text{SHDN}}$ generates a pull down on the GATE output with a 90µA current sink and places the LTC4365 in low current mode (10µA). If unused, connect to V_{IN}. If V_{IN} goes below ground, or if V_{IN} rings to 60V, use a current limiting resistor of at least 100k.

UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider to set the desired V_{IN} undervoltage fault threshold. Input to an accurate, fast (1µs) comparator with a 0.5V falling threshold and 25mV of hysteresis. When UV falls below its threshold, a 50mA current sink pulls down on the GATE output. When UV rises back above 0.525V, and after a 36ms recovery delay waiting period, the GATE charge pump is enabled. The low leakage current of the UV input allows the use of large valued resistors for the external resistive divider. If unused, connect to V_{IN}. While connected to V_{IN}, if V_{IN} goes below ground, or if V_{IN} rings to 60V, use a current limiting resistor of at least 100k.

V_{IN}: Power Supply Input. Maximum protection range: –40V to 60V. Operating range: 2.5V to 34V.

V_{OUT}: Output Voltage Sense Input. This pin senses the voltage at the output side of the external N-channel MOSFET. The GATE charge pump voltage is referenced to V_{OUT}. It is used as the charge pump input when V_{OUT} is greater than approximately 6.5V.

BLOCK DIAGRAM



OPERATION

Many of today's electronic systems get their power from external sources such as a wall wart adapter, batteries and custom power supplies. These power sources are often unreliable, wired incorrectly, out of spec, or just plain wrong. This can lead to supply voltages that are too high, too low, or even negative. If these power sources are applied directly to the electronic systems, the systems could be subject to damage. The LTC4365 is an input voltage fault protection N-channel MOSFET controller. The part isolates an input supply from its load to protect the load from unexpected supply voltage conditions, while providing a low loss path for qualified power.

To protect electronic systems from improperly connected power supplies, system designers will often add discrete diodes, transistors and high voltage comparators. The high voltage comparators enable system power only if the input supply falls within a desired voltage window. A Schottky diode or P-channel MOSFET typically added in series with the supply protects against reverse supply connections.

The LTC4365 provides accurate overvoltage and undervoltage comparators to ensure that power is applied to the system only if the input supply meets the user selectable voltage window. Reverse supply protection circuits automatically isolate the load from negative input voltages. During normal operation, a high voltage charge pump enhances the gate of external N-channel power MOSFETs. Power consumption is 10µA during shutdown and 125µA while operating. The LTC4365 integrates all these functions in tiny TSOT-23 and 3mm × 2mm DFN packages.

APPLICATIONS INFORMATION

The LTC4365 is an N-channel MOSFET controller that protects a load from faulty supply connections. A basic application circuit using the LTC4365 is shown in Figure 1. The circuit provides a low loss connection from V_{IN} to V_{OUT} as long as the voltage at V_{IN} is between 3.5V and 18V. Voltages at V_{IN} outside of the 3.5V to 18V range are prevented from getting to the load and can be as high as 60V and as low as –40V. The circuit of Figure 1 protects against negative voltages at V_{IN} as shown. No other external components are needed.

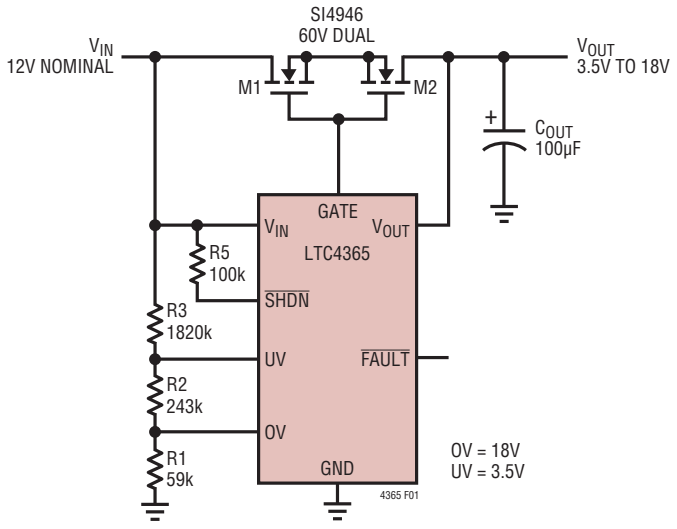


Figure 1. LTC4365 Protects Load from –40V to 60V V_{IN} Faults

During normal operation, the LTC4365 provides up to 9.8V of gate enhancement to the external back-to-back N-channel MOSFETs. This turns on the MOSFET, thus connecting the load at V_{OUT} to the supply at V_{IN}.

GATE Drive

The LTC4365 turns on the external N-channel MOSFETs by driving the GATE pin above V_{OUT}. The voltage difference between the GATE and V_{OUT} pins (gate drive) is a function of V_{IN} and V_{OUT}.

APPLICATIONS INFORMATION

Figure 2 highlights the dependence of the gate drive on V_{IN} and V_{OUT}. When system power is first turned on ($\overline{SHDN}$ low to high, V_{OUT} = 0V), gate drive is at a maximum for all values of V_{IN}. This helps prevent start-up problems into heavy loads by ensuring that there is enough gate drive to support the load.

As V_{OUT} ramps up from 0V, the absolute value of the GATE voltage remains fixed until V_{OUT} is greater than the lower of (V_{IN} –1V) or 6V. Once V_{OUT} crosses this threshold, gate drive begins to increase up to a maximum of 9.8V (for $V_{IN} \geq$ 12V). The curves of Figure 2 were taken with a GATE load of –1µA. If there were no load on GATE, the gate drive for each V_{IN} would be slightly higher.

Note that when V_{IN} is at the lower end of the operating range, the external N-channel MOSFET must be selected with a corresponding lower threshold voltage.

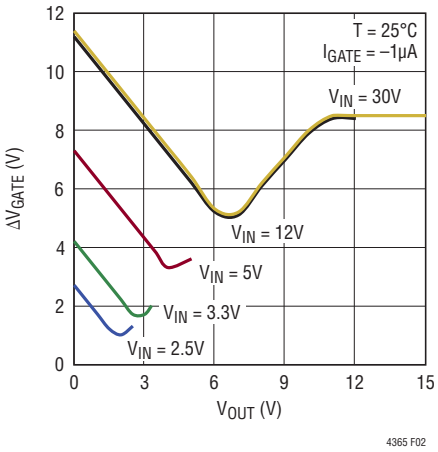


Figure 2. Gate Drive (GATE – V_{OUT}) vs V_{OUT}

Table 1 lists some external MOSFETs compatible with different V_{IN} supply voltages.

Table 1. Dual MOSFETs for Various Supply Ranges

V_{IN}	MOSFET	$V_{TH(MAX)}$	$V_{GS(MAX)}$	$V_{DS(MAX)}$
2.5V	SiB914	0.8V	5V	8V
3.3V	Si5920	1.0V	5V	8V
5V	Si7940	1.5V	8V	12V
≤30V	Si4230	3.0V	20V	30V
≤60V	Si9945	3.0V	20V	60V

Overvoltage and Undervoltage Protection

The LTC4365 provides two accurate comparators to monitor for overvoltage (OV) and undervoltage (UV) conditions at V_{IN}. If the input supply rises above the user adjustable OV threshold, the gate of the external MOSFET is quickly turned off, thus disconnecting the load from the input. Similarly, if the input supply falls below the user adjustable UV threshold, the gate of the external MOSFET also is quickly turned off. Figure 3 shows a UV/OV application for an input supply of 12V.

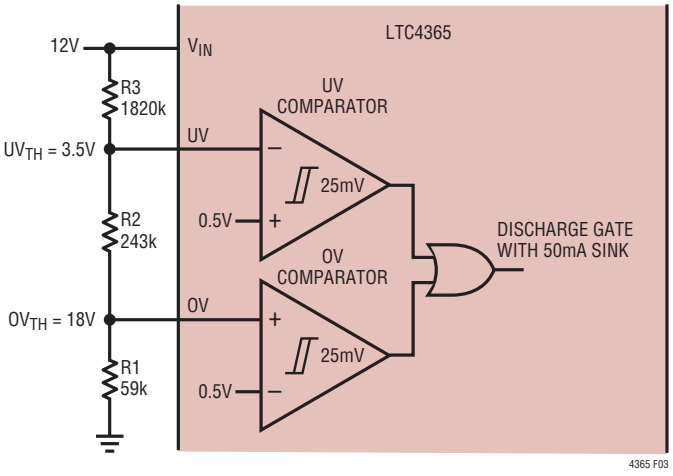


Figure 3. UV, OV Comparators Monitor 12V Supply

The external resistive divider allows the user to select an input supply range that is compatible with the load at V_{OUT}. Furthermore, the UV and OV inputs have very low leakage currents (typically < 1nA at 100°C), allowing for large values in the external resistive divider. In the application of Figure 3, the load is connected to the supply only if V_{IN} lies between 3.5V and 18V. In the event that V_{IN} goes above 18V or below 3.5V, the gate of the external N-channel MOSFET is immediately discharged with a 50mA current sink, thus isolating the load from the supply.

APPLICATIONS INFORMATION

Figure 4 shows the timing associated with the UV pin. Once a UV fault propagates through the UV comparator (t_{FAULT}), the $\overline{FAULT}$ output is asserted low and a 50mA current sink discharges the GATE pin. As V_{OUT} falls, the GATE pin tracks V_{OUT}.

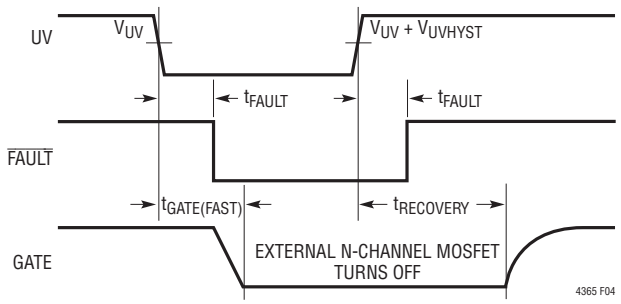


Figure 4. UV Timing (OV < (V_{OV} – V_{OVHYST}), $\overline{SHDN}$ > 1.2V)

Figure 5 shows the timing associated with the OV pin. Once an OV fault propagates through the OV comparator (t_{FAULT}), the $\overline{FAULT}$ output is asserted low and a 50mA current sink discharges the GATE pin. As V_{OUT} falls, the GATE pin tracks V_{OUT}.

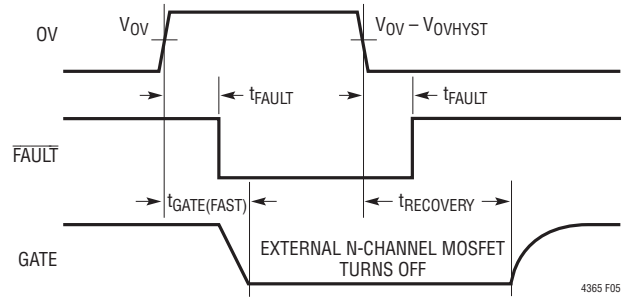


Figure 5. OV Timing (UV > (V_{UV} + V_{UVHYST}), $\overline{SHDN}$ > 1.2V)

When both the UV and OV faults are removed, the external MOSFET is not immediately turned on. The input supply must remain within the user selected power good window for at least 36ms ($t_{RECOVERY}$) before the load is again connected to the supply. This recovery timeout period filters noise (including line noise) at the input supply and prevents chattering of power at the load.

Procedure for Selecting UV/OV External Resistor Values

The following 3-step procedure helps select the resistor values for the resistive divider of Figure 3. This procedure minimizes UV and OV offset errors caused by leakage currents at the respective pins.

1. Choose maximum tolerable offset at the UV pin, $V_{OS(UV)}$. Divide by the worst case leakage current at the UV pin, I_{UV} (10nA). Set the sum of R1 + R2 equal to $V_{OS(UV)}$ divided by 10nA. Note that due to the presence of R3, the actual offset at UV will be slightly lower:

$$R1+R2=\frac{V_{OS(UV)}}{I_{UV}}$$

2. Select the desired V_{IN} UV trip threshold, UV_{TH}. Find the value of R3:

$$R3=2\bullet\frac{V_{OS(UV)}}{I_{UV}}\bullet\left(UV_{TH}-0.5V\right)$$

3. Select the desired V_{IN} OV trip threshold, OV_{TH}. Find the values of R1 and R2:

$$R1=\frac{\left(\frac{V_{OS(UV)}}{I_{UV}}\right)+R3}{2\bullet OV_{TH}}$$

$$R2=\frac{V_{OS(UV)}}{I_{UV}}-R1$$

The example of Figure 3 uses standard 1% resistor values. The following parameters were selected:

$V_{OS(UV)}$ = 3mV

I_{UV} = 10nA

UV_{TH} = 3.5V

OV_{TH} = 18V

APPLICATIONS INFORMATION

The resistor values can then be solved:

$$1.\ R1+R2=\frac{3mV}{10nA}=300k$$

$$2.\ R3=2\bullet\frac{3mV}{10nA}\bullet(3.5V-0.5V)=1.8M$$

The closest 1% value: R3 = 1.82M:

$$3.\ R1=\frac{300k+1.82M}{2\bullet 18V}=58.9k$$

The closest 1% value: R1 = 59k:

R2 = 300k – 59k = 241k

The closest 1% value: R2 = 243k

Therefore: OV = 17.93V, UV = 3.51V.

Reverse V_{IN} Protection

The LTC4365's rugged and hot-swappable V_{IN} input helps protect the more sensitive circuits at the output load. If the input supply is plugged in backwards, or a negative supply is inadvertently connected, the LTC4365 prevents this negative voltage from passing to the output load.

The LTC4365 employs a novel, high speed reverse supply voltage monitor. When the negative V_{IN} voltage is detected, an internal switch connects the gates of the external back-to-back N-channel MOSFETs to the negative input supply.

As shown in Figure 6, external back-to-back N-channel MOSFETs are required for reverse supply protection. When V_{IN} goes negative, the reverse V_{IN} comparator closes the internal switch, which in turn connects the gates of the external MOSFETs to the negative V_{IN} voltage. The body diode (D1) of M1 turns on, but the body diode (D2) of M2 remains in reverse blocking mode. This means that the common source connection of M1 and M2 remains about a diode drop higher than V_{IN}. Since the gate voltage of M2 is shorted to V_{IN}, M2 will be turned off and no current can flow from V_{IN} to the load at V_{OUT}. Note that the voltage rating of M2 must withstand the reverse voltage excursion at V_{IN}.

Figure 7 illustrates the waveforms that result when V_{IN} is hot plugged to –20V. V_{IN}, GATE and V_{OUT} start out at ground just before the connection is made. Due to the parasitic inductance of the V_{IN} and GATE connections, the voltage at the V_{IN} and GATE pins ring significantly below –20V. Therefore, a 40V N-channel MOSFET was selected to survive the overshoot.

The speed of the LTC4365 reverse protection circuits is evident by how closely the GATE pin follows V_{IN} during the negative transients. The two waveforms are almost indistinguishable on the scale shown.

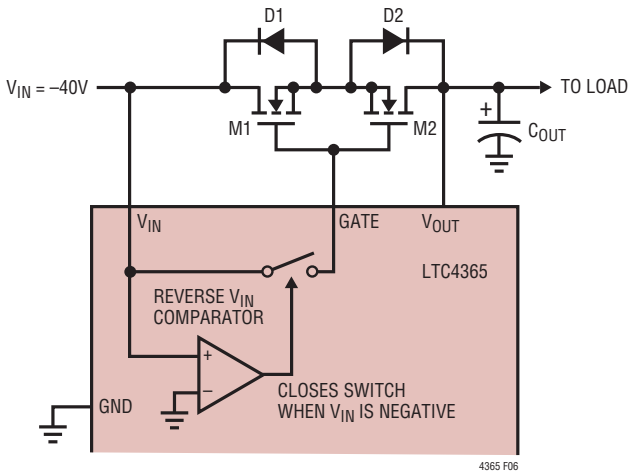


Figure 6. Reverse V_{IN} Protection Circuits

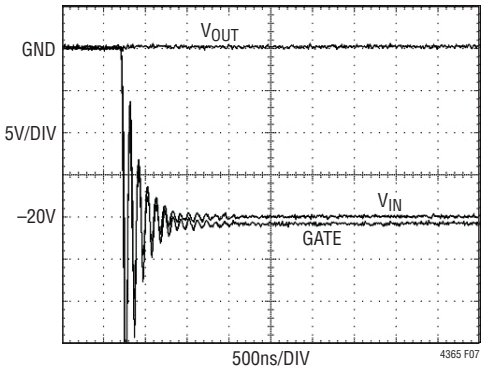


Figure 7. Hot Swapping V_{IN} to –20V

APPLICATIONS INFORMATION

The trace at V_{OUT}, on the other hand, does not respond to the negative voltage at V_{IN}, demonstrating the desired reverse supply protection. The waveforms of Figure 7 were captured using a 40V dual N-channel MOSFET, a 10µF ceramic output capacitor and no load current on V_{OUT}.

Recovery Timer

The LTC4365 has a recovery delay timer that filters noise at V_{IN} and helps prevent chatter at V_{OUT}. After either an OV or UV fault has occurred, the input supply must return to the desired operating voltage window for at least 36ms in order to turn the external MOSFET back on as illustrated in Figures 4 and 5.

Going out of and then back into fault in less than 36ms will keep the MOSFET off continuously. Similarly, coming out of shutdown ($\overline{SHDN}$ low to high) triggers an 800µs start-up delay timer (see Figure 10).

The recovery timer is also active while the LTC4365 is powering up. The 36ms timer starts once V_{IN} rises above $V_{IN(UVLO)}$ and V_{IN} lies within the user selectable UV/OV power good window. See Figure 8.

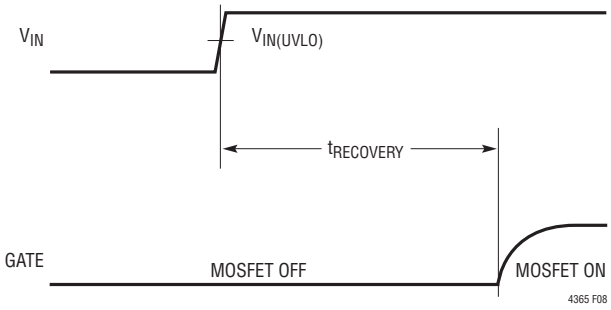


Figure 8. Recovery Timing During Power-On (OV = GND, UV = $\overline{SHDN}$ = V_{IN})

Gentle Shutdown

The $\overline{SHDN}$ input turns off the external MOSFETs in a gentle, controlled manner. When $\overline{SHDN}$ is asserted low, a 90µA current sink slowly begins to turn off the external MOSFETs.

Once the voltage at the GATE pin falls below the voltage at the V_{OUT} pin, the current sink is throttled back and a feedback loop takes over. This loop forces the GATE voltage to track V_{OUT}, thus keeping the external MOSFETs off as V_{OUT} decays. Note that when V_{OUT} < 4.5V, the GATE pin is pulled to within 400mV of ground.

Gentle gate turn off reduces load current slew rates and mitigates voltage spikes due to parasitic inductances. To further decrease GATE pin slew rate, place a capacitor across the gate and source terminals of the external MOSFETs. The waveforms of Figure 9 were captured using the Si4230 dual N-channel MOSFETs, and a 2A load with 100µF output capacitor.

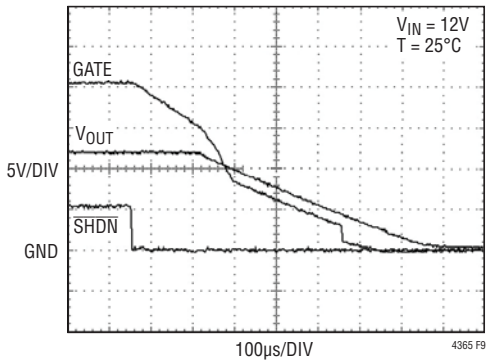


Figure 9. Gentle Shutdown: GATE Tracks V_{OUT} as V_{OUT} Decays

FAULT Status

The $\overline{FAULT}$ high voltage open drain output is driven low if $\overline{SHDN}$ is asserted low, if V_{IN} is outside the desired UV/OV voltage window, or if V_{IN} has not risen above $V_{IN(UVLO)}$. Figures 4, 5 and 10 show the $\overline{FAULT}$ output timing.

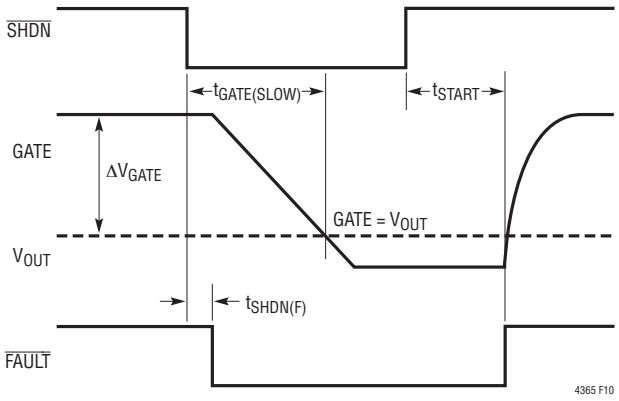


Figure 10. Gentle Shutdown Timing

APPLICATIONS INFORMATION

Select Between Two Input Supplies

With the part in shutdown, the V_{IN} and V_{OUT} pins can be driven by separate power supplies. The LTC4365 then automatically drives the GATE pin just below the lower of the two supplies, thus turning off the external back-to-back MOSFETs. The application of Figure 11 uses two LTC4365s to select between two power supplies. Care should be taken to ensure that only one of the two LTC4365s is enabled at any given time.

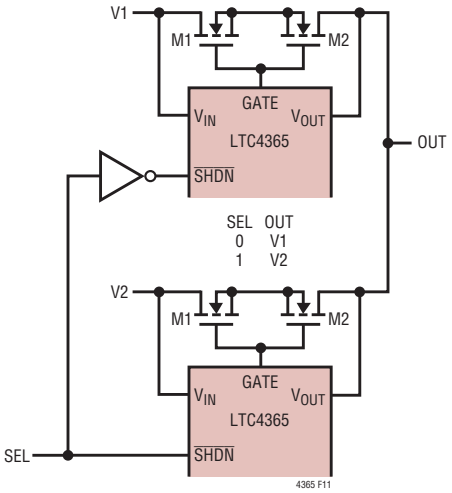


Figure 11. Selecting One of Two Supplies

Single MOSFET Application

When reverse V_{IN} protection is not needed, only a single external N-channel MOSFET is necessary. The application circuit of Figure 12 connects the load to V_{IN} when V_{IN} is less than 30V, and uses the minimal set of external components.

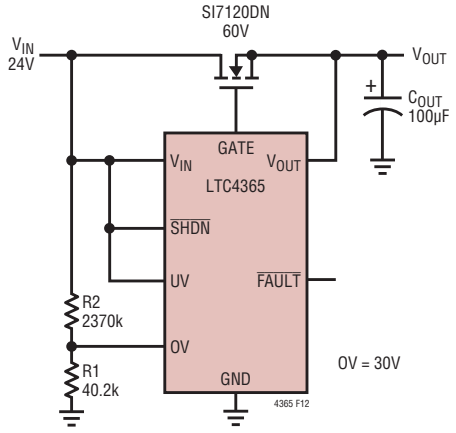


Figure 12. Small Footprint Single MOSFET Application Protects Against 60V

Limiting Inrush Current During Turn-On

The LTC4365 turns on the external N-channel MOSFET with a 20µA current source. The maximum slew rate at the GATE pin can be reduced by adding a capacitor on the GATE pin:

$$\text{Slew Rate} = \frac{20\mu A}{C_{GATE}}$$

Since the MOSFET acts like a source follower, the slew rate at V_{OUT} equals the slew rate at GATE.

Therefore, inrush current is given by:

$$I_{INRUSH} = \frac{C_{OUT}}{C_{GATE}} \bullet 20\mu A$$

For example, a 1A inrush current to a 330µF output capacitance requires a GATE capacitance of:

$$C_{GATE} = \frac{20\mu A \bullet C_{OUT}}{I_{INRUSH}}$$

$$C_{GATE} = \frac{20\mu A \bullet 330\mu F}{1A} = 6.6nF$$

The 6.8nF C_{GATE} capacitor in the application circuit of Figure 13 limits the inrush current to approximately 1A. R_{GATE} makes sure that C_{GATE} does not affect the fast GATE turn off characteristics during UV/OV faults, or during reverse V_{IN} connection. R4A and R4B help prevent high frequency oscillations with the external N-channel MOSFET and related board parasitics.

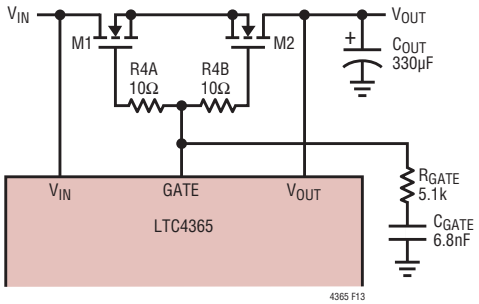


Figure 13. Limiting Inrush Current with C_{GATE}

APPLICATIONS INFORMATION

Transients During OV Fault

The circuit of Figure 14 was used to display transients during an overvoltage condition. The nominal input supply is 24V and it has an overvoltage threshold of 30V. The parasitic inductance is that of a 1 foot wire (roughly 300nH). Figure 15 shows the waveforms during an overvoltage condition at V_{IN}. These transients depend on the parasitic inductance and resistance of the wire along with the capacitance at the V_{IN} node. D1 is an optional power clamp (TVS, Tranzorb) recommended for applications where the DC input voltage can exceed 24V and with large V_{IN} parasitic inductance. No clamp was used to capture the waveforms of Figure 15. In order to maintain reverse supply protection, D1 must be a bi-directional clamp rated for at least 225W peak pulse power dissipation.

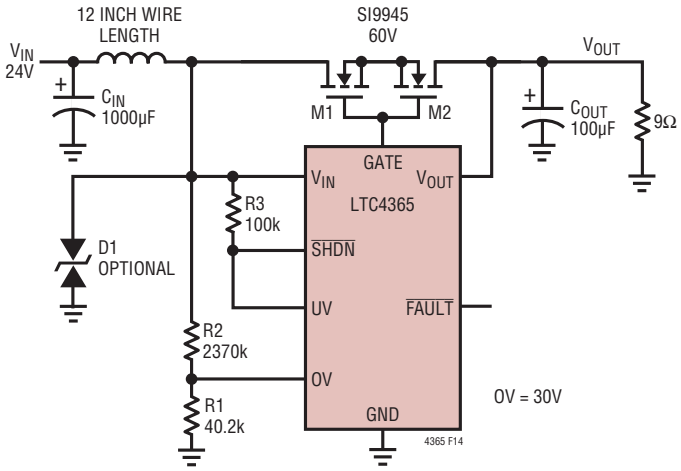


Figure 14. OV Fault with Large V_{IN} Inductance

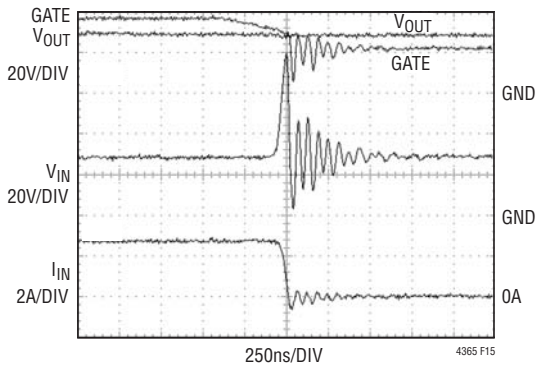


Figure 15. Transients During OV Fault When No Tranzorb (TVS) Is Used

MOSFET Selection

To protect against a negative voltage at V_{IN}, the external N-channel MOSFETs must be configured in a back-to-back arrangement. Dual N-channel packages are thus the best choice. The MOSFET is selected based on its power handling capability, drain and gate breakdown voltages, and threshold voltage.

The drain to source breakdown voltage must be higher than the maximum voltage expected between V_{IN} and V_{OUT}. Note that if an application generates high energy transients during normal operation or during Hot Swap™, the external MOSFET must be able to withstand this transient voltage.

Due to the high impedance nature of the charge pump that drives the GATE pin, the total leakage on the GATE pin must be kept low. The gate drive curves of Figure 2 were measured with a 1µA load on the GATE pin. Therefore, the leakage on the GATE pin must be no greater than 1µA in order to match the curves of Figure 2. Higher leakage currents will result in lower gate drive. The dual N-channel MOSFETs shown in Table 1 all have a maximum GATE leakage current of 100nA. Additionally, Table 1 lists representative MOSFETs that would work at different values of V_{IN}.

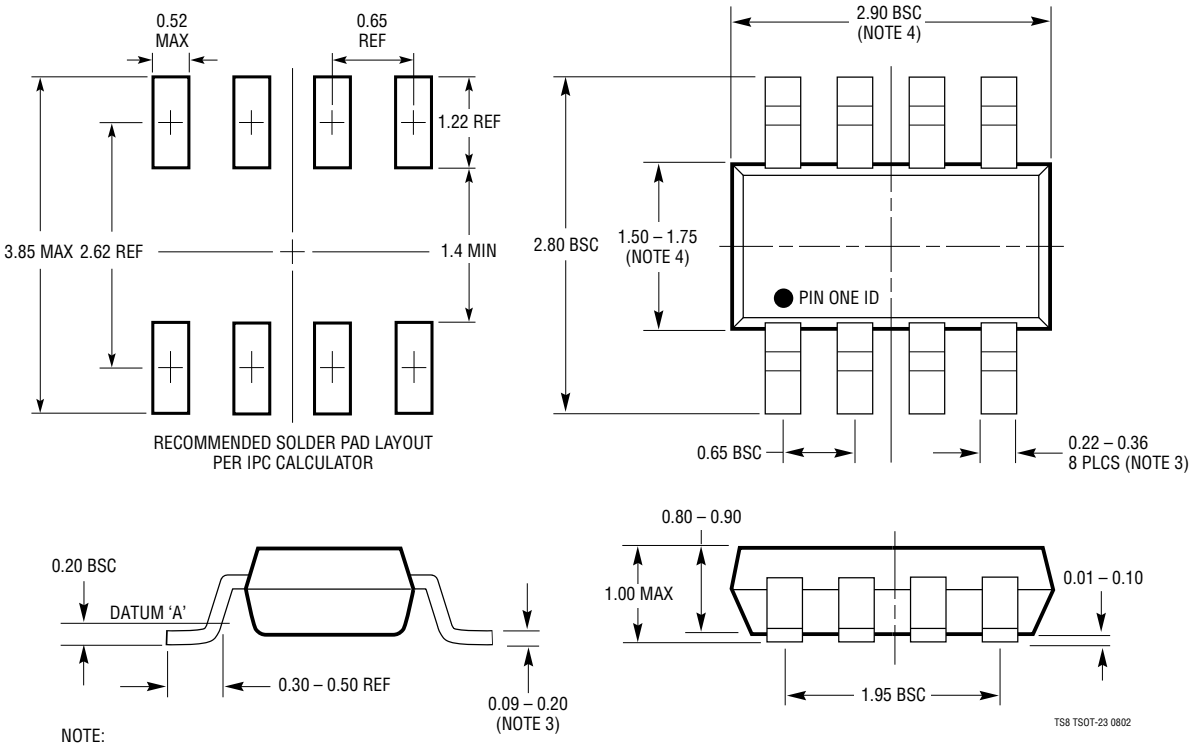
Layout Considerations

The trace length between the V_{IN} pin and the drain of the external MOSFET should be minimized, as well as the trace length between the GATE pin of the LTC4365 and the gates of the external MOSFETs.

Place the bypass capacitors at V_{OUT} as close as possible to the external MOSFET. Use high frequency ceramic capacitors in addition to bulk capacitors to mitigate Hot Swap ringing. Place the high frequency capacitors closest to the MOSFET. Note that bulk capacitors mitigate ringing by virtue of their ESR. Ceramic capacitors have low ESR and can thus ring near their resonant frequency.

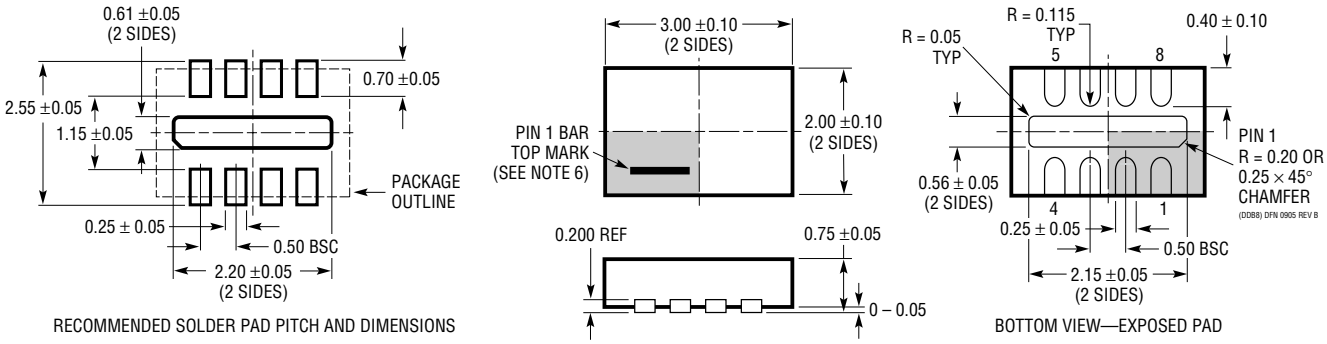
PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

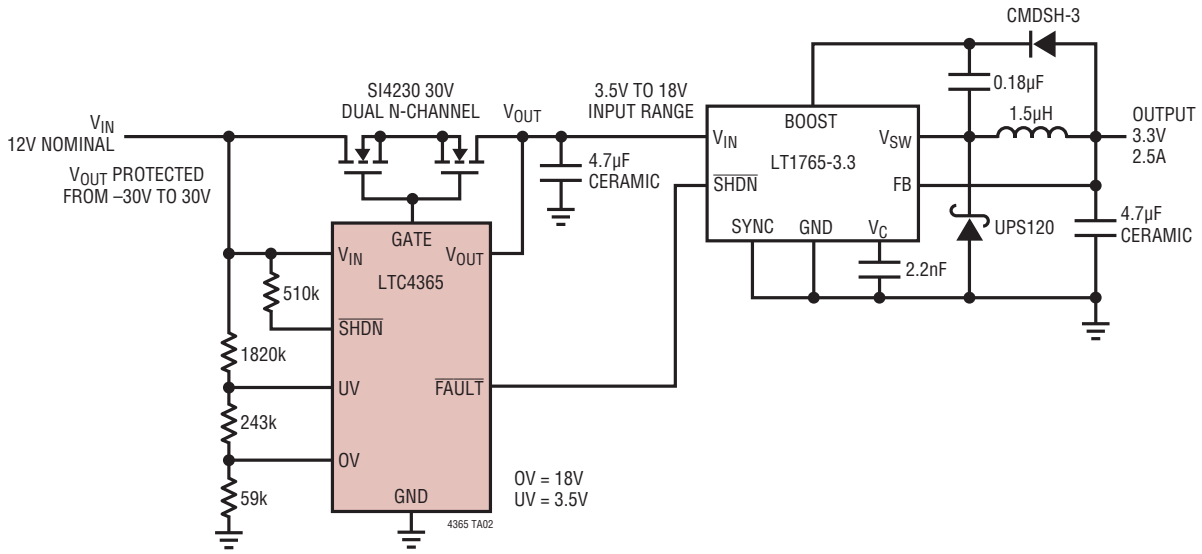
DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

LTC4365 Protects Step Down Regulator from –30V to 30V V_{IN} Faults



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4356	Surge Stopper Overvoltage/Overcurrent Protection Regulator	Wide Operating Range: 4V to 80V, Reverse Protection to –60V, Adjustable Output Clamp Voltage
LTC1696	Overvoltage Protection Controller	ThinSOT Package, 2.7V to 28V
LTC1735	High Efficiency Synchronous Step-Down Switching Regulator	Output Fault Protection, 16-Pin SSOP
LTC1778	No R_{SENSE}™ Wide Input Range Synchronous Step-Down Controller	Up to 97% Efficiency, $4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le (0.9)(V_{IN})$, I_{OUT} Up to 20A
LTC2909	Triple/Dual Inputs UV/OV Negative Monitor	Pin Selectable Input Polarity Allows Negative and OV Monitoring
LTC2912/LTC2913	Single/Dual UV/OV Voltage Monitor	Ads UV and OV Trip Values, ±1.5% Threshold Accuracy
LTC2914	Quad UV/OV Monitor	For Positive and Negative Supplies
LTC3727/LTC3727-1	2-Phase, Dual, Synchronous Controller	$4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 14V$
LTC3827/LTC3827-1	Low I_Q, Dual, Synchronous Controller	$4V \le V_{IN} \le 36V$, $0.8V \le V_{OUT} \le 10V$, 80µA Quiescent Current
LTC3835/LTC3835-1	Low I_Q, Synchronous Step-Down Controller	Single Channel LTC3827/LTC3827-1
LT3845	Low I_Q, Synchronous Step-Down Controller	$4V \le V_{IN} \le 60V$, $1.23V \le V_{OUT} \le 36V$, 120µA Quiescent Current
LT3850	Dual, 550kHz, 2-Phase Synchronous Step-Down Controller	Dual 180° Phased Controllers, V_{IN} 4V to 24V, 97% Duty Cycle, 4mm × 4mm QFN-28, SSOP-28 Packages
LT4256	Positive 48V Hot Swap Controller with Open-Circuit Detect	Foldback Current Limiting, Open-Circuit and Overcurrent Fault Output, Up to 80V Supply
LTC4260	Positive High Voltage Hot Swap Controller with ADC and I^2C	Wide Operating Range 8.5V to 80V
LTC4352	Ideal MOSFET ORing Diode	External N-Channel MOSFETs Replace ORing Diodes, 0V to 18V
LTC4354	Negative Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 1µs Turn-Off, 80V Operation
LTC4355	Positive Voltage Diode-OR Controller	Controls Two N-Channel MOSFETs, 0.5µs Turn-Off, 80V Operation

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