12-/24-/48-Port IEEE 802.3 at PoE PSE Controller

FEATURES

- **Fully Compliant IEEE 802.3at Type 1 and 2 PSE**
- **Up to 48 PSE Ports**
- **Industry-Standard Register Map**
- **+80V/–20V Tolerant Port-Facing Pins**
- **ECC-Protected eFlash and Data RAMs**
- **Low Power Path Dissipation per Channel**
  - **100mΩ Sense Resistance**
  - **30mΩ or Lower MOSFET $R_{DS(ON)}$**
- **Chipset Provides Electrical Isolation**
  - **Eliminates Optos and Isolated 3.3V Supply**
- **Very High Reliability Multipoint PD Detection**
- Continuous Per-Port Voltage and Current Monitoring
- 1MHz I^2C Compatible Serial Control Interface
- Pin or I^2C Programmable PD Power
- Available in 24-Lead 4mm × 4mm (LTC9101-2A) and 64-Lead 7mm × 11mm (LTC9102) QFN Packages

APPLICATIONS

- PoE PSE Switches/Routers and Midspans

DESCRIPTION

The LTC®9101-2A/LTC9102 chipset is a (up to) 48-port power sourcing equipment (PSE) controller designed for use in IEEE 802.3at Type 1 and 2 compliant Power over Ethernet (PoE) systems. The LTC9101-2A/LTC9102 is designed to power compliant 802.3af and 802.3at PDs. The LTC9101-2A/LTC9102 chipset delivers lowest-in-industry heat dissipation using low $R_{DS(ON)}$ external MOSFETs and 0.1Ω sense resistance per power channel. A transformer-isolated communication protocol replaces expensive optocouplers and a complex isolated 3.3V supply, resulting in significant bill of materials (BOM) cost savings.

Advanced power management features include per-port 14-bit current/voltage monitoring, programmable current limits, and versatile fast shutdown of preselected ports. PD detection uses a proprietary multipoint detection mechanism, ensuring excellent immunity from false PD identification. 1-event and 2-event physical classification are supported. The LTC9101-2A/LTC9102 includes an I^2C serial interface operable up to 1MHz. The LTC9101-2A/LTC9102 is pin or I^2C programmable to negotiate PD-delivered power up to 25.5W.

TYPICAL APPLICATION

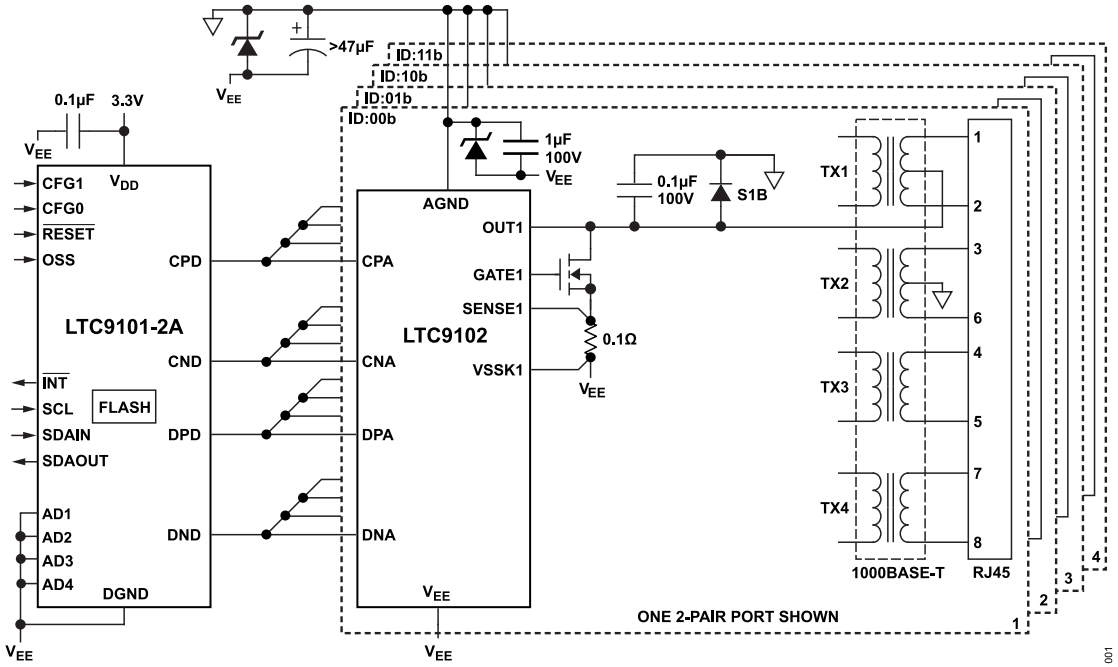

Figure 1. 802.3at 2-Pair Application, 1 Port Shown

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ABSOLUTE MAXIMUM RATINGS

LTC9101-2A

Table 1. Absolute Maximum Ratings (Notes 1, 4)

PARAMETER	RATING
Supply Voltages (with respect to DGND)	
V_{DD}	–0.3V to 3.6V
CAP1, CAP2	–0.3V to 1.32V
Digital Pins	
ADn, CFGn, OSS, SDAIN, SDAOUT, SCL, $\overline{RESET}$, $\overline{INT}$	–0.3V to V_{DD} + 0.3V
Analog Pins	
CPD, CND, DPD, DND	–0.3V to V_{DD} + 0.3V
Operating Ambient Temperature Range	–40°C to 85°C
Operating Junction Temperature Range (Note 2)	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C

LTC9102

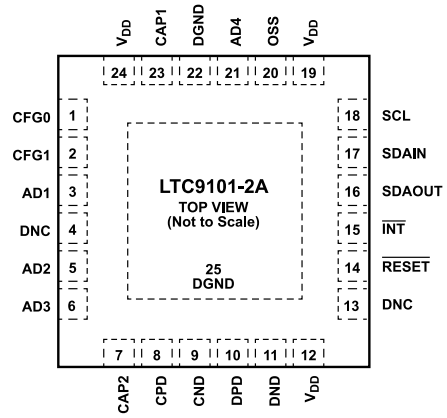
Table 2. Absolute Maximum Ratings (Note 1)

PARAMETER	RATING
Supply Voltages (with respect to V_{EE})	
AGND	–0.3V to 80V
PWRIN	–0.3V to 80V
CAP3, CAP4	–0.3V to 5V
VSSKn	–0.3V to 0.3V
Analog Pins	
SENSEn, OUTn	–20V to 80V
GATEn, IDn, PWRMDn	–0.3V to 80V
CPA, CNA, DPA, DNA	–0.3V to CAP3 + 0.3V
EXT3	–0.3V to 30V
Operating Ambient Temperature Range	–40°C to 85°C
Operating Junction Temperature Range (Note 2)	–40°C to 125°C
Storage Temperature	–65°C to 150°C

ESD CAUTION

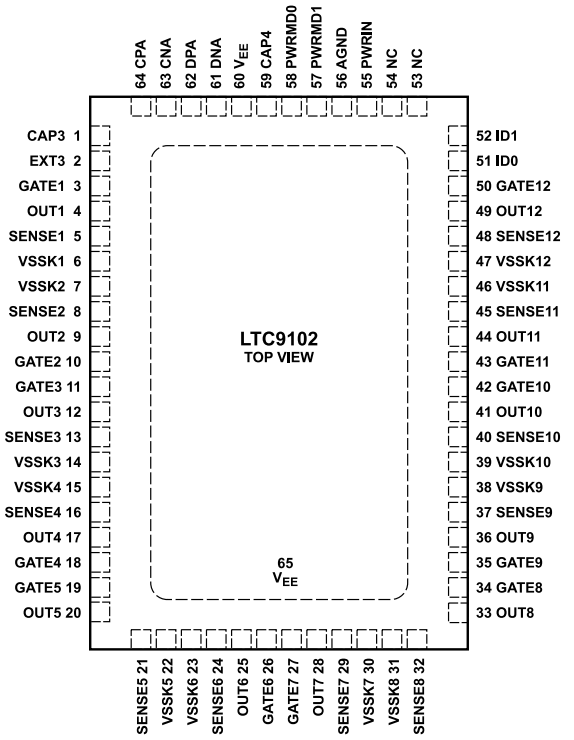
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.
2. θ_{JC} = 4°C/W, θ_{JA} = 47°C/W
3. EXPOSED PAD (PIN 25) IS DGND, MUST BE SOLDERED TO PCB. 002

Figure 2. LTC9101-2A



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. θ_{JC} = 1°C/W, θ_{JA} = 22°C/W
3. EXPOSED PAD (PIN 65) IS V_{EE}, MUST BE SOLDERED TO PCB. 003

Figure 3. LTC9102

ORDERING INFORMATION

Table 3. Ordering Information

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC9101AUF-2A#PBF	LTC9101AUF-2A#TRPBF	9101A	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC9102AUKJ#PBF	LTC9102AUKJ#TRPBF	LTC9102	64-Lead (7mm × 11mm) Plastic QFN	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges. Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The * denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AGND – V_{EE} = 55V and V_{DD} – DGND = 3.3V, unless otherwise noted. (Notes 3 and 4)

Table 4. Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Main PoE Supply Voltage	AGND – V_{EE}					
		Type 2 Compliant Output	*	51		57	V
	LTC9102 Undervoltage Lockout	AGND – V_{EE}	*		8.2	9	V
V_{DD}	V_{DD} Supply Voltage	V_{DD} – DGND	*	3	3.3	3.6	V
	Undervoltage Warning				2.8		V
	Undervoltage Lockout				2.6		
	V_{DD} Slew Rate, Falling	2.4 ≤ V_{DD} – DGND ≤ 3.0 (Note 7)				20	mV/µs
V_{CAP1}, V_{CAP2}	Internal Regulator Supply Voltage	V_{CAP1} – DGND, V_{CAP2} – DGND (Note 13)			1.2		V
V_{CAP3}	Internal 3.3V Regulator Supply Voltage	CAP3 – V_{EE} (Note 13)	*	3	3.3	3.6	V
$t_{CAP3EXT}$	CAP3 External Supply Rise Time	0.5V < CAP3 < V_{CAP3}(Min), EXT3 Tied to CAP3 (Note 7)	*			1	ms
V_{CAP4}	Internal 4.3V Regulator Supply Voltage	CAP4 – V_{EE} (Note 13)	*		4.3		V
I_{EE}	V_{EE} Supply Current	PWRIN Pin Connected to AGND, EXT3 LOW, All Gates Fully Enhanced		7.7	11	14	mA
	3.3V Rail Supply Current	From CAP3 = 3.3V (EXT3 HIGH)		4.2	5.4	6.6	mA
I_{DD}	V_{DD} Supply Current	(V_{DD} – DGND) = 3.3V	*		40	60	mA
Detection/Connection Check							
	Forced Current	Load Resistance 15.5k to 32k	*	220	240	260	µA
			*	143	160	180	µA
	Forced Voltage	Load Resistance 18.5k to 27.5k	*	7	8	9	V
			*	3	4	5	V
	Detection Current Compliance	AGND – OUTn = 0V	*		0.8	0.9	mA
V_{OC}	Detection Voltage Compliance	AGND – OUTn, Open Port	*		10.4	12	V
	Detection Voltage Slew Rate	AGND – OUTn, C_{PORT} = 150nF (Note 7)				0.01	V/µs
	Min. Valid Signature Resistance		*	15.5	17	18.5	kΩ
	Max. Valid Signature Resistance		*	27.5	29.7	32	kΩ
Classification							
V_{CLASS}	Classification Voltage	AGND – OUTn, SENSEn – VSSKn < 5mV	*	16		20.5	V
	Classification Current Compliance	SENSEn – VSSKn, OUTn = AGND (Note 15)	*	7	8	9	mV
	Classification Threshold	SENSEn – VSSKn (Note 15)					
		Class Signature 0 to 1	*	0.5	0.65	0.8	mV
		Class Signature 1 to 2	*	1.3	1.45	1.6	mV
		Class Signature 2 to 3	*	2.1	2.3	2.5	mV
		Class Signature 3 to 4	*	3.1	3.3	3.5	mV
		Class Signature 4 to Overcurrent	*	4.5	4.8	5.1	mV
V_{MARK}	Classification Mark State Voltage	AGND – OUTn, SENSEn – VSSKn < 5mV	*	7.5	9	10	V
	Mark State Current Compliance	OUTn = AGND	*	7	8	9	mV
Gate Driver							
	GATE Pin Pull-Down Current	Port Off, GATEn = V_{EE} + 5V			1		mA
	GATE Pin Fast Pull-Down Current	GATEn = V_{EE} + 5V			65		mA
	GATE Pin On Voltage	GATEn – V_{EE}, I_{GATEn} = 1µA	*	11		14	V
Output Voltage Sense							
V_{PG}	Power Good Threshold Voltage	OUTn – V_{EE}	*	2	2.4	2.8	V
	OUT Pin Pull-Up Resistance to AGND	Port On			2500		kΩ
		Port Off	*	300	500	700	kΩ

ELECTRICAL CHARACTERISTICS

Table 4. Electrical Characteristics (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense							
V_{LIM}	Active Current Limit	OUTn – V_{EE} < 10V					
		Class 1 to Class 3	*	40	42.5	45	mV
		Class 4	*	80	85	90	mV
V_{INRUSH}	Active Current Limit, Inrush	OUTn – V_{EE} < 30V (Note 16)	*	40	42.5	45	mV
V_{HOLD}	DC Disconnect Sense Voltage	SENSEn – VSSKn, Class 0 to 4	*	500	700	900	µV
V_{SC}	Short-Circuit Sense	SENSEn – VSSKn – V_{LIM}			60		mV
Port Current Readback (See Typical Performance Characteristics, Note 17)							
	Full-Scale Range	(Notes 7, 15)			204.6		mV
	LSB Weight	|SENSEn – VSSKn|, VSSKn = V_{EE} (Note 15)			24.98		µV/LSB
	Conversion Period				1.967		ms
V_{EE} Readback (See Typical Performance Characteristics, Note 17)							
	Full-Scale Range	(Note 7)			82		V
	LSB Weight	|AGND – V_{EE}|			10.01		mV/LSB
	Conversion Period				1.967		ms
Digital Interface							
V_{ILD}	Digital Input Low Voltage	ADn, $\overline{RESET}$, OSS, CFGn (Note 6)	*			0.8	V
	I^2C Input Low Voltage	SCL, SDAIN (Note 6)	*			1	V
V_{IHD}	Digital Input High Voltage		*	2.2			V
	Digital Output Low Voltage	I_{SDAOUT} = 3mA, $I_{\overline{INT}}$ = 3mA	*			0.4	V
		I_{SDAOUT} = 5mA, $I_{\overline{INT}}$ = 5mA	*			0.7	V
	Internal Pull-Up to V_{DD}	ADn, $\overline{RESET}$, OSS			50		kΩ
	Internal Pull-Down to DGND	CFG0			50		kΩ
	EXT3 Pull-Down to V_{EE}				50		kΩ
	IDn Internal Pull-Up to CAP4	IDn = 0V			5		µA
PSE Timing Characteristics (Note 7)							
t_{DET}	Detection Time	Beginning to End of Detection	*		380	500	ms
t_{CEV}	Class Event Duration		*	6	15	20	ms
t_{CEVON}	Class Event Turn On Duration	C_{PORT} = 0.6µF	*			0.1	ms
t_{CLASS}	Class Event I_{CLASS} Measurement Timing		*	6			ms
t_{ME1}	Mark Event Duration (Except Last Mark Event)	(Note 11)	*	6	9.6	12	ms
t_{ME2}	Last Mark Event Duration	(Note 11)	*	6	20		ms
t_{PON}	Power On Delay	From End of Valid Detect to End of Valid Inrush (Note 14)	*			400	ms
t_{ED}	Fault Delay	From Power On Fault to Next Detect	*	1.0	1.3	1.8	s
t_{START}	Maximum Current Limit Duration During Inrush	t_{START} = 0x0	*	50	60	75	ms
t_{CUT}	Maximum Current Overload Duration	t_{CUT} = 0x0	*	50	60	75	ms
t_{LIM}	Maximum Current Limit Duration After Inrush	(Note 12)					
		Type 1, t_{LIM} = 0x0		50	60	75	ms
		Spare, t_{LIM} = 0x1		12	17	18	ms
		Type 2, t_{LIM} = 0x2		10	13	14	ms
		Spare, t_{LIM} = 0x3		6	11	12	ms
t_{MPS}	Maintain Power Signature (MPS) Pulse Width Sensitivity	Current Pulse Width to Reset Disconnect Timer (Note 8)	*			6	ms
t_{DIS}	Maintain Power Signature (MPS) Dropout Time	t_{DIS} = 0x0 (Note 5)	*	320	370	400	ms
$t_{OSS-OFF}$	Shutdown Priority Delay		*		6.5	10	µs
t_{r_OSS}	OSS Rise Time		*	1		300	ns
t_{f_OSS}	OSS Fall Time		*	1		300	ns

ELECTRICAL CHARACTERISTICS

Table 4. Electrical Characteristics (Continued)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{OSS_IDL}	OSS Idle Time				50		µs
	I^2C Watchdog Timer Duration		*	1.5	2	3	s
	Minimum Pulse Width for Masked Shutdown		*	3			µs
	Minimum Pulse Width for $\overline{RESET}$		*	4.5			µs
I^2C Timing (Note 7)							
f_{SCLK}	Clock Frequency		*			1	MHz
t_1	Bus Free Time	Figure 30 (Note 9)	*	480			ns
t_2	Start Hold Time	Figure 30 (Note 9)	*	240			ns
t_3	SCL Low Time	Figure 30 (Note 9)	*	480			ns
t_4	SCL High Time	Figure 30 (Note 9)	*	240			ns
t_5	SDAIN Data Hold Time	Figure 30 (Note 9)	*	60			ns
	Data Clock to SDAOUT Valid	Figure 30 (Note 9)	*			250	ns
t_6	Data Set-Up Time	Figure 30 (Note 9)	*	80			ns
t_7	Start Set-Up Time	Figure 30 (Note 9)	*	240			ns
t_8	Stop Set-Up Time	Figure 30 (Note 9)	*	240			ns
t_r	SCL, SDAIN Rise Time	Figure 30 (Note 9)	*			120	ns
t_f	SCL, SDAIN Fall Time	Figure 30 (Note 9)	*			60	ns
	Fault Present to $\overline{INT}$ Pin Low	(Notes 9, 10)	*			150	ns
	Stop Condition to $\overline{INT}$ Pin Low	(Notes 9, 10)	*			1.5	µs
	ARA to $\overline{INT}$ Pin High Time	(Note 9)	*			1.5	µs
	SCL Fall to ACK Low	(Note 9)	*			250	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifespan.

Note 2: This chipset includes overtemperature protection to protect the device during momentary overload conditions. Junction temperature exceeds 140°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: All currents into device pins are positive; all currents out of device pins are negative.

Note 4: The LTC9102 operates with a negative supply voltage (with respect to AGND). To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude.

Note 5: t_{DIS} is the same as t_{MPDO} defined by IEEE 802.3.

Note 6: The LTC9101-2A digital interface operates with respect to DGND. All logic levels are measured with respect to DGND.

Note 7: Guaranteed by design, not subject to test.

Note 8: The IEEE 802.3 defines MPS as the set of minimum PSE and PD input current requirements to maintain power. An LTC9101-2A/LTC9102 port resets its MPS timer when $V_{SENSEn} - VSSKn \geq V_{HOLD}$ for t_{MPS} and removes port power when $V_{SENSEn} - VSSKn \geq V_{HOLD}$ for a period longer than t_{DIS}. See the Disconnect section.

Note 9: Values measured at V_{IHD}.

Note 10: If a fault condition occurs during an I^2C transaction, the $\overline{INT}$ pin is not pulled down until a stop condition is present on the I^2C bus.

Note 11: Load characteristics of the LTC9102 during Mark: $7V < (AGND - V_{OUTn}) < 10V$.

Note 12: Refer to the LTC9101-2A software interface data sheet for information on serial bus usage, and device configuration and status registers.

Note 13: Do not source or sink current from CAP1, CAP2, CAP3, and CAP4.

ELECTRICAL CHARACTERISTICS

Note 14: t_{PON} is measured from end of valid detect.

Note 15: Port current measurements depend on sense resistor value (0.1Ω typical). See the External Component Selection section for details.

Note 16: See Inrush Control for details on inrush threshold selection.

Note 17: ADC characteristics and typical performance are described in terms of LTC9102 hardware capability. Measurements from LTC9102 are processed and synthesized by the LTC9101-2A. Refer to the LTC9101-2A software interface data sheet for register descriptions and LSB weights, as presented to the user (port current, port voltage, V_{EE} voltage, and system temperature).

TYPICAL PERFORMANCE CHARACTERISTICS

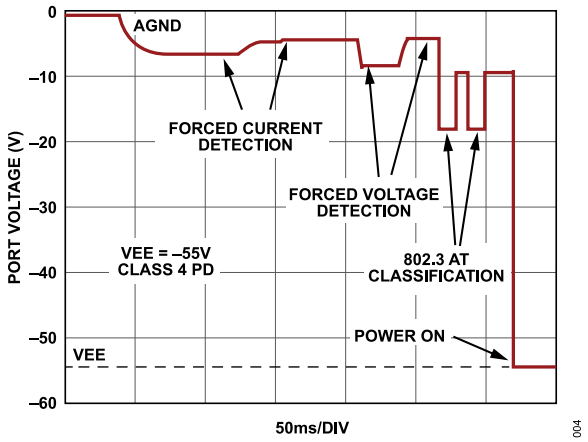


Figure 4. 802.3at Power-On Sequence

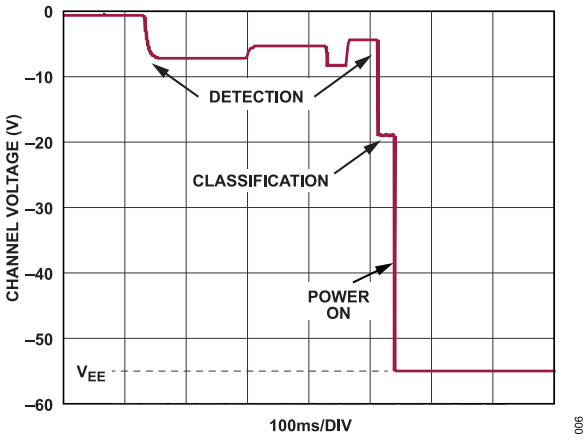


Figure 5. Power-On Sequence, Type 1 Mode

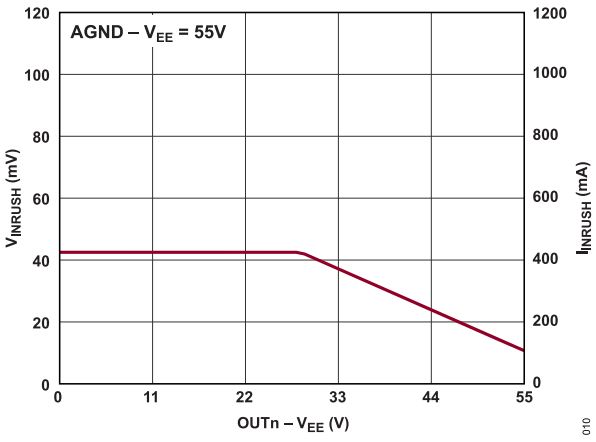


Figure 6. Inrush Current Limit

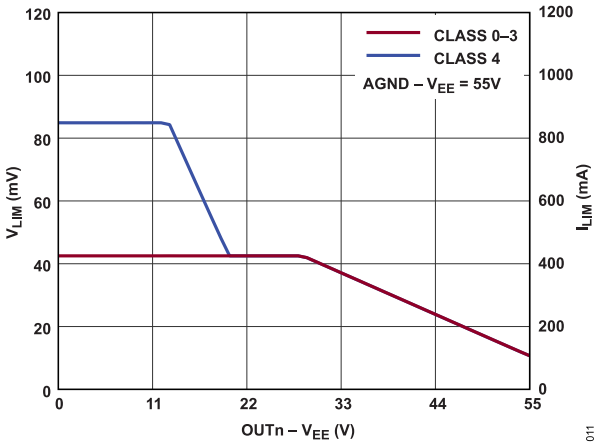


Figure 7. Power-On Current Limits

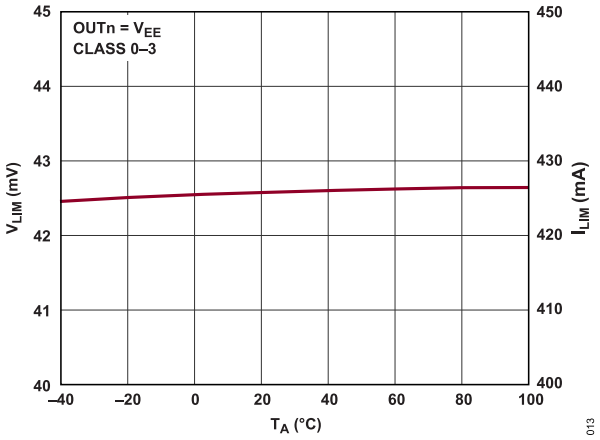


Figure 8. I_{LIM} vs. Temperature

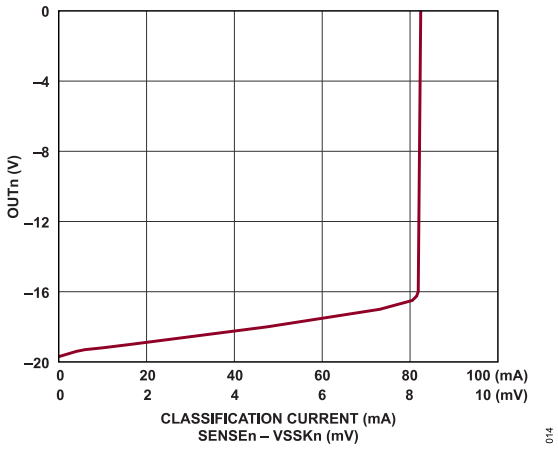


Figure 9. Classification Current Compliance

TYPICAL PERFORMANCE CHARACTERISTICS

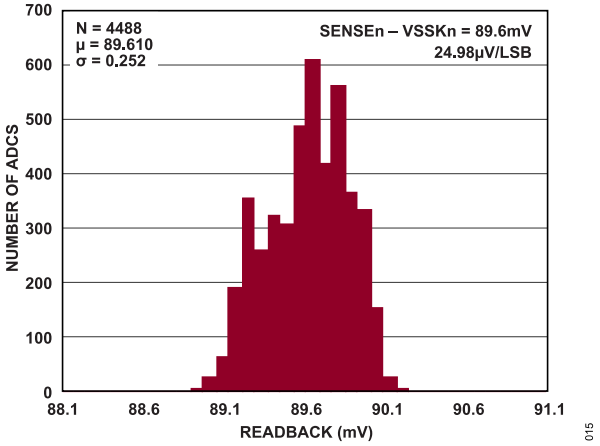


Figure 10. Port Current Readback

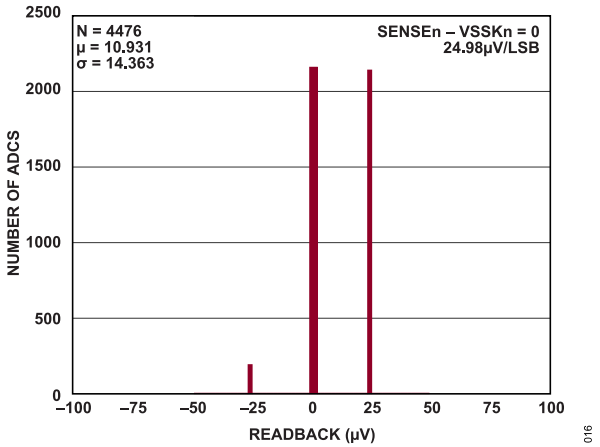


Figure 11. Port Current Readback Offset

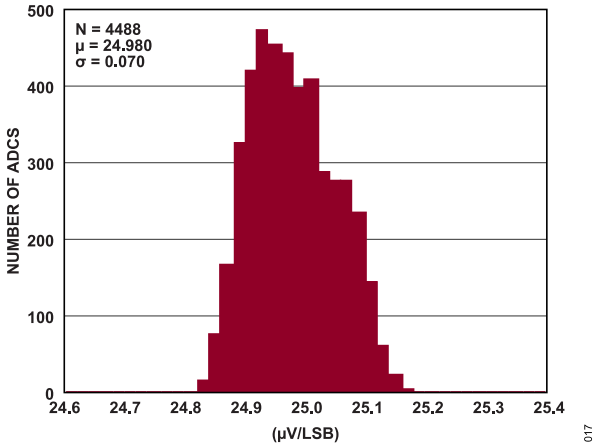


Figure 12. Port Current Readback LSB

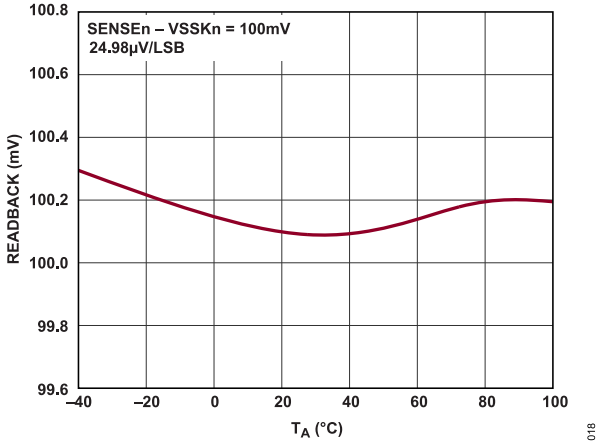


Figure 13. Port Current Readback vs. Temperature

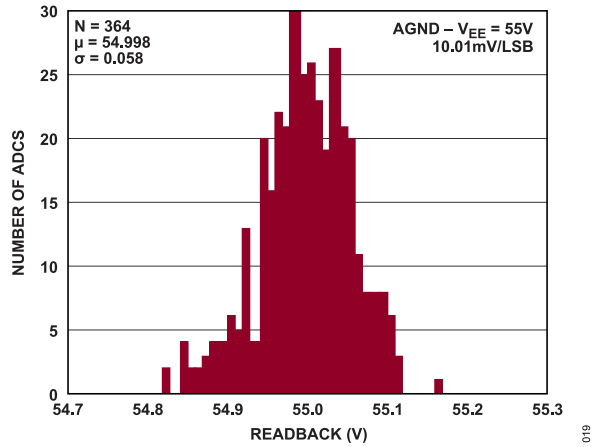


Figure 14. V_{EE} Readback

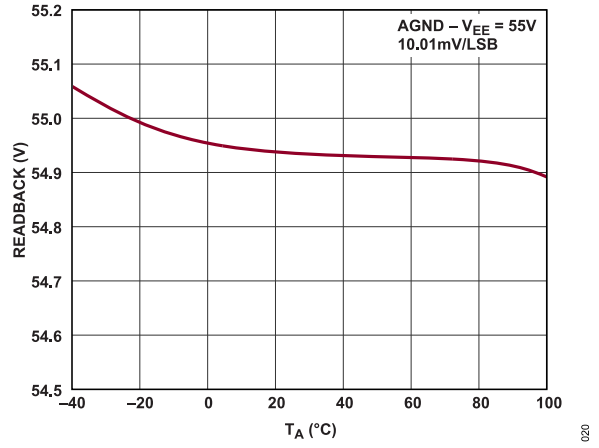


Figure 15. V_{EE} Readback vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

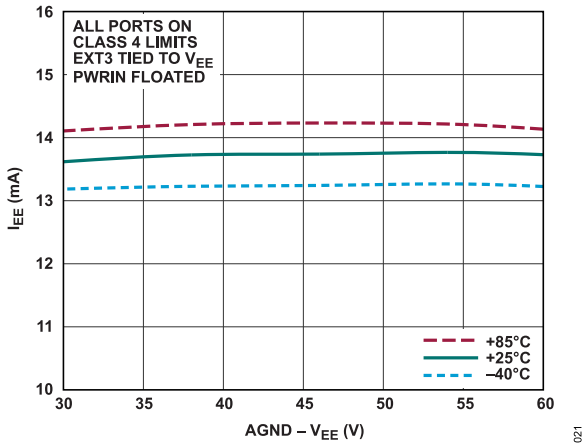


Figure 16. V_{EE} Supply Current vs. Voltage and Temperature

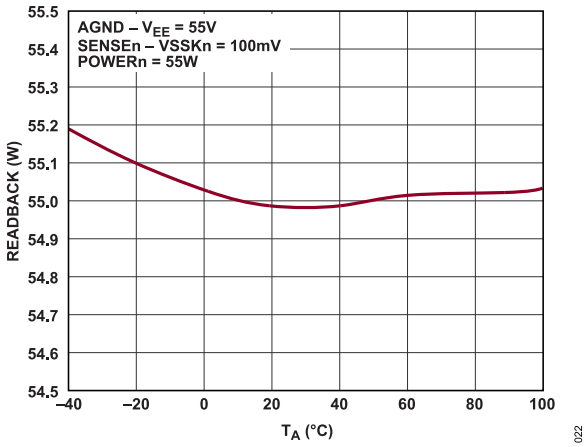


Figure 17. Port Power Readback vs. Temperature

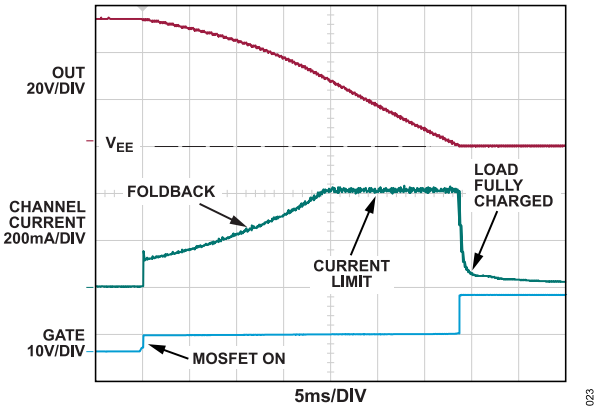


Figure 18. Powering Up into 180µF

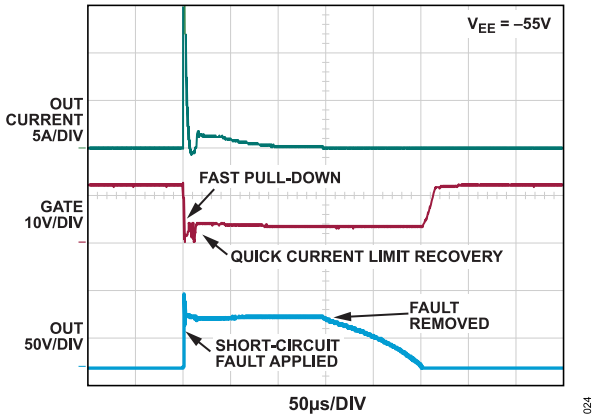


Figure 19. Short-Circuit Recovery

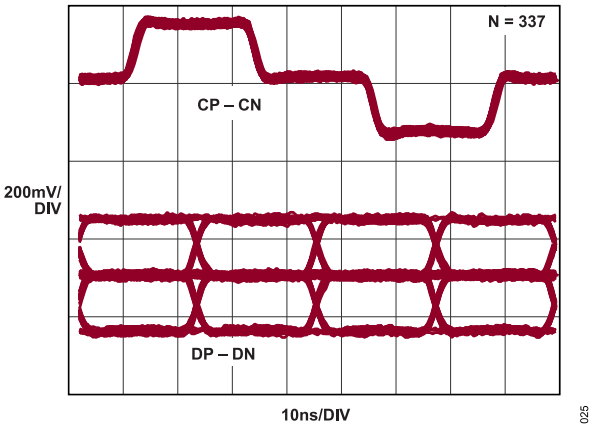


Figure 20. Clock and Data Write Eye Diagram

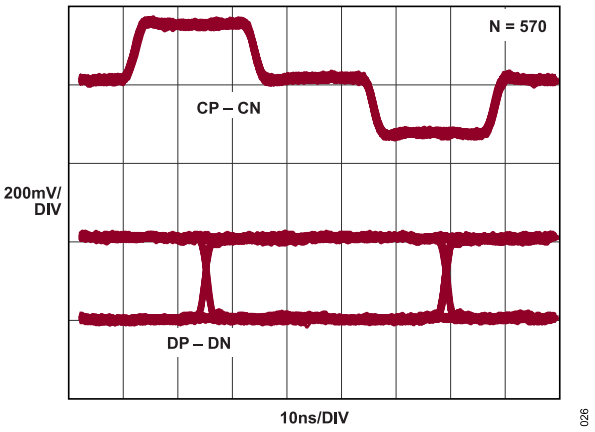


Figure 21. Clock and Data Read Eye Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

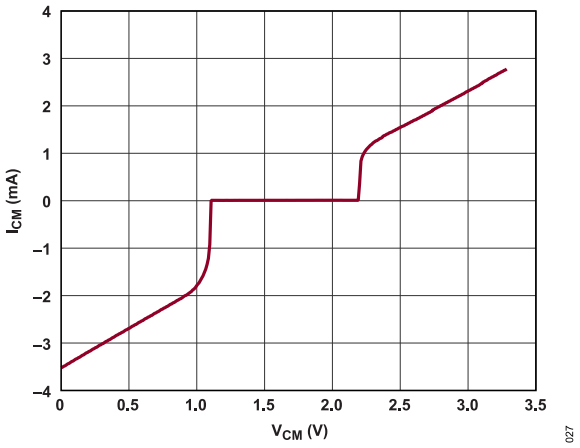


Figure 22. LTC9102 CP/CN and DP/DN Common Mode Correction Current

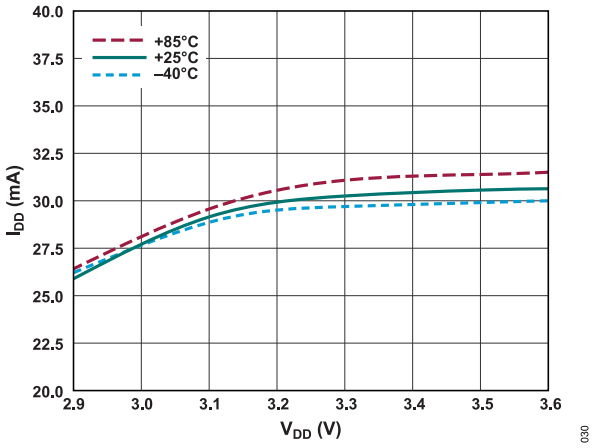


Figure 25. V_{DD} Supply Current vs. Voltage and Temperature

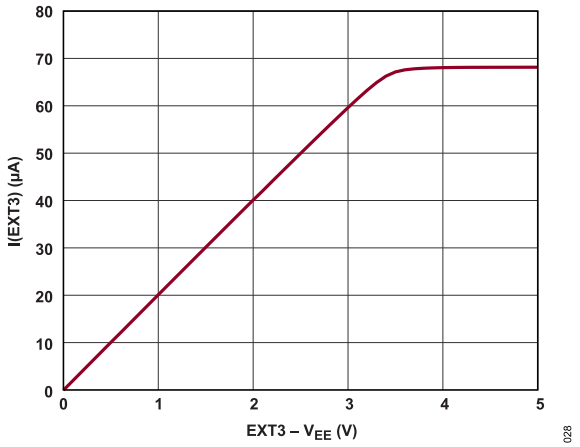


Figure 23. EXT3 Pin Current vs. Voltage

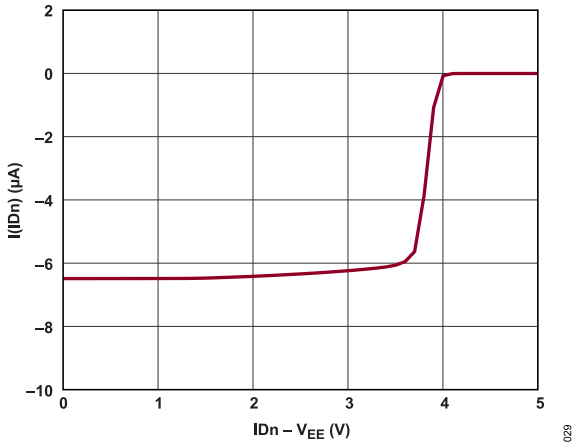


Figure 24. IDn Pin Current vs. Voltage

TEST TIMING DIAGRAMS

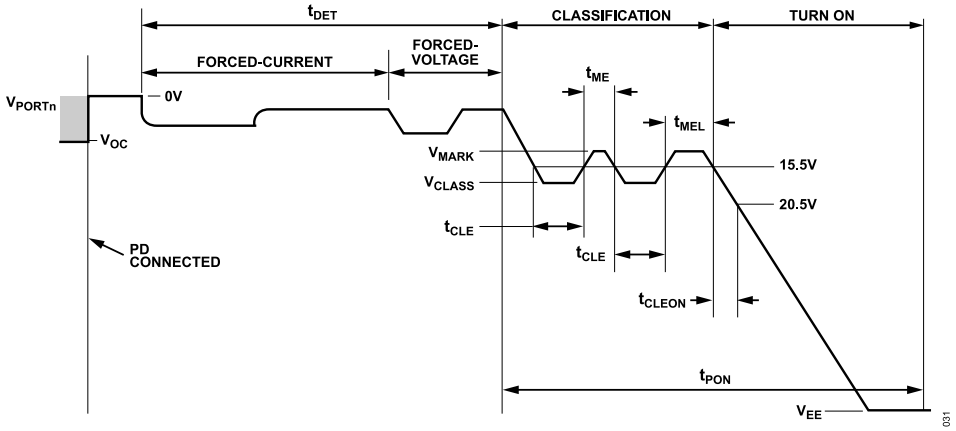


Figure 26. Detect, Class, and Turn-On Timing

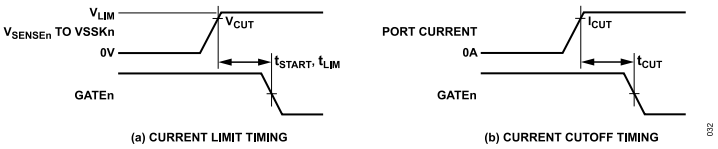


Figure 27. Current Limit and Cutoff Timings

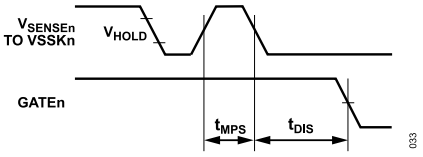


Figure 28. DC Disconnect Timing

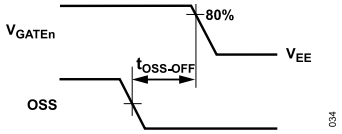


Figure 29. One-Bit Shutdown Priority Timing

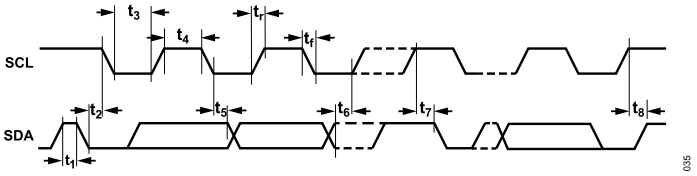


Figure 30. I²C Interface Timing

TEST TIMING DIAGRAMS

I²C TIMING DIAGRAMS

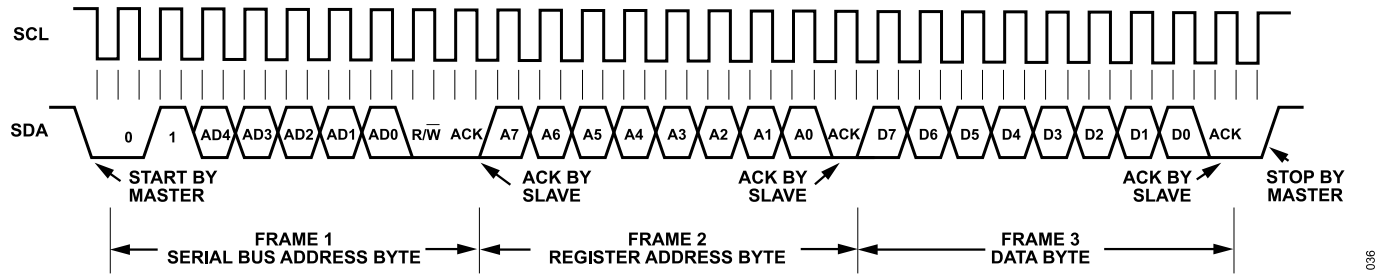


Figure 31. Writing to a Register

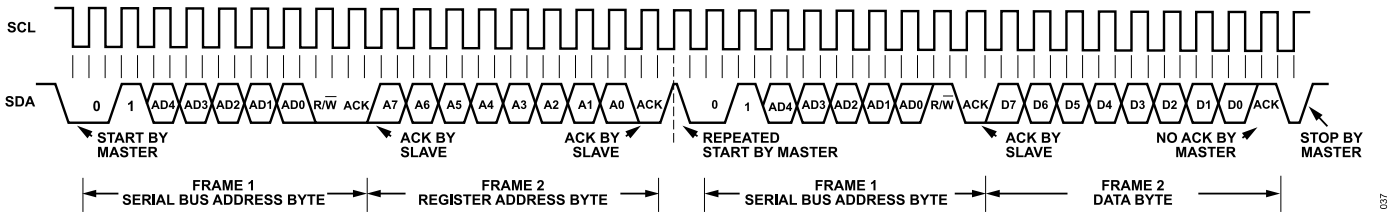


Figure 32. Reading from a Register

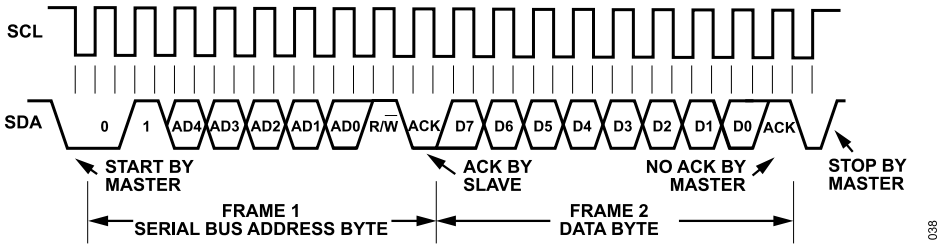


Figure 33. Reading the Interrupt Register (Short Form)

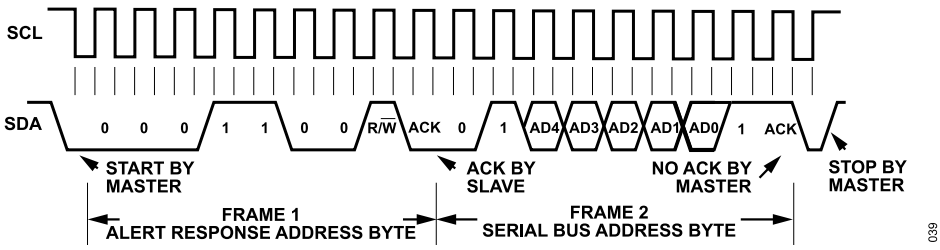


Figure 34. Reading from Alert Response Address

PIN FUNCTIONS

Pin No.	Mnemonic	Description
LTC9101-2A		
Pins 2, 1, Respectively	CFG[1:0]	Device Configuration Inputs. Tie the configuration pins high or low to set number of ports and number of connected LTC9102s. See Table 7 for details.
Pins 7, 23, Respectively	CAP[2:1]	Core Power Supply Bypass Capacitors. Connect each pin to a 1µF capacitance to DGND for the internal 1.2V regulator bypass. Do not use other capacitor values. Do not source or sink current from this pin.
Pin 8	CPD	Clock Transceiver Positive Input Output (Digital). Connect to CPA through a data transformer.
Pin 9	CND	Clock Transceiver Negative Input Output (Digital). Connect to CNA through a data transformer.
Pin 10	DPD	Data Transceiver Positive Input Output (Digital). Connect to DPA through a data transformer.
Pin 11	DND	Data Transceiver Negative Input Output (Digital). Connect to DNA through a data transformer.
Pins 12, 19, 24	V_{DD}	V_{DD} IO Power Supply. Connect to a 3.3V power supply relative to DGND. Each V_{DD} pin must be locally bypassed with at least a 0.1µF capacitor. A 10µF bulk capacitor must be connected across V_{DD} for increased surge immunity.
Pin 14	$\overline{\text{RESET}}$	Reset Input, Active Low. When $\overline{\text{RESET}}$ is low, the LTC9101-2A/LTC9102 is held inactive with all ports off and all internal registers reset. When $\overline{\text{RESET}}$ is pulled high, the LTC9101-2A/LTC9102 begins normal operation. $\overline{\text{RESET}}$ can be connected to an external capacitor or RC network to provide a power turn-on delay. Internal filtering of $\overline{\text{RESET}}$ prevents glitches less than 1µs wide from resetting the LTC9101-2A/LTC9102. Internally pulled up to V_{DD}.
Pin 15	$\overline{\text{INT}}$	Interrupt Output, Open Drain. $\overline{\text{INT}}$ pulls low when any one of several events occur in the LTC9101-2A. It returns to a high impedance state when bits 6 or 7 are set in the "Reset" register. The $\overline{\text{INT}}$ signal can be used to generate an interrupt to the host processor, eliminating the need for continuous software polling. Individual $\overline{\text{INT}}$ events can be disabled using the "Int Mask" register. Refer to the LTC9101-2A software interface data sheet for more information. $\overline{\text{INT}}$ is only updated between I^2C transactions.
Pin 16	SDAOUT	Serial Data Output, Open Drain Data Output for the I^2C Serial Interface Bus. The LTC9101-2A uses two pins to implement the bidirectional SDA function to simplify opto-isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.
Pin 17	SDAIN	Serial Data Input. High impedance data input for the I^2C serial interface bus. The LTC9101-2A uses two pins to implement the bidirectional SDA function to simplify opto-isolation of the I^2C bus. To implement a standard bidirectional SDA pin, tie SDAOUT and SDAIN together. See Applications Information for more information.
Pin 18	SCL	Serial Clock Input. High impedance clock input for the I^2C serial interface bus. The SCL pin should be connected directly to the I^2C SCL bus line. SCL must be tied high if the I^2C serial interface bus is not used.
Pin 20	OSS	Maskable Shutdown Input, Active High. Supports 1-bit shutdown priority. See the Over Supply Shutdown (OSS)) section for details. Internally pulled down to DGND.
Pins 21, 6, 5, 3, Respectively	AD[4:1]	I^2C Address Bits 4 to 1. Tie the address pins high or low to set the base I^2C serial address. The base address is ($01A_4A_3A_2A_1$0b). Internally pulled up to V_{DD}. See Bus Addressing for details.
Pins 22, 25	DGND	Digital Ground. DGND should be connected to the return from the V_{DD} supply.
LTC9102		
Pin 1	CAP3	Analog Internal 3.3V Power Supply Bypass Capacitor. Connect a 1µF ceramic cap to V_{EE}. A 3.3V power supply may be connected to this pin to improve power supply efficiency. The EXT3 pin must be pulled to CAP3 to shut off the internal 3.3V regulator if power is supplied externally. Do not source or sink current from this pin. Do not connect to CAP3 except as explicitly instructed in the Analog Devices documentation (for example, strapping LTC9102 pins and terminating the serial interface).
Pin 2	EXT3	External 3.3V Enable. Connect the EXT3 pin to CAP3 to shut off the

PIN FUNCTIONS

Pin No.	Mnemonic	Description
		internal 3.3V regulator when power is supplied externally. Float or connect to V_{EE} for internal regulator operation.
Pins 47, 46, 39, 38, 31, 30, 23, 22, 15, 14, 7, 6, Respectively	VSSK[12:1]	Kelvin Sense to V_{EE}. Connect to V_{EE} side of sense resistor for channel "n" through a 0.1Ω resistor. Do not connect directly to V_{EE} plane. See Kelvin Sense for requirements.
Pins 48, 45, 40, 37, 32, 29, 24, 21, 16, 13, 8, 5, Respectively	SENSE[12:1]	Current-Sense Input, channel "n". SENSEn monitors the external MOSFET current through a 0.1Ω sense resistor between SENSEn and VSSKn. If the voltage across the sense resistor reaches the current limit threshold I_{LIM-2P}, the GATEn pin voltage is lowered to maintain constant current in the external MOSFET. See Applications Information for further details. If the channel is unused, tie SENSEn to V_{EE}.
Pins 49, 44, 41, 36, 33, 28, 25, 20, 17, 12, 9, 4, Respectively	OUT[12:1]	Output Voltage Monitor, channel "n". Connect OUTn to the output channel. A current limit foldback circuit limits the power dissipation in the external MOSFET by reducing the current limit threshold when the drain-to-source voltage exceeds 10V. A port power good event is raised when the voltage from OUTn to V_{EE} drops below 2.4V (typ). A 500k resistor is connected internally from OUTn to AGND when the channel is idle. If the channel is unused, the OUTn pin must float.
Pins 50, 43, 42, 35, 34, 27, 26, 19, 18, 11, 10, 3, Respectively	GATE[12:1]	Gate Drive, channel "n". Connect GATEn to the gate of the external MOSFET for channel "n". When the MOSFET is turned on, the gate voltage is driven to 12V (typ) above V_{EE}. During a current limit condition, the voltage at GATEn is reduced to maintain constant current through the external MOSFET. If the fault timer expires, GATEn is pulled down, turning the MOSFET off, and raising a port fault event. If the channel is unused, the GATEn pin must float.
Pins 52, 51, Respectively	ID[1:0]	Transceiver ID. Sets the address of the LTC9102 on the multidrop high-speed data interface. ID numbering must start at 00b. Tie high by connecting to CAP3. Tie low by connecting to V_{EE}. See the Device Configuration section for details.
Pin 55	PWRIN	Startup Regulator Bypass and External Low Voltage Supply Input. Power for the internal 4.3V and 3.3V internal supplies. An internal regulator maintains the voltage of this pin above 6V. An external resistor or supply may be connected to this node to improve the power efficiency of the LTC9102. Connect a 1µF capacitor between this pin and V_{EE}.
Pin 56	AGND	Analog Ground.
Pins 57, 58, Respectively	PWRMD[1:0]	Maximum Power Mode Input. These pins must be left unconnected for all LTC9101-2A/LTC9102 applications.
Pin 59	CAP4	Analog Internal 4.3V Power Supply Bypass Capacitor. Connect a 1µF ceramic cap to V_{EE}. Do not source or sink current from this pin.
Pins 60, 65	V_{EE}	Main PoE Supply Input. Connect to a –51V to –57V supply, relative to AGND. Voltage depends on PSE Type (Type 3 or 4).
Pin 61	DNA	Data Transceiver Negative Input Output (Analog). Connect to DND through a data transformer.
Pin 62	DPA	Data Transceiver Positive Input Output (Analog). Connect to DPD through a data transformer.
Pin 63	CNA	Clock Transceiver Negative Input Output (Analog). Connect to CND through a data transformer.
Pin 64	CPA	Clock Transceiver Positive Input Output (Analog). Connect to CPD through a data transformer.
Common Pins		
LTC9101-2A Pins 4, 13; LTC9102 Pins 53, 54	NC, DNC	All pins identified with “NC” or “DNC” must be left unconnected.

APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet, or PoE, is a standard protocol for sending DC power over copper Ethernet data wiring. The IEEE group that administers the 802.3 Ethernet data standards added PoE powering capability in 2003. This original PoE standard, known as 802.3af, allowed for 48V DC power at up to 13W. 802.3af was widely popular, but 13W was not adequate for some applications. In 2009, the IEEE released a new standard, known as 802.3at or PoE+, increasing the voltage and current requirements to provide 25.5W of delivered power. IEEE 802.3af and 802.3at are commonly known as PoE 1. In 2018, the IEEE released the latest PoE standard, known as 802.3bt or PoE 2. 802.3bt maximizes PD delivered power at 71.3W.

The IEEE standard also defines PoE terminology. A device that provides power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: endpoints (typically network switches or routers), which provide data and power; and midspans, which provide power but pass through data. Midspans are typically used to add PoE capability to existing non-PoE networks. PDs are typically IP phones, wireless access points, security cameras, and similar devices.

LTC9101-2A/LTC9102 Product Overview

The LTC9101-2A/LTC9102 is a sixth generation PSE controller that implements up to 48 (25.5W) 2-pair PSE ports in an endpoint application. Virtually all necessary circuitry is included to implement an IEEE 802.3at compliant PSE design, requiring an external power MOSFET and sense resistor per port; these minimize power loss compared to alternative designs with onboard MOSFETs, and increase system reliability.

The LTC9101-2A/LTC9102 chipset implements an optional proprietary isolation scheme for inter-chip communication. This architecture substantially reduces BOM cost by replacing expensive opto-isolators and isolated power supplies with a single low-cost transformer. A single LTC9101-2A is capable of controlling a bus of up to four LTC9102s over this transformer-isolated interface. Direct connection of the LTC9101-2A and the associated LTC9102s is also possible.

The LTC9101-2A/LTC9102 offers a configurable interrupt signal triggered by per-port events, per-port power on control and fault telemetry, per-port current monitoring, V_{EE} monitoring, and one second rolling current and voltage averaging.

The LTC9101-2A/LTC9102 also offers advanced sixth-generation PSE features including internal eFlash for storage of firmware updates and custom user configuration packages, I^2C quad virtualization for full backwards-compatibility with quad-based IC drivers, ultralow 100mΩ sense resistors, +80V/–20V tolerant port-facing pins, and improvements to cable surge ride through.

Each LTC9102 power channel is implemented with dedicated detection and classification hardware. This allows all ports to detect, classify, and power on simultaneously, drastically reducing power on latency across a switch. Other less advanced PSEs are subject to visible delays as PDs, for example, LED lights, power on a port-by-port basis.

V_{EE} and port current measurements are performed simultaneously, enabling coherent and precise per-port power monitoring.

802.3AT 2-PAIR OPERATION

The LTC9101-2A includes up to 12 groups of four identical ports. Each group of four ports is referred to as a quad. In the LTC9101-2A architecture, each quad contains register configuration and status for four 802.3at ports.

The terms port, channel, and power channel are used interchangeably throughout this document. These terms refer to a single 802.3at PSE port.

802.3at Type 1 Mode

All 802.3at-compliant PSEs are fully backwards compatible with existing 802.3at Type 1 PDs, as shown in Table 5. 802.3at-compliant PSEs are forwards interoperable with new 802.3bt Type 3 and Type 4 PDs.

Note that an 802.3at PSE does not pass an 802.3bt PSE compliance test, and an 802.3bt PSE does not pass an 802.3at PSE compliance test. This is by design of the respective standards. 802.3at and 802.3bt devices are designed to be interoperable.

Table 5. PSE Maximum Delivered Power, Per-Port

DEVICE			PSE			
	STANDARD		802.3at		802.3bt	
		TYPE	1	2	3	4
PD	802.3at	1	13W	13W	13W	13W
		2	13W[1]	25.5W	25.5W	25.5W
	802.3bt	3	13W[1]	25.5W[1]	51W	51W
		4	13W[1]	25.5W[1]	51W[1]	71.3W

[1] Indicates PD allocated less power than requested.

POE BASICS

Common Ethernet data connections consist of two or four twisted pairs of copper wire (commonly known as Ethernet cable), transformer-coupled at each end to avoid ground loops. PoE systems take advantage of this coupling arrangement by applying voltage between the center-taps of the data transformers to transmit power from the PSE to the PD without affecting data transmission. Figure 35 shows a high level PoE system schematic.

To avoid damaging legacy data equipment that does not expect to see DC voltage, the PoE standard defines a protocol that determines when the PSE may apply and remove power. Valid

APPLICATIONS INFORMATION

PDs are required to have a 25k common-mode resistance at their input. When such a PD is connected to the cable, the PSE detects this signature resistance and applies power. When the PD is later disconnected, the PSE senses the open circuit and removes power. The PSE also removes power in the event of a current fault or short circuit.

When a PD is detected, the PSE looks for a classification signature that tells the PSE the maximum power the PD draws. The PSE can use this information to allocate power among several ports, to police the power consumption of the PD, or to reject a PD that draws more power than the PSE has available.

Table 6. 802.3at-Specified Power Allocations

PD CLASS	PSE OUTPUT POWER	ALLOCATED CABLING LOSS	PD INPUT POWER
1	4W	0.16W	3.84W
2	7W	0.51W	6.49W
0, 3	15.4W	1.4W	13W
4	30W	4.5W	25.5W

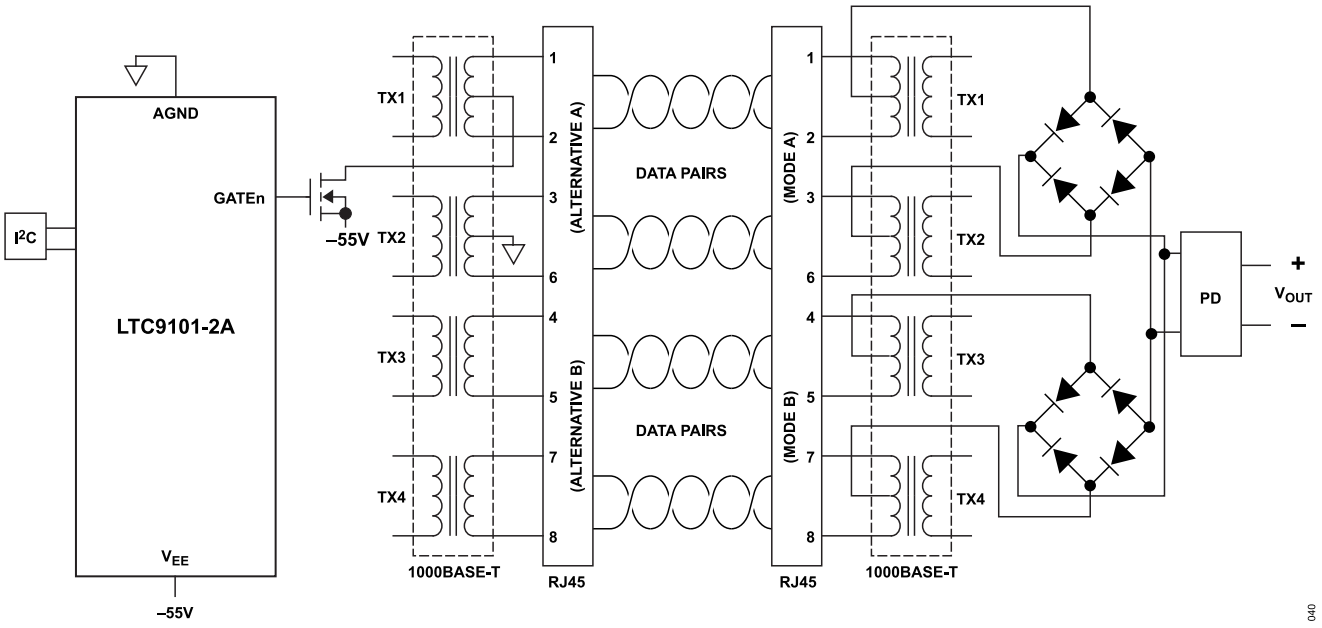


Figure 35. 2-Pair Power over Ethernet System Diagram, Endpoint PSE

Table 7. Device Configuration Options

CFG [1:0]	NUMBER OF PORTS	NUMBER OF 9101s	NUMBER OF 9102s	I²C ADDRESSES	I²C ADDRESS OFFSET											
					0	1	2	3	4	5	6	7	8	9	10	11
0 00	12	1	1	3	✓	✓	✓									
1 01	24	1	2	6	✓	✓	✓	✓	✓	✓						
2 10	36	1	3	9	✓	✓	✓	✓	✓	✓	✓	✓	✓			
3 11	48	1	4	12	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

APPLICATIONS INFORMATION

DEVICE CONFIGURATION

An LTC9101-2A can control between one and four LTC9102. Each LTC9102 controls 12 ports. Thus, each LTC9101-2A can control up to 48 ports.

As described later in Bus Addressing, each group of four ports occupies a single I^2C address.

OPERATING MODES

The LTC9101-2A/LTC9102 controls up to 48 independent ports, each of which can operate in one of two modes: manual or semi-auto. A third mode, shutdown, disables the port (see Table 8).

Table 8. Operating Modes

MODE	PORT MODE	DETECT/CLASS	POWER-UP
Semi-Auto	10b	Host Enabled	Upon Request
Manual	01b	Once Upon Request	Upon Request
Shutdown	00b	Disabled	Disabled

In manual mode, the port waits for instructions from the host system before taking any action. When commanded by the host, the port runs a single detection or classification cycle and reports the result in its "Port Status" register. The host may command the port to immediately apply or remove power with no requirement for valid detection or classification results. Manual mode is not compliant with IEEE specifications.

In semi-auto mode, the port repeatedly attempts to detect and classify any PD attached to it. The port reports the status of these attempts back to the host. When commanded to apply power, the port verifies the presence of a compliant PD and applies power if a compliant device is connected. The host must enable detection and classification.

In shutdown mode, the port is disabled and does not detect or power a PD.

Regardless of which mode it is in, the LTC9101-2A/LTC9102 removes power automatically from any port that generates a fault. It also automatically removes power from any port that generates a disconnect event if disconnect detection is enabled. The host controller may also command the port to remove power at any time.

DETECTION

Detection Overview

To avoid damaging network devices not designed to tolerate DC voltage, a PSE must determine whether the connected device is a valid PD before applying power. The IEEE 802.3 specification requires that a valid PD has a common-mode resistance of 25k ±5% at any port voltage below 10V. The PSE must accept resistances that fall between 19k and 26.5k, and it must reject resistances above 33k or below 15k (shaded regions in Figure 36). The PSE may choose to accept or reject resistances in the undefined areas between the must-accept and must-reject ranges. In particular, the PSE must reject standard computer network interface cards (NICs), many of which have 150Ω common-mode termination resistors that are damaged if power is applied to them (the black region at the left of Figure 36).

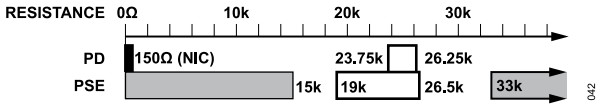


Figure 36. IEEE 802.3 Signature Resistance Ranges

Multipoint Detection

The LTC9101-2A/LTC9102 uses a multipoint method to detect PDs. False-positive detections are rejected by checking for signature resistance with both forced current and forced voltage measurements.

Initially, two test currents are forced onto the port (through the OUTn pin) and the resulting voltages are measured. The LTC9101-2A calculates the difference between the two V-I points to determine the resistive slope while removing offset caused by series diodes or leakage at the port (see Figure 37). If the forced current detection yields a valid signature resistance, two test voltages are then forced onto the port and the resulting currents are measured and subtracted. Both methods must report valid resistances to report a valid detection. PD signature resistances between 17k and 29k (typical) are accepted as valid and reported as "Detect Valid" in the corresponding "Detection Status" register. Values outside this range, including open and short circuits, are also reported. If the port measures less than 1V during any forced current test, the detection cycle aborts and "Short Circuit" is reported. Table 9 shows the possible detection results.

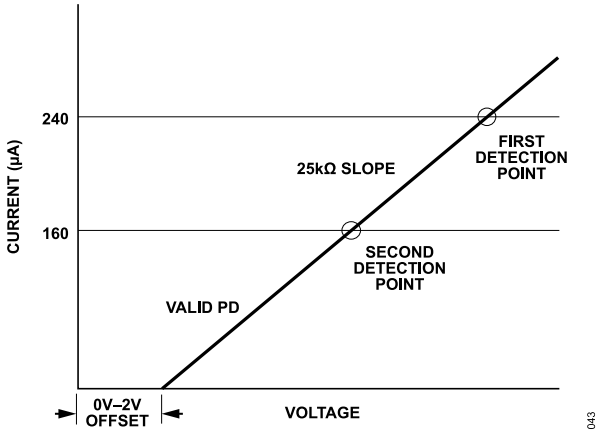


Figure 37. PD Detection

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Table 9. Detection Status

MEASURED PD SIGNATURE (TYPICAL)	DETECTION RESULT
Incomplete or Not Yet Tested	Detect Status Unknown
V_{PD} < 1V	Short Circuit
C_{PD} > 2.7µF	C_{PD} Too High
R_{PD} < 17k	R_{SIG} Too Low
17k < R_{PD} < 29k	Detect Valid
R_{PD} > 29k	R_{SIG} Too High
R_{PD} > 50k	Open Circuit
I_{PSE} = 0 and V_{PD} > 10V	PSE Detected or Port is Precharged
MOSFET Fault	MOSFET Fault Detected

More on Operating Modes

The port's operating mode determines when the LTC9101-2A/LTC9102 runs a detection cycle. In manual mode, the port remains idle until the host orders a detect cycle. It then runs detection, reports the result, and returns to idle to wait for another command.

In semi-auto mode, the LTC9101-2A/LTC9102 autonomously polls a port for PDs, but does not apply power until commanded to do so by the host. The "Detection/Classification Status" registers are updated at the end of each detection/classification cycle.

In semi-auto mode, if a valid signature resistance is detected and classification is enabled, the port classifies the PD and reports the Class result. If a power-on request is not received from the host, the port waits for 150ms (typical) and repeats the detection cycle. This periodically refreshes the "Detection/Classification Status" registers.

The LTC9101-2A offers a rich selection of power-on commands for IEEE compliance, power negotiation, and powering non-standard devices. Refer to the LTC9101-2A software interface data sheet for details on the power on pushbuttons.

Detection is disabled for a port when the LTC9101-2A/LTC9102 is initially powered up, when the port is in shutdown mode, or when the corresponding "Detect Enable" bit is cleared.

Detection of Legacy PDs

Proprietary PDs that predate the original IEEE 802.3af standard are commonly referred to as legacy PDs. One type of legacy PD uses a large common-mode capacitance (>10µF) as the detection signature.

Legacy PDs may be inferred by detection and classification results. The LTC9101-2A/LTC9102 provides all the tools necessary to identify and power on legacy PDs.

CLASSIFICATION

802.3af Classification

A PD may optionally present a classification signature to the PSE to indicate the maximum power it draws while operating. The IEEE specification defines this signature as a constant current draw when the PSE port voltage is in the V_{CLASS} range (between 15.5V and 20.5V), as shown in Figure 39, with the current level indicating one of five possible PD signatures. Figure 38 shows a typical PD load line, starting with the slope of the 25k signature resistor below 10V, then transitioning to the classification signature current (in this case, "Class 3") in the V_{CLASS} range. Table 10 shows the possible classification values.

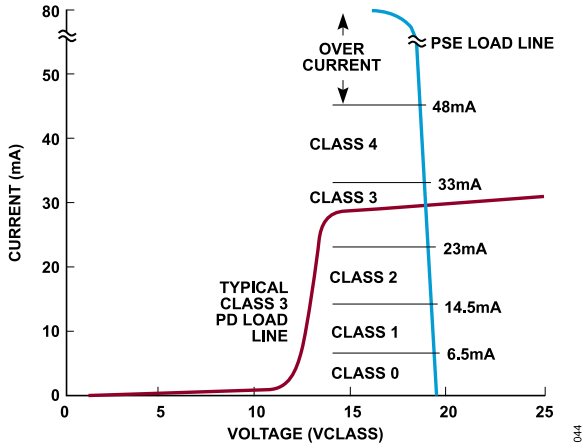

Figure 38. PD Classification

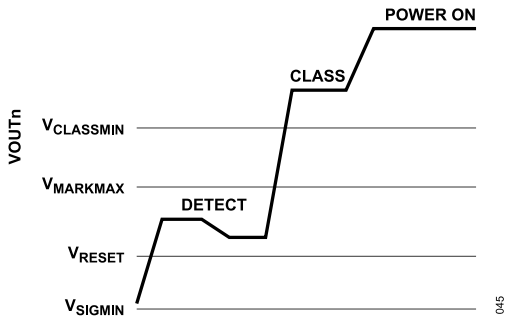

Figure 39. Type 1 or 2 PSE, 1-Event Class Sequence

Table 10. Type 1 and Type 2 PD Classification Values

CLASS	RESULT
Class 0	No Class Signature Present; Treat Like Class 3
Class 1	3.84W
Class 2	6.49W
Class 3	13W
Class 4	25.5W (Type 2)

If classification is enabled, the PSE classifies the PD immediately after a successful detection cycle. The PSE measures the PD classification signature by applying V_{CLASS} to the port through OUTn and measuring the resulting current; it then reports the discovered class in the appropriate "Port Status" register.

Classification is disabled for a port when the port is in shutdown mode or when the corresponding "Class Enable" bit is cleared.

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LLDP Classification

Introduced in 802.3at and extended by 802.3bt, the PoE specification defines a Link Layer Discovery Protocol (LLDP) method of classification. The LLDP method adds extra fields to the Ethernet LLDP data protocol.

Although the LTC9101-2A/LTC9102 is compatible with this classification method, it cannot perform LLDP classification directly as it does not have access to the data path. LLDP classification allows the host to perform LLDP communication with the PD and update the PD's power allocation. The LTC9101-2A/LTC9102 supports changing the "Police" levels dynamically, enabling system-level LLDP support.

802.3at 2-Event Classification

In 802.3at, 802.3af classification is named Type 1 classification. The 802.3at standard introduces an extension of Type 1 classification: Type 2 (2-event) classification. Type 2 PSEs are required to perform classification.

A Type 2 PD requesting 25.5W presents class signature 4 during all class events. If a Type 2 PSE with 25.5W of available power measures class signature 4 during the first class event, it forces the PD to V_{MARK} (9V typical), pauses briefly, and issues a second class event, as shown in Figure 40. The second class event informs the PD that the PSE has allocated 25.5W.

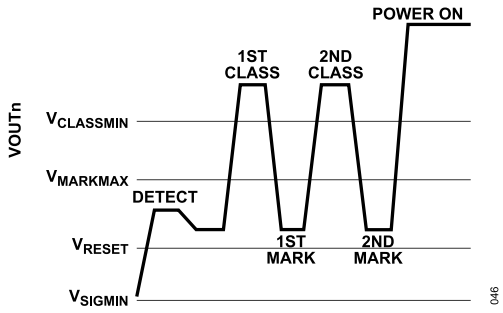

Figure 40. Type 2 PSE, 2-Event Class Sequence

Note that the second classification event only runs if required by the IEEE classification procedure. For example, a Class 0 to 3 PD is only issued a single class event, as shown in Figure 39.

The concept of demotion is introduced in 802.3at. A Type 2 PD may be connected to a PSE only capable of delivering 13W, perhaps due to power management limitations. In this case, the PSE performs a single classification event, as shown in Figure 39, and note that 25.5W is requested. Due to the limited power availability, the PSE does not issue a second event and proceeds directly to power on the PD. The presence of a single class event informs the Type 2 PD that it is demoted to 13W. If demoted, the PD is subject to power limitations and may operate in a reduced power mode.

Invalid Multi-Event Classification Combinations

The 802.3at specification defines a set of valid class signature combinations. All PDs return the same classification signature on the first two class events.

Any individual class signature that exceeds the class current limit is flagged as an invalid classification result. Any sequence of class signatures that does not represent a legal sequence is likewise flagged as an invalid classification result.

POWER CONTROL

The primary function of the LTC9101-2A/LTC9102 is to control power delivery to the PSE port.

The LTC9101-2A/LTC9102 delivers power by controlling the gate drive voltage of an external power MOSFET while monitoring the current (through an external sense resistor) and the output voltage (across the OUT pin).

The LTC9101-2A/LTC9102 connects the V_{EE} power supply to the PSE port in a controlled manner, meeting the power demands of the PD while minimizing power dissipation in the external MOSFET and disturbances to the V_{EE} backplane.

Inrush Control

When commanded to apply power to a port, the LTC9101-2A/LTC9102 ramp up the GATE pin, raising the external MOSFET gate voltage in a controlled manner.

During a typical inrush, the MOSFET gate voltage rises until the external MOSFET is fully enhanced or the port reaches the inrush current limit (I_{INRUSH}). I_{INRUSH} is set automatically by the PSE. I_{INRUSH} is 425mA (typical).

The GATE pin is servoed if port current exceeds I_{INRUSH}, actively limiting current to I_{INRUSH}. When the GATE pin is not being servoed, the final V_{GS} is 12V (typical).

During inrush, each port runs a timer (t_{START}). The port stays in inrush until t_{START} expires. When t_{START} expires, the PSE inspects port voltage and current. Inrush is successful if the MOSFET is fully enhanced and the port is drawing current below I_{INRUSH}.

If inrush is not successful, power is removed and the corresponding t_{START} fault is set. Otherwise, the port advances to power on and the programmed current limiting thresholds are used as described in the Current Limit section.

Port Current Policing

The current policing threshold (Police) is monitored on a per-port basis. When the output current over a t_{CUT} moving average exceeds the specified threshold, power is removed from the port and the corresponding I_{CUT} fault is set. The "Police" threshold and

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t_{CUT} timer duration are programmable. Refer to the LTC9101-2A software interface data sheet for encoding details.

Current Limit

Each LTC9101-2A/LTC9102 port includes an implicit current limiting threshold (I_{LIM-2P}), with a corresponding timer (t_{LIM}). The I_{LIM} threshold is a function of the applied "Police" threshold, as shown in Table 11.

Table 11. I_{LIM} Values

Police	I_{LIM} (Typical)
≤320mA	425mA[1]
>320mA	850mA

[1] PDs powered on as "Class 4" devices (that is, 2-event classification) maintain an 850mA I_{LIM} threshold regardless of the "Police" setting.

The LTC9101-2A/LTC9102 actively controls the MOSFET gate drive to keep the port current below I_{LIM}. Figure 7 shows that the LTC9101-2A/LTC9102 I_{LIM} threshold is implemented as a two-stage foldback circuit that reduces the port current if the port voltage falls below the normal operating voltage. This keeps MOSFET power dissipation at safe levels. The I_{LIM} current limiting circuit is always enabled and actively limiting port current.

The t_{LIM} timer duration is adjustable, as shown in Table 12. Each quad offers an independent timer duration control. The t_{LIM} timer duration may be adjusted at any time. The updated timer duration is immediately applied to all ports in the affected quad.

Table 12. T_{LIM} Settings

Field	T_{LIM} (Typical)
00b (Default)	Type 1 T_{LIM} 60ms
01b	Spare T_{LIM} 17ms
10b	Type 2 T_{LIM} 13ms
11b	Spare T_{LIM} 11ms

MOSFET Fault Detection

LTC9101-2A/LTC9102 PSE ports are designed to tolerate significant levels of abuse, but in extreme cases it is possible for an external MOSFET to be damaged. A failed MOSFET may short source to drain, which makes the port appear to be on when it should be off; this condition may also cause the sense resistor to fuse open, turning off the port but causing SENSE to rise to an abnormally high voltage. A failed MOSFET may also short from gate to drain, causing GATE to rise to an abnormally high voltage. OUT, SENSE, and GATE are designed to tolerate up to 80V faults without damage.

If the LTC9101-2A/LTC9102 detects any of these conditions for more than 3.8ms, it disables all port functionality, reduces the gate drive pull-down current for the port, and reports a "MOSFET Fault" detection status. This is typically a permanent fault, but the host can attempt to recover by resetting the port, setting the port to shutdown mode, or by resetting the entire chip if a port reset fails to clear the fault. If the MOSFET is in fact bad, the fault quickly returns, and the port disables itself again. The remaining ports of the LTC9101-2A/LTC9102 are unaffected.

An open or missing MOSFET does not trigger a "MOSFET Fault" detection status, but causes a t_{START} fault if the LTC9101-2A/LTC9102 attempts to turn on the port.

Disconnect

The LTC9101-2A/LTC9102 monitors powered ports to ensure the PD continues to draw the minimum specified current. The I_{HOLD} threshold, monitored as the V_{HOLD} threshold across the 0.1Ω sense resistor, is used to determine if a PD is disconnected.

A disconnect timer (t_{DIS}) counts up whenever the port current is below the I_{HOLD} threshold, indicating that the PD is disconnected. If the t_{DIS} timer expires, the port is turned off and the corresponding disconnect fault is set. Alternatively, if the current increases above I_{HOLD} for a duration greater than t_{MPS} before the t_{DIS} timer expires, the t_{DIS} timer resets and the PD remains powered.

Although not recommended, the DC disconnect feature can be disabled by clearing the corresponding "DC Disconnect Enable" bit. Disabling the DC disconnect feature forces the LTC9101-2A/LTC9102 out of compliance with the IEEE standard. A powered port stays powered after the PD is removed; the still-powered port may be subsequently connected to a non-PoE data device, potentially causing damage.

The LTC9101-2A/LTC9102 does not include AC disconnect circuitry.

Fast Surge Recovery

High reliability systems demand excellent surge recovery. It is increasingly important for a PSE to minimize power disruption to the PDs during extreme power transients. Furthermore, PDs that do not meet minimum bulk capacitance requirements are particularly vulnerable to power brownouts with traditional PSE solutions. The LTC9101-2A/LTC9102 provides an improved hot swap responsiveness with excellent recovery from surge events.

During a surge event, the LTC9102 GATE pin quickly turns off the external MOSFET current flow to protect the PSE, the MOSFET, and downstream circuitry. As the surge dissipates, the LTC9102 quickly turns the MOSFET back on in a safe, current limited manner, while minimizing power disruption to the PD. The LTC9102 fast MOSFET turn off and power recovery better support both IEEE compliant PDs and PDs with lower bulk capacitance in high reliability applications.

Port Current Readback

The LTC9101-2A measures the current through each port with per-port A/D converters. Note that port current is only valid when

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the port is powered on and reads zero at all other times. Samples are taken continuously; a moving one second average is updated every 100ms.

Port Voltage and V_{EE} Readback

The LTC9101-2A/LTC9102 continuously measures the V_{EE} voltage with a dedicated A/D converter. This global V_{EE} measurement is fully synchronized to all port current measurements and can monitor down to the LTC9102 UVLO threshold.

Temperature Readback

In addition to the overtemperature fault in the supply event register, the LTC9101-2A also reports the die temperature of each corresponding LTC9102.

Overtemperature Protection

Overtemperature protection automatically removes power from the affected ports when the LTC9102 temperature exceeds a preset threshold (150°C, typ.). Ports are prevented from resuming operation until the die temperature drops below a preset recovery threshold (125°C, typ.). Refer to the LTC9101-2A software interface data sheet for details.

Over Supply Shutdown (OSS)

The LTC9101-2A provides a low latency port shedding feature to quickly reduce the system load when required. By allowing a preconfigured set of ports to be turned off, the current on an overloaded main power supply can be reduced rapidly while keeping high priority devices powered.

In 1-bit priority mode, each port can be configured to high or low priority. On a rising edge of the OSS HW pin, the low priority ports are shut down within 6.5µs.

If power is removed from a port due an OSS event, the corresponding "Disconnect", "Power Good", "Power Enable", and "OSS" event bits are set for that port or quad. Refer to the LTC9101-2A software interface data sheet for port disable effects.

If a port is turned off through OSS, the corresponding "Detection and Classification Enable" bits remain enabled, so the port begins redetection.

Port Remapping

The LTC9101-2A/LTC9102 supports the ability to remap ports logically. This can be achieved by writing the appropriate values into the port remapping register to achieve the remapping (see Table 13). By default, there is no remapping.

Table 13. Port Remapping

CODE	REMAPPING
00b	Port 1
01b	Port 2
10b	Port 3
11b	Port 4

Within a quad, any physical port can be mapped to any logical port.

Code Download

The LTC9101-2A firmware is field-upgradable by downloading and executing firmware images.

Contact Analog Devices for code download procedures and firmware images.

Firmware images are stored in a dedicated flash partition. A fully-compliant IEEE 802.3at firmware image is preconfigured on the LTC9101-2A. The firmware image may be overwritten by the user.

Two complete copies of the firmware image are maintained under separate error correction code (ECC) and cyclic redundancy check (CRC) protection for maximum data protection.

Stored Configurations

Custom I^2C register map initial values may optionally be stored in a dedicated flash partition (configuration package). When shipped from the factory, the LTC9101-2A contains a default configuration package, where register map initial values are as specified in the LTC9101-2A software interface data sheet. Register map default configurations may be stored during manufacturing bring up or field-updated through configuration package download, and are auto-loaded on reset.

Contact Analog Devices applications support for assistance in generating custom configuration packages. Configuration packages are downloaded using the same code download mechanisms as firmware packages. Package headers ensure configuration packages are identified and stored in the appropriate flash partition.

If a stored configuration is used, CFG[1:0] are still required to inform the LTC9101-2A how many LTC9102s are attached. AD[4:1] are still required to inform the LTC9101-2A of the base I^2C chip address.

Two identical copies of the configuration image are maintained under separate ECC and CRC protection for maximum data protection.

SERIAL DIGITAL INTERFACE

Overview

The LTC9101-2A communicates with the host using a standard SMBus/I^2C 2-wire interface. The LTC9101-2A is a slave-only device, and communicates with the host controller using standard SMBus protocols. Interrupts are signaled to the host through $\overline{INT}$.

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The timing diagrams (Figure 30 through Figure 34) show typical communication waveforms and their timing relationships. More information about the SMBus data protocols can be found at www.smbus.org.

Bus Addressing

The LTC9101-2A's primary 7-bit serial bus address is $01A_4A_3A_2A_10b$, with bits 4:1 set by AD[4:1] respectively. See Table 7 for device configuration options. Depending on device configuration, up to 12 I^2C addresses are populated from the I^2C base address upwards. All LTC9101-2As also respond to the broadcast address 1111111b, allowing the host to write the same command (typically configuration commands) to multiple LTC9101-2As in a single transaction. If the LTC9101-2A is asserting $\overline{INT}$, it also responds to the alert response address (0001100b) per the SMBus specification.

Each LTC9101-2A/LTC9102 is logically composed of multiple four port groups, known as quads, each packed into a single I^2C address. See Device Configuration section for details. For example, if CFG[1:0] is set to 00, an LTC9101-2A is configured as a 12-port device when attached to an LTC9102 (see Table 7). This configuration requires consecutive I^2C addresses, with quad offset 0 starting at the I^2C base address.

Interrupts and SMBAlert

Most port events can be configured to trigger an interrupt, asserting $\overline{INT}$ and alerting the host to the event. This removes the need for the host to poll the LTC9101-2A, minimizing serial bus traffic and conserving host CPU cycles. Multiple LTC9101-2As can share a common $\overline{INT}$ line, with the host using the SMBAlert protocol (ARA) to determine which LTC9101-2A caused an interrupt.

Register Description

For information on serial bus usage, and device configuration and status, refer to the LTC9101-2A software interface data sheet, which can be requested through the Analog Devices Software Request Form.

ISOLATION REQUIREMENTS

IEEE 802.3 Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, network segments are not required to be isolated from each other, provided that the segments are connected to devices residing within a single building on a single power distribution system.

If the PSE is part of a larger system, contains additional external non-Ethernet ports, or must be referenced to protective ground for some other reason, the PoE subsystem must be electrically isolated from the rest of the system.

The LTC9101-2A/LTC9102 chipset simplifies PSE isolation by allowing the LTC9101-2A chip to reside on the non-isolated side. There it can receive power from the main logic supply and connect directly to the I^2C/SMBus bus. In this case, the SDAIN and SDAOUT pins can be tied together and act as a standard I^2C/SMBus SDA pin. Isolation between the LTC9101-2A and LTC9102 is implemented using a proprietary transformer-based communication protocol. The High-Speed Data Interface section of this data sheet provides additional details.

For simple devices, such as unmanaged PoE switches, the isolation requirement can be met using an isolated main power supply for the entire device. This strategy can be used if the device has no electrically conducting ports other than twisted-pair Ethernet. The LTC9101-2A may directly connect to the LTC9102s in the above circumstances, or if the system already provides isolation.

EXTERNAL COMPONENT SELECTION

Power Supplies

The LTC9101-2A/LTC9102 requires two supply voltages to operate. V_{DD} requires 3.3V (nominally) relative to DGND. V_{EE} requires a negative voltage of between –51V to –57V for Type 2 PSEs, relative to AGND.

Digital Power Supply

V_{DD} provides digital power for the LTC9101-2A processor. Place a ceramic decoupling cap of at least 0.1µF from each V_{DD} to DGND, as close as practical to each LTC9101-2A. In addition, each LTC9101-2A must include a bulk cap of 10µF for robust surge immunity. A 1.2V core voltage supply is generated internally and requires a 1µF ceramic decoupling cap between the CAP1 pin and DGND, and between CAP2 and DGND.

In systems using Analog Devices' proprietary isolation, V_{DD} should be delivered by the host controller's non-isolated 3.3V supply. To maintain required isolation, LTC9102 AGND and LTC9101-2A DGND must not be connected. If using the direct connection scheme, the LTC9101-2A DGND must be connected to LTC9102 V_{EE}.

Main PoE Power Supply

V_{EE} is the main isolated PoE supply that provides power to the PDs. Because it supplies a relatively large amount of power and is subject to significant current transients, it requires more design care than a simple logic supply. For minimum IR loss and best system efficiency, set V_{EE} near maximum amplitude (57V), leaving enough margin to account for transient overshoot or undershoot, temperature drift, and the line regulation specifications of the particular power supply used.

A bypass capacitor and a transient voltage suppressor (TVS) between each LTC9102 AGND and V_{EE} are very important for reliable operation. If a short circuit occurs at one of the output ports, it can

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take as long as 1µs for the LTC9102 to begin regulating the current. During this time, the current is limited only by the small impedances in the circuit; a high current spike typically occurs, causing a voltage transient on the V_{EE} supply and possibly causing the LTC9101-2A/LTC9102 to reset due to a UVLO fault. A 1µF, 100V X7R capacitor and a SMAJ58A near each LTC9102 are recommended to minimize spurious resets. An electrolytic bulk capacitor of at least 47µF, 100V, and a bulk TVS are also recommended per system.

LTC9102 Low Voltage Power Supplies

The LTC9102 includes internal voltage regulators that generate low voltage supplies directly from the main PoE power supply. At start-up, an internal regulator generates 6V at PWRIN, drawing power from AGND. Internal 4.3V and 3.3V rails are sub-regulated from PWRIN. The PWRIN pin requires a local 1µF, 100V bypass capacitor.

Pull-up resistors can be connected from PWRIN to AGND to dissipate heat outside the LTC9102 package. Optionally, an external power supply can be connected to PWRIN to override the start-up regulator and reduce power dissipation.

Figure 41 shows a pull-up resistor configuration with the internal 3.3V regulator. Bypass resistors R1, R2, R3, and R4 draw heat away from the LTC9102s. Note that the voltage of the PWRIN pin changes based on the LTC9102 operating mode and its corresponding current consumption. If more current is consumed than the bypass resistors provide, the start-up regulator maintains the voltage at 6V typical. The LTC9102 can operate without the pull-up resistors in space-constrained applications.

In applications with an external PWRIN supply, a 6.5V regulator provides an optimum voltage to override the internal 6V start-up regulator, while minimizing the LTC9102 device heating. The external supply may be shared across multiple LTC9102s.

A 3.3V power supply can be connected directly to the CAP3 pin, as shown in Figure 42. This provides the most power efficient sleep mode. When supplying external 3.3V power, tie the EXT3 pin to CAP3. This disables the internal 3.3V regulator and prevents power back-feed. The 3.3V regulator must power up within $t_{CAP3EXT}$ specified in the Electrical Characteristics table.

If using the direct connection scheme, the 3.3V regulator that supplies the LTC9101-2A can also supply the LTC9102s. This is the recommended option when the LTC9101-2A and LTC9102 are on the same side of the system isolation barrier.

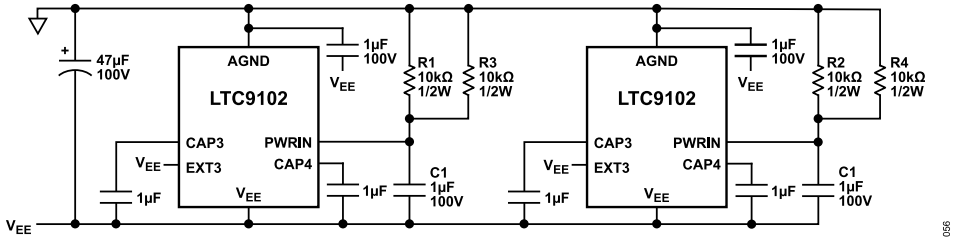

Figure 41. Power Supply Configuration with Internal 3.3V Supply

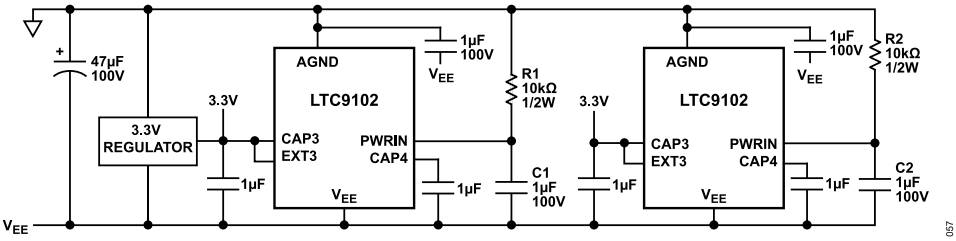

Figure 42. Power Supply Configuration with External 3.3V Regulator

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High-Speed Data Interface

The communication between the LTC9101-2A and LTC9102s is through a high-speed data interface over either a proprietary isolation scheme or direct connection scheme. For proper operation, strict layout guidelines must be met (see High-Speed Data Interface Layout).

In the proprietary isolation scheme, the LTC9101-2A/LTC9102 chipset uses a single pair of transformers to isolate the LTC9101-2A from one to four LTC9102s (see Figure 43). In this case, the SDAIN and SDAOUT pins can be shorted to each other and tied directly to the I^2C/SMBus bus. The transformers should be 10Base-T or 10/100Base-T with a 1:1 turns ratio. Optimally, the selected transformers do not have common-mode chokes. These transformers typically provide 1500V of isolation between the LTC9101-2A and the LTC9102s. Significant BOM cost reductions can be achieved using the proprietary isolation scheme.

In the direct connection scheme, the LTC9101-2A/LTC9102 chipset relies on pre-existing system isolation. In this scheme, the LTC9101-2A connects directly to one or more LTC9102s using a proprietary communication protocol (see Figure 44).

External MOSFET

Careful selection of the power MOSFET is critical to system reliability. Choosing a MOSFET requires extensive analysis and testing of the MOSFET SOA curve against the various PSE current limit conditions. Analog Devices recommends the PSMN075-100MSE for PSEs configured to deliver up to 25.5W maximum pairset power. These MOSFETs are selected for their proven reliability in PoE applications. Contact Analog Devices applications support before using a MOSFET other than this recommended part.

Sense Resistors

The LTC9101-2A/LTC9102 is designed for a low 0.1Ω current sense resistance per port, laid out as shown in the Layout Requirements section, Figure 46. To meet the I_{HOLD}, and I_{LIM} accuracy required by the IEEE specification, the sense resistors should have ±1% tolerance or better, and no more than ±200ppm/°C temperature coefficient.

Port Output Cap

Each port requires a 0.1µF cap across OUTn to AGND (see Figure 45) to keep the LTC9102 stable while in current limit during start-up or overload. Common ceramic capacitors often have significant voltage coefficients; this means the capacitance is reduced as the applied voltage increases. To minimize this problem, X7R ceramic capacitors rated for at least 100V are recommended and must be located close to the LTC9102.

Surge Protection

Ethernet ports can be subject to significant cable surge events. To keep PoE voltages below a safe level and protect the application against damage, protection components, as shown in Figure 45, are required at the main supply, at the LTC9102 supply pins, and at each port.

Bulk transient voltage suppression (TVS_{BULK}) and bulk capacitance (C_{BULK}) are required across the main PoE supply, and should be sized to accommodate system level surge requirements.

Across each LTC9102 AGND pin and V_{EE} pin is a SMAJ58A 58V TVS (D1) and a 1µF, 100V bypass capacitor (C1). These components must be placed close to the LTC9102 pins.

Each port requires an S1B clamp diode from OUTn to supply AGND. This diode steers harmful surges into the supply rails, where they are absorbed by the surge suppressors and the V_{EE} bypass capacitance. The layout of these paths must be low impedance.

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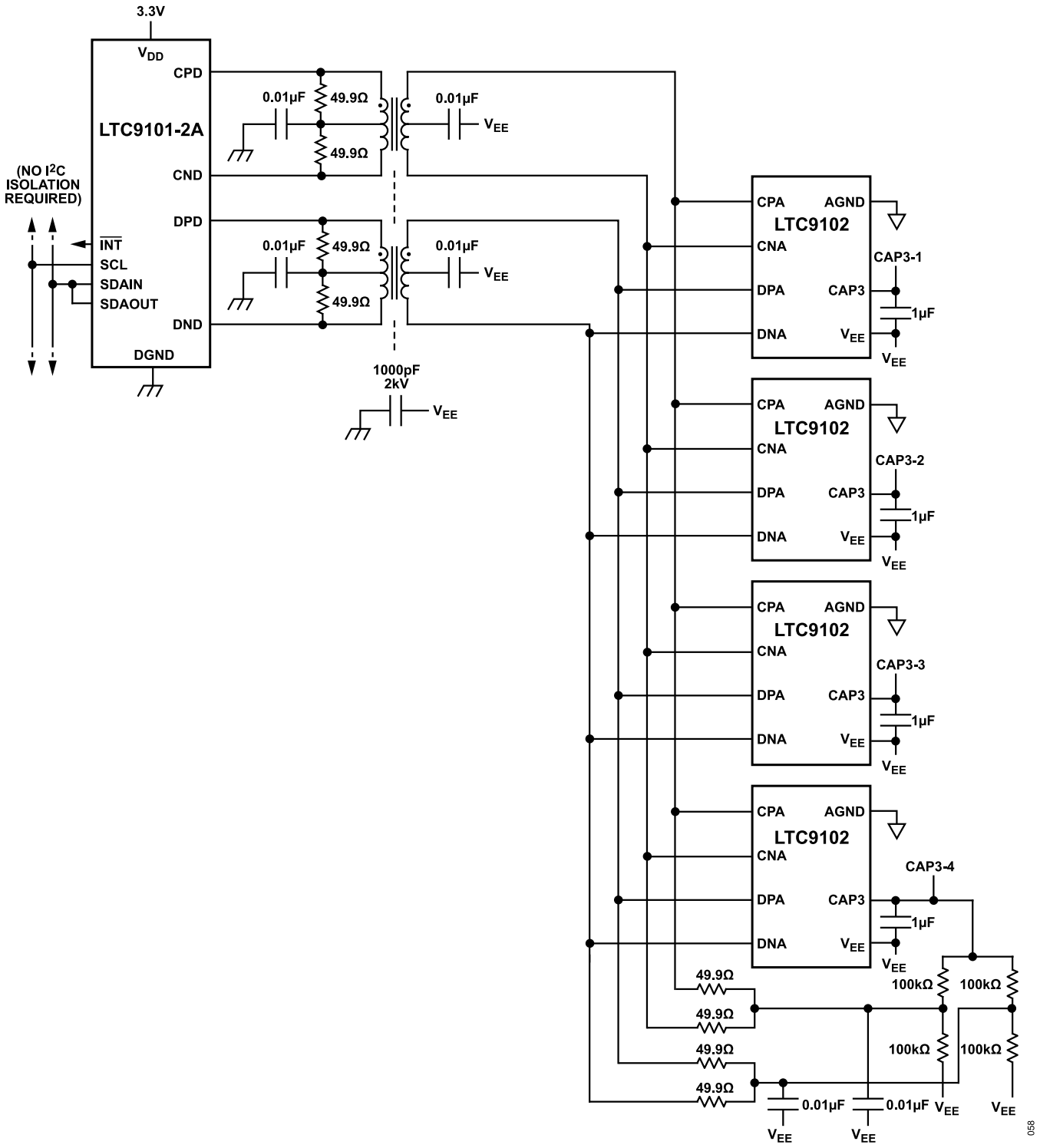
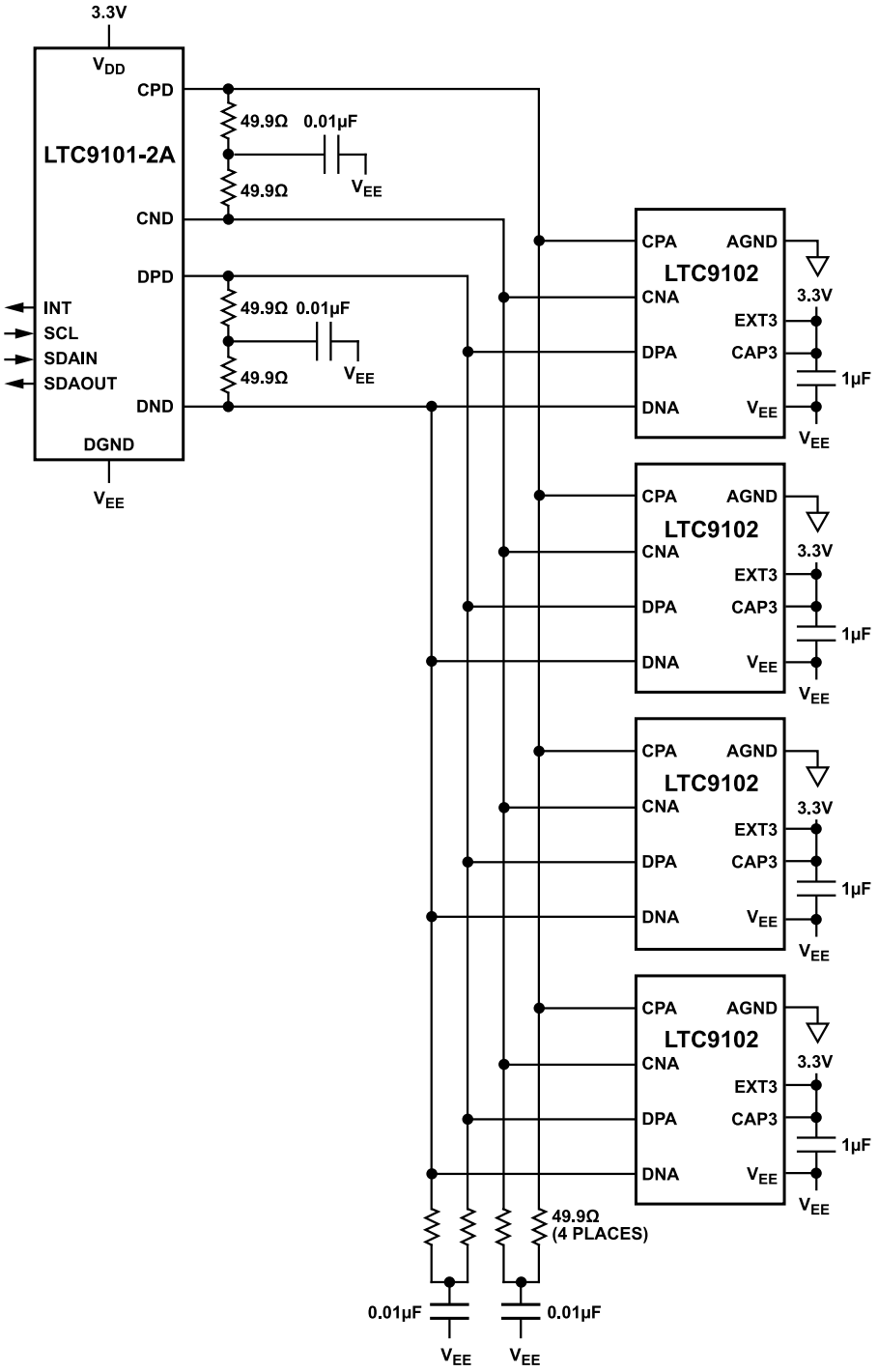


NOTES
1. MULTIPLE LTC9102 DEVICES ON THE HIGH-SPEED DATA INTERFACE ARE DAISY CHAINED.
2. THE HIGH-SPEED DATA INTERFACE IS TERMINATED AT BOTH ENDS.
3. THE 100k RESISTORS AT THE END OF THE HIGH-SPEED DATA INTERFACE CONNECT TO THE LAST LTC9102 CAP3.
4. THE MAXIMUM LENGTH OF THE HIGH-SPEED DATA INTERFACE IS 20 INCHES.
5. THE HIGH-SPEED DATA INTERFACE DIFFERENTIAL IMPEDANCE IS 100Ω.

Figure 43. LTC9101-2A/LTC9102 Proprietary Isolation Scheme

APPLICATIONS INFORMATION



NOTES
1. MULTIPLE LTC9102 DEVICES ON THE HIGH-SPEED DATA INTERFACE ARE DAISY CHAINED.
2. THE HIGH-SPEED DATA INTERFACE IS TERMINATED AT BOTH ENDS.
3. THE MAXIMUM LENGTH OF THE HIGH-SPEED DATA INTERFACE IS 20 INCHES.
4. THE HIGH-SPEED DATA INTERFACE DIFFERENTIAL IMPEDANCE IS 100Ω.

059

Figure 44. LTC9101-2A/LTC9102 Direct Connection Scheme

APPLICATIONS INFORMATION

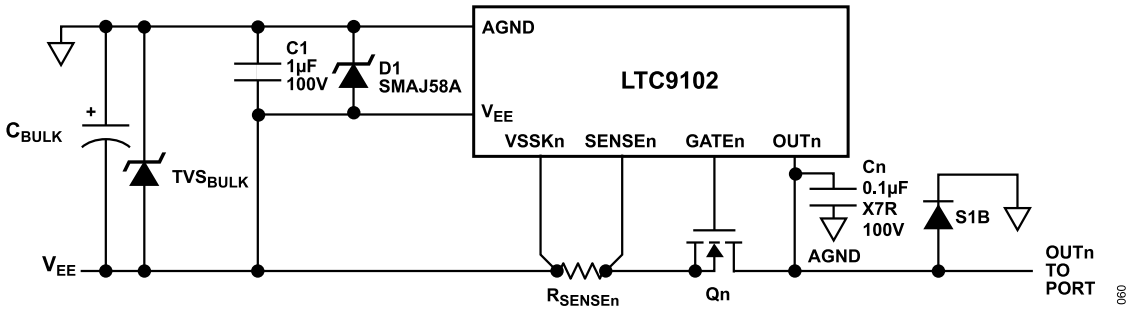


Figure 45. LTC9102 Surge Protection

Table 14. Component Selection for PSE Maximum Class

PSE CLASS	SENSE RESISTOR	HOT SWAP MOSFET	FUSE	ETHERNET TRANSFORMER
Class 3	100mΩ, 1%, 50mW	PSMN075-100MSE	SF-0603HI075F-2	7490220120
Class 4	100mΩ, 1%, 100mW	PSMN075-100MSE	SF-0603HI100F-2	7490220121

LAYOUT REQUIREMENTS

Strict adherence to board layout, parts placement, and routing requirements is critical for IEEE compliance, parametric measurement accuracy, system robustness, and thermal dissipation. Refer to the DC3160A-KIT demo kit for example layout references.

Kelvin Sense

Proper connection of the port current Kelvin sense lines is important for current threshold accuracy and IEEE compliance. See Figure 46 for an example layout of these Kelvin sense lines. The LTC9102 VSSKn pin is Kelvin connected to the sense resistor (V_{EE} side) pad and is not otherwise connected to V_{EE} copper areas. Similarly, the LTC9102 SENSEn pin is Kelvin connected to the sense resistor (SENSEn side) pad and is not otherwise connected in the power path. Figure 46 shows the two Kelvin traces from the LTC9102 to the sense resistor (R_{SENSEn}).

High-Speed Data Interface Layout

The LTC9101-2A/LTC9102 chipset communicates across a proprietary high-speed, multidrop data interface. This allows for a single LTC9101-2A to control up to four LTC9102s.

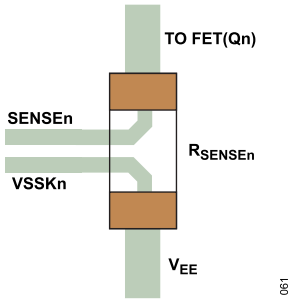


Figure 46. R_{SENSE} Kelvin Connections

The data-lines require impedance matched traces to each LTC9102. The data bus termination resistors must be located at the LTC9102 farthest away from the isolation transformers. For isolated applications, the DC biasing resistors must connect to the LTC9102 CAP3 pin farthest away from the isolation transformers. Figure 43 and Figure 44 show how to design the interface with 100Ω differential transmission lines, and terminate 100Ωs differentially. Limit the high-speed data interface line length to 20 inches. Minimize the transmission stubs between the LTC9102s and the high-speed data interface.

TYPICAL APPLICATIONS

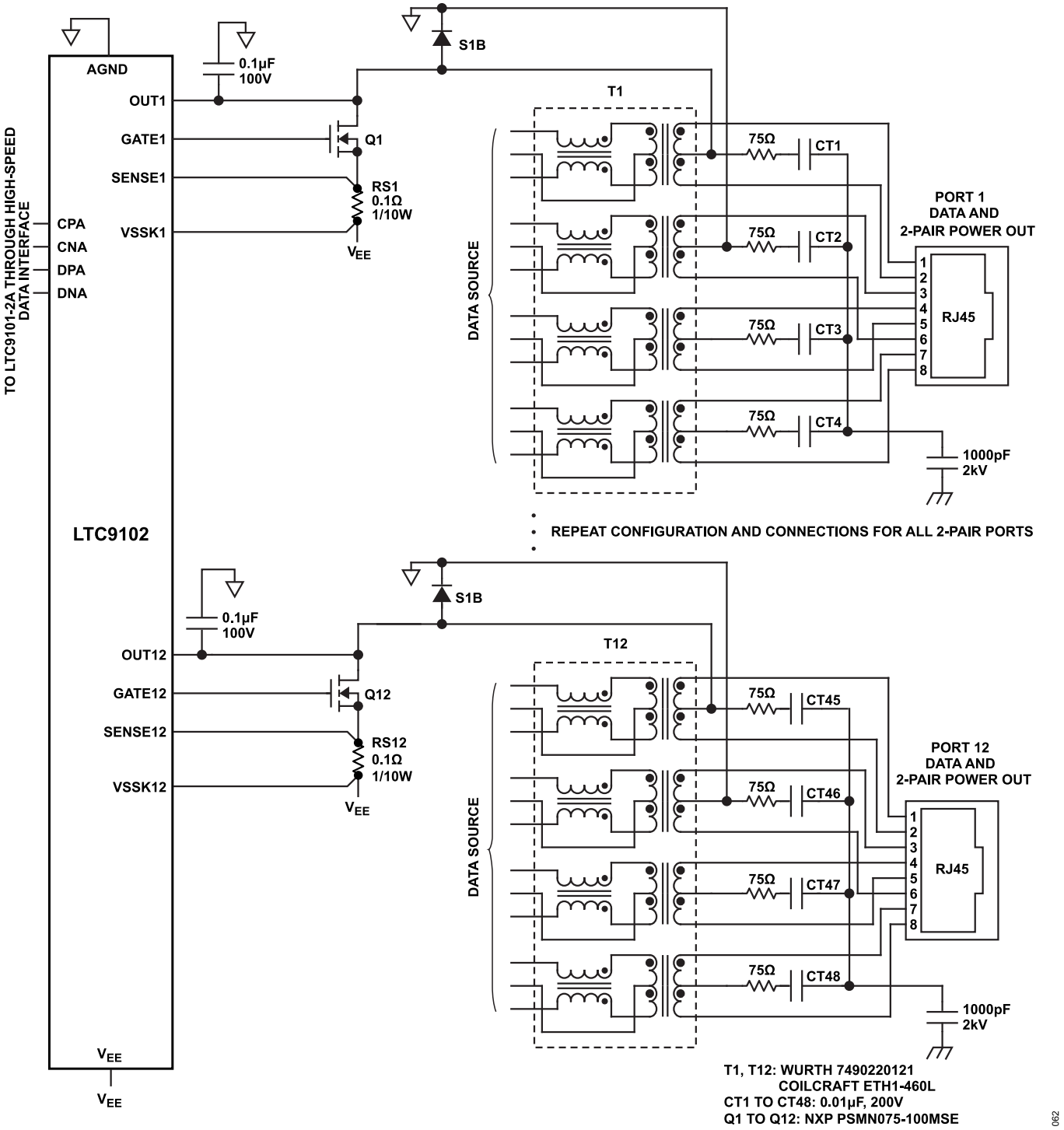
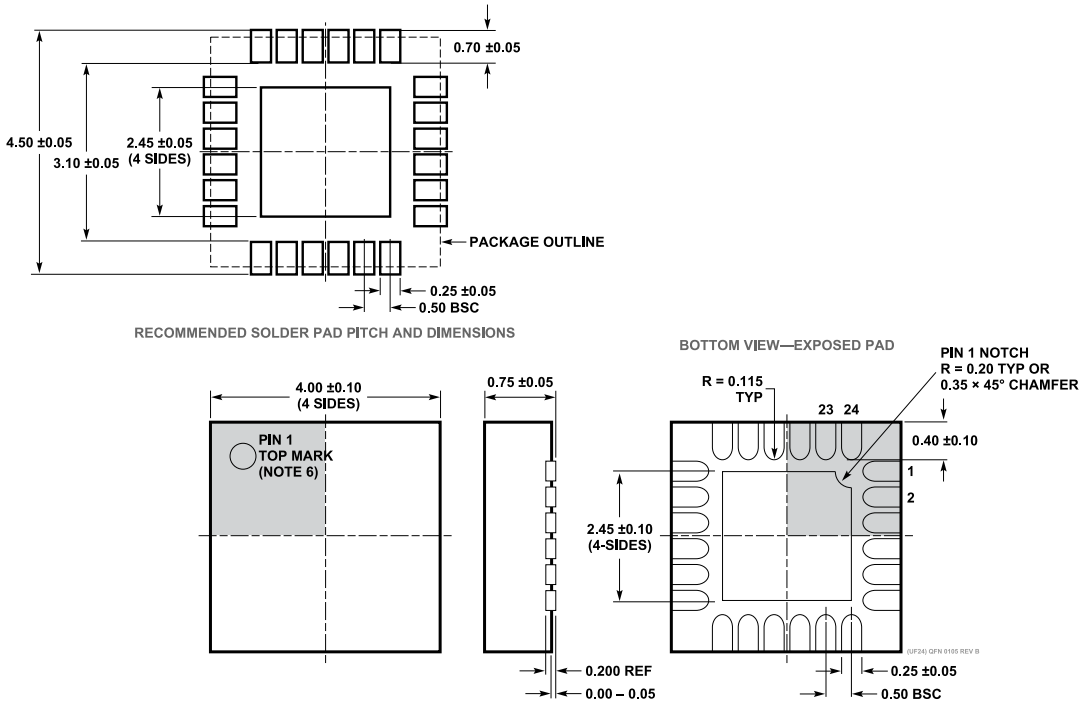


Figure 47. Alternative A (MDI-X) and B(S), 2-Pair, 1000BASE-T, IEEE 802.3at, Type 2 PSE, Ports 1 and 12 Shown

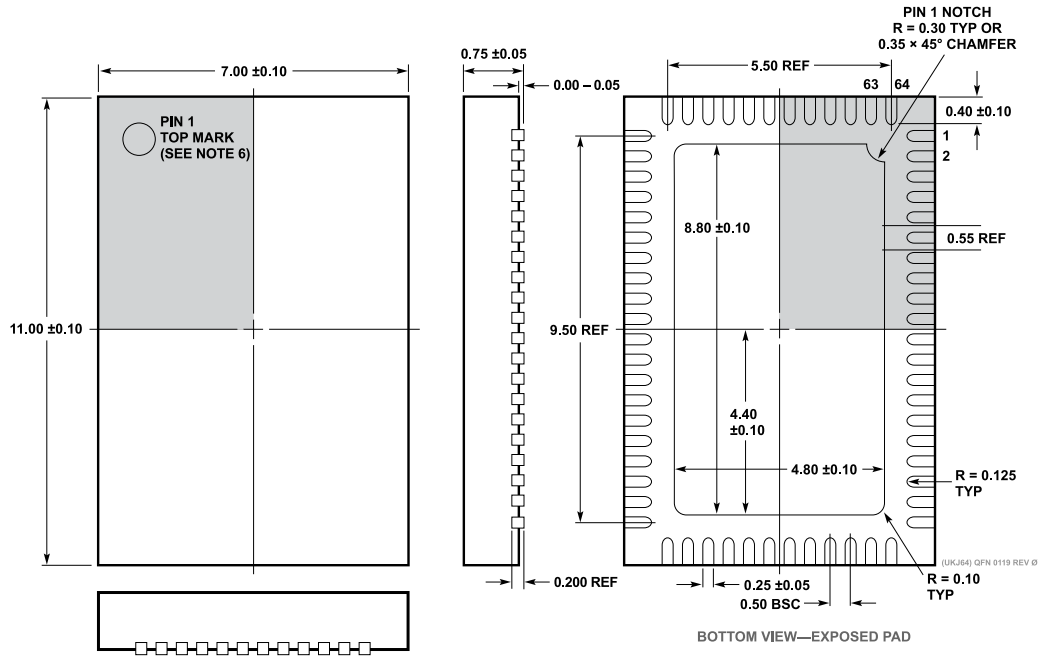
PACKAGE DESCRIPTION



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 48. UF Package
24-Lead Plastic QFN (4 mm × 4 mm)
(Reference LTC DWG 05-08-1697 Rev B)

PACKAGE DESCRIPTION



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

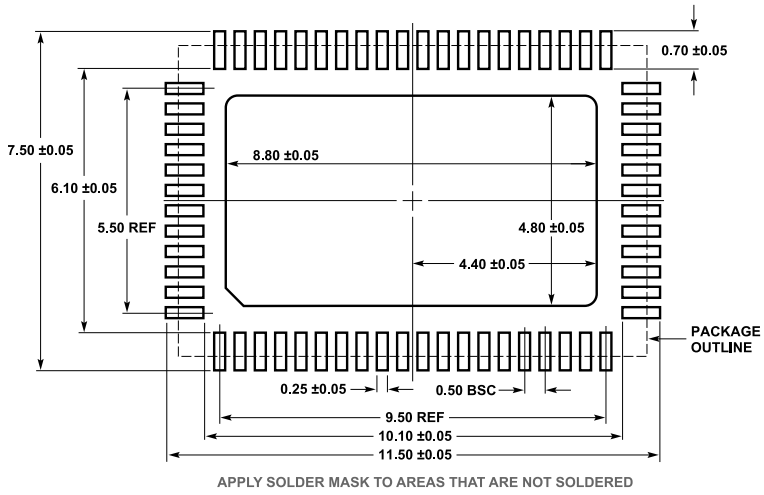
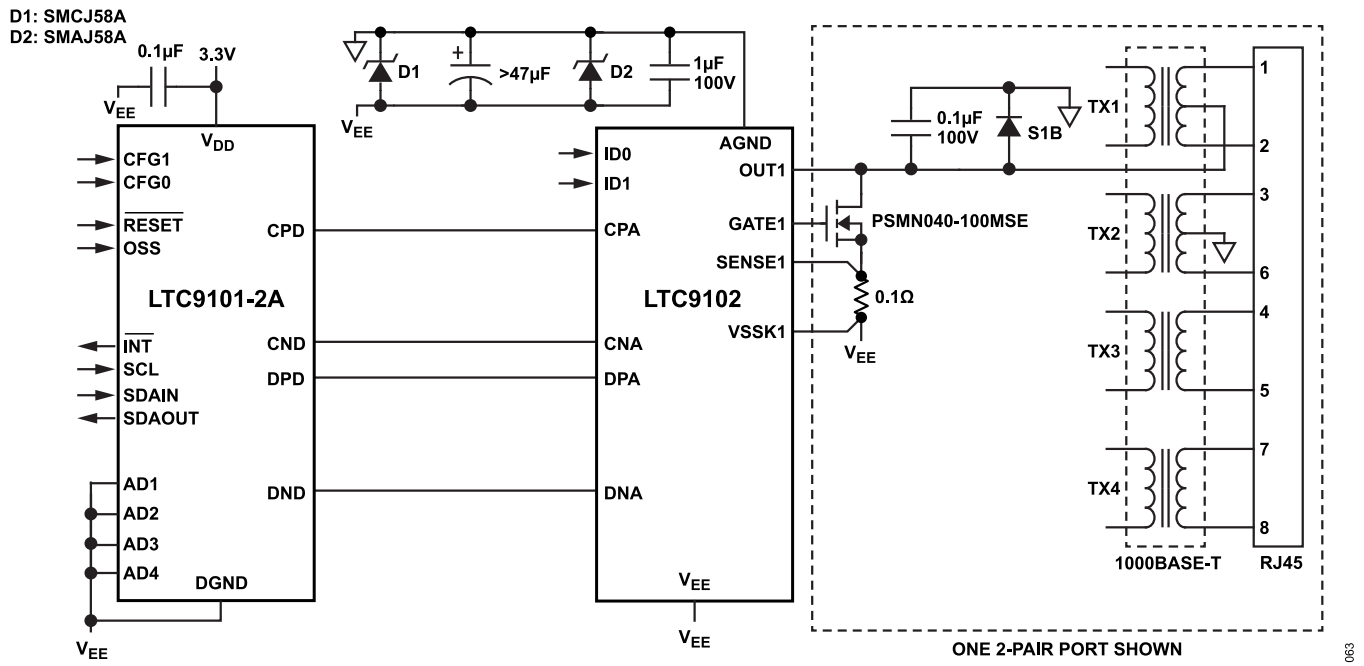


Figure 49. UKJ Package
64-Lead Plastic QFN (7 mm × 11 mm)
(Reference LTC DWG 05-08-1780 Rev 0)

TYPICAL APPLICATION



RELATED PARTS

Table 15. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTC9101-1/LTC9102/ LTC9103	48-Port IEEE 802.3at/802.3bt PoE PSE Controller	Lowest in Industry Power Path Dissipation with 0.1Ω Sense, Transformer Isolated Communications
LTC9101-2/LTC9102	24-Port IEEE 802.3bt PoE PSE Controller	Industry Standard Register Map, Lowest in Industry Power Path Dissipation with 0.1Ω Sense, Direct or Transformer Isolated Communications
LTC4292/LTC4291-1	4-Port IEEE 802.3bt PoE PSE Controller	Transformer Isolation, 14-bit Current Monitoring per Port with Programmable Current Limit, Supports Type 1 to Type 4 PDs
LT®4293	LTPoE++®/IEEE 802.3bt PD Interface Controller	External Switch, LTPoE++ and IEEE 802.3bt Support, Configurable Class and AUX Support
LT4294	IEEE 802.3bt PD Controller	External Switch, IEEE 802.3bt Support, Configurable Class and AUX Support
LT4295	IEEE 802.3bt PD with Forward/Flyback Switching Regulator Controller	External Switch, IEEE 802.3bt Support, Configurable Class, Forward or No-Opto Flyback Operation, Frequency, PG/SG Delays, Soft-Start, and Aux Support as Low as 9V, Including Housekeeping Buck, Slope Compensation
LTC4290/LTC4271	8-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports IEEE 802.3af, IEEE 802.3at, and LTPoE++ PDs
LTC4263	Single IEEE 802.3af PSE Controller	Internal MOSFET Switch
LTC4265	IEEE 802.3at PD Interface Controller	Internal 100V, 1A Switch, 2-Event Classification Recognition
LTC4266	Quad IEEE 802.3at PoE PSE Controller	With Programmable I_{CUT}/I_{LIM}, 2-Event Classification, and Port Current and Voltage Monitoring
LTC4267	IEEE 802.3af PD Interface with Integrated Switching Regulator	Internal 100V, 400mA Switch, Dual Inrush Current, Programmable Class
LTC4270/LTC4271	12-Port PoE/PoE+/LTPoE++ PSE Controller	Transformer Isolation, Supports Type 1, Type 2, and LTPoE++ PDs
LTC4278	IEEE 802.3at PD Interface with Integrated Flyback Switching Regulator	2-Event Classification, Programmable Class, Synchronous No-Opto Flyback Controller, 50kHz to 250kHz, 12V Aux Support
LTC4279	Single PoE/PoE+/LTPoE++ PSE Controller	Supports IEEE 802.3af, IEEE 802.3at, LTPoE++, and Proprietary PDs