

1.5MHz, 600mA Synchronous Step-Down Regulator with Bypass Transistor

FEATURES

- Dynamically Adjustable Output from 0.3V to 3.5V
- 600mA Output Current
- Internal 0.08Ω P-Channel MOSFET Bypass Transistor
- High Efficiency: Up to 96%
- 1.5MHz Constant Frequency Operation
- No Schottky Diode Required
- Low Dropout Operation: 100% Duty Cycle
- 2.5V to 5V Input Voltage Range
- Shutdown Mode Draws < 1μA Supply Current
- Current Mode Operation for Excellent Line and Load Transient Response
- Overtemperature Protected
- Available in 8-Lead 3mm × 3mm DFN Package

APPLICATIONS

- WCDMA Cell Phone Power Amplifiers
- Wireless Modems

DESCRIPTION

The LTC[®]3408 is a high efficiency monolithic synchronous buck regulator optimized for WCDMA power amplifier applications. The output voltage can be dynamically programmed from 0.3V to 3.5V. At $V_{OUT} > 3.6V$ an internal 0.08Ω bypass P-channel MOSFET connects V_{OUT} directly to V_{IN} , eliminating power loss through the inductor.

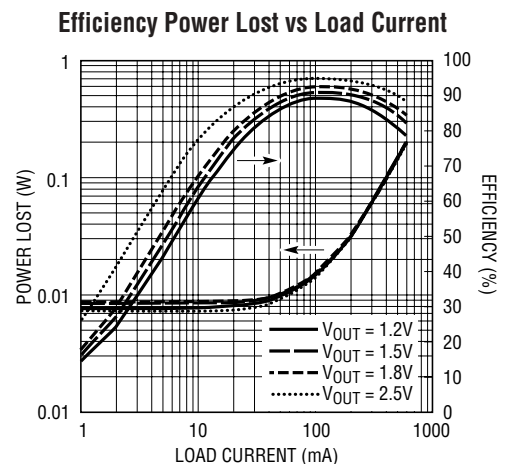
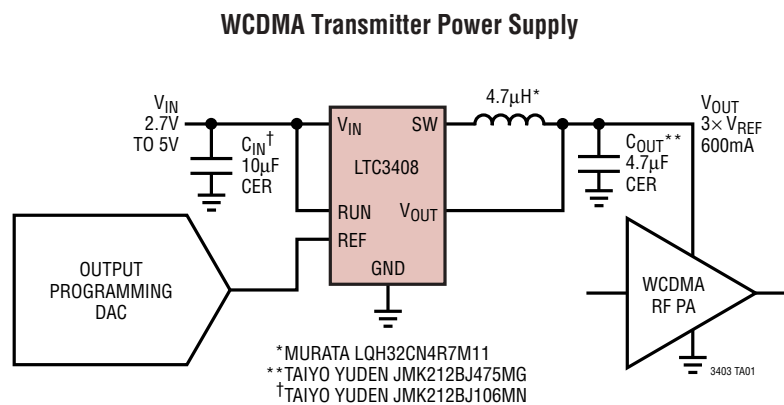
The input voltage range is 2.5V to 5V making the LTC3408 ideally suited for single Li-Ion battery-powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems.

Switching frequency is internally set at 1.5MHz, allowing the use of small surface mount inductors and capacitors. The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode.

The LTC3408 is available in a low profile (0.75mm) 8-lead 3mm × 3mm DFN package.

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 U.S. Patent Numbers: 5481178, 6580258, 6304066, 6127815, 6498466, 6611131

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (< 300μs)	-0.3V to 6V
Input Supply Voltage (DC)	-0.3V to 5.5V
RUN, REF, V _{OUT} Voltages	-0.3V to V _{IN}
SW Voltage (DC)	-0.3V to (V _{IN} + 0.3V)
P-Channel Switch Source Current (DC)	800mA
N-Channel Switch Sink Current (DC)	800mA
Peak SW Sink and Source Current	1.3A
Bypass P-Channel FET Source Current (DC)	1A
Operating Temperature Range (Note 2) ..	-40°C to 85°C
Junction Temperature (Note 3)	125°C
Storage Temperature Range	-65°C to 125°C

PACKAGE/ORDER INFORMATION

<p>DD PACKAGE 8-LEAD (3mm × 3mm) PLASTIC DFN EXPOSED PAD IS GND (PIN 9) MUST BE SOLDERED TO PCB</p> <p>T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 3°C/W</p>	ORDER PART NUMBER
	LTC3408EDD
	DD PART MARKING
	LAEA

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V _{OUT}	Regulated Output Voltage	V _{REF} = 1.1V V _{REF} = 0.1V	● 3.23	3.3	3.37	V	
ΔV _{OUT}	Output Voltage Line Regulation	V _{IN} = 2.5V to 5V, V _{REF} = 0.6V	● 0.25	0.3	0.35	V	
ΔV _{OUT}	Output Voltage Line Regulation	V _{IN} = 2.5V to 5V, V _{REF} = 0.6V	●	0.1	0.4	%/V	
I _{PK}	Peak Inductor Current	V _{IN} = 3V, V _{REF} = 0.9V		0.70	1	1.25	A
V _{LOADREG}	Output Voltage Load Regulation			0.7		%	
V _{IN}	Input Voltage Range		● 2.5		5	V	
I _S	Input Current	V _{RUN} = 1.2V, SW = Open		1.5	2.5	mA	
I _S	Shutdown Current	V _{RUN} = 0V, SW = Open		0.1	1	μA	
f _{OSC}	Oscillator Frequency	V _{REF} ≥ 0.25V V _{REF} ≤ 0.1V	● 1.2	1.5	1.8	MHz	
f _{OSC}	Oscillator Frequency	V _{REF} ≥ 0.25V V _{REF} ≤ 0.1V	● 550	700	850	kHz	
V _{REF}	Bypass PFET Turn-Off Threshold	V _{REF} = \bar{V}	1.167	1.2		V	
V _{REF}	Bypass PFET Turn-On Threshold	V _{REF} = \underline{V}		1.21	1.26	V	
R _{PFET}	R _{DS(ON)} of P-Channel FET	I _{SW} = 160mA, Wafer Level I _{SW} = 160mA, DD Package		0.3	0.4	Ω	
R _{PFET}	R _{DS(ON)} of P-Channel FET	I _{SW} = 160mA, Wafer Level I _{SW} = 160mA, DD Package		0.4		Ω	
R _{NFET}	R _{DS(ON)} of N-Channel FET	I _{SW} = -160mA, Wafer Level I _{SW} = -160mA, DD Package		0.3	0.4	Ω	
R _{NFET}	R _{DS(ON)} of N-Channel FET	I _{SW} = -160mA, Wafer Level I _{SW} = -160mA, DD Package		0.4		Ω	
R _{BYPASS}	R _{DS(ON)} of Bypass P-Channel FET	I _{OUT} = 100mA, V _{IN} = 3V, Wafer Level I _{OUT} = 100mA, V _{IN} = 3V, DD Package (Note 4)		0.05	0.08	Ω	
R _{BYPASS}	R _{DS(ON)} of Bypass P-Channel FET	I _{OUT} = 100mA, V _{IN} = 3V, Wafer Level I _{OUT} = 100mA, V _{IN} = 3V, DD Package (Note 4)		0.08		Ω	
I _{LSW}	SW Leakage	V _{RUN} = 0V, V _{SW} = 0V or 5V, V _{IN} = 5V		±0.01	±1	μA	
I _{LBYP}	Bypass PFET Leakage	V _{OUT} = 0V, V _{IN} = 5V, V _{REF} = 0V		±0.01	±1	μA	
V _{RUN}	RUN Threshold		● 0.3	1	1.5	V	
I _{RUN}	RUN Input Current	V _{RUN} = 0V or 2.5V	●	±0.01	±1	μA	
I _{REF}	REF Input Current		●	±0.01	±1	μA	

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3408E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the -40°C to 85°C operating

temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$LTC3408: T_J = T_A + (P_D)(43°C/W)$$

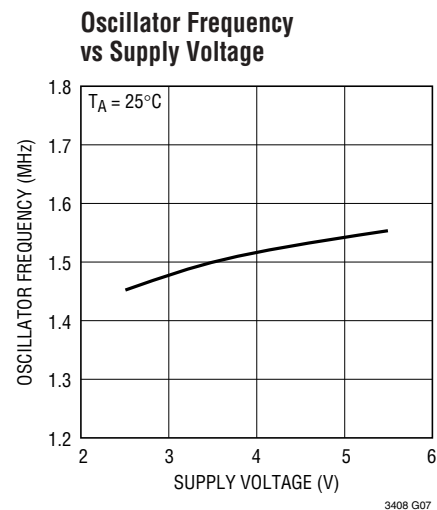
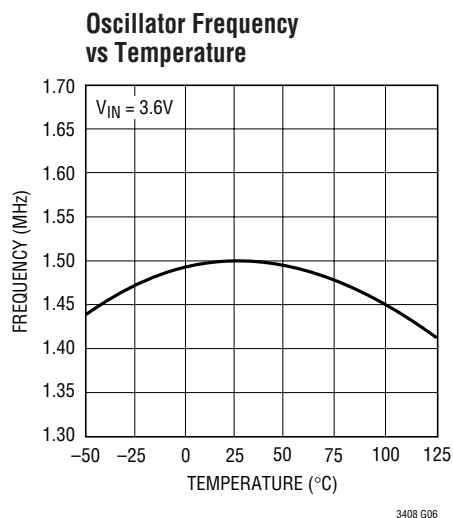
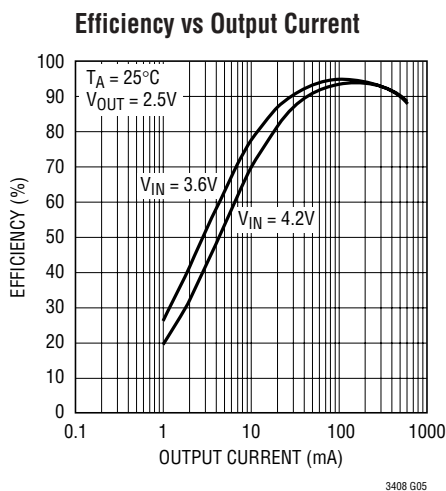
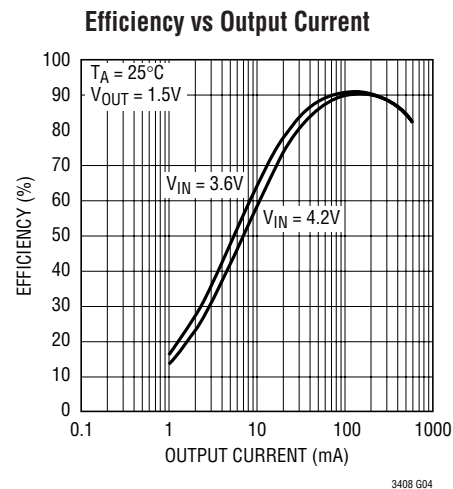
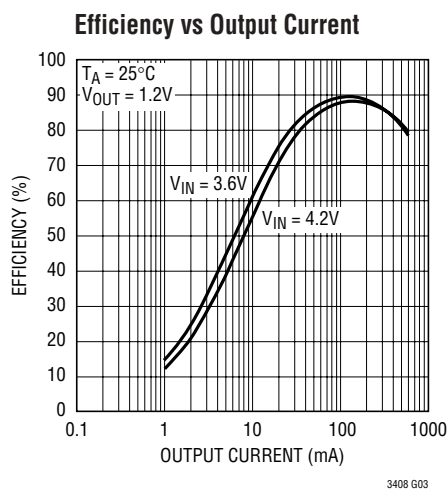
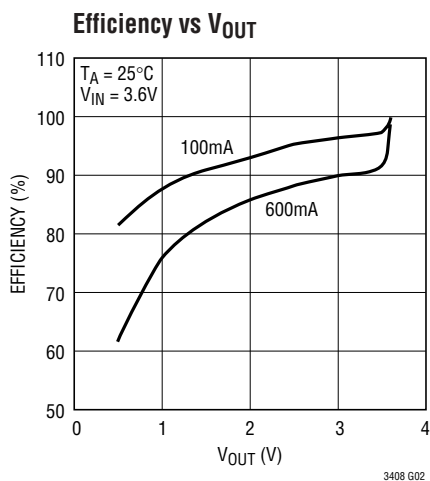
ELECTRICAL CHARACTERISTICS

Note 4: When $V_{REF} > 1.2V$ and $V_{REF} \times 3 > V_{IN}$, the P-channel FET will be on in parallel with the bypass PFET reducing the overall $R_{DS(ON)}$.

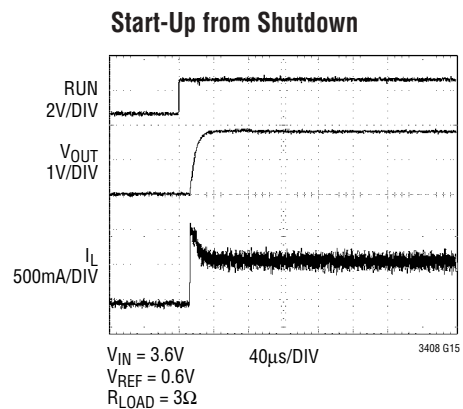
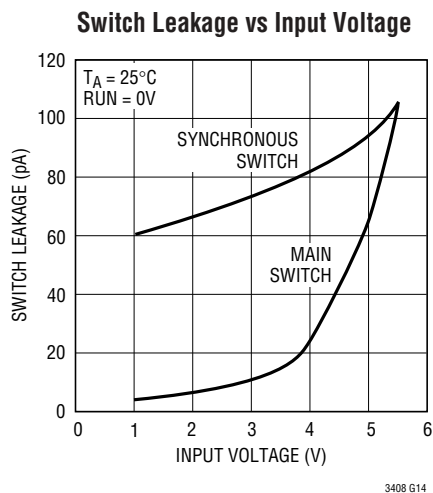
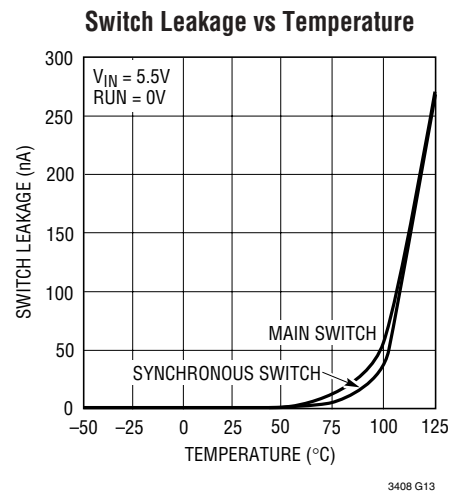
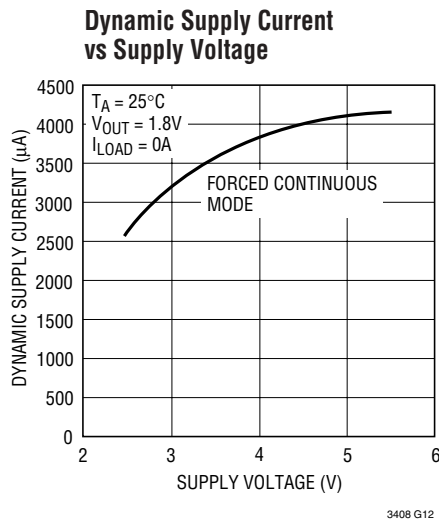
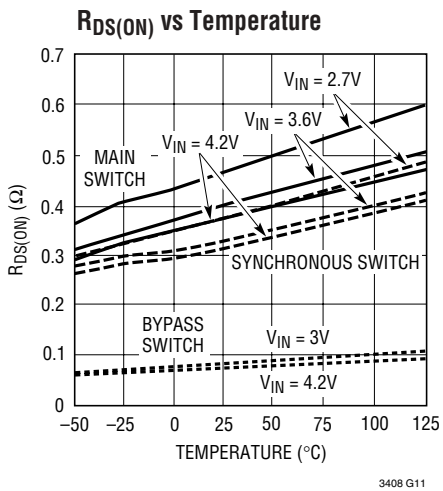
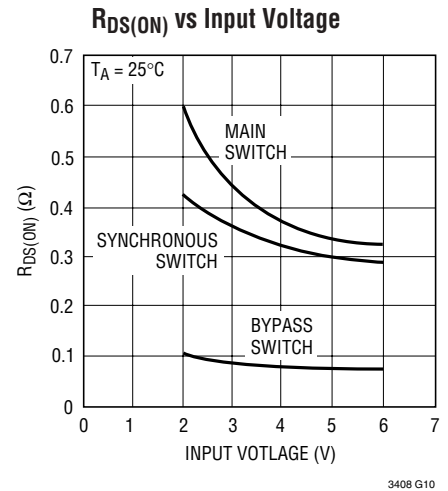
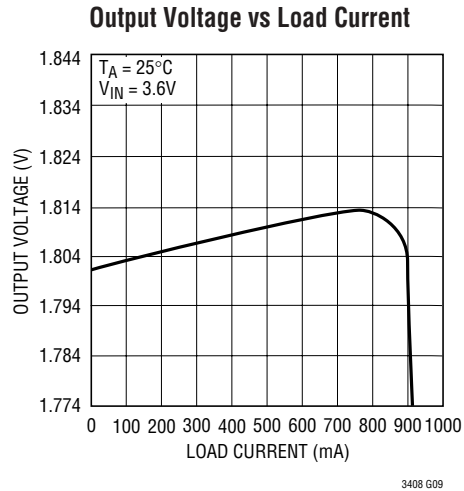
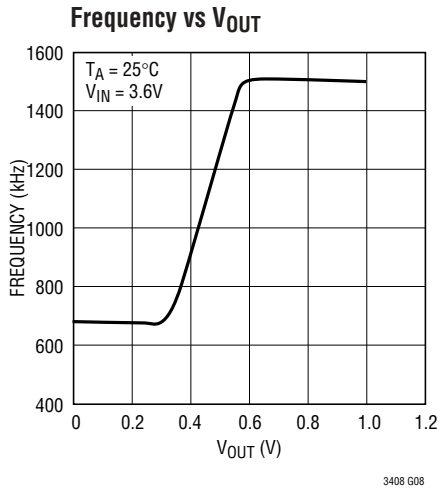
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction

temperature will exceed $125^{\circ}C$ when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

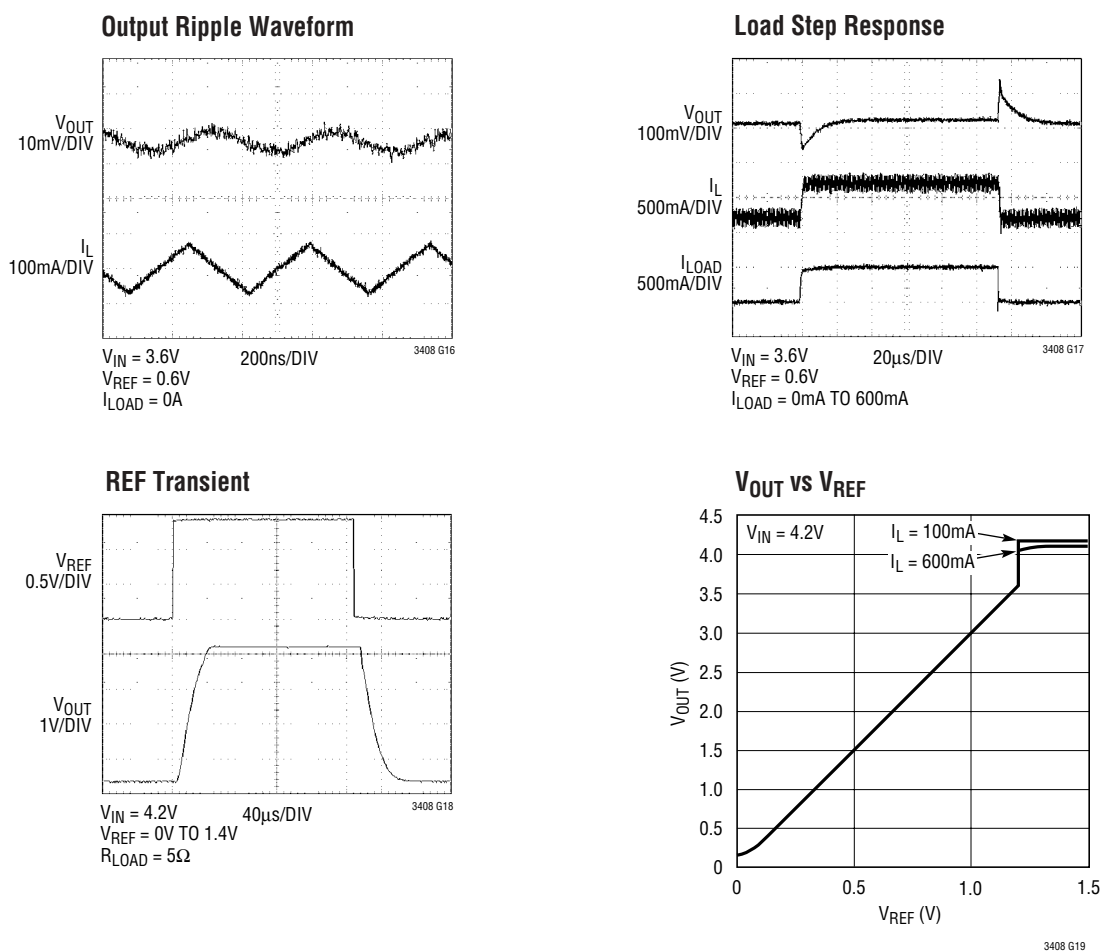
TYPICAL PERFORMANCE CHARACTERISTICS (From Figure 1)



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TYPICAL PERFORMANCE CHARACTERISTICS (From Figure 1)



PIN FUNCTIONS

V_{OUT} (Pins 1, 8): Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down by 3 for comparison to the external reference voltage. The drain of the P-channel bypass MOSFET is connected to this pin.

V_{IN} (Pins 2, 7): Main Supply Pin. Must be closely decoupled to GND, Pin 3, with a 10 μ F or greater ceramic capacitor.

GND (Pin 3): Ground Pin.

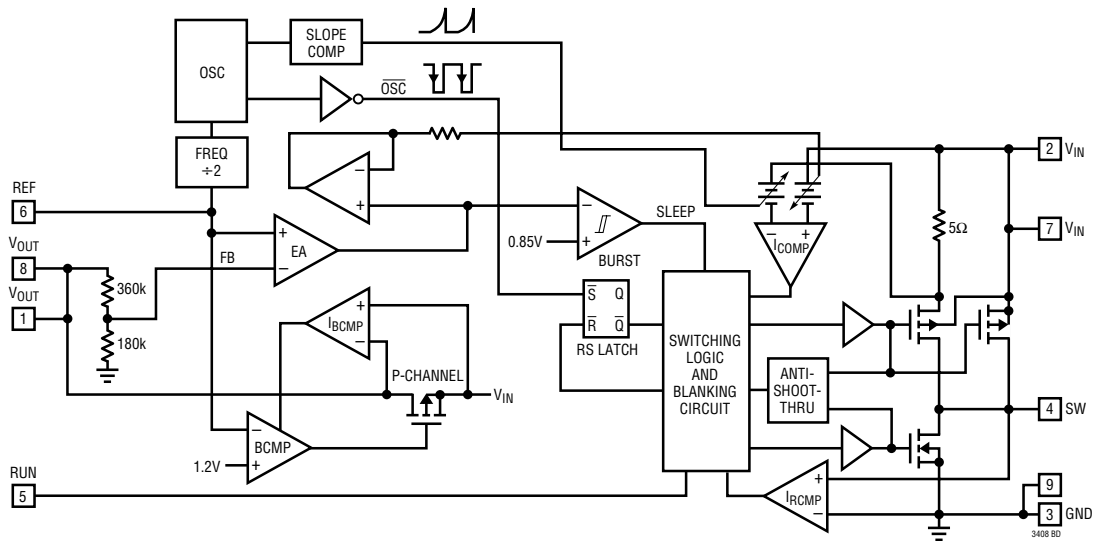
SW (Pin 4): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

RUN (Pin 5): Run Control Input. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. In shutdown, all functions are disabled drawing <1 μ A supply current. Do not leave RUN floating.

REF (Pin 6): External Reference Input. Controls the output voltage to 3 \times the applied voltage at REF. Also turns on the bypass MOSFET when $V_{REF} > 1.2V$.

Exposed Pad (Pin 9): Connect to GND, Pin 3.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

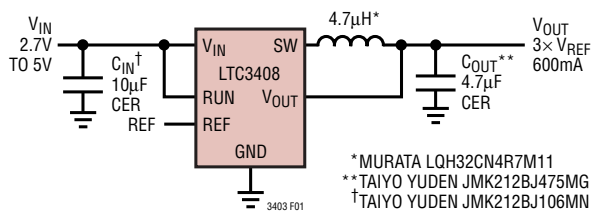


Figure 1. Typical Application

Main Control Loop

The LTC3408 uses a constant frequency, current mode step-down architecture. The main (P-channel MOSFET), synchronous (N-channel MOSFET) and bypass (P-channel MOSFET) switches are internal. During normal operation, the internal main switch is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch, is controlled by the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage, FB, relative to the external reference, which in turn, causes the EA amplifier’s output voltage to increase until the average inductor current matches the new load current. While the main switch is off, the synchronous switch is turned on until the beginning of the next clock cycle.

The LTC3408 operates in forced continuous mode where the inductor current is constantly cycled. In this mode, the

output voltage can respond quickly to the external reference voltage by sourcing or sinking current as needed.

Controlling the Output Voltage

The output voltage can be dynamically programmed from 0.3V to 3.5V using the REF input. Because the gain to V_{OUT} from REF is internally set to 3, the corresponding input range at REF is 0.1V to 1.167V. V_{OUT} can be modulated during operation by driving REF with an external DAC.

When REF exceeds 1.2V, a 0.08Ω internal bypass P-channel MOSFET connects V_{IN} to V_{OUT}, dramatically reducing the drop across the inductor and the main switch.

Short-Circuit Protection

A current sense comparator monitors the current across the bypass P-channel MOSFET with a trip current of about 2.5A. When this current is exceeded during a V_{OUT} short to ground, the bypass P-channel MOSFET is immediately turned off. The propagation delay of the current sensing comparator, I_{BCMP}, detecting an overcurrent condition to turning off the bypass P-channel MOSFET is approximately 100ns. Once the bypass P-channel MOSFET is off for about 10µs to 20µs, it is allowed to turn back on. The initial current limit is then lowered to about 1.6A after the first current limit trip. If the short to ground persists, the current comparator will trip at the lower current limit, turning

OPERATION (Refer to Functional Diagram)

off and on the bypass P-channel MOSFET with a frequency of approximately 50kHz to 100kHz at 1.6A peak current. This will continue until the short is removed. While the bypass P-channel MOSFET is pulsing intermittently, the inherent current limit of the step-down regulator limits its peak current to about 1A.

Dropout Operation

If the reference voltage would cause V_{OUT} to exceed V_{IN} , the LTC3408 enters dropout operation. During dropout, the main switch remains on continuously and operates at 100% duty cycle. If the voltage at REF is less than 1.2V, the bypass P-channel MOSFET will stay off even in dropout operation. The output voltage is then determined by the input voltage minus the voltage drop across the main switch and the inductor. If the voltage at REF is greater than 1.2V,

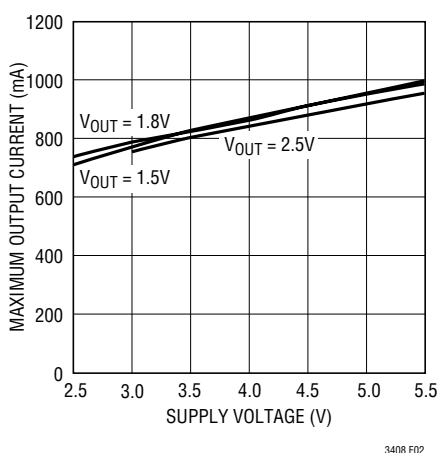


Figure 2. Maximum Output Current vs Input Voltage

but less than $V_{IN}/3$, the bypass P-channel MOSFET will be on, but the main switch will be off. For best performance and lowest voltage drop from V_{IN} to V_{OUT} , always ensure that the REF voltage is greater than both 1.2V and $V_{IN}/3$.

An important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3408 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information section).

Low Supply Operation

The LTC3408 will operate with input supply voltages as low as 2.5V, but the maximum allowable output current is reduced at this low voltage. Figure 2 shows the reduction in the maximum output current as a function of input voltage for various output voltages.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles $>40\%$. However, the LTC3408 uses a patent-pending scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

APPLICATIONS INFORMATION

The basic LTC3408 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT} .

Inductor Selection

For most applications, the value of the inductor will fall in the range of 4 μ H to 6 μ H. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple

currents. As Equation 1 shows, a greater difference between V_{IN} and V_{OUT} produces a larger ripple current. Where these voltages are subject to change, the highest V_{IN} and lowest V_{OUT} will determine the maximum ripple current. A reasonable starting point for setting ripple current is $I_L = 120mA$ (20% of the maximum load, 600mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (1)$$

APPLICATIONS INFORMATION

At output voltages below 0.6V, the switching frequency decreases linearly to a minimum of approximately 700kHz. This places the maximum ripple current (in forced continuous mode) at the highest input voltage and the lowest output voltage. In practice, the resulting output ripple voltage is 10mV to 15mV using the components specified in Figure 1.

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 660mA rated inductor should be enough for most applications (600mA + 60mA). For better efficiency, choose a low DC-resistance inductor.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price versus size requirements and any radiated field/EMI requirements than on what the LTC3408 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3408 applications.

Table 1. Representative Surface Mount Inductors

PART NUMBER	VALUE (μH)	DCR (ΩMAX)	MAX DC CURRENT (A)	SIZE WxLxH (mm ³)
Sumida CDRH2D11	4.7	0.135	0.5	3.2 x 3.2 x 1.2
Sumida CDRH2D18/LD	4.7	0.078	0.63	3.2 x 3.2 x 2.0
Sumida CMD4D06	4.7	0.216	0.75	3.5 x 4.1 x 0.8
Murata LQH32C	4.7	0.150	0.65	2.5 x 3.2 x 2.0
Taiyo Yuden LBLQ2016	4.7	0.250	0.210	1.6 x 2.0 x 1.6
Toko D312C	4.7	0.20	0.79	3.6 x 3.6 x 1.2

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN} . To prevent large voltage transients, a low ESR input capacitor sized for the

maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple V_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8f C_{OUT}} \right)$$

where f = operating frequency, C_{OUT} = output capacitance and I_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since I_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

The bulk capacitance values in Figure 1(a) ($C_{IN} = 10\mu\text{F}$, $C_{OUT} = 4.7\mu\text{F}$) are tailored to mobile phone applications, in which the output voltage is expected to slew quickly according to the needs of the power amplifier. Holding the output capacitor to 4.7μF facilitates rapid charging and discharging. When the output voltage descends quickly in

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forced continuous mode, the LTC3408 will actually pull current from the output until the command from V_{REF} is satisfied. On alternate half cycles, this current actually exits the V_{IN} terminal, potentially causing a rise in V_{IN} and forcing current into the battery. To prevent deterioration of the battery, use sufficient bulk capacitance with low ESR; at least $10\mu\text{F}$ is recommended.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3408's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN} . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size. Ceramic capacitors of Y5V material are not recommended because normal operating voltages cause their bulk capacitance to become much less than the nominal value.

Programming the Output Voltage With a DAC

The output voltage can be dynamically programmed to any voltage from 0.3V to 3.5V with an external DAC driving the REF pin. When the output is commanded low, the output voltage descends quickly in forced continuous mode pulling current from the output and transferring it to the input. If the input is not connected to a low impedance source capable of absorbing the energy, the input voltage could rise above the absolute maximum voltage of the part

and get damaged. The faster V_{OUT} is commanded low, the higher is the voltage spike at the input. For best results, ramp the REF pin from high to low as slow as the application will allow. Avoid abrupt changes in voltage of $>0.2\text{V}/\mu\text{s}$. If ramp control is unavailable, an RC filter with a time constant of $10\mu\text{s}$ can be inserted between the REF pin and the DAC as shown in Figure 3.

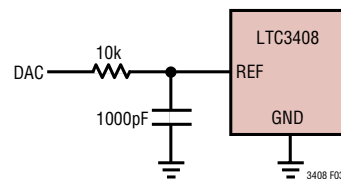


Figure 3. Filtering the REF Pin

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3408 circuits: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at low load currents can be misleading since the actual power lost is of little consequence as illustrated in Figure 4.

1. The V_{IN} quiescent current consists of two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ , moves from V_{IN} to ground. The resulting dQ/dt is typically larger than the DC bias current. In continuous mode,

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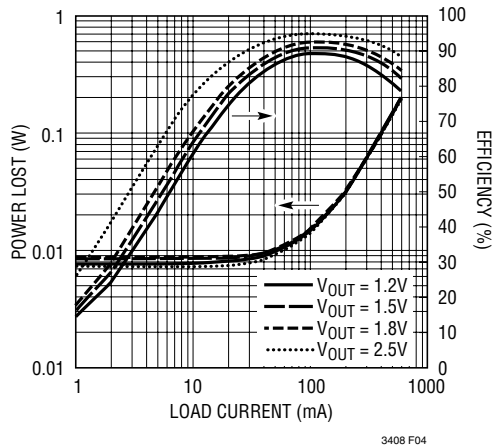


Figure 4. Power Lost vs Load Current

$I_{\text{GATECHG}} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} , thus, their effects will be more pronounced at higher supply voltages. (The gate charge of the bypass FET is, of course, negligible because it is infrequently cycled.)

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} , and external inductor R_L . In continuous mode, the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{\text{DS(ON)}}$ and the duty cycle (DC) as follows:

$$R_{\text{SW}} = (R_{\text{DS(ON)TOP}})(\text{DC}) + (R_{\text{DS(ON)BOT}})(1 - \text{DC})$$

The $R_{\text{DS(ON)}}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Hence, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In most applications the LTC3408 does not dissipate much heat due to its high efficiency. But, in applications where the LTC3408 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum

junction temperature of the part. If the junction temperature reaches approximately 150°C , both power switches will be turned off and the SW node will become high impedance.

To prevent the LTC3408 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = (\text{PD})(\theta_{\text{JA}})$$

where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J , is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3408 in dropout at an input voltage of 2.7V, a load current of 600mA ($0.9\text{V} \leq V_{\text{REF}} < 1.2\text{V}$) and an ambient temperature of 70°C . With $V_{\text{REF}} < 1.2\text{V}$, the entire 600mA flows through the main P-channel FET. From the typical performance graph of switch resistance, the $R_{\text{DS(ON)}}$ of the P-channel switch at 70°C is approximately 0.52Ω . Therefore, power dissipated by the part is:

$$\text{PD} = (I_{\text{LOAD}})^2 \cdot R_{\text{DS(ON)}} = 187.2\text{mW}$$

For the 8L DFN package, the θ_{JA} is $43^\circ\text{C}/\text{W}$. Thus, the junction temperature of the regulator is:

$$T_J = 70^\circ\text{C} + (0.1872)(43) = 78^\circ\text{C}$$

which is below the maximum junction temperature of 125°C .

Modifying this example, suppose that V_{REF} is raised to 1.2V or higher. This turns on the bypass P-channel FET as well as the main P-channel FET. Assume that the inductor's DC resistance is 0.1Ω , the $R_{\text{DS(ON)}}$ of the main P-channel switch is 0.52Ω , and the $R_{\text{DS(ON)}}$ of the bypass P-channel switch is 0.08Ω . The current through the P-channel switch and the inductor will be 69mA, causing power dissipation of $(0.069\text{A})^2 \cdot 0.62\Omega = 2.9\text{mW}$. The bypass FET will

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dissipate $(0.531A)^2 \cdot 0.08\Omega = 22.6mW$. Thus, $T_J = 70^\circ C + (0.0143 + 0.0425)(43) = 71.1^\circ C$.

Reductions in power dissipation occur at higher supply voltages, where the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(I_{LOAD} \cdot ESR)$, where ESR is the effective series resistance of C_{OUT} . I_{LOAD} also begins to charge or discharge C_{OUT} , which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large ($>1\mu F$) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT} , causing a rapid drop in V_{OUT} . No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately $(25 \cdot C_{LOAD})$. Thus, a $10\mu F$ capacitor charging to $3.3V$ would require a $250\mu s$ rise time, limiting the charging current to about $130mA$.

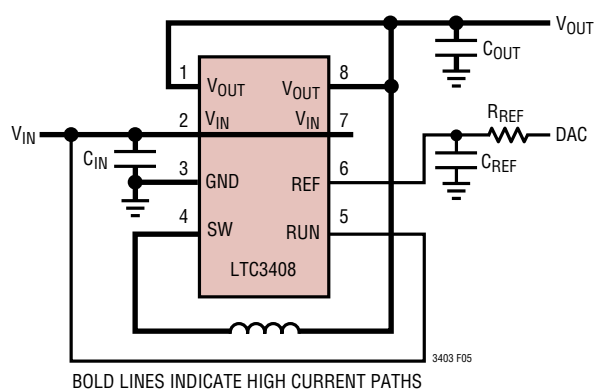


Figure 5. Layout Diagram

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3408. These items are also illustrated graphically in Figures 5 and 6. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC drive to the internal power MOSFETs.
3. Keep the (-) plates of C_{IN} and C_{OUT} as close as possible.

Design Example

As a design example, assume the LTC3408 is used in a single lithium-ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of $4.2V$ down to about $2.7V$. The load current requirement is a maximum of $0.6A$ but most of the time it will be in standby mode, requiring only $2mA$. Efficiency at both low and high load currents is important. Output voltage is $2.5V$. With this information we can calculate L using Equation (1),

$$L = \frac{1}{f(\Delta I_L)} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (2)$$

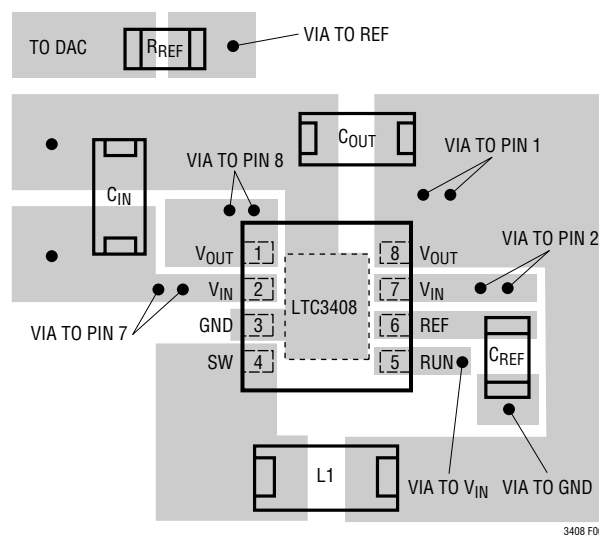


Figure 6. Suggested Layout

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Substituting $V_{OUT} = 2.5V$, $V_{IN} = 4.2V$, $I_L = 120mA$ and $f = 1.5MHz$ in Equation (2) gives:

$$L = \frac{2.5V}{1.5MHz(120mA)} \left(1 - \frac{2.5V}{4.2V}\right) = 5.6\mu H$$

A $4.7\mu H$ inductor works well for this application. For best efficiency choose a $660mA$ or greater inductor with less than 0.2Ω series resistance.

C_{IN} will require an RMS current rating of at least $0.3A \cong LOAD(MAX)/2$ at temperature and C_{OUT} will require an

ESR of less than 0.25Ω . In most cases, a ceramic capacitor will satisfy this requirement.

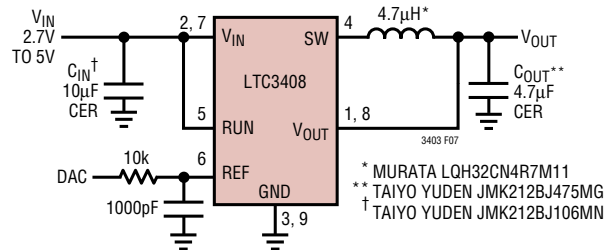
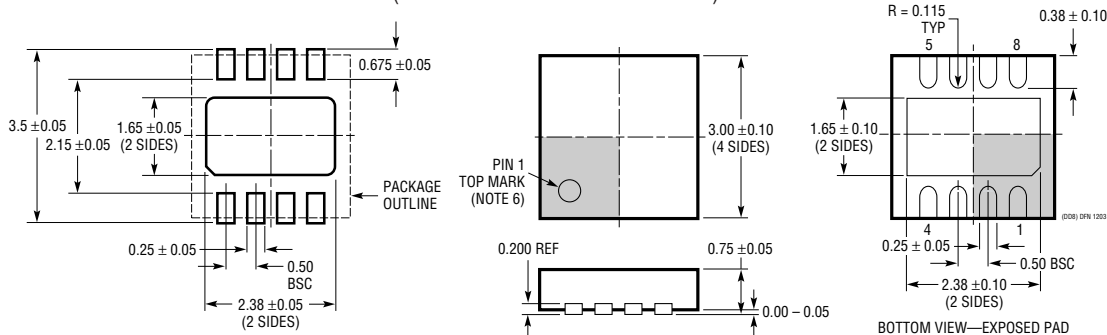


Figure 7

PACKAGE DESCRIPTION

DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:

- DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
- DRAWING NOT TO SCALE
- ALL DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
- EXPOSED PAD SHALL BE SOLDER PLATED
- SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3403	1.5MHz, 600mA Synchronous Step-Down Regulator with Bypass Transistor	Up to 96% Efficiency, V_{IN} : 2.5V to 5V, V_{OUT} : 0.3V to 3.5V, $I_Q = 20\mu A$, $I_{SD} < 1\mu A$, DFN Package
LTC3405/LTC3405A-1.5/ LTC3405A-1.8	1.5MHz, 300mA (I_{OUT}) Synchronous Monolithic Step-Down Regulators	Up to 95% Efficiency, V_{IN} : 2.5V to 5.5V, $I_Q = 20\mu A$, Fixed Output Voltages Available, ThinSOT™ Package
LTC3406B/LTC3406B-1.5/ LTC3406B-1.8	1.5MHz, 600mA, (I_{OUT}) Synchronous Monolithic Step-Down Regulators with Burst Mode Defeat	Up to 95% Efficiency, with Pulse Skipping Mode Enabled, Fixed Output Voltages Available, ThinSOT Package
LTC3407/LTC3407-2	1.5MHz/2.25MHz, 600mA/800mA Dual (I_{OUT}) Synchronous Monolithic Step-Down Regulator	Up to 91% Efficiency, V_{IN} : 2.5V to 5.5V, $I_Q = 4\mu A$, MS10 Package
LTC5505	ThinSOT RF Power Detector with Buffered Output and >40dB Dynamic Range	300MHz to 3GHz, Temperature Compensated, LTC5505-1: -28dBm to 18dBm, LTC5505-2: -32dBm to 12dBm, $V_{CC} = 2.7V$ to 6V

Burst Mode is a registered trademark of Linear Technology Corporation. ThinSOT is a trademark of Linear Technology Corporation.

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