Wide V_{IN}, Multi-Output DC/DC Converter and PowerPath Controller

FEATURES

- **Low Loss PowerPath™ Control: Seamless, Automatic Transition from Battery to USB or Wall Adapter Power**
- **Wide V_{IN} Range: 1.8V to 5.5V**
- **Buck-Boost V_{OUT}: 1.5V to 5.25V**
- **Buck-Boost Generates 3.3V at 300mA for $V_{IN} \geq 1.8V$, 3.3V at 800mA for $V_{IN} \geq 3V$**
- **Dual 350mA Buck Regulators, V_{OUT}: 0.6V to V_{IN}**
- **38µA Quiescent Current in Burst Mode® Operation**
- **1.8V, 50mA Always-On LDO**
- **Protected 100mA Hot Swap™ Output**
- **Pushbutton On/Off Control**
- Current Limited 200mA MAX Output
- Programmable Power-Up Sequencing
- 24-lead 4mm × 4mm × 0.75mm QFN Package

APPLICATIONS

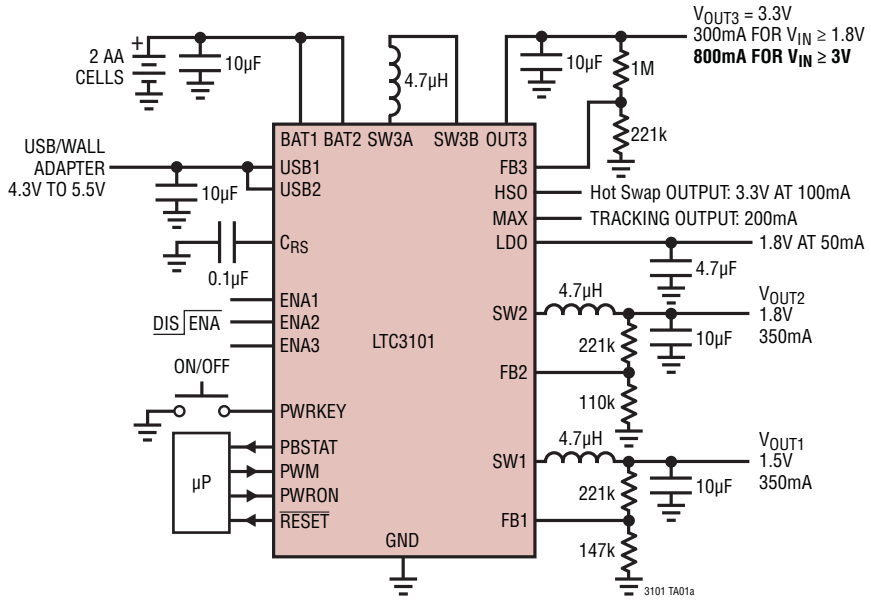
- Ultra-Portable Digital Video Cameras
- Personal Handheld GPS Navigators
- Portable Medical Instruments

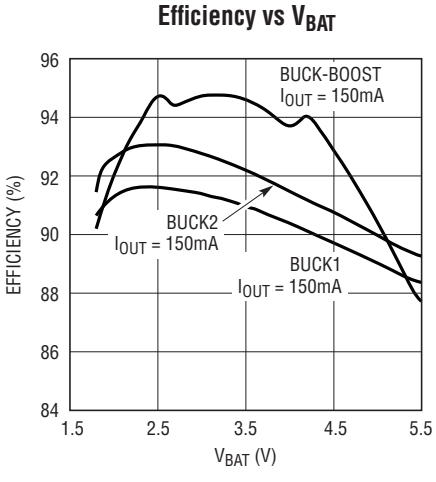
DESCRIPTION

The LTC®3101 is a complete power management solution for low power portable devices. It provides three high efficiency switching DC/DC converters which seamlessly transition from battery to USB/wall adapter power when available. A synchronous buck-boost regulator provides complete flexibility, allowing operation from a single Li-Ion/Polymer battery, 2 to 3 AA cells, a USB port or any other power source operating from 1.8V to 5.5V.

Two always-alive outputs, a 50mA LDO and a 200mA MAX output that tracks the higher voltage input supply, provide power for critical functions or additional external regulators. Flash memory cards can be directly powered from the protected 100mA Hot Swap output. Pushbutton control logic and a programmable-duration microprocessor reset generator simplify interfacing to a microprocessor while internal sequencing and independent enable pins provide flexible power-up options. The LTC3101 is available in a low profile (0.75mm) 24-lead 4mm × 4mm QFN package.

TYPICAL APPLICATION



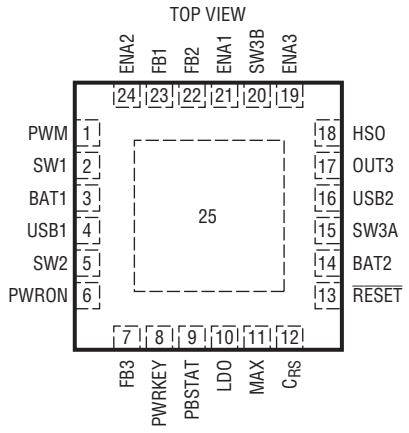


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{BAT1}, V_{BAT2}, V_{USB1}, V_{USB2} ..... –0.3V to 6V
V_{SW1}, V_{SW2}, V_{SW3A}, V_{SW3B}
DC..... –0.3V to 6V
Pulsed (<100ns) ..... –1.0V to 7V
Voltage (All Other Pins)..... –0.3V to 6V
Operating Temperature Range (Note 2).... –40°C to 85°C
Maximum Junction Temperature (Note 5)..... 125°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3101EUF#PBF	LTC3101EUF#TRPBF	3101	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{USB1} = V_{USB2} = V_{BAT1} = V_{BAT2} = 3V and V_{OUT3} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Voltage	Battery Powered USB Powered	● ●	1.8 1.8		5.5 5.5	V V
Undervoltage Lockout Threshold	Battery Powered, V_{BAT} Rising USB Powered, V_{USB} Rising	● ●		1.7 1.7	1.8 1.8	V V
Input Quiescent Current in Standby	V_{PWRON} = 0V, V_{PWRKEY} = 3V			15		µA
Input Quiescent Current in Burst Mode Operation	All Converters Enabled, V_{FB1} = V_{FB2} = V_{FB3} = 0.66V			38		µA
Oscillator Frequency		●	1.02	1.27	1.52	MHz
Buck Converter 1						
Feedback Voltage (FB1 Pin)		●	583	596	609	mV
Feedback Pin Input Current (FB1 Pin)				1	50	nA
P-Channel Current Limit	Battery Powered (Note 3) USB Powered (Note 3)		440 440	540 540		mA mA
Maximum Duty Cycle		●	100			%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{USB1} = V_{USB2} = V_{BAT1} = V_{BAT2} = 3V and V_{OUT3} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Duty Cycle		●			0	%
ENA1 Input Logic Threshold		●	0.3	0.7	1.0	V
ENA1 Pull-Down Resistance	V_{PWRON} = 3V or V_{PWRKEY} = 0V			4.0		MΩ
N-Channel Switch Resistance				0.34		Ω
P-Channel Switch Resistance	Battery Powered USB Powered			0.55 0.58		Ω Ω
N-Channel Switch Leakage	V_{SW1} = $V_{USB1,2}$ = $V_{BAT1,2}$ = 5.5V			0.1	5	µA
P-Channel Switch Leakage	V_{SW1} = 0V, $V_{USB1,2}$ = $V_{BAT1,2}$ = 5.5V			0.1	10	µA
Power Good Threshold	V_{FB1} Falling	●	–11	–8	–5	%
Power Good Hysteresis				2.5		%
Buck Converter 2						
Feedback Voltage (FB2 Pin)		●	583	596	609	mV
Feedback Pin Input Current (FB2 Pin)				1	50	nA
P-Channel Current Limit	Battery Powered (Note 3) USB Powered (Note 3)		440 440	540 540		mA mA
Maximum Duty Cycle		●	100			%
Minimum Duty Cycle		●			0	%
ENA2 Input Logic Threshold		●	0.3	0.7	1.0	V
ENA2 Pull-Down Resistance	V_{PWRON} = 3V or V_{PWRKEY} = 0V			4.0		MΩ
N-Channel Switch Resistance				0.34		Ω
P-Channel Switch Resistance	Battery Powered USB Powered			0.55 0.58		Ω Ω
N-Channel Switch Leakage	V_{SW2} = $V_{USB1,2}$ = $V_{BAT1,2}$ = 5.5V			0.1	5	µA
P-Channel Switch Leakage	V_{SW2} = 0V, $V_{USB1,2}$ = $V_{BAT1,2}$ = 5.5V			0.1	10	µA
Power Good Threshold	V_{FB2} Falling	●	–11	–8	–5	%
Power Good Hysteresis				2.5		%
Buck-Boost Converter						
Operating Output Voltage		●	1.5		5.25	V
Feedback Voltage (FB3 Pin)		●	584	599	614	mV
Feedback Pin Input Current (FB3 Pin)				1	50	nA
Inductor Current Limit	BAT or USB Powered (Note 3)		1.2	1.5		A
Reverse Inductor Current Limit	(Note 3)			400		mA
Burst Mode Inductor Current Limit	(Note 3)			450		mA
Maximum Duty Cycle	Percentage of Period SW3B is Low in Boost Mode	●	82	87		%
Minimum Duty Cycle	Percentage of Period SW3A is High in Buck Mode	●			0	%
ENA3 Input Logic Threshold		●	0.3	0.7	1.0	V
ENA3 Pull-Down Resistance	V_{PWRON} = 3V or V_{PWRKEY} = 0V			4.0		MΩ
N-Channel Switch Resistance	Switch B (From SW3A to GND) Switch C (From SW3B to GND)			0.150 0.140		Ω Ω
P-Channel Switch Resistance	Switch A´ (From BAT2 to SW3A) Switch A (From USB2 to SW3A) Switch D (From OUT3 to SW3B)			0.150 0.180 0.195		Ω Ω Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{USB1} = V_{USB2} = V_{BAT1} = V_{BAT2} = 3V and V_{OUT3} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
N-Channel Switch Leakage	$V_{SW3A,B}$ = $V_{USB1,2}$ = $V_{BAT1,2}$ = V_{OUT3} = 5.5V			0.1	5	µA
P-Channel Switch Leakage	$V_{SW3A,B}$ = 0V, $V_{USB1,2}$ = $V_{BAT1,2}$ = V_{OUT3} = 5.5V			0.1	10	µA
Power Good Threshold	V_{FB3} Falling	●	–11.5	–8.5	–5.5	%
Power Good Hysteresis				2.5		%
MAX Output						
Current Limit	V_{MAX} = 2.0V	●	200	300		mA
Switch Resistance	From BAT2 to MAX From USB2 to MAX			0.890 0.930		Ω Ω
Load Dependent Supply Current				1.0		µA/mA
LDO Output						
Output Voltage	I_{LDO} = 1mA	●	1.755	1.800	1.845	V
Current Limit	V_{LDO} = 1.0V	●	50	110		mA
Line Regulation	Input Voltage (V_{MAX}) = 1.8V to 5.5V, I_{LDO} = 1mA			0.1		%
Load Regulation	I_{LDO} = 1mA to 50mA			0.9		%
Reverse Current in Shutdown	$V_{BAT1,2}$ = $V_{USB1,2}$ = 0V, V_{LDO} = 1.8V			0.1	1	µA
Load Dependent Supply Current				12		µA/mA
Dropout Voltage	V_{MAX} = 1.75V, I_{LDO} = 10mA			25		mV
Hot Swap Output						
Switch Resistance				0.730		Ω
Switch Current Limit	V_{HSO} = 2.0V	●	100	150		mA
Pushbutton Logic and µP Reset Generator						
PBSTAT Deglitching Duration			15	24		ms
PBSTAT Low Voltage	I_{PBSTAT} = 1mA			20	50	mV
$\overline{RESET}$ Low Voltage	$I_{\overline{RESET}}$ = 1mA			20	50	mV
C_{RS} Pin Charging Current			0.9	1.0	1.1	µA
C_{RS} Pin Threshold Voltage	V_{CRS} Rising		1.176	1.200	1.224	V
Logic Inputs						
PWRKEY, PWRON, PWM Input Logic Threshold		●	0.3	0.7	1.0	V
PWRKEY Pull-Up Resistance				400		kΩ
PWRON Pull-Down Resistance				4.0		MΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3101 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are ensured by design, characterization and correlation with statistical process controls.

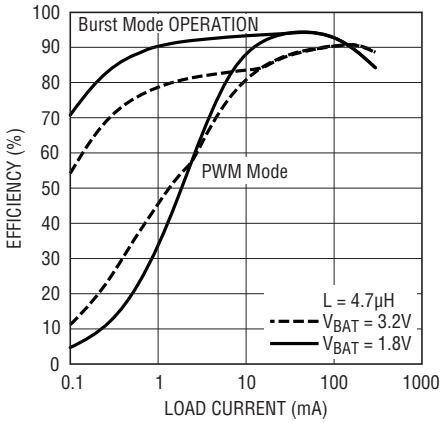
Note 3: Current measurements are performed when the LTC3101 is not switching. The current limit values measured in operation will be somewhat higher due to the propagation delay of the comparators.

Note 4: The LTC3101 is tested in a proprietary non-switching test mode that internally connects the error amplifiers in a closed-loop configuration.

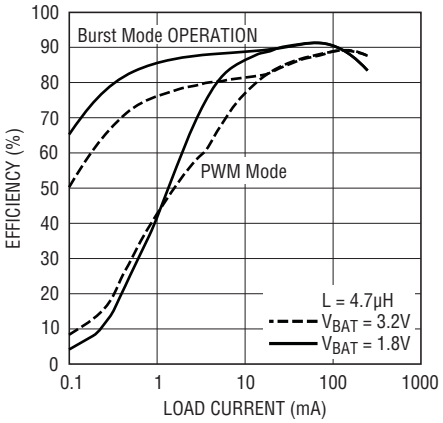
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

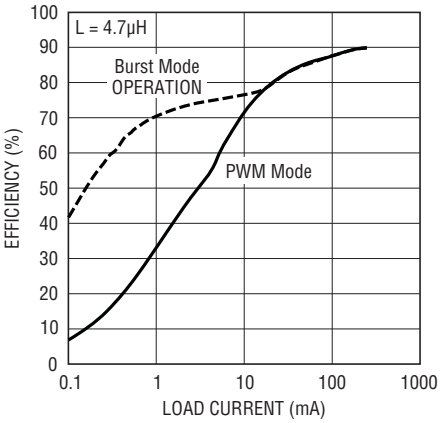
Buck Efficiency 2 AA Cells to 1.5V



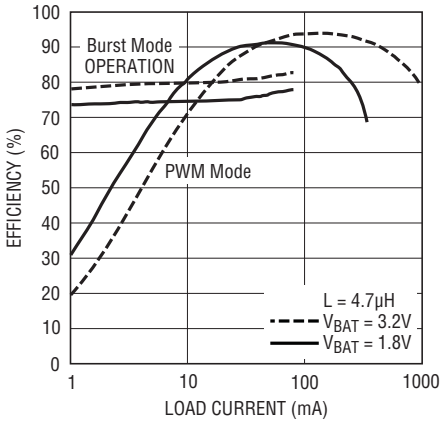
Buck Efficiency 2 AA Cells to 1.2V



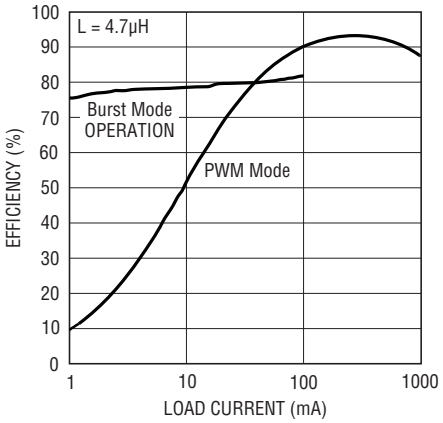
Buck Efficiency USB (5V) to 1.8V



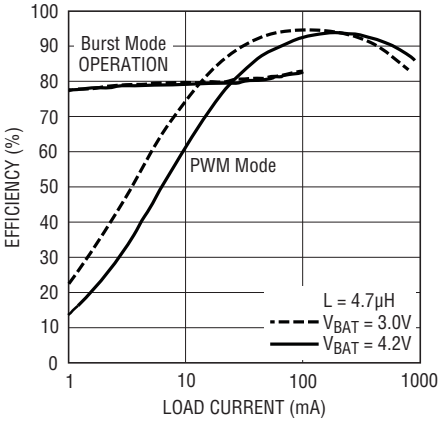
Buck-Boost Efficiency 2 AA Cells to 3.3V



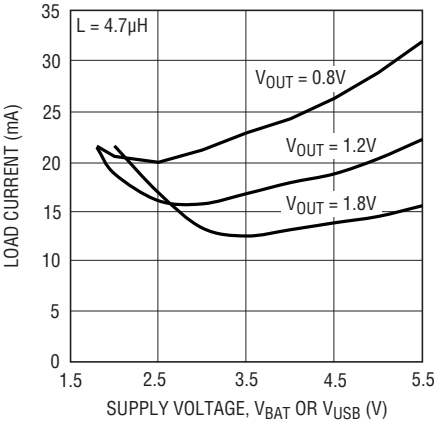
Buck-Boost Efficiency USB (5V) to 3.3V



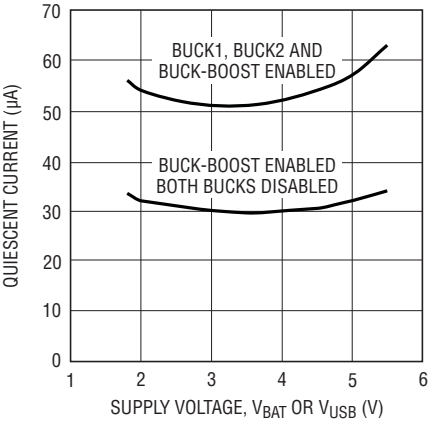
Buck-Boost Efficiency Li-Ion to 3.3V



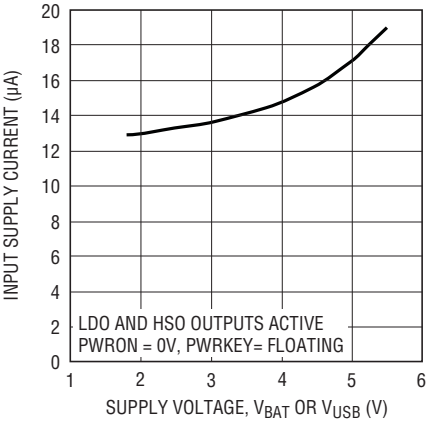
Buck Burst Mode Threshold



No-Load Quiescent Current in Burst Mode Operation

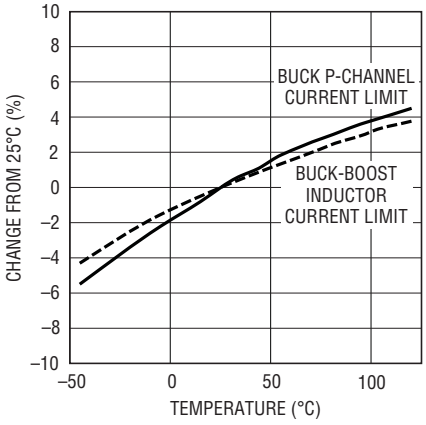


Standby Quiescent Current



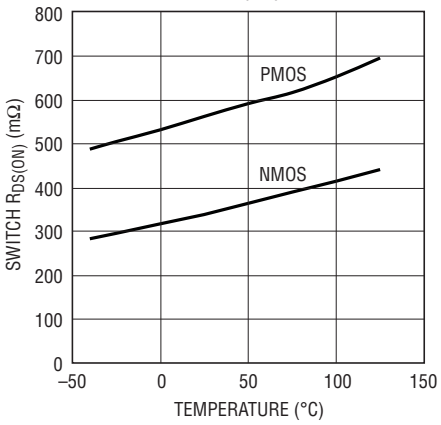
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Current Limit Thresholds vs Temperature



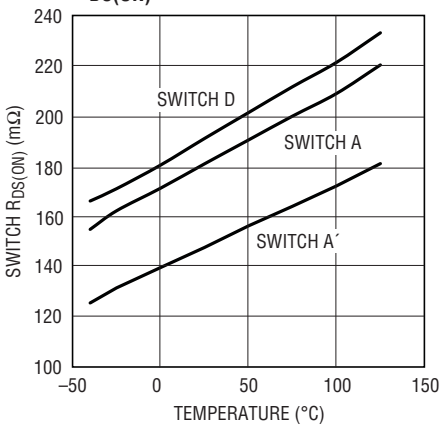
3101 G10

Buck Switch $R_{DS(ON)}$



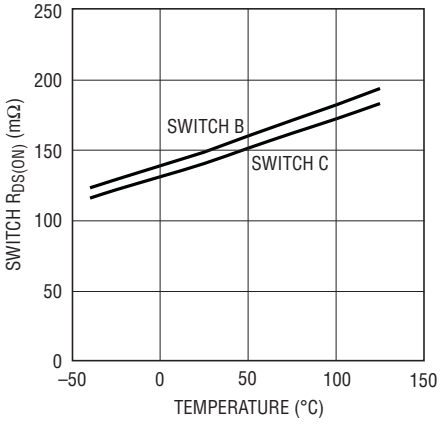
3101 G11

Buck-Boost P-Channel Switch $R_{DS(ON)}$



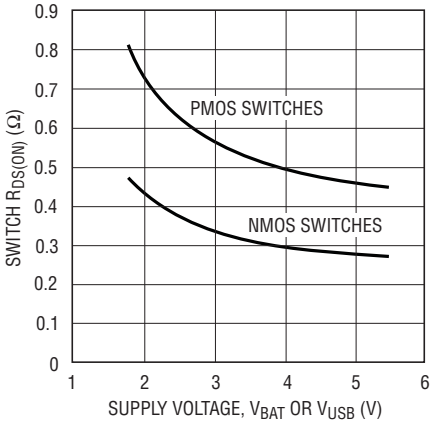
3101 G12

Buck-Boost N-Channel Switch $R_{DS(ON)}$



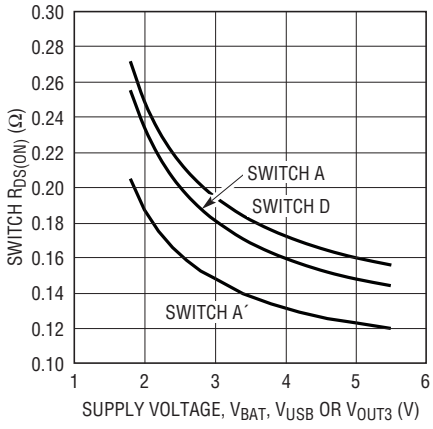
3101 G13

Buck Switch $R_{DS(ON)}$



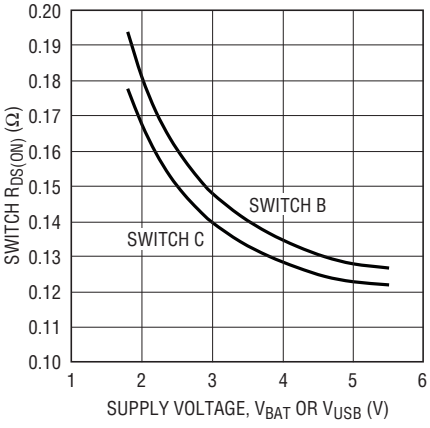
3101 G14

Buck-Boost P-Channel Switch $R_{DS(ON)}$



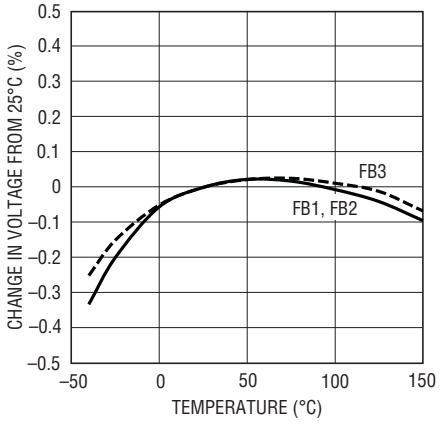
3101 G15

Buck-Boost N-Channel Switch $R_{DS(ON)}$



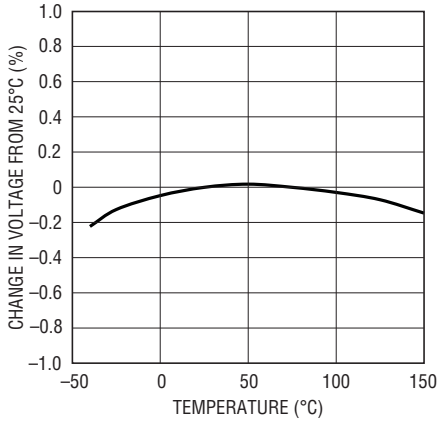
3101 G16

Feedback Voltages



3101 G17

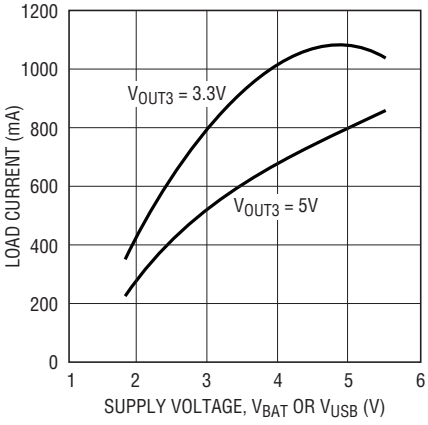
LDO Output Voltage



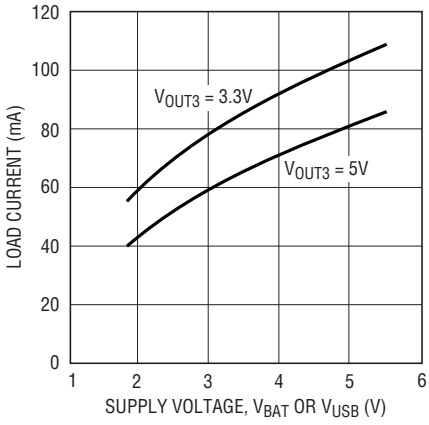
3101 G18

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

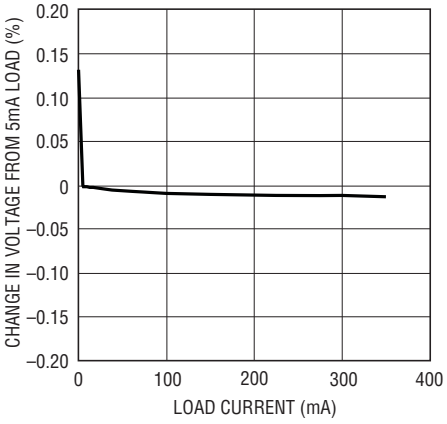
Buck-Boost Maximum Load Current, PWM Mode



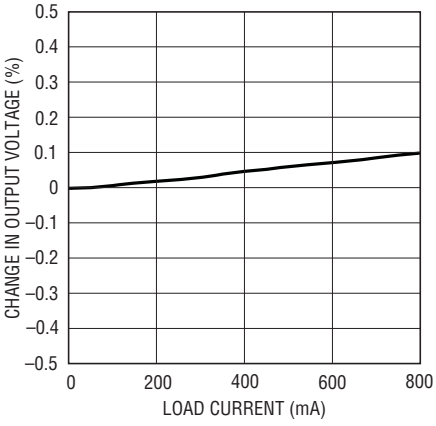
Buck-Boost Maximum Load Current, Burst Mode Operation



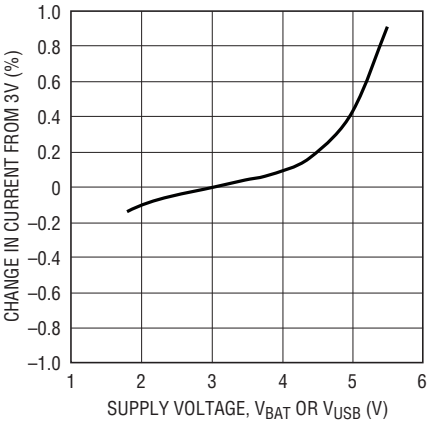
Buck Output Voltage vs Load Current



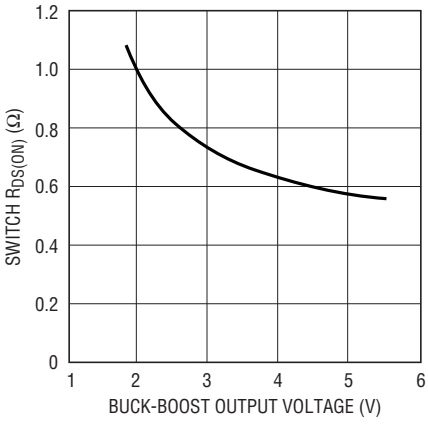
Buck-Boost Output Voltage vs Load Current



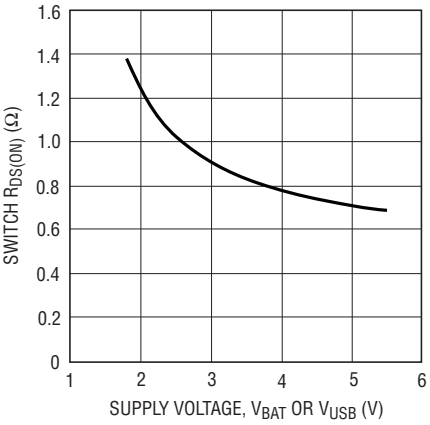
C_{RS} Pin Current



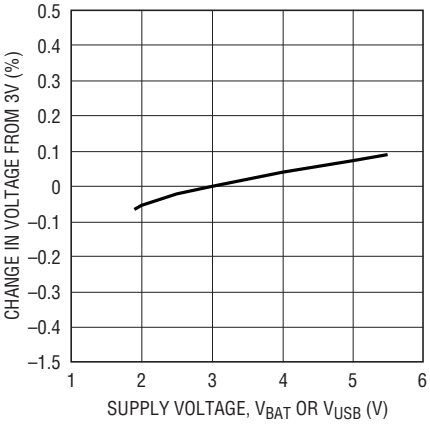
Hot Swap Switch $R_{DS(ON)}$



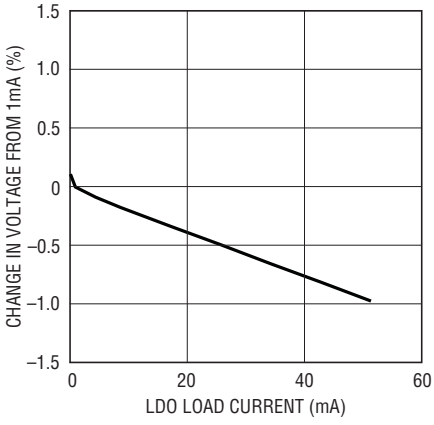
MAX Output Switch $R_{DS(ON)}$



LDO Output Voltage vs Supply Voltage

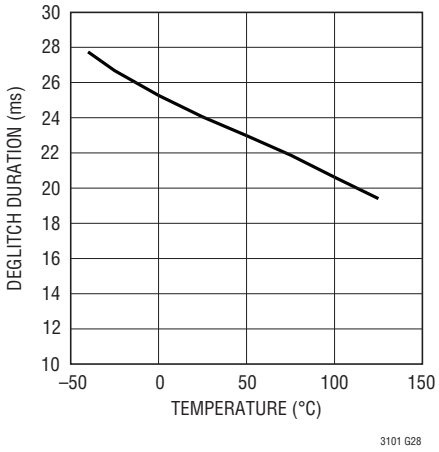


LDO Output Voltage vs Load Current

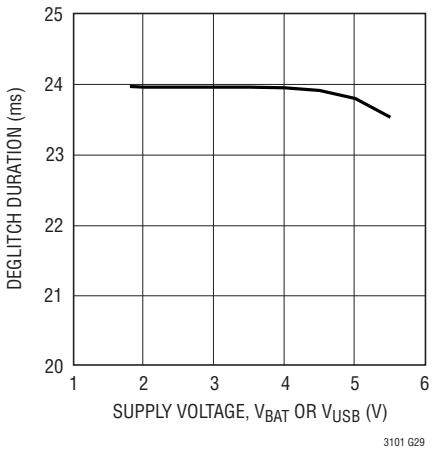


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

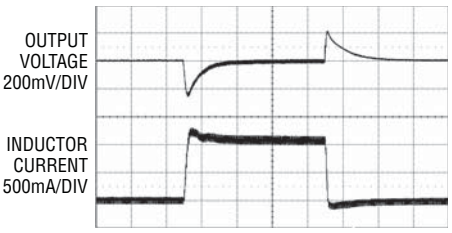
PBSTAT Deglitch Duration



PBSTAT Deglitch Duration

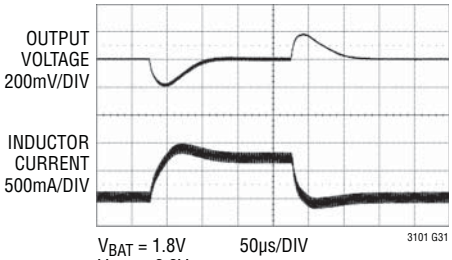


Buck-Boost Load Step, 0mA to 800mA



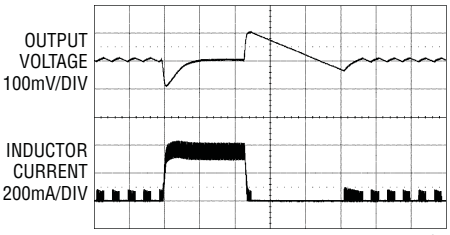
V_{BAT} = 3V 50µs/DIV
V_{OUT} = 3.3V
L = 4.7µH
C_{OUT} = 10µF

Buck-Boost Load Step, 0mA to 300mA



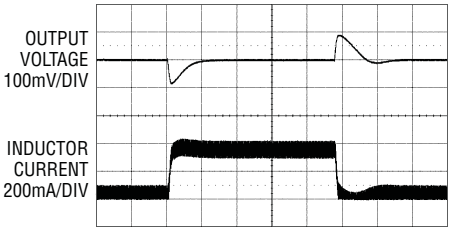
V_{BAT} = 1.8V 50µs/DIV
V_{OUT} = 3.3V
L = 4.7µH
C_{OUT} = 10µF

Buck Load Step, Burst Mode Operation, 10mA to 350mA



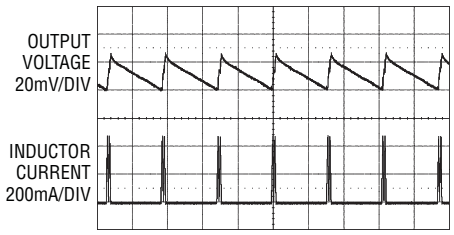
V_{BAT} = 3V 50µs/DIV
V_{OUT} = 1.2V
L = 4.7µH
C_{OUT} = 10µF
C_{FF} = 18pF

Buck Load Step, PWM Mode, 35mA to 350mA



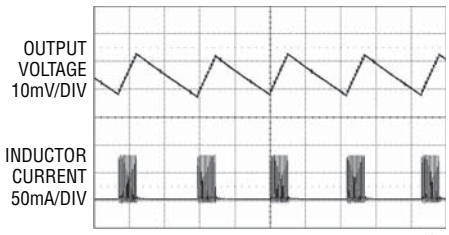
V_{BAT} = 3V 50µs/DIV
V_{OUT} = 1.2V
L = 4.7µH
C_{OUT} = 10µF
C_{FF} = 18pF

Buck-Boost Burst Mode Ripple



V_{BAT} = 3V 20µs/DIV
V_{OUT} = 3.3V
L = 4.7µH
C_{OUT} = 10µF
I_{LOAD} = 10mA

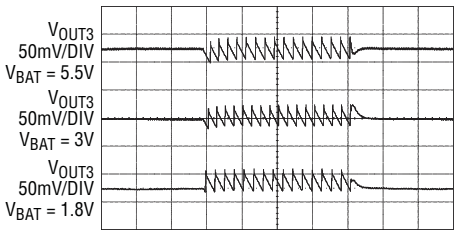
Buck Burst Mode Ripple



V_{BAT} = 3V 20µs/DIV
V_{OUT} = 1.2V
L = 4.7µH
C_{OUT} = 10µF
C_{FF} = 18pF
I_{LOAD} = 5mA

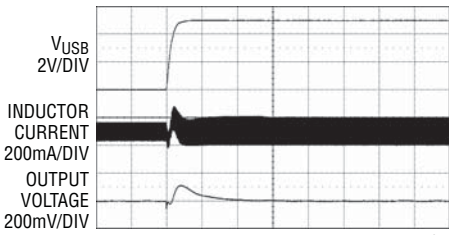
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Buck-Boost Burst to PWM Mode Transient



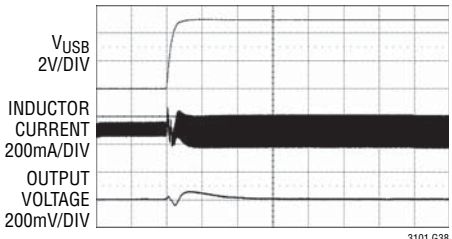
V_{OUT3} = 3.3V 200µs/DIV
L = 4.7µH
C_{OUT} = 10µF
I_{LOAD} = 5mA

Buck Output Voltage Transient on USB Hot Plug



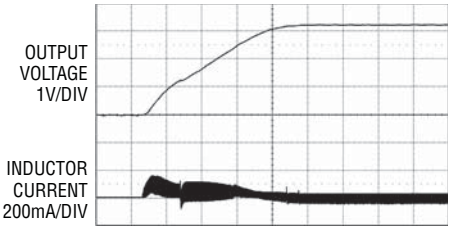
V_{BAT} = 3V 100µs/DIV
V_{OUT} = 1.8V
I_{LOAD} = 100mA

Buck-Boost Output Voltage Transient on USB Hot Plug



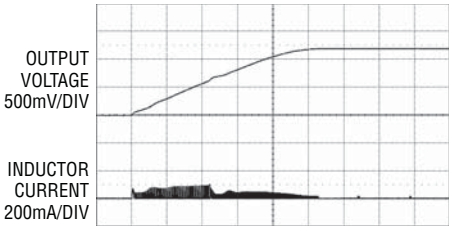
V_{BAT} = 3V 100µs/DIV
V_{OUT} = 3.3V
I_{LOAD} = 100mA

Buck-Boost Soft-Start, PWM Mode



V_{BAT} = 3V 200µs/DIV
V_{OUT} = 3.3V
L = 4.7µH
C_{OUT} = 10µF

Buck Soft-Start, PWM Mode



V_{BAT} = 3V 200µs/DIV
V_{OUT} = 1.2V
L = 4.7µH
C_{OUT} = 10µF

PIN FUNCTIONS

PWM (Pin 1): Pulse Width Modulation/Burst Mode Selection Input. Forcing this pin high causes all switching converters to operate in low noise fixed frequency PWM mode. Forcing this pin low enables Burst Mode operation for all converters. With PWM held low, the buck-boost converter will operate solely in Burst Mode operation and can only support a minimal load current (typically 50mA). With PWM low, the buck converters will automatically transition from Burst Mode operation at light load currents to PWM mode at heavy load currents.

SW1 (Pin 2): Buck Converter 1 Switch Pin. This pin should be connected to one side of the buck inductor.

BAT1 (Pin 3): Battery Power Input for Both Buck Converters. A 4.7µF or larger bypass capacitor should be connected between this pin and ground. The bypass capacitor should be located as close to the IC as possible and should via directly down to the ground plane. **Pins BAT1 and BAT2 must be connected together in the application.**

USB1 (Pin 4): USB or Wall Adapter Power Input for Both Buck Converters. A 4.7µF or larger bypass capacitor should be connected from this pin to ground. The bypass capacitor should be located as close to the IC as possible and should via directly down to the ground plane. **Pins USB1 and USB2 must be connected together in the application.**

SW2 (Pin 5): Buck Converter 2 Switch Pin. This pin should be connected to one side of the buck inductor.

PWRON (Pin 6): Power-On Input. Forcing this input high enables the IC. Typically, the PWRKEY input is used to initially enable the LTC3101 while the microprocessor is powering up. Once the microprocessor is initialized, it forces PWRON high to keep the LTC3101 enabled when the momentary pushbutton connected to PWRKEY is released. In applications that do not require pushbutton control, the IC can be enabled directly by forcing PWRON high.

FB3 (Pin 7): Feedback Voltage Input for the Buck-Boost Converter. The resistor divider connected to this pin sets the output voltage for buck-boost converter.

PWRKEY (Pin 8): Pushbutton Power $\overline{ON}$/OFF Key. Forcing this pin to ground will turn on the LTC3101 DC/DC converters in the internally controlled sequence and initiate a microprocessor reset. This pin is usually connected to an external momentary switch that is used to turn on the IC. This pin has an internal pull-up resistor that is automatically connected to the higher of the two input supplies, battery or USB.

PBSTAT (Pin 9): Power $\overline{ON}$/OFF Key Status Pin. This is a debounced, open-drain output that indicates the state of the PWRKEY pin to the microprocessor. In the typical application, the microprocessor monitors this pin to detect a second pushbutton activation indicating a power-down request.

LDO (Pin 10): Always-Alive LDO Output. This output is internally regulated to 1.8V (typical) and is guaranteed to supply an external load of up to 50mA. The LDO output is always active whenever either supply, battery or USB power, is present (independent of the states of all enables and the pushbutton interface). This output can be utilized to power an external real time clock or charge a supercapacitor for temporary memory backup when both power sources are removed.

MAX (Pin 11): Power Output That Tracks the Higher Voltage Input Supply. This output is driven to the higher of the two power inputs, USB2 or BAT2. This output can support a load current of up to 200mA and is short-circuit protected. The MAX output can be used to power an LCD display or external LDOs. The MAX output is operational whenever either supply, BAT2 or USB2, is present, independent of the state of all enables and the pushbutton interface.

C_{RS} (Pin 12): Power-on Reset Duration Programming Capacitor. An external capacitor is connected from C_{RS} to ground to set the duration of the microprocessor power-on reset signal.

PIN FUNCTIONS

$\overline{\text{RESET}}$ (Pin 13): Active-Low µP Reset and Fault Signal. This pin provides an active-low microprocessor reset signal. During the power-up sequence, the µP reset signal is held low until all converters are in regulation for a duration programmed by the C_{RS} capacitor. In addition, this pin is held low during a fault condition and when the IC is disabled in order to prevent spurious turn-on of the microprocessor.

BAT2 (Pin 14): Battery Power Input for the Buck-Boost Converter. A 10µF or larger bypass capacitor should be connected between this pin and ground. The bypass capacitor should be located as close to the IC as possible and should via directly down to the ground plane. **Pins BAT1 and BAT2 must be connected together in the application.**

SW3A (Pin 15): Buck-Boost Switch Pin. This pin should be connected to one side of the buck-boost inductor.

USB2 (Pin 16): USB or Wall Adapter Power Input for the Buck-Boost Converter. A 10µF or larger bypass capacitor should be connected from this pin to ground. The bypass capacitor should be located as close to the IC as possible and should via directly down to the ground plane. **Pins USB1 and USB2 must be connected together in the application.**

OUT3 (Pin 17): Buck-Boost Output Voltage. This pin is the power output for the buck-boost regulator. It should be connected to a low ESR capacitor with a value of at least 10µF. For higher output current applications (>400mA), it is recommended that a 22µF or larger output capacitor be used. The capacitor should be placed as close to the IC as possible and should have a short return path to ground.

HSO (Pin 18): Hot Swap Output. An internal current-limited switch connects the HSO output to the buck-boost output voltage after the buck-boost output reaches regulation. With the buck-boost operating in PWM mode, this output is guaranteed to support a 100mA load and is short-circuit protected.

ENA3 (Pin 19): Enable Pin for Buck-Boost Converter. Forcing this pin above 1V will turn on the buck-boost converter when the IC is enabled (via the pushbutton interface). Forcing this pin below 0.3V will disable the buck-boost converter.

SW3B (Pin 20): Buck-Boost Switch Pin. This pin should be connected to one side of the buck-boost inductor.

ENA1 (Pin 21): Enable Pin for Buck Converter 1. Forcing this pin above 1V will turn on the buck converter when the IC is enabled (via the pushbutton interface). Forcing this pin below 0.3V will disable buck converter 1.

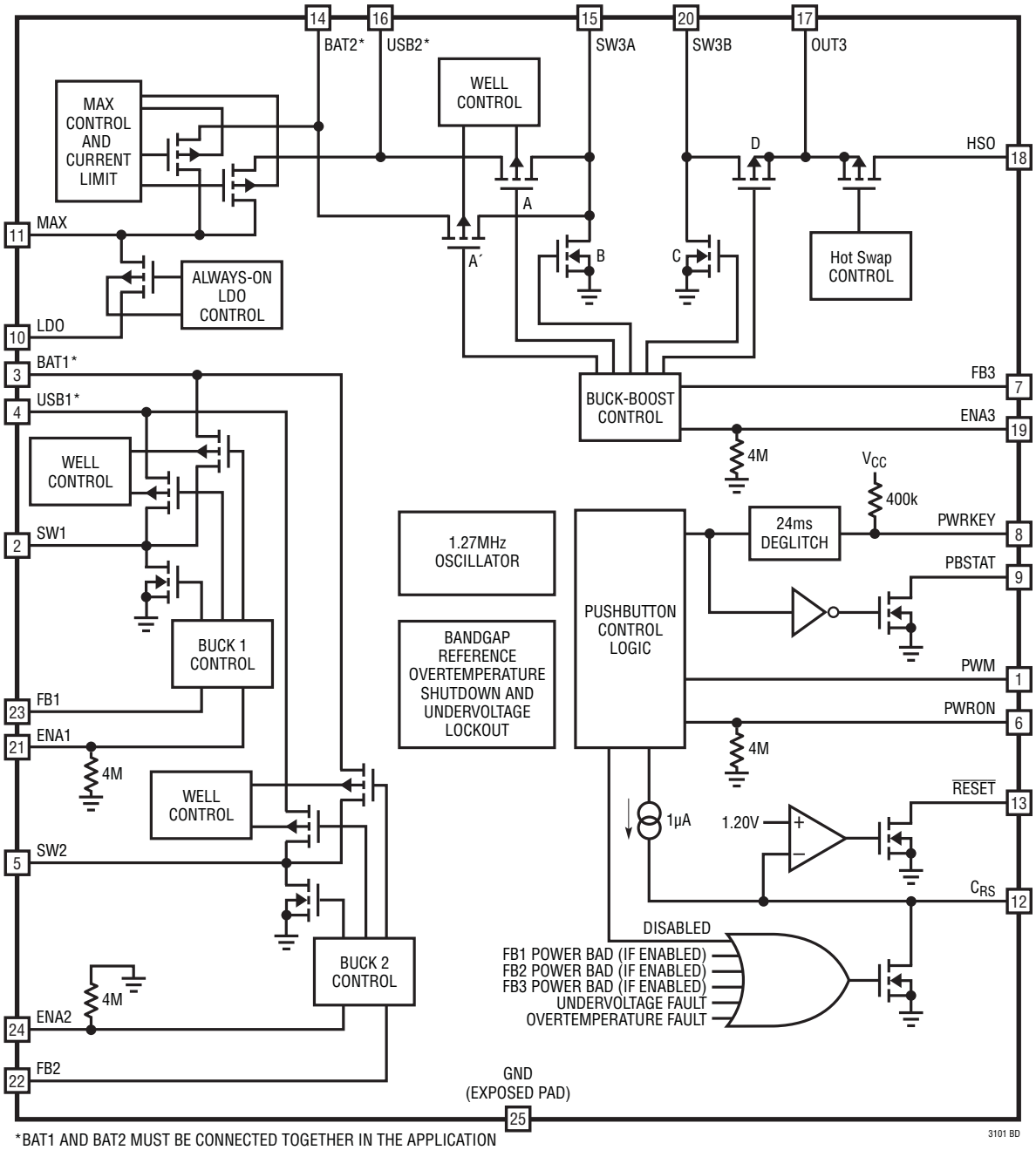
FB2 (Pin 22): Feedback Voltage Input for Buck Converter 2. The resistor divider connected to this pin sets the output voltage for buck converter 2.

FB1 (Pin 23): Feedback Voltage Input for Buck Converter 1. The resistor divider connected to this pin sets the output voltage for buck converter 1.

ENA2 (Pin 24): Enable Pin for Buck Converter 2. Forcing this pin above 1V will turn on the buck converter when the IC is enabled (via the pushbutton interface). Forcing this pin below 0.3V will disable buck converter 2.

Exposed Pad (Pin 25): Small-Signal and Power Ground for the IC. **The Exposed Pad must be soldered to the PCB and electrically connected to ground through the shortest and lowest impedance connection possible.**

BLOCK DIAGRAM



*BAT1 AND BAT2 MUST BE CONNECTED TOGETHER IN THE APPLICATION
USB1 AND USB2 MUST BE CONNECTED TOGETHER IN THE APPLICATION

OPERATION

INTRODUCTION

The LTC3101 provides a complete power management solution for low power portable devices. It generates a total of six output voltage rails and provides a seamless, automatic transition between two input power sources. The LTC3101 contains three high efficiency synchronous DC/DC converters: a 5-switch buck-boost DC/DC converter and two synchronous 3-switch step-down DC/DC converters. The buck-boost DC/DC converter is typically utilized to provide a 3V or 3.3V rail that lies within the input voltage range. The two step-down converters can be configured to provide two lower voltage output rails, such as a 1.8V rail for SDRAM and a 1.2V rail to supply the system microprocessor.

The LTC3101 can operate from any power source over the wide input voltage range of 1.8V to 5.5V. All three switching DC/DC converters operate from a common 1.27MHz oscillator and a single pin can be used to place all three DC/DC converters into Burst Mode operation to reduce the total no-load quiescent current with all six output voltage rails active to only 38µA (typical). In standby operation, with only the LDO and MAX outputs active, the input current is reduced to 15µA (typical).

The 5-switch buck-boost DC/DC converter generates a user-programmable output voltage rail that can lie within the voltage range of the input power sources. Utilizing a proprietary switching algorithm, the buck-boost converter maintains high efficiency and low noise operation with input voltages that are above, below, or even equal to the required output rail. A protected Hot Swap output powered by the buck-boost output voltage rail is enabled once the buck-boost reaches regulation. This provides a current-limited output that can be shorted without affecting the primary buck-boost output. One use of the Hot Swap output is to power external flash memory cards that need to be hot-plugged without disrupting the primary buck-boost output rail.

The synchronous buck converters are typically used to provide two high efficiency lower voltage rails and support 100% duty cycle operation to extend battery life. The output voltage of each buck converter is independently user programmable and can be set as low as 0.6V.

An always-alive LDO provides a fixed 1.8V output at 50mA which can be utilized to power critical functions such as a real time clock. Reverse blocking allows the LDO to be used to charge a supercapacitor for memory retention when both power sources are removed. The MAX output generates a secondary always-alive, current-limited output rail that tracks the higher voltage input power source (battery or USB) and is convenient for powering additional external LDOs and circuitry that can function directly from a wide input voltage range.

A pushbutton interface and internal supply sequencing complete the LTC3101 as a total power supply solution while requiring only a minimal number of supporting external components. Integral to the pushbutton control is an internal microprocessor reset generator with a reset duration that can be easily programmed using a single external capacitor allowing the interface to be customized to each particular application.

The extensive functionality and flexibility of the LTC3101, along with its small size and high efficiency, make it an excellent power solution for a wide variety of low power portable electronic products.

PUSHBUTTON INTERFACE

The LTC3101 includes a pushbutton interface that allows a single momentary pushbutton to control the sequenced power-up and power-down of all output rails in coordination with an external microprocessor. In addition, three independent enable pins allow an unused DC/DC converter to be independently disabled and also provide the means to manually implement an alternate power-up sequence.

The LTC3101 can be enabled by either forcing PWRON high or by forcing PWRKEY low. In either case, the DC/DC converters (if enabled by their respective enable pin) will power up in the internally fixed default sequence: buck converter 1, buck converter 2, and finally the buck-boost converter. In the typical application, the power-on sequence is initiated when the PWRKEY is driven low by an external momentary pushbutton. Once the microprocessor is powered up it must assert PWRON high before the pushbutton is released, thereby forcing the LTC3101 to

OPERATION

remain enabled. Power-down is usually accomplished by having the microprocessor monitor PBSTAT to detect an additional push of the pushbutton. Once this is detected, the microprocessor disables the LTC3101 by forcing PWRON low (or simply releasing PWRON and allowing it be pulled low by its internal pull-down resistor). In this manner, a single external momentary pushbutton is all that is required to provide sequenced power-up and power-down control.

Figure 1 depicts the waveforms in the standard power-up sequence. In this example, it is assumed that all three DC/DC converter rails are used in the application and therefore ENA1, ENA2 and ENA3 are driven high (or tied to the MAX output). An external normally-open pushbutton is connected between ground and the PWRKEY pin. When the pushbutton is not pressed, PWRKEY is pulled high via an internal 400k pull-up resistor. Until the power-up sequence is initiated, the IC is in the standby state, and only the LDO and MAX outputs are active.

The standard power-up sequence is initiated when the pushbutton is pressed, forcing PWRKEY low for a duration that is longer than the 24ms (typical) internal debouncing duration. Once the PWRKEY is held low for the debouncing duration, PBSTAT is driven low to indicate the pushbutton status. In addition, buck converter 1 is enabled and its output begins rising into regulation. Once the feedback voltage of buck converter 1 reaches its power good threshold, buck converter 2 is enabled. After buck converter 2 reaches its power good threshold, the buck-boost converter is enabled. Finally, once the buck-boost output reaches its power good threshold, the Hot Swap output is enabled and simultaneously the microprocessor reset duration begins when a 1µA (nominal) current begins charging the external C_{RS} capacitor. The microprocessor reset output, $\overline{RESET}$, is driven low throughout this entire power-up sequence until the C_{RS} pin is charged to 1.2V (typical). Once $\overline{RESET}$ goes high, the microprocessor in the application initializes and must drive the PWRON input of the LTC3101 high in order to keep the LTC3101 enabled. If PWRON is not driven high by the time PWRKEY returns high (i.e., the pushbutton is released) then the LTC3101 will be disabled and all outputs will be actively discharged to ground.

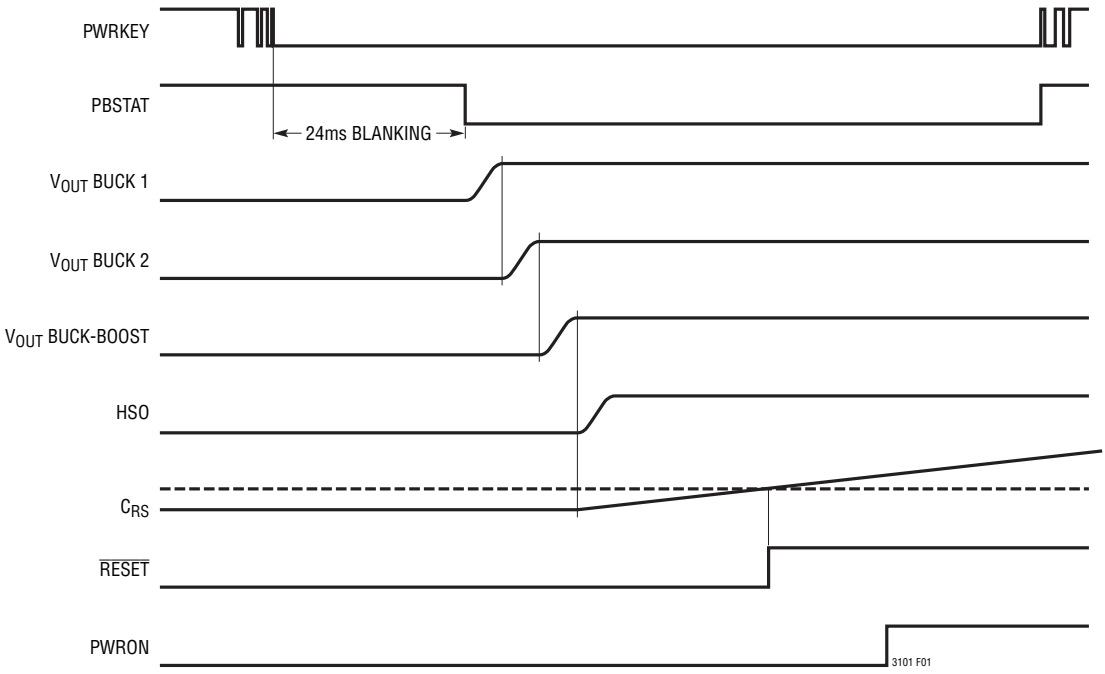


Figure 1. Power-Up Sequence Waveforms

OPERATION

Independent Enables

Each of the buck converters and the buck-boost converter have independent enable pins (ENA1, ENA2 and ENA3). These provide an additional degree of flexibility by allowing any unused channels to be independently disabled and skipped in the power-up sequence. For example, if the additional low voltage rail generated by the second buck converter is not required, it can be disabled by simply forcing ENA2 to ground. The power-up sequence will be unaffected except that second buck converter will be skipped. As a result, buck converter 1 will power up and the buck-boost will be enabled as soon as buck converter 1 reaches regulation. Any unused channels can be disabled in this fashion and they will simply be skipped in the power-up sequence.

Manual Power-Up Via The PWRON Pin

If the pushbutton interface is not required, the LTC3101 can be manually enabled by simply forcing the PWRON pin high. When PWRON is forced high any channels that are enabled via their independent enable pin will power up in the standard sequence (buck converter 1, buck converter 2 and then the buck-boost converter). An arbitrary power-up sequence can be forced manually, by forcing all enables (ENA1, ENA2, ENA3) low while bringing PWRON high. Then, after waiting 10µs for the logic to initialize, the individual converters can be manually enabled via their independent enable pins in any order required. For example, a simultaneous power-up is initiated by bringing PWRON high while holding ENA1, ENA2 and ENA3 low. Then after a 10µs or longer delay, ENA1, ENA2 and ENA3 can be brought high simultaneously causing the two buck rails and the buck-boost rail to begin rising simultaneously.

Fault Conditions

On an overtemperature or input undervoltage fault condition, all DC/DC converters, the LDO, and the MAX output are disabled and the C_{RS} pin is driven low which results in the microprocessor reset output, $\overline{RESET}$, being driven low as well. In the standard application, this will cause the microprocessor to release the PWRON pin, thereby disabling the LTC3101. Consequently, the LTC3101 will not automatically re-enable even if the fault condition clears. Instead, the LTC3101 will have to be restarted via repeating the normal power-up sequence. Alternatively, if PWRON is held high until the fault condition clears, then any enabled converters will power up in the default sequence once the fault clears and the microprocessor reset will clear after its programmed delay.

If the power good comparator for any converter indicates a fault condition (loss of regulation), the C_{RS} pin and $\overline{RESET}$ pins are driven low. In a typical application, this will place the microprocessor in the reset condition which will release the force on PWRON and therefore disable the LTC3101. However, if PWRON is maintained high, all converters will remain enabled through the fault condition. Once the fault condition clears, the affected converter output will recover, and C_{RS} will begin charging. After the programmed reset duration, $\overline{RESET}$ will be released.

LDO OUTPUT

The LDO output generates a regulated 1.8V (nominal) output voltage rail that is guaranteed to support a 50mA load. The LDO output remains active whenever a valid supply is present on either the USB2 or BAT2 inputs and is unaffected by the pushbutton interface. Its always-on status allows the LDO to power critical functions such as a real time clock which must remain powered under all conditions.

The LDO output is reverse blocking in shutdown (i.e., when undervoltage lockout threshold is reached) allowing its output to stay charged when both input supplies are removed with reverse leakage guaranteed to be under 1µA. This allows the LDO to be used to charge a supercapacitor for memory retention purposes or powering standby functions during times when both power sources are removed. The LDO is specifically designed to be stable with a small 4.7µF capacitor, but to also maintain stable operation with arbitrarily large capacitance supercapacitors without requiring a series isolation resistor.

The LDO output is current-limit protected. On an undervoltage or overtemperature fault, the LDO is disabled until the fault condition clears.

OPERATION

MAX OUTPUT

The MAX output generates a protected output rail that tracks the higher of the two input supplies, BAT2 or USB2. The MAX output is current-limit protected and is guaranteed to support a 200mA load.

The MAX output is an always-alive output, meaning it is always enabled independent of the state of the pushbutton interface. This allows the MAX output to power additional LDOs or critical circuitry that must remain powered in standby. In addition, the MAX output can be used to efficiently power additional application circuits that can operate directly from a wide input voltage range without burdening one of the switching converters. The MAX output is also a convenient supply for forcing logic inputs (such as PWM, ENA1, ENA2 and ENA3) high since it is powered whenever either input supply is present.

The MAX output is disabled in undervoltage lockout and during overtemperature shutdown. Since the MAX output serves as the input to the LDO, it is recommended that it be bypassed with a 1µF or greater ceramic capacitor if the LDO is to be used in the application.

Hot Swap (HSO) OUTPUT

The HSO output is generated by a protected power switch from the output of the buck-boost converter. It provides a current-limited output that can be shorted to ground without disrupting the buck-boost output voltage. This is primarily intended to be used as a supply rail for flash memory cards which can be hot-plugged in the application. When a card is hot-plugged into the HSO output, the supply bypass capacitors on the card are gradually charged via the current-limited output without affecting the buck-boost output rail. The HSO output is not enabled until the buck-boost is enabled and the buck-boost power good comparator indicates it is in regulation.

BUCK CONVERTER OPERATION

The LTC3101 contains two independent buck DC/DC converters each capable of supplying a 350mA load. Each has an adjustable output voltage that can be set as low as 0.6V. In addition, each buck converter supports low dropout operation to extend battery life. These converters can be utilized in Burst Mode operation to improve light-load efficiency and no-load standby current or in PWM mode to ensure low noise operation. Each buck converter has dual P-channel power switches and a single N-channel synchronous rectifier. The dual P-channel power switches allow the buck converters to operate directly from either the battery or USB inputs (BAT1 or USB1). The buck converters will automatically and seamlessly transition to operate from the higher voltage supply. Both buck converters feature short-circuit protection and frequency foldback to prevent inductor current run-away during low resistance output short conditions.

PWM Mode Operation

If the PWM pin is forced high, both buck converters will operate in fixed frequency pulse width modulation mode using current mode control. At the start of each oscillator cycle, the active P-channel switch is turned on and remains on until the inductor current with superimposed slope compensation ramp exceeds the error amplifier output. At this point, the synchronous rectifier is turned on and remains on until the inductor current falls to zero or a new switching cycle is initiated. As a result, the buck converter operates with discontinuous inductor current at light loads in order to improve efficiency. At extremely light loads, the minimum on-time of the P-channel switch will be reached and the buck converter will begin turning off for multiple cycles in order to maintain regulation.

Burst Mode Operation

When the PWM pin is forced low, both buck converters will automatically and independently transition between Burst Mode operation at sufficiently light loads (below approximately 10mA) and PWM mode at heavier loads. Burst Mode entry is determined by the peak inductor current and therefore the load current at which Burst Mode operation will be entered depends on the input voltage, the output voltage and the inductor value. Typical curves for Burst Mode entry threshold are provided in the Typical Performance Characteristics section of this data sheet. In dropout operation, the active P-channel switch will remain on continuously and Burst Mode operation will not be entered.

OPERATION

Low Dropout Operation

As the input voltage decreases to a value approaching the output regulation voltage, the duty cycle increases to the maximum on-time of the P-channel switch. Further reduction of the supply voltage will force the main switch to remain on for more than one cycle and subharmonic switching will occur to provide a higher effective duty cycle. If the input voltage is decreased further, the buck converter will enter 100% duty cycle operation and the P-channel switch will remain on continuously. In this dropout state, the output voltage is determined by the input voltage less the resistive voltage drop across the P-channel switch and series resistance of the inductor.

Slope Compensation

Current mode control requires the use of slope compensation to prevent sub-harmonic oscillations in the inductor current waveform at high duty cycle operation. This function is performed internally on the LTC3101 through the addition of a compensating ramp to the current sense signal. In some current mode ICs, current limiting is performed by clamping the error amplifier voltage to a fixed maximum. This leads to a reduced output current capability at low step-down ratios. In contrast, the LTC3101 performs current-limiting prior to addition of the slope compensation ramp and therefore achieves a peak inductor current limit that is independent of duty cycle.

Output Short-Circuit Operation

When the output is shorted to ground, the error amplifier will saturate high and the P-channel switch will turn on at the start of each cycle and remain on until the current limit trips. During this minimum on-time of the P-channel switch, the inductor current will increase rapidly but will decrease very slowly during the remainder of the period due to the very small reverse voltage produced by a hard output short. To eliminate the possibility of inductor current runaway in this situation, the switching frequency of the buck converters is reduced by a factor of four when the voltage on the respective feedback pin (FB1 or FB2) falls below 0.3V. This provides additional time for the inductor current to reset and thereby protects against a build-up of current in the inductor.

Internal Voltage Mode Soft-Start

Each buck converter has an independent internal voltage mode soft-start circuit with a nominal duration of 800µs. The buck converters remain in regulation during soft-start and will therefore respond to output load transients which occur during this time. In addition, the output voltage rise-time has minimal dependency on the size of the output capacitor or load current during start-up.

Error Amplifier and Internal Compensation

The LTC3101 buck converters utilize internal transconductance error amplifiers. Compensation of the buck converter feedback loops is performed internally to reduce the size of the application circuit and simplify the design process. The compensation network has been designed to allow use of a wide range of output capacitors while simultaneously ensuring a rapid response to load transients.

Power Good Comparator Operation

Each buck converter has an internal power good comparator that monitors the respective feedback pin voltage (FB1 or FB2). The power good comparator outputs are used at power-up for sequencing purposes. During normal operation, the power good comparators are used to monitor the output rails for a fault condition. If either buck power good comparator indicates a fault condition, the C_{RS} and $\overline{\text{RESET}}$ pins are driven low. This can be used to reset a microprocessor in the application circuit when either buck converter output rail loses regulation.

The buck power good comparator will trip when the respective feedback pin falls 8% (nominally) below the regulation voltage. With a rising output voltage, the power good comparator will typically clear when the respective feedback voltage rises to within 5.5% of the regulation voltage. In addition, there is a 60µs typical deglitching delay in the power good comparators in order to prevent false trips due to brief voltage transients occurring on load steps.

OPERATION

BUCK-BOOST CONVERTER OPERATION

The buck-boost converter is a synchronous 5-switch DC/DC converter with the capability to operate efficiently with input voltages that are above, below or equal to the output regulation voltage. A proprietary switching algorithm provides a smooth transition between operational modes while maintaining high efficiency and low noise performance. Referring to the Block Diagram, the buck-boost converter has two P-channel input power switches, A and A´. This provides the capability for the buck-boost converter to operate directly from either input power source, USB or battery. The buck-boost converter automatically and seamlessly transitions to the higher voltage input supply.

PWM Mode Operation

When the PWM pin is held high, the LTC3101 buck-boost converter operates in a fixed frequency pulse width modulation mode using voltage mode control. A proprietary switching algorithm allows the converter to transition between buck, buck-boost, and boost modes without discontinuity in inductor current or loop characteristics. The switch topology for the buck-boost converter is shown in Figure 2.

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A (or A´) and B are pulse width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 85%, the switch pair AC begins turning on for a small fraction of the switching period. As the input voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionally. As the input voltage drops below the output voltage, the AC phase will eventually increase to the point that there is no longer any BD phase. At this point, switch A remains on continuously while switch pair CD is pulse width modulated to obtain the desired output voltage. At this point, the converter is operating solely in boost mode.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout all three operational modes. These advantages result in increased efficiency and stability in comparison to the traditional 4-switch buck-boost converter.

Error Amplifier and Internal Compensation

The buck-boost converter utilizes a voltage mode error amplifier with an internal compensation network as shown in Figure 3.

Notice that resistor R2 of the external resistor divider network plays an integral role in determining the frequency response of the compensation network. The ratio of R2 to R1 is set to program the desired output voltage but this still allows the value of R2 to be adjusted to optimize the

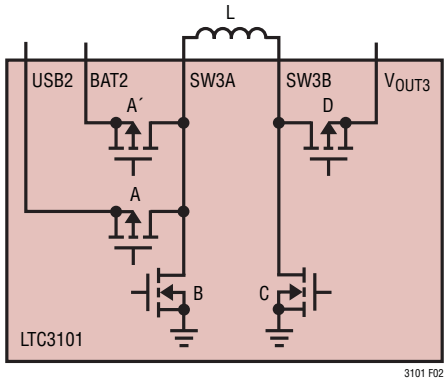


Figure 2. Buck-Boost Switch Topology

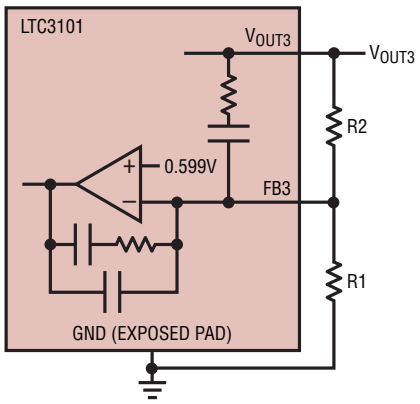


Figure 3. Buck-Boost Error Amplifier and Compensation

OPERATION

transient response of the converter. Increasing the value of R2 generally leads to greater stability at the expense of reduced transient response speed. Increasing the value of R2 can yield substantial transient response improvement in cases where the phase margin has been reduced due to use of a small value output capacitor or a large inductance (particularly with large boost step-up ratios). Conversely, decreasing the value of R2 increases the loop bandwidth which can improve the speed of the converter's transient response. This can be useful in improving the transient response if a large value output capacitor is utilized. In this case, the increased bandwidth created by decreasing R2 is used to counteract the reduced converter bandwidth caused by the large output capacitor.

Current Limit Operation

The buck-boost converter has two current limit circuits. The primary current limit is an average current limit circuit which injects an amount of current into the feedback node which is proportional to the extent that the switch A (or A´) current exceeds the current limit value. Due to the high gain of the feedback loop, the injected current forces the error amplifier output to decrease until the average current through switch A decreases approximately to the current limit value. The average current limit utilizes the error amplifier in an active state and thereby provides a smooth recovery with little overshoot once the current limit fault condition is removed. Since the current limit is based on the average current through switch A (or A´), the peak inductor current in current limit will have a dependency on the duty cycle (i.e., on the input and output voltages) in the overcurrent condition.

The speed of the average current limit circuit is limited by the dynamics of the error amplifier. On a hard output short, it would be possible for the inductor current to increase substantially beyond current limit before the average current limit circuit would react. For this reason, there is a second current limit circuit which turns off switch A (and A´) if the current ever exceeds approximately 165% of the average current limit value. This provides additional protection in the case of an instantaneous hard output short.

Reverse Current Limit

A reverse current comparator on switch D monitors the current entering the OUT3 pin. When this current exceeds 400mA (typical) switch D will be turned off for the remainder of the switching cycle. This feature protects the buck-boost converter from excessive reverse current if the buck-boost output is held above the regulation voltage by an external source.

Burst Mode Operation

With the PWM pin held low, the buck-boost converter operates utilizing a variable frequency switching algorithm designed to improve efficiency at light load and reduce the standby current at zero load. In Burst Mode operation, the inductor is charged with fixed peak amplitude current pulses. These current pulses are repeated as often as necessary to maintain the output regulation voltage. The maximum output current, I_{MAX}, which can be supplied in Burst Mode operation is dependent upon the input and output voltage as given by the following formula:

$$I_{MAX} = \frac{0.15 \bullet V_{IN}}{V_{IN} + V_{OUT}} \left(A\right)$$

If the buck-boost load exceeds the maximum Burst Mode current capability, the output rail will lose regulation and the power good comparator will indicate a fault condition.

In Burst Mode operation, the error amplifier is not used but is instead placed in a low current standby mode to reduce supply current and improve light load efficiency.

Internal Voltage Mode Soft-Start

The buck-boost converter has an internal voltage mode soft-start circuit with a nominal duration of 800µs. The converter remains in regulation during soft-start and will therefore respond to output load transients that occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load. During soft-start, the buck-boost converter is forced into PWM mode operation regardless of the state of the PWM pin.

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Power Good Comparator Operation

The buck-boost converter contains an internal power good comparator that continuously monitors the voltage of the feedback pin FB3. The output of this comparator is used during power-up for sequencing purposes. In addition, during operation, if the power good comparator indicates a fault condition, C_{RS} and $\overline{RESET}$ will be driven low. This feature can be used to reset a microprocessor in the application circuit if the buck-boost output loses regulation.

In Burst Mode operation (PWM = low), the buck-boost power good comparator will indicate a fault when the feedback voltage falls approximately 8.5% below the regulation voltage. There is approximately 2.5% hysteresis in this threshold when the output voltage is returning good. In addition, there is a 60µs typical deglitching delay in order to prevent false trips due to short duration voltage transients in response to load steps.

In PWM mode, operation of the power good comparator is complicated by the fact that the feedback pin voltage is driven to the reference voltage independent of the output voltage through the action of the voltage mode error amplifier. Since the soft-start is voltage mode, the feedback voltage will track the output voltage correctly during soft-start, and the power good comparator output will correctly indicate the point at which the buck-boost attains regulation at the end of soft-start. However, once in regulation, the feedback voltage will no longer track the output voltage and the power good comparator will not immediately respond to a loss of regulation in the output. For this reason, the power good comparator output is also designed to indicate a fault condition if the buck-boost converter enters current limit. The only means by which a loss of regulation can occur is if the current limit has been reached thereby preventing the buck-boost converter from delivering the required output current. In such cases, the occurrence of current limit will directly cause the power good comparator to indicate a fault state. However, there may be cases at the boundary of reaching current limit when the buck-boost converter is continuously in current limit, causing the power good comparator to indicate a fault, but the output voltage may be slightly above the actual power good threshold.

COMMON FUNCTIONS

Thermal Shutdown

If the die temperature exceeds 150°C all DC/DC converters will be disabled. In addition, the LDO and MAX outputs are disabled. All power devices are turned off and all switch nodes will be high impedance. The soft-start circuits for all converters are reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. All DC/DC converters (if enabled) and the LDO and MAX outputs will restart when the die temperature drops to approximately 140°C.

Undervoltage Lockout

If the supply voltage decreases below 1.65V (typical) then all DC/DC converters will be disabled and all power devices are turned off. In addition, the MAX and LDO outputs are disabled. The LDO is forced into its reverse blocking state, allowing the LDO output to remain powered with less than 1µA reverse current being drawn by the LTC3101. The soft-start circuits for all DC/DC converters are reset during undervoltage lockout to provide a smooth restart once the input voltage rises above the undervoltage lockout threshold.

Active Output Discharge

All three DC/DC converter outputs are actively discharged to ground when disabled through 1kΩ (typical) impedances. The buck converter outputs are discharged through the inductor via a pull-down resistor on the respective switch pin.

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The basic LTC3101 application circuit is shown as the Typical Application on the front page of this data sheet. The external component selection is dependent upon the required performance of the IC in each particular application given considerations and tradeoffs such as PCB area, output voltages, output currents, ripple voltages and efficiency. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the application circuit.

C_{RS} Capacitor Selection

A capacitor from the C_{RS} pin to ground is used to program the duration of the microprocessor reset signal on the $\overline{RESET}$ pin. A low leakage ceramic capacitor should be utilized to ensure reliable temperature independent operation. At the start of the active-low reset pulse, a 1µA (typical) current begins charging the C_{RS} capacitor. The $\overline{RESET}$ pulse ends when the voltage at the C_{RS} pin reaches 1.20V (typical). Therefore, the required C_{RS} capacitor value, C_{RS}, is given by the following equation where t_{RESET} is the desired reset duration in milliseconds:

$$C_{RS} = \frac{t_{RESET}}{1200}\ (\mu F)$$

If the microprocessor reset function of the LTC3101 is unused, the C_{RS} pin can be left unconnected.

LDO Output Capacitance

The LDO has been specifically designed for stable operation with a wide range of output capacitors. For most applications, a low ESR ceramic capacitor of at least 4.7µF should be utilized. Large valued supercapacitors can be connected directly to the LDO output without requiring a series isolation resistor for loop stability. However, if the supercapacitor has significant ESR, it may be necessary to place a small 4.7µF ceramic in parallel with the supercapacitor to maintain an adequate phase margin.

MAX Capacitor Selection

The MAX output serves as the input to the LDO. Therefore, even if the MAX output is unused directly in the application, it is recommended that it be bypassed with a 1µF or larger ceramic capacitor. There is no limit to the maximum capacitance on this pin. However, the soft-start duration is formed by the current-limited output charging the capacitance attached to the pin so larger output capacitors will result in proportionally longer soft-start durations.

Buck Inductor Selection

The choice of buck inductor value influences both the efficiency and the magnitude of the output voltage ripple. Larger inductance values will reduce inductor current ripple and will therefore lead to lower output voltage ripple. For a fixed DC resistance, a larger value inductor will yield higher efficiency by lowering the peak current to be closer to the average output current. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Given a desired peak-to-peak current ripple, ΔI_L, the required inductance can be calculated via the following expression, where f represents the switching frequency in MHz:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)\ (\mu H)$$

A reasonable choice for ripple current is ΔI_L = 140mA which represents 40% of the maximum 350mA load current. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current in order to prevent core saturation and loss of efficiency during operation. To optimize efficiency the inductor should have a low DC resistance (DCR).

In particularly space-restricted applications it may be advantageous to use a much smaller value inductor at the expense of larger ripple current. In such cases, the converter will operate in discontinuous conduction for a wider range of output loads and efficiency will be reduced. In addition, there is a minimum inductor value required to maintain stability of the current loop as determined by the fixed internal slope compensation. Specifically, if the

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buck converter is going to be utilized at duty cycles over 40%, the inductance value must be at least equal to L_{MIN} as given by the following equation:

$$L_{MIN} = 2.5 \bullet V_{OUT}\ (\mu H)$$

Table 1 depicts the minimum required inductance for several common output voltages.

Table 1. Buck Minimum Inductance

OUTPUT VOLTAGE	MINIMUM INDUCTANCE
0.8V	2.0µH
1.2V	3.0µH
1.8V	4.7µH
2.0V	5.0µH
2.7V	6.8µH

A large variety of low ESR, high current power inductors are available that are well suited to LTC3101 buck converter applications. The tradeoff generally involves PCB area, application height, required output current and efficiency. Table 2 provides a representative sampling of small surface mount inductors that are well suited for use with the LTC3101 buck converters. All inductor specifications are listed at an inductor value of 4.7µH for comparison purposes but other values within these inductor families are generally well suited to this application as well. Within each family (i.e., at a fixed inductor size), the DC resistance generally increases and the maximum current generally decreases with increased inductance.

Table 2. Representative Buck Inductors

PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft				
LPS3015	4.7	0.20	1.2	3.0 × 3.0 × 1.5
EPL2014	4.7	0.23	0.88	2.0 × 2.0 × 1.4
EPL2010	4.7	0.43	0.65	2.0 × 2.0 × 1.0
LPS4018	4.7	0.125	1.9	4.0 × 4.0 × 1.8
Cooper-Bussmann				
SD3118	4.7	0.162	1.31	3.1 × 3.1 × 1.8
SD3112	4.7	0.246	0.80	3.1 × 3.1 × 1.2
SD3110	4.7	0.285	0.68	3.1 × 3.1 × 1.0
SD10	4.7	0.154	1.08	5.2 × 5.2 × 1.0
Murata				
LQH3NP	4.7	0.26	0.80	3.0 × 3.0 × 0.9
LQM31PN	4.7	0.30	0.70	3.2 × 1.6 × 0.85
LQH32CN	4.7	0.15	0.65	3.2 × 2.5 × 2.0
Panasonic				
ELLVEG	4.7	0.24	0.70	3.0 × 3.0 × 1.0
ELL4G	4.7	0.16	0.86	3.8 × 3.8 × 1.1
ELL4LG	4.7	0.09	1.10	3.8 × 3.8 × 1.8
Sumida				
CDRH2D09	4.7	0.167	0.42	3.2 × 3.2 × 1.0
CDRH3D16/LD	4.7	0.081	0.62	3.2 × 3.2 × 1.8
CDRH2D09B	4.7	0.218	0.70	3.0 × 2.8 × 1.0
Taiyo-Yuden				
CBC2518	4.7	0.2	0.68	2.5 × 1.8 × 1.8
CBC3225T	4.7	0.1	1.01	3.2 × 2.5 × 2.5
NR3010T	4.7	0.19	0.75	3.0 × 3.0 × 1.0
TOKO				
DE2812C	4.7	0.13	1.2	3.0 × 3.2 × 1.2
D310F	4.7	0.26	0.9	3.8 × 3.8 × 1.0
DB3015C	4.7	0.09	0.86	3.2 × 3.2 × 1.8
Wurth				
744028004	4.7	0.265	0.90	2.8 × 2.8 × 1.1
744032004	4.7	0.280	0.49	3.2 × 2.5 × 2.0
744029003	4.7	0.170	0.80	2.8 × 2.8 × 1.35

Buck Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. In addition to controlling the ripple magnitude, the value of the output capacitor also sets the loop crossover frequency and therefore can impact loop stability. In general, there is both a minimum and maximum capacitance value required to ensure stability of the loop. If the output capacitance is too small, the loop crossover frequency will increase to the point where switching delay and the high frequency parasitic poles of the error amplifier will degrade the phase margin. In addition, the wider bandwidth produced by a small output capacitor will make the loop more susceptible to switching noise. Table 3 depicts the minimum recommended output capacitance for several typical output voltages. At the other extreme, if the output capacitor is too large, the crossover frequency can decrease too far below the compensation zero and also lead to degraded phase margin. In such cases, the phase margin and transient performance can be improved by simply increasing the size of the feedforward capacitor in parallel with the upper resistor divider resistor. (See Buck Output Voltage Programming section for more details).

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Table 3. Buck Minimum Recommended Output Capacitance

OUTPUT VOLTAGE	MINIMUM RECOMMENDED OUTPUT CAPACITANCE
0.6V	22µF
0.8V	22µF
1.2V	10µF
1.8V	10µF
2.7V	4.7µF
3.3V	4.7µF

Buck Input Capacitor Selection

The BAT1 and USB1 pins provides current to the power stages of both buck converters. It is recommended that a low ESR ceramic capacitor with a value of at least 4.7µF be used to bypass each of these pins. These capacitors should be placed as close to the respective pin as possible and should have a short return path to the backpad of the IC.

Buck Output Voltage Programming

The buck output voltages are programmed via external resistor dividers connected to the respective feedback pin (FB1 or FB2) as shown in Figure 4.

The resistor divider resistors control the output voltage according to the following formula:

$$V_{OUT1,2} = 0.596\left(1+\frac{R2}{R1}\right)(V) \quad (1)$$

If the impedance of the resistor divider is too high it will increase noise sensitivity due to coupling of stray noise to the feedback pin. In addition, the parallel resistance of the resistor divider resistors in series with the input capacitance of the feedback pin produce a parasitic pole that can reduce the loop phase margin if it becomes too low in frequency. For these reasons, it is recommended that the resistance of R1 in parallel with R2 be kept under 300k. A reasonable compromise between noise immunity and quiescent current is provided by choosing R2 = 221k. The required value for R1 can then be calculated via Equation 1.

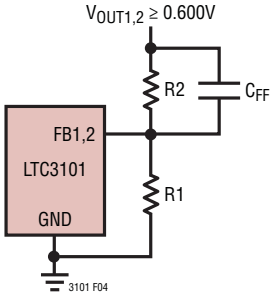

Figure 4. Setting the Buck Output Voltages

To further increase the noise immunity of the feedback pin and improve the transient response of the buck converter, a small value feedforward capacitor, C_{FF}, can be added in parallel with the upper feedback divider resistor, R2. This reduces the impedance of the feedback pin at high frequencies thereby increasing its immunity from picking up stray noise. In addition, this adds a pole-zero pair to the loop dynamics which generates a phase boost that can improve the phase margin and increase the speed of the transient response, resulting in smaller voltage deviation on load transients. The zero frequency depends not only on the value of the feedforward capacitor, but also on the upper resistor divider resistor. Specifically, the zero frequency, f_{ZERO}, is given by the following equation:

$$f_{ZERO} = \frac{1}{2 \bullet \pi \bullet R2 \bullet C_{FF}}$$

Ideally, the phase boost generated by the pole-zero pair should be centered at the loop crossover frequency. Table 4 provides the recommended feedback divider resistor values and corresponding feedforward capacitors for several commonly utilized output voltages.

Table 4. Buck Resistor Divider and Feedforward Capacitor Values

V_{OUT}	R1	R2	C_{FF}	C_{OUT}
0.6V	–	0	–	22µF
0.8V	649k	221k	18pF	22µF
1.0V	324k	221k	18pF	22µF
1.2V	221k	221k	18pF	10µF
1.5V	147k	221k	18pF	10µF
1.8V	110k	221k	18pF	10µF
2.0V	86.6k	205k	18pF	10µF
2.7V	56.2k	200k	18pF	4.7µF
3.3V	48.7k	221k	18pF	4.7µF

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If a substantially larger output capacitor is utilized, the bandwidth of the loop will be reduced. In such cases, the feedforward capacitor can be increased in value in order to lower the zero frequency and improve the transient response.

Buck-Boost Output Voltage Programming

The buck-boost output voltage is set via an external resistor divider connected to the FB3 pin as shown in Figure 5.

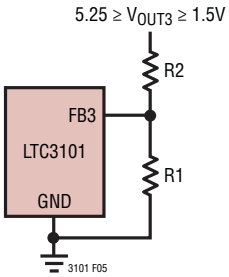

Figure 5. Setting the Buck-Boost Output Voltage

The resistor divider values determine the buck-boost output voltage according to the following formula:

$$V_{OUT3} = 0.599\left(1+\frac{R2}{R1}\right)(V) \quad (2)$$

The buck-boost converter utilizes voltage mode control and in addition to setting the output voltage, the value of R2 plays an integral role in the dynamics of the feedback loop. In general, a larger value for R2 will increase stability and reduce the speed of the transient response. A smaller value of R2 will reduce stability but increase the speed of the transient response. A good starting point is to choose R2 = 1M and then calculate the required value of R1 to set the desired output voltage according to Equation 2. If a large output capacitor is used, the bandwidth of the converter is reduced. In such cases R2 can be reduced to improve the transient response. If a large inductor or small output capacitor is utilized the loop will be less stable and the phase margin can be improved by increasing the value of R2.

Buck-Boost Inductor Selection

To achieve high efficiency, a low ESR inductor should be utilized for the buck-boost converter. In addition, the buck-boost inductor must have a saturation current rating that is greater than the worst-case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple will be larger in buck and boost mode then in the buck-boost region. The peak-to-peak inductor current ripple for each mode can be calculated from the following formulas, where f is the frequency in MHz and L is the inductance in µH:

$$\Delta I_{L(P\text{-}P)(BUCK)} = \frac{V_{OUT}}{f \bullet L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)$$

$$\Delta I_{L(P\text{-}P)(BOOST)} = \frac{V_{IN}}{f \bullet L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)$$

In addition to affecting output current ripple, the size of the inductor can also impact the stability of the feedback loop. In boost mode, the converter transfer function has a right half plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductor can move this zero to a frequency that is low enough to degrade the phase margin of the feedback loop. It is recommended that the inductor value be chosen less than 10µH if the buck-boost converter is to be used in the boost region.

In addition to affecting the efficiency of the buck-boost converter, the inductor DC resistance can also impact the maximum output capability of the buck-boost converter at low input voltage. In buck mode, the buck-boost output current is limited only by the inductor current reaching the current limit value. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These include switch resistances, inductor resistance, and PCB trace resistance. Use of an inductor with high DC resistance can degrade the output current capability from that shown in the graph in the Typical Performance Characteristics section of this data sheet.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 5

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provides a small sampling of inductors that are well suited to many LTC3101 buck-boost converter applications. All inductor specifications are listed at an inductance value of 4.7µH for comparison purposes but other values within these inductor families are generally well suited to this application. Within each family (i.e., at a fixed size), the DC resistance generally increases and the maximum current generally decreases with increased inductance.

Table 5. Representative Buck-Boost Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft				
LPS4018	4.7	125	1.9	4.0 × 4.0 × 1.8
LPS4012	4.7	175	1.8	4.0 × 4.0 × 1.2
ME3220	4.7	190	1.5	3.2 × 2.5 × 2.0
MSS5121	4.7	95	1.66	5.4 × 5.4 × 2.1
Cooper-Bussmann				
SD12	4.7	118	1.29	5.2 × 5.2 × 1.2
SD14	4.5	94	1.74	5.2 × 5.2 × 1.4
Panasonic				
ELL6PG	4.7	58	1.5	6.0 × 6.0 × 2.0
ELL5PS	4.7	61	1.5	5.0 × 5.0 × 1.85
Sumida				
CDRH3D18	4.7	86	1.35	4.0 × 4.0 × 2.0
CDRH4D15/S	4.7	103	1.4	4.7 × 4.7 × 1.7
CDRH4D22/HP	4.7	66	2.2	5.0 × 5.0 × 2.4
Taiyo-Yuden				
NR6020T	4.7	58	2.0	6.0 × 6.0 × 2.0
NP04SZB	4.7	75	1.8	5.0 × 5.0 × 2.0
TOKO				
DE2815C	4.7	100	1.3	3.0 × 2.8 × 1.5
DP418C	4.7	50	1.50	4.2 × 4.2 × 1.8
DE4514C	4.7	100	1.9	4.7 × 4.9 × 1.4
Wurth				
744042004	4.7	82	1.65	4.8 × 4.8 × 1.8
7447785004	4.7	78	2.20	5.9 × 6.2 × 3.3
7447745056	4.7	57	2.40	5.2 × 5.8 × 2.0

Buck-Boost Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. The capacitor should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f is the frequency in MHz, C_{OUT} is the capacitance in µF, L is the inductance in µH, and I_{LOAD} is the output current in Amps.

$$\Delta V_{P-P(BUCK)} = \frac{1}{8 \bullet L \bullet C_{OUT} \bullet f^2} \bullet \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN}}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}(V_{OUT} - V_{IN})}{C_{OUT} \bullet V_{OUT} \bullet f}$$

Given that the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode. In addition to controlling the ripple magnitude, the value of the output capacitor also affects the location of the resonant frequency in the open-loop converter transfer function. If the output capacitor is too small, the bandwidth of the converter will extend high enough to degrade the phase margin. To prevent this from happening, it is recommended that a minimum value of 10µF be used for the buck-boost output capacitor. If the required buck-boost load current is greater than 400mA, it is recommended that the output capacitor be increased to 22µF to improve output voltage ripple and loop stability.

Buck-Boost Input Capacitor Selection

The supply current to the buck-boost converter is provided by the USB2 and BAT2 pins. In addition, these pins provide power to the internal circuitry of the LTC3101. It is recommended that a low ESR ceramic capacitor with a value of at least 10µF be located as close to each of these pins as possible. In addition, the return trace from each pin to the ground plane should be made as short as possible.

Capacitor Vendor Information

Both the input bypass capacitors and DC/DC converter output capacitors used with the LTC3101 must be low ESR and designed to handle the large AC currents generated by switching converters. This is important to maintain proper functioning of the IC and to reduce output ripple. Many modern low voltage ceramic capacitors experience significant loss in capacitance from their rated value with increased DC bias voltages. For example, it is not uncommon for a small surface mount ceramic capacitor

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to lose 45% of its rated capacitance when operated near its rated voltage. As a result, it is sometimes necessary to use a larger value capacitance or a capacitor with a higher voltage rating than required in order to actually realize the intended capacitance at the full operating voltage. For details, consult the capacitor vendor's curve of capacitance versus DC bias voltage.

The capacitors listed in Table 6 provide a sampling of small surface mount ceramic capacitors that are well suited to LTC3101 application circuits. All listed capacitors are either X5R or X7R dielectric in order to ensure that capacitance loss over temperature is minimized.

Table 6. Representative Bypass and Output Capacitors

PART NUMBER	VALUE (µF)	VOLTAGE (V)	SIZE (mm) L × W × H (FOOTPRINT)
AVX			
12106D475K	4.7	6.3	1.6 × 0.8 × 0.86 (0603)
12104D106K	10	4	1.6 × 0.8 × 1.02 (0603)
12106D106K	10	6.3	2.0 × 1.25 × 1.4 (0805)
12106D226K	22	6.3	2.0 × 1.25 × 1.4 (0805)
Kemet			
C0603C475K9P	4.7	6.3	1.6 × 0.8 × 0.8 (0603)
C0603C106K9P	10	6.3	1.6 × 0.8 × 0.8 (0603)
C0805C476K9P	47	6.3	2.0 × 1.25 × 1.25 (0805)
Murata			
GRM18	4.7	6.3	1.6 × 0.8 × 0.8 (0603)
GRM21	4.7	10	2.0 × 1.25 × 1.25 (0805)
GRM21	10	10	2.0 × 1.25 × 1.25 (0805)
GRM21	22	6.3	2.0 × 1.25 × 1.25 (0805)
Samsung			
CL10A475KP5LNN	4.7	10	1.6 × 0.8 × 0.55 (0603)
CL10A106KQ8NNN	10	6.3	1.6 × 0.8 × 0.90 (0603)
CL21A226MQCLRN	22	6.3	2.0 × 1.25 × 0.95 (0805)
CL21A476MQYNNN	47	6.3	2.0 × 1.25 × 1.45 (0805)
Taiyo Yuden			
JMK107BJ	10	6.3	1.6 × 0.8 × 0.8 (0603)
LMK107BJ	4.7	10	1.6 × 0.8 × 0.8 (0603)
JMK212BJ	22	6.3	2.0 × 1.25 × 0.85 (0805)
JMK212BJ	47	6.3	2.0 × 1.25 × 0.85 (0805)
TDK			
C1608X5ROJ	4.7	6.3	1.6 × 0.8 × 0.8 (0603)
C1608X5R0J	6.8	6.3	1.6 × 0.8 × 0.8 (0603)
C1608X5R0J	10	6.3	1.6 × 0.8 × 0.8 (0603)
C2012X5R0J	15	6.3	2.0 × 1.25 × 0.85 (0805)

PCB Layout Considerations

The LTC3101 switches large currents at high frequencies. Special attention should be paid to the PCB layout to ensure a stable, noise-free and efficient application circuit.

Figure 6 presents a representative PCB layout to outline some of the primary considerations. A few key guidelines are listed:

1. All circulating high current paths should be kept as short as possible. This can be accomplished by keeping the routes to all components in Figure 6 as short and as wide as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on USB1, USB2, BAT1 and BAT2 should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The Exposed Pad is the small-signal and power ground connection for the LTC3101. Multiple vias should connect the backpad directly to the ground plane. In addition maximization of the metallization connected to the backpad will improve the thermal environment and increase the power handling capabilities of the IC.
3. The components shown in bold and their connections should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
4. Connections to all of the components shown in bold should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.
5. To prevent large circulating currents from disrupting the output voltage sensing, the ground for each resistor divider should be returned to the ground plane using a via placed close to the IC and away from the power connections.
6. Keep the connection from the resistor dividers to the feedback pins FB1 and FB2 as short as possible and away from the switch pin connections.
7. Crossover connections (such as the one shown from SW3A to the inductor) should be made on inner copper layers if available. If it is necessary to place these on the ground plane, make the trace on the ground plane as short as possible to minimize the disruption to the ground plane.

APPLICATIONS INFORMATION

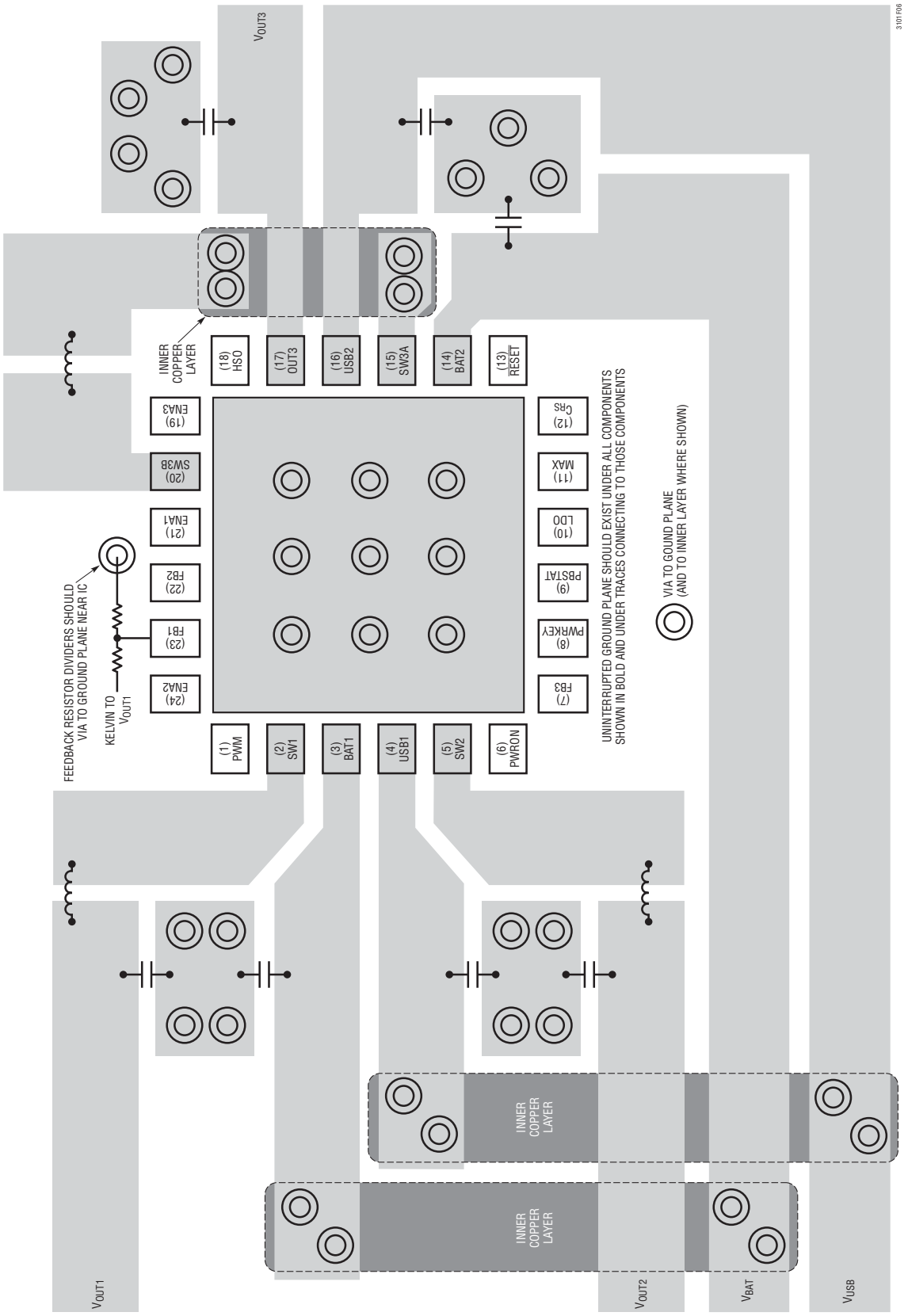
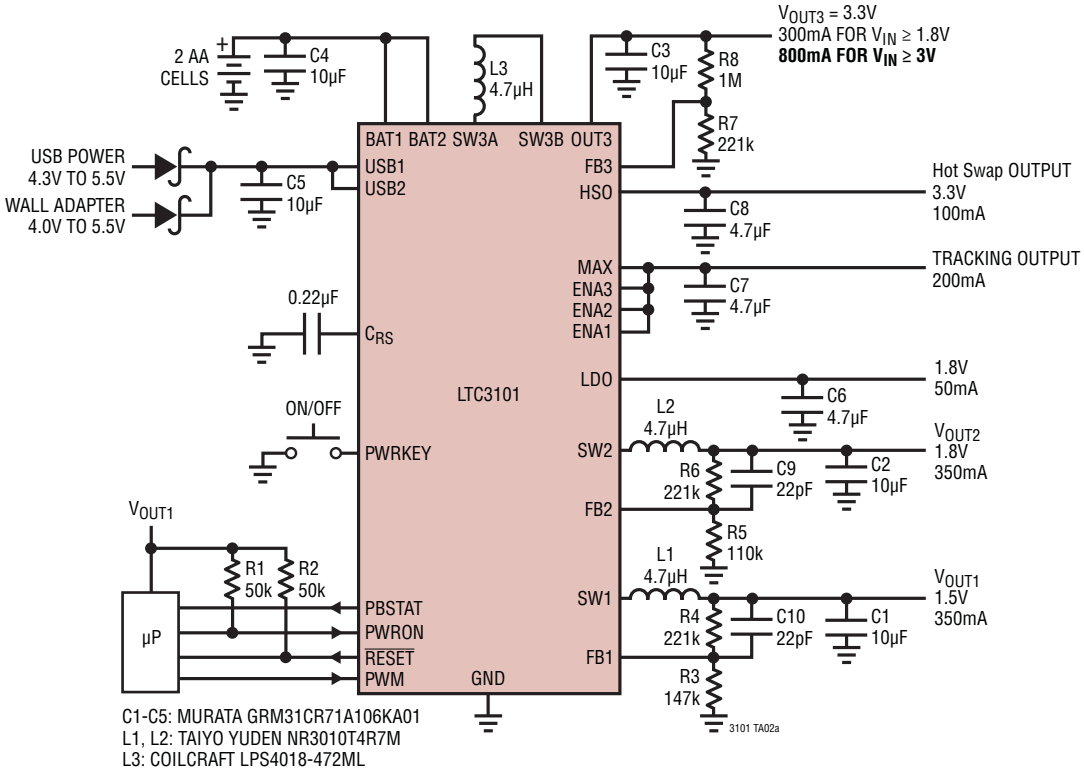


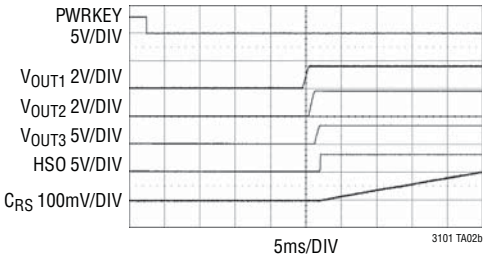
Figure 6. PCB Layout Recommendations

TYPICAL APPLICATIONS

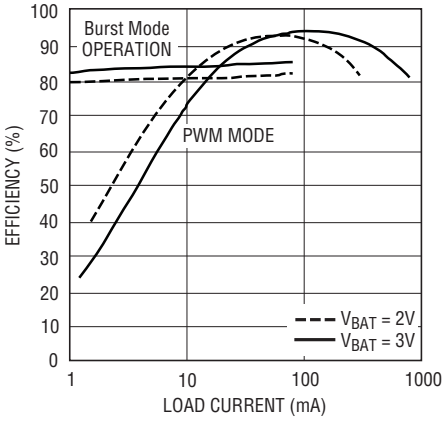
2 AA Cell/USB/Wall Adapter Power Supply with Six Output Rails and Pushbutton On/Off



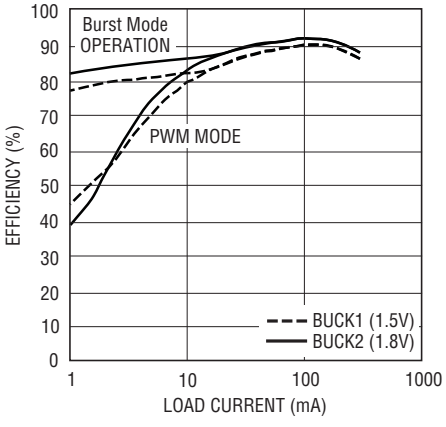
Waveforms During Power-Up



Buck-Boost Converter Efficiency vs Load Current

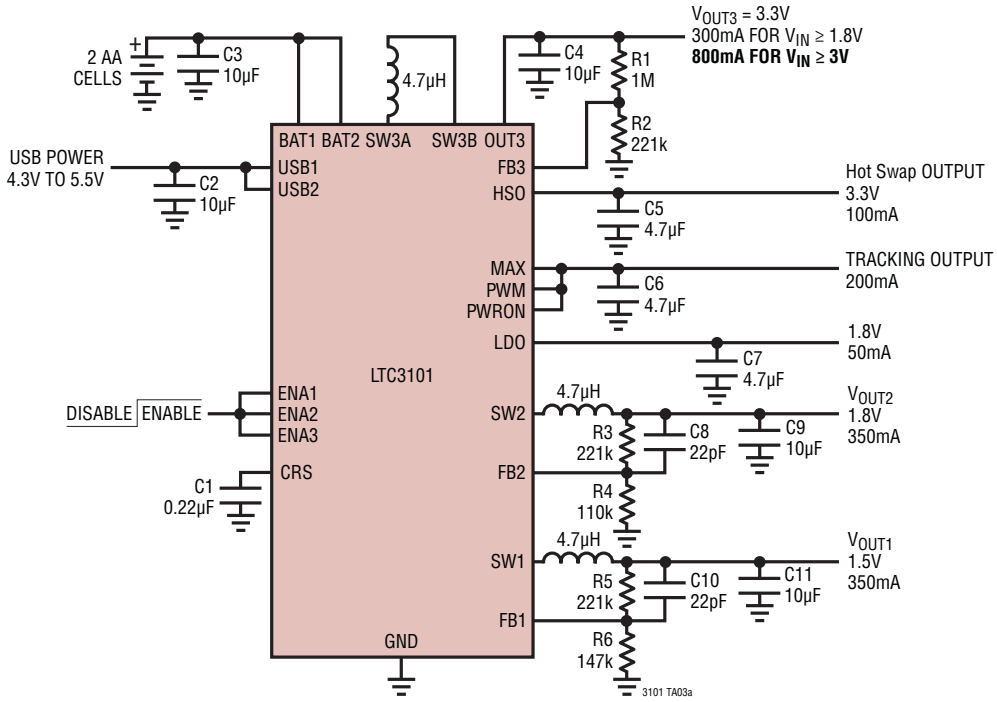


Buck Converter Efficiency vs Load Current, V_{BAT} = 3V

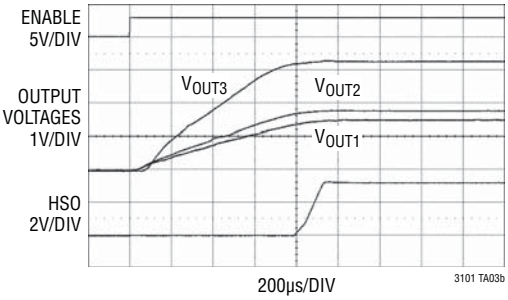


TYPICAL APPLICATIONS

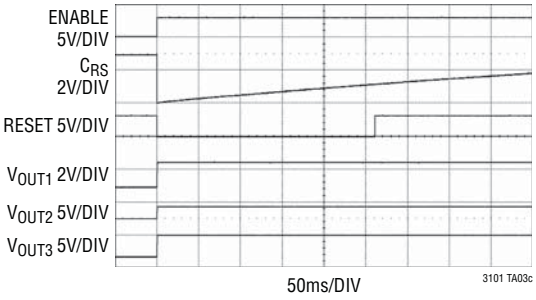
Manual Enable with Simultaneous Start-Up



Power-Up Waveforms

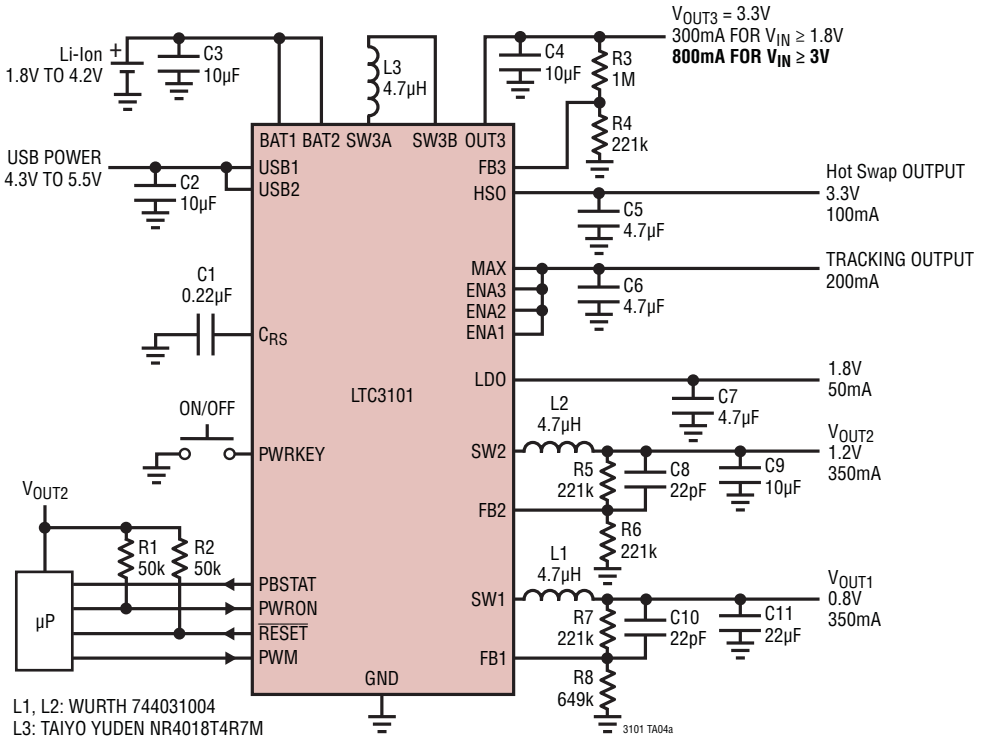


RESET Timing During Power Up

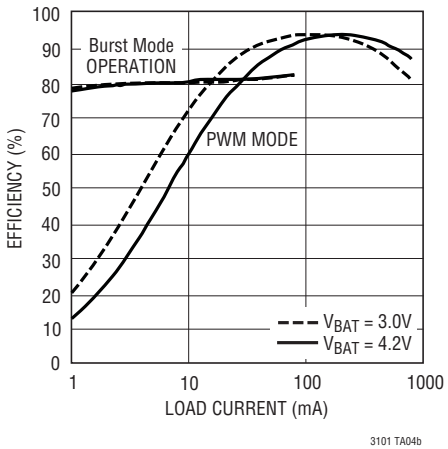


TYPICAL APPLICATIONS

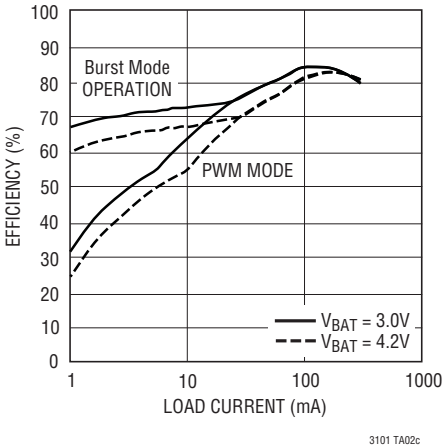
Li-Ion/USB-Powered Six Output Power Supply with Pushbutton Control



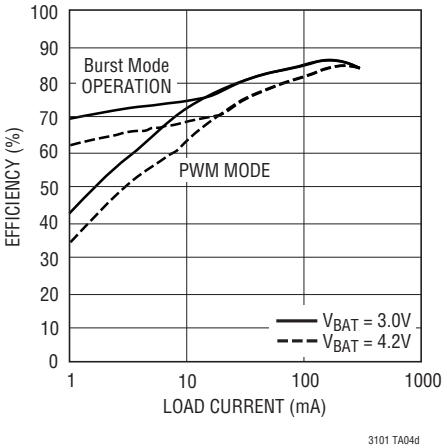
Buck-Boost Efficiency vs Load Current



Buck Converter 1 Efficiency vs Load Current

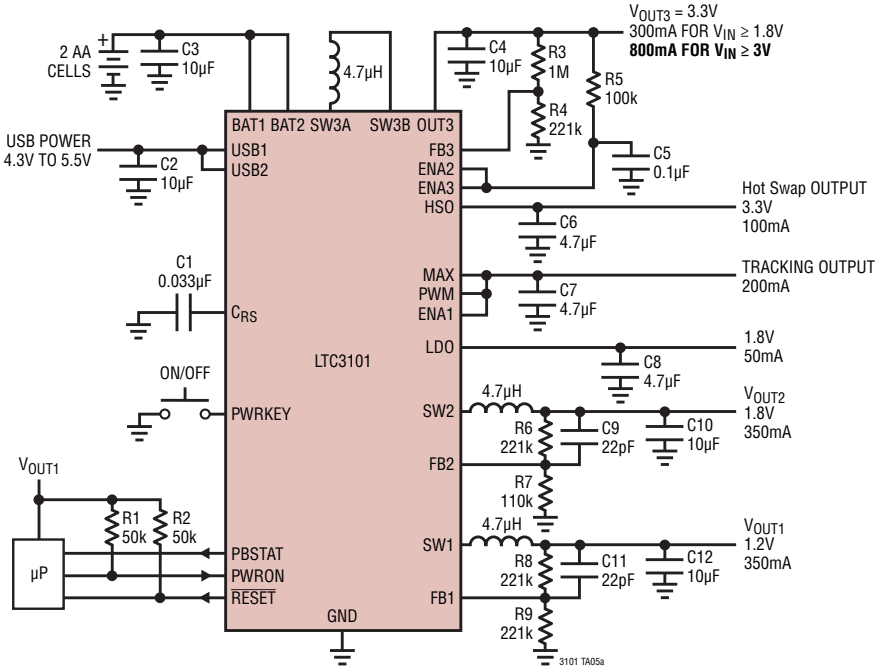


Buck Converter 2 Efficiency vs Load Current

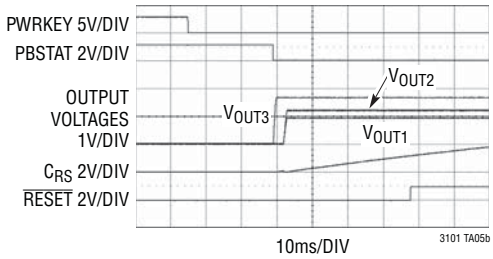


TYPICAL APPLICATIONS

Sequenced Start-Up, Buck-Boost Followed by Buck Converters

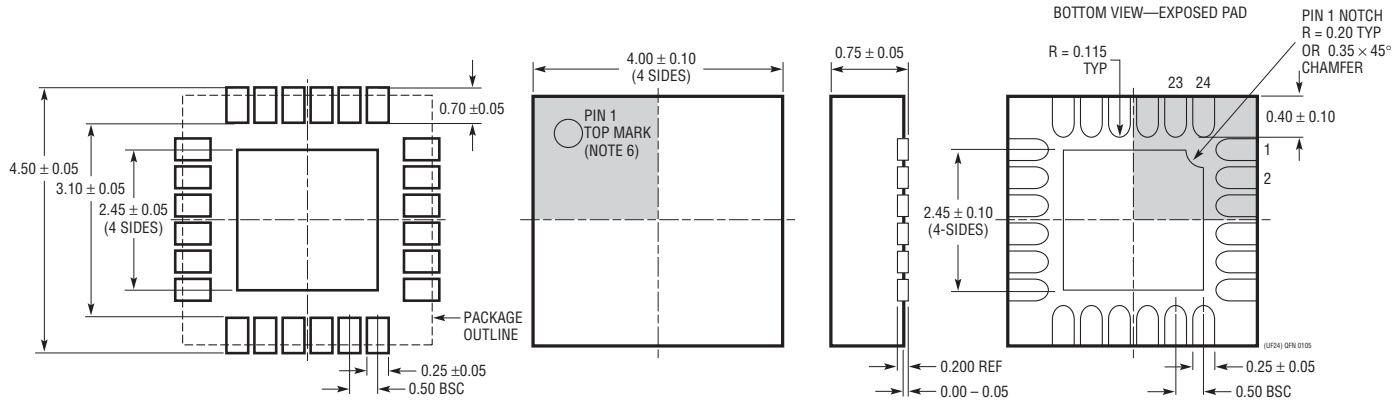


Power-Up Waveforms



PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3009	3µA I_Q, 20mA Low Dropout Linear Regulator	V_{IN}: 1.6V to 20V, V_{OUT} as Low as 0.6V, I_Q = 3µA, I_{SD} < 1µA, SC70 and DFN Packages
LTC3100	700mA Synchronous Step-Up, 250mA Step-Down DC/DC Converters, 100mA LDO	V_{IN}: 0.65V to 5V, Step-Up V_{OUT}: 1.5V to 5.25V, Step-Down V_{OUT} as Low as 0.6V, I_Q = 15µA, I_{SD} < 1µA, QFN Package
LTC3409	600mA, Low V_{IN}, 2.6MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 1.6V to 5.5V, V_{OUT} as Low as 0.61V, I_Q = 65µA, I_{SD} < 1µA, DFN Package
LTC3440	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.5V to 5.5V, V_{OUT}: 2.5V to 5.25V, I_Q = 25µA, I_{SD} < 1µA, MSOP and DFN Packages
LTC3441	1.2A (I_{OUT}), 1MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.4V to 5.25V, I_Q = 25µA, I_{SD} < 1µA , DFN Package
LTC3442	1.2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter with Programmable Burst Mode Operation	V_{IN}: 2.4V to 5.5V, V_{OUT}: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, DFN Package
LTC3444	400mA (I_{OUT}), 1.5MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 2.75V to 5.5V, V_{OUT}: 0.5V to 5V, I_{SD} < 1µA, DFN Package
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	V_{IN}: 3V to 5.5V, Transition Between Inputs, I_Q = 110µA, I_{SD} < 2µA, QFN Package
LTC3456	2-Cell, Multi-Output DC/DC Converter with USB Power Manager	V_{IN}: 1.8V to 5.5V, Dual DC/DC Converter and Hot Swap Outputs, Seamless Transition Between Inputs, I_Q = 180µA, I_{SD} < 1µA, QFN Package
LTC3520	1A (I_{OUT}) Synchronous Buck-Boost and 600mA Step-Down DC/DC Converters with LDO Controller	V_{IN}: 2.2V to 5.5V, Buck-Boost V_{OUT}: 2.2V to 5.25V, Step-Down V_{OUT} as Low as 0.8V, I_Q = 55µA, I_{SD} < 1µA, QFN Package
LTC3522	400mA (I_{OUT}) Synchronous Buck-Boost and 200mA Step-Down DC/DC Converters	V_{IN}: 2.4V to 5.5V, Buck-Boost V_{OUT}: 2.2V to 5.25V, Step-Down V_{OUT} as Low as 0.6V, I_Q = 25µA, I_{SD} < 1µA, QFN Package
LTC3523	Synchronous 600mA Step-Up and 400mA Step-Down 2.4MHz DC/DC Converters	V_{IN}: 1.8V to 5.5V, Step-Up V_{OUT}: 1.8V to 5.25V, Step-Down V_{OUT} as Low as 0.6V, I_Q = 45µA, I_{SD} < 2µA, QFN Package
LTC3527	Dual 2.2MHz 800mA/400mA Synchronous Step-Up DC/DC Converters	V_{IN}: 0.5V to5V, V_{OUT}: 1.6V to 5.25V, I_Q = 40µA, I_{SD} < 1µA, DFN Package
LTC3530	600mA (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 12µA, I_{SD} < 2µA, QFN Package
LTC3533	2A (I_{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V_{IN}: 1.8V to 5.5V, V_{OUT}: 1.8V to 5.25V, I_Q = 40µA, I_{SD} < 1µA, DFN Package
LTC3537	600mA, 2.2MHz Synchronous Step-Up DC/DC Converter and 100mA LDO	V_{IN}: 0.68V to 5V, V_{OUT}: 1.5V to 5.25V, I_Q = 30µA, I_{SD} < 1µA, QFN Package
LTC3549	250mA, Low V_{IN}, 2.25MHz Synchronous Step-Down DC/DC Converter	V_{IN}: 1.6V to 5.5V, V_{OUT} as Low as 0.61V, I_Q = 50µA, I_{SD} < 1µA, DFN Package
LTC3555	High Efficiency USB Power Manager, Li-Ion/Polymer Battery Charger and Triple Step-Down DC/DC Converters	V_{IN}: 2.7V to 5.5V, 1.5A Maximum Charge Current, 180mΩ Ideal Diode, Two 400mA and One 1A Buck DC/DC, I_Q = 20µA, QFN Package
LTC3556	High Efficiency USB Power Manager with Dual Step-Down and Buck-Boost DC/DC Converters	V_{IN}: 2.7V to 5.5V, 1.5A Maximum Charge Current, 1A Buck-Boost DC/DC, Dual 400mA Step-Down DC/DC, I_Q = 20µA, QFN Package
LTC3557	USB Power Manager with Li-Ion Charger and Three Step-Down Regulators	V_{IN}: 2.7V to 5.5V, Seamless Transition Between Inputs, 1.5A Charging Current, Two 400mA and One 600mA Step-Down DC/DC, QFN Package
LTC3566/ LTC3567	Switching USB Power Manager with Li-Ion/Polymer Charger, 1A Buck-Boost Converter Plus LDO	Multi-Function PMIC: Switchmode Power Manager and 1A Buck-Boost Regulator Plus LDO, Charge Current Programmable up to 1.5A from Wall Adapter Input, Synchronous Buck-Boost Converters Efficiency: >95%, ADJ Output: Down to 0.8V at 1A, LTC3567 Has I^2C Interface, 4mm × 4mm QFN-24 Package
LTC3586	Switching USB Power Manager with Li-Ion/Polymer Charger Plus Dual Buck Plus Buck-Boost Plus Boost DC/DC	Maximizes Available Power from USB Port, "Instant On" Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, Two 400mA Synchronous Buck Regulators, One 1A Buck-Boost Regulator, One 600mA Boost Regulator, 4mm × 6mm 38-Pin QFN Package

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