Low Noise, 500ksps, 1-/2-Channel, 12-Bit ADCs

FEATURES

- **12-Bit Resolution**
- **500ksps Sampling Rate**
- **Low Noise: SINAD = 72.8dB**
- Guaranteed No Missing Codes
- Single 5V Supply
- Auto-Shutdown Scales Supply Current with Sample Rate
- Low Power: 14mW at 500ksps
  70µW at 1ksps
  35µW Sleep Mode
- 1-Channel (LTC2302) and 2-Channel (LTC2306) Versions
- Unipolar or Bipolar Input Ranges (Software Selectable)
- Internal Conversion Clock
- SPI/MICROWIRE™ Compatible Serial Interface
- Separate Output Supply OV_{DD} (2.7V to 5.25V)
- Software Compatible with the LTC2308
- 10-Pin (3mm × 3mm) DFN Package

APPLICATIONS

- High Speed Data Acquisition
- Industrial Process Control
- Motor Control
- Accelerometer Measurements
- Battery-Operated Instruments
- Isolated and/or Remote Data Acquisition

DESCRIPTION

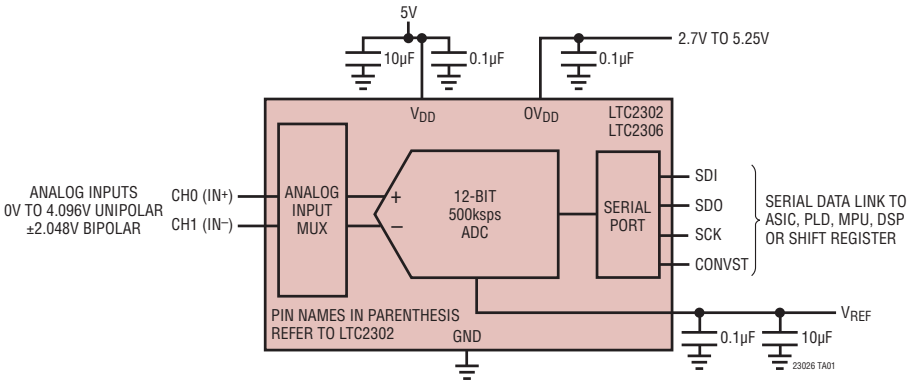
The LTC®2302/LTC2306 are low noise, 500ksps, 1-/2-channel, 12-bit ADCs with an SPI/MICROWIRE compatible serial interface. These ADCs include a fully differential sample-and-hold circuit to reduce common mode noise. The internal conversion clock allows the external serial output data clock (SCK) to operate at any frequency up to 40MHz.

The LTC2302/LTC2306 operate from a single 5V supply and draw just 2.8mA at a sample rate of 500ksps. The auto-shutdown feature reduces the supply current to 14µA at a sample rate of 1ksps.

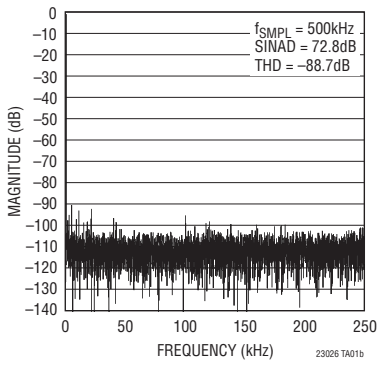
The LTC2302/LTC2306 are packaged in a tiny 10-pin 3mm × 3mm DFN. The low power consumption and small size make the LTC2302/LTC2306 ideal for battery-operated and portable applications, while the 4-wire SPI compatible serial interface makes these ADCs a good match for isolated or remote data acquisition systems.

	NUMBER OF INPUT CHANNELS		
TYPE	**1**	**2**	**8**
Int Reference			LTC2308
Ext Reference	LTC2302	LTC2306	

TYPICAL APPLICATION



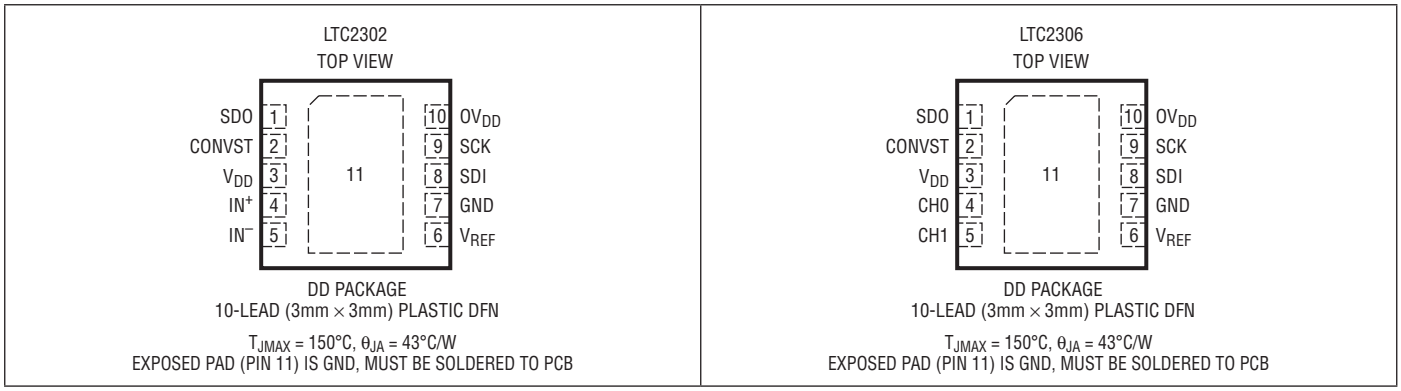
8192 Point FFT, f_{IN} = 1kHz (LTC2306)



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{DD}, OV_{DD})..... –0.3V to 6V
Analog Input Voltage (Note 3)
CH0(IN^+)-CH1(IN^-),
REF .....(GND – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage
(Note 3).....(GND – 0.3V) to (V_{DD} + 0.3V)
Digital Output Voltage ... (GND – 0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC2302C/LTC2306C ..... 0°C to 70°C
LTC2302I/LTC2306I..... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2302CDD#PBF	LTC2302CDD#TRPBF	LDGV	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2302IDD#PBF	LTC2302IDD#TRPBF	LDGV	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2306CDD#PBF	LTC2306CDD#TRPBF	LDGW	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2306IDD#PBF	LTC2306IDD#TRPBF	LDGW	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 6)	●		±0.3	±1	LSB
Differential Linearity Error		●		±0.25	±1	LSB
Bipolar Zero Error	(Note 7)	●		±1	±6	LSB
Bipolar Zero Error Drift				0.002		LSB/°C
Unipolar Zero Error	(Note 7)	●		±1	±6	LSB
Unipolar Zero Error Drift				0.002		LSB/°C
Unipolar Zero Error Match (LTC2306)				±0.3	±3	LSB
Bipolar Full-Scale Error	(Note 8)	●		±1.5	±8	LSB
Bipolar Full-Scale Error Drift				0.05		LSB/°C
Unipolar Full-Scale Error	(Note 8)	●		±1.2	±6	LSB
Unipolar Full-Scale Error Drift				0.05		LSB/°C
Unipolar Full-Scale Error Match (LTC2306)				±0.3	±3	LSB

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (CH0, CH1, IN^+)	(Note 9)	●	–0.05		V_{DD}	V
V_{IN}^-	Absolute Input Range (CH0, CH1, IN^-)	Unipolar (Note 9) Bipolar (Note 9)	● ●	–0.05 –0.05		$V_{DD}/2$ V_{DD}	V V
$V_{IN}^+ – V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ – V_{IN}^-$ (Unipolar) $V_{IN} = V_{IN}^+ – V_{IN}^-$ (Bipolar)	● ●		0 to V_{REF} $±V_{REF}/2$		V V
I_{IN}	Analog Input Leakage Current		●			±1	µA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			55 5		pF pF
CMRR	Input Common Mode Rejection Ratio				70		dB

REFERENCE INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{REF} Input Range		●	0.1		V_{DD}	V
I_{REF}	Reference Input Current	f_{SMPL} = 0ksps, V_{REF} = 4.096V f_{SMPL} = 500ksps, V_{REF} = 4.096V	● ●		50 230	80 260	µA µA
C_{REF}	Reference Input Capacitance				55		pF

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 1kHz	●	71	72.8		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 1kHz	●	71	73.2		dB
THD	Total Harmonic Distortion	f_{IN} = 1kHz, First 5 Harmonics	●		–88	–78	dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1kHz	●	79	89		dB
	Channel-to-Channel Isolation	f_{IN} = 1kHz			–109		dB
	Full Linear Bandwidth	(Note 11)			700		kHz
	–3dB Input Linear Bandwidth				25		MHz
	Aperature Delay				13		ns
	Transient Response	Full-Scale Step			240		ns

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	High Level Input Current	V_{IN} = V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	OV_{DD} = 4.75V, I_{OUT} = –10µA OV_{DD} = 4.75V, I_{OUT} = –200µA	 ●	 4	4.74		V V
V_{OL}	Low Level Output Voltage	OV_{DD} = 4.75V, I_{OUT} = 160µA OV_{DD} = 4.75V, I_{OUT} = 1.6mA	 ●		0.05	 0.4	V V
I_{OZ}	Hi-Z Output Leakage	V_{OUT} = 0V to OV_{DD}, CONVST High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance	CONVST High			15		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
OV_{DD}	Output Driver Supply Voltage		●	2.7		5.25	V
I_{DD}	Supply Current Sleep Mode	C_L = 25pF CONVST = 5V, Conversion Done	● ●		2.8 7	3.5 15	mA µA
P_D	Power Dissipation Sleep Mode				14 35		mW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●			500	kHz
f_{SCK}	Shift Clock Frequency		●			40	MHz
t_{WHCONV}	CONVST High Time	(Note 9)	●	20			ns
t_{HD}	Hold Time SDI After SCK↑		●	2.5			ns
t_{SUDI}	Setup Time SDI Stable Before SCK↑		●	0			ns
t_{WHCLK}	SCK High Time	$f_{SCK} = f_{SCK(MAX)}$	●	10			ns
t_{WLCLK}	SCK Low Time	$f_{SCK} = f_{SCK(MAX)}$	●	10			ns
$t_{WLCONVST}$	CONVST Low Time During Data Transfer	(Note 9)	●	410			ns
$t_{HCONVST}$	Hold Time CONVST Low After Last SCK↓	(Note 9)	●	20			ns
t_{CONV}	Conversion Time		●		1.3	1.6	µs
t_{ACQ}	Acquisition Time	7th SCK↑ to CONVST↑ (Note 9)	●	240			ns
t_{dDO}	SDO Data Valid After SCK↓	C_L = 25pF (Note 9)	●		10.8	12.5	ns
t_{hDO}	SDO Hold Time SCK↓	C_L = 25pF	●	4			ns
t_{en}	SDO Valid After CONVST↓	C_L = 25pF	●		11	15	ns
t_{dis}	Bus Relinquish Time	C_L = 25pF	●		11	15	ns
t_r	SDO Rise Time	C_L = 25pF			4		ns
t_f	SDO Fall Time	C_L = 25pF			4		ns
t_{CYC}	Total Cycle Time				2		µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with V_{DD} and OV_{DD} wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below ground or above V_{DD}, they will be clamped by internal diodes. These products can handle input currents greater than 100mA below ground or above V_{DD} without latchup.

Note 4: V_{DD} = 5V, OV_{DD} = 5V, V_{REF} = 4.096V, f_{SMPL} = 500ksps, unless otherwise specified.

Note 5: Linearity, offset and full-scale specifications apply for a single-ended analog input with respect to GND for the LTC2306 and IN^+ with respect to IN^- tied to GND for the LTC2302.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111. Unipolar zero error is the offset voltage measured from +0.5LSB when the output code flickers between 0000 0000 0000 and 0000 0000 0001.

Note 8: Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error. Unipolar full-scale error is the deviation of the last code transition from ideal and includes the effect of offset error.

Note 9: Guaranteed by design, not subject to test.

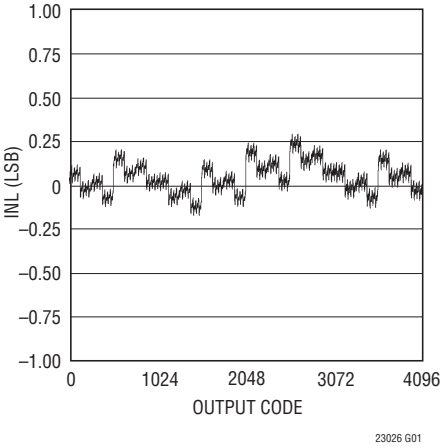
Note 10: All specifications in dB are referred to a full-scale ±2.048V input with a 4.096V reference voltage.

Note 11: Full linear bandwidth is defined as the full-scale input frequency at which the SINAD degrades to 60dB or 10 bits of accuracy.

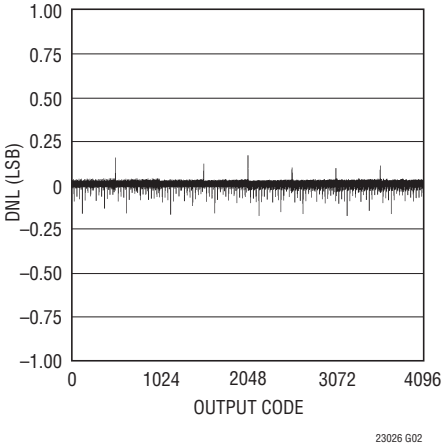
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2302) T_A = 25°C, V_{DD} = OV_{DD} = 5V, V_{REF} = 4.096V, f_{SMPL} = 500ksps, unless otherwise noted.

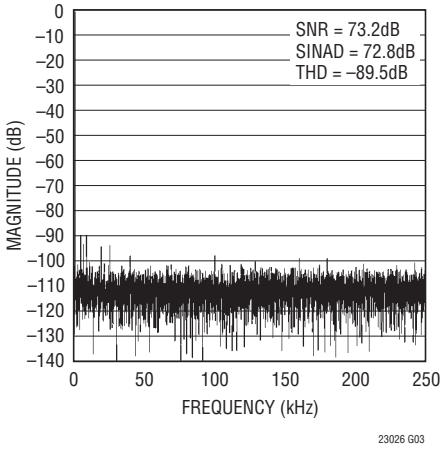
Integral Nonlinearity vs Output Code



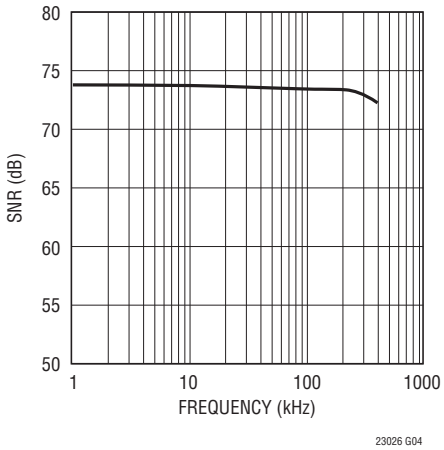
Differential Nonlinearity vs Output Code



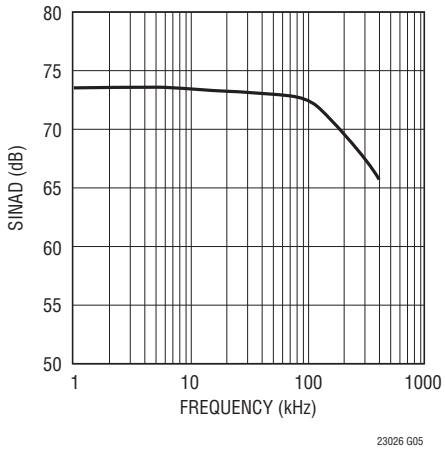
1kHz Sine Wave 8192 Point FFT Plot



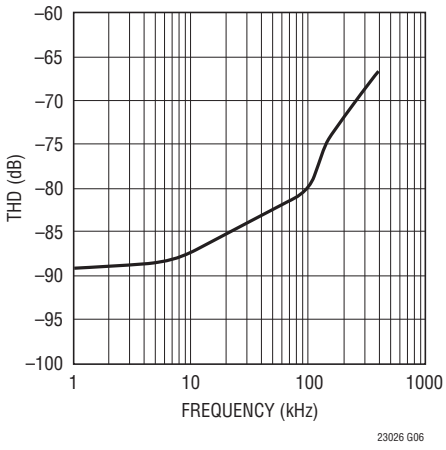
SNR vs Input Frequency



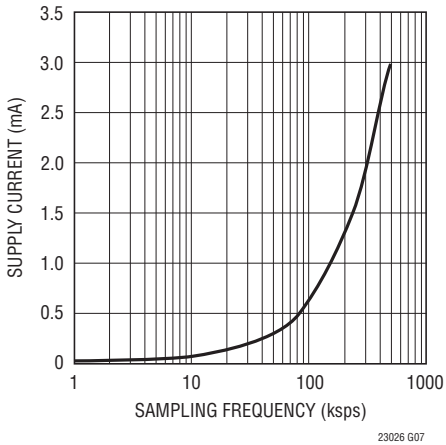
SINAD vs Input Frequency



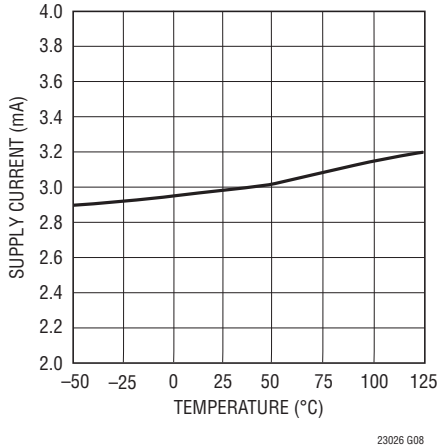
THD vs Input Frequency



Supply Current vs Sampling Frequency



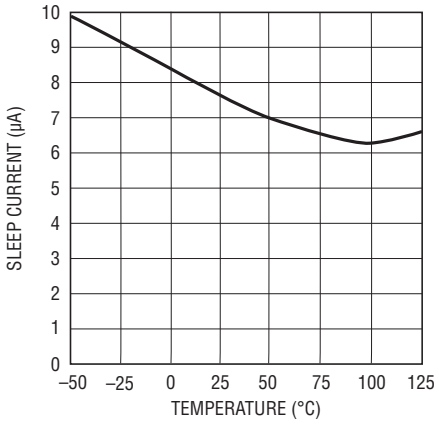
Supply Current vs Temperature



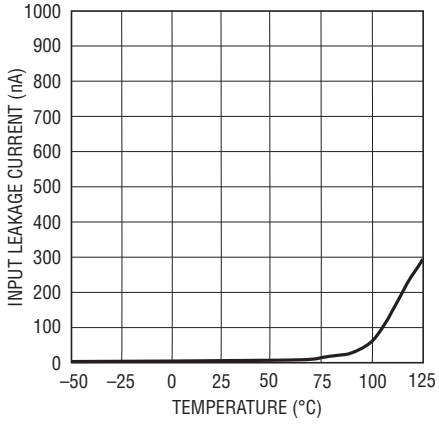
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2302) T_A = 25°C, V_{DD} = OV_{DD} = 5V, V_{REF} = 4.096V, f_{SMPL} = 500ksps, unless otherwise noted.

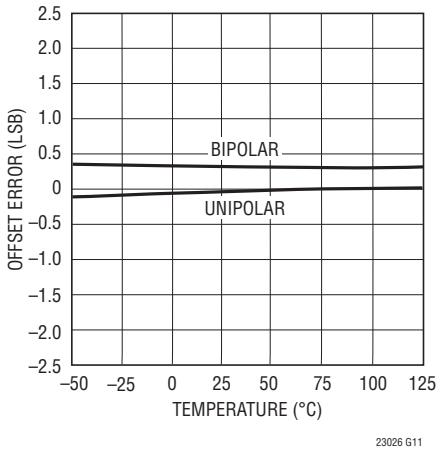
Sleep Current vs Temperature



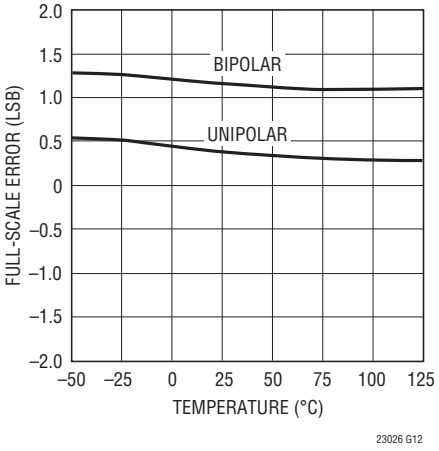
Analog Input Leakage Current vs Temperature



Offset Error vs Temperature



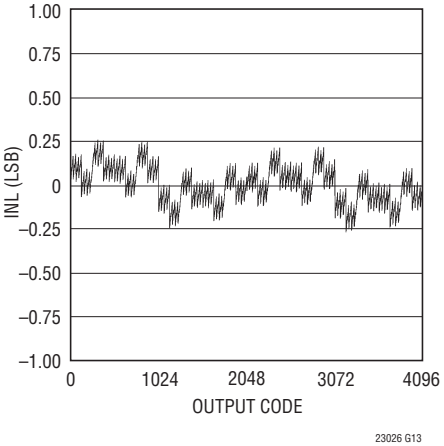
Full-Scale Error vs Temperature



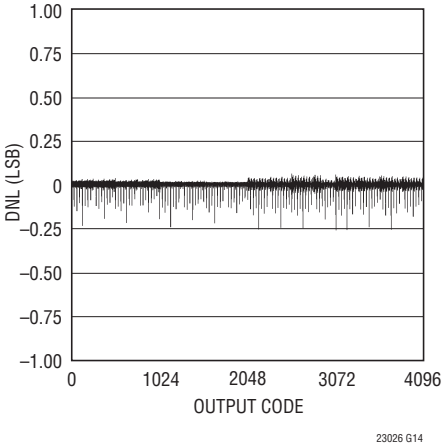
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2306) T_A = 25°C, V_{DD} = OV_{DD} = 5V, V_{REF} = 4.096V, f_{SMPL} = 500ksps, unless otherwise noted.

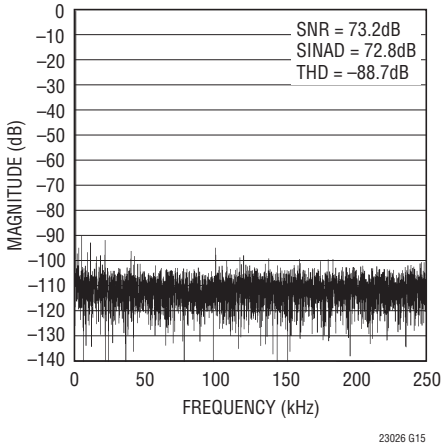
Integral Nonlinearity vs Output Code



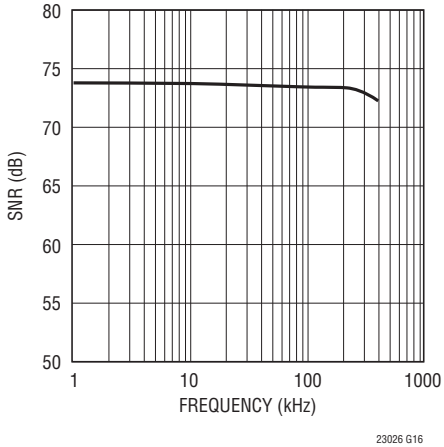
Differential Nonlinearity vs Output Code



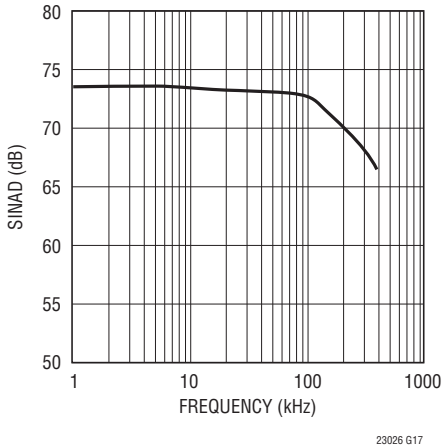
1kHz Sine Wave 8192 Point FFT Plot



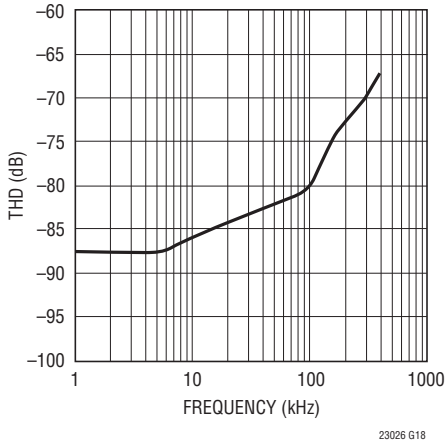
SNR vs Input Frequency



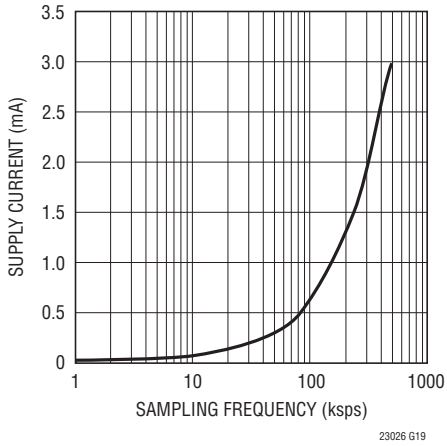
SINAD vs Input Frequency



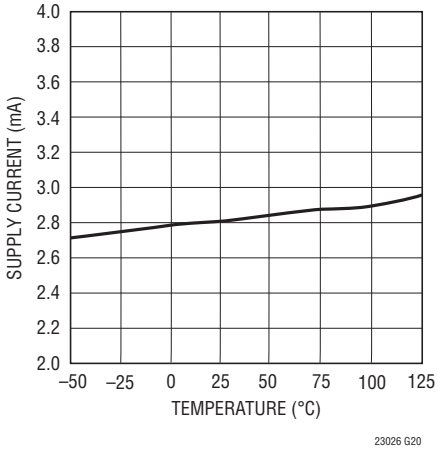
THD vs Input Frequency



Supply Current vs Sampling Frequency



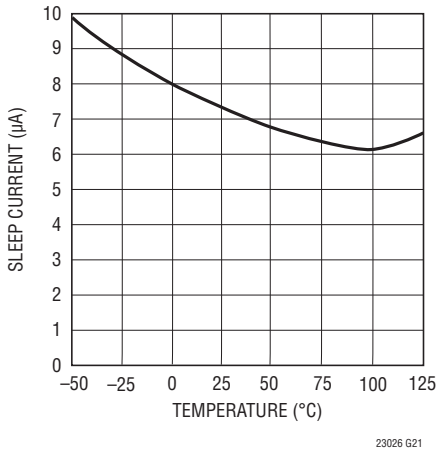
Supply Current vs Temperature



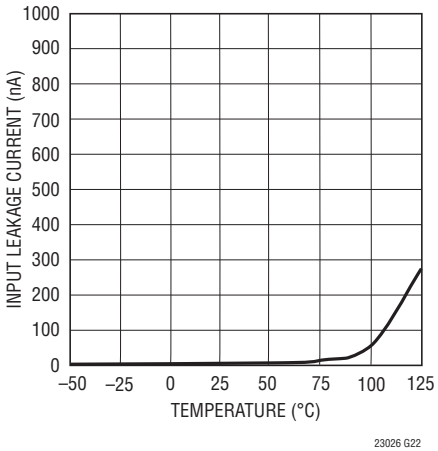
TYPICAL PERFORMANCE CHARACTERISTICS

(LTC2306) T_A = 25°C, V_{DD} = OV_{DD} = 5V, V_{REF} = 4.096V, f_{SMPL} = 500ksps, unless otherwise noted.

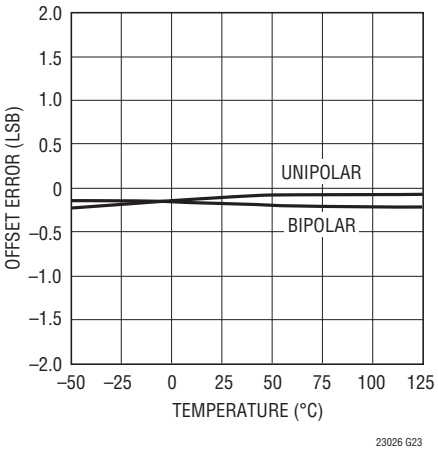
Sleep Current vs Temperature



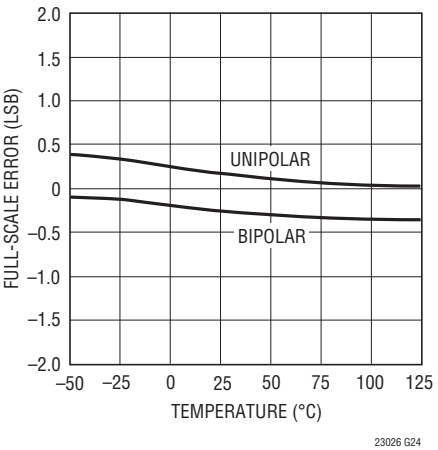
Analog Input Leakage Current vs Temperature



Offset Error vs Temperature



Full-Scale Error vs Temperature



PIN FUNCTIONS

LTC2302

SDO (Pin 1): Three-State Serial Data Out. SDO outputs the data from the previous conversion. SDO is shifted out serially on the falling edge of each SCK pulse. SDO is enabled by a low level on CONVST.

CONVST (Pin 2): Conversion Start. A rising edge at CONVST begins a conversion. For best performance, ensure that CONVST returns low within 40ns after the conversion starts or after the conversion ends.

V_{DD} (Pin 3): 5V Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor in parallel.

IN^+, IN^- (Pin 4, Pin 5): Positive (IN^+) and Negative (IN^-) Differential Analog Inputs.

V_{REF} (Pin 6): Reference Input. Connect an external reference at V_{REF}. The range of the external reference is 0.1V to V_{DD}. Bypass to GND with a minimum 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor.

GND (Pin 7): Ground. All GND pins must be connected to a solid ground plane.

SDI (Pin 8): Serial Data Input. The SDI serial bit stream configures the ADC and is latched on the rising edge of the first 6 SCK pulses.

SCK (Pin 9): Serial Data Clock. SCK synchronizes the serial data transfer. The serial data input at SDI is latched on the rising edge of SCK. The serial data output at SDO transitions on the falling edge of SCK.

OV_{DD} (Pin 10): Output Driver Supply. Bypass OV_{DD} to GND with a 0.1µF ceramic capacitor close to the pin. The range of OV_{DD} is 2.7V to 5.25V.

Exposed Pad (Pin 11): Exposed Pad Ground. Must be soldered directly to ground plane.

LTC2306

SDO (Pin 1): Three-State Serial Data Out. SDO outputs the data from the previous conversion. SDO is shifted out serially on the falling edge of each SCK pulse. SDO is enabled by a low level on CONVST.

CONVST (Pin 2): Conversion Start. A rising edge at CONVST begins a conversion. For best performance, ensure that CONVST returns low within 40ns after the conversion starts or after the conversion ends.

V_{DD} (Pin 3): 5V Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} to GND with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor in parallel.

CH0, CH1 (Pin 4, Pin 5): Channel 0 and Channel 1 Analog Inputs. CH0, CH1 can be configured as single-ended or differential input channels. See the Analog Input Multiplexer section.

V_{REF} (Pin 6): Reference Input. Connect an external reference at V_{REF}.The range of the external reference is 0.1V to V_{DD}. Bypass to GND with a minimum 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor.

GND (Pin 7): Ground. All GND pins must be connected to a solid ground plane.

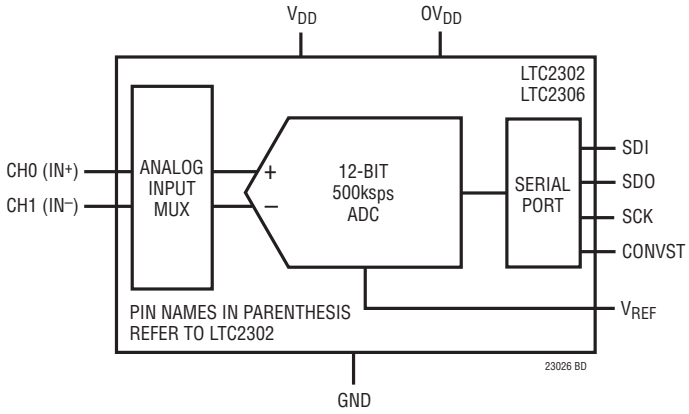
SDI (Pin 8): Serial Data Input. The SDI serial bit stream configures the ADC and is latched on the rising edge of the first 6 SCK pulses.

SCK (Pin 9): Serial Data Clock. SCK synchronizes the serial data transfer. The serial data input at SDI is latched on the rising edge of SCK. The serial data output at SDO transitions on the falling edge of SCK.

OV_{DD} (Pin 10): Output Driver Supply. Bypass OV_{DD} to OGND with a 0.1µF ceramic capacitor close to the pin. The range of OV_{DD} is 2.7V to 5.5V.

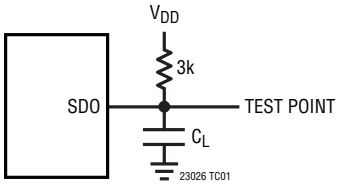
Exposed Pad (Pin 11): Exposed Pad Ground. Must be soldered directly to ground plane.

BLOCK DIAGRAM

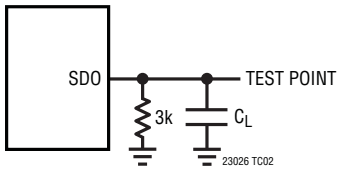


TEST CIRCUITS

Load Circuit for t_{dis} Waveform 1

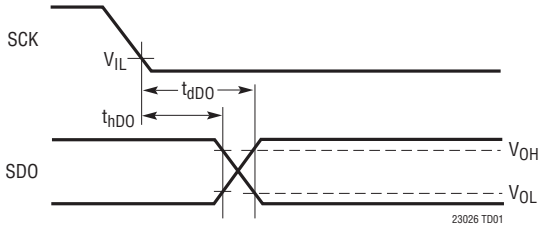


Load Circuit for t_{dis} Waveform 2, t_{en}

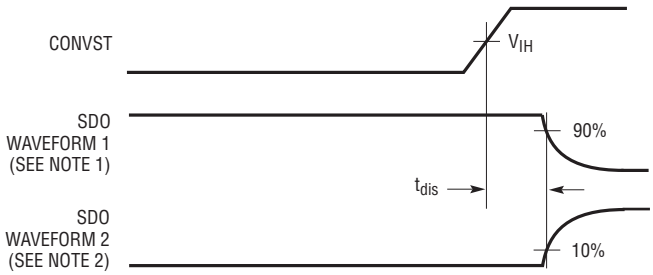


TIMING DIAGRAMS

Voltage Waveforms for SDO Delay Times, t_{dDO} and t_{hDO}



Voltage Waveforms for t_{dis}



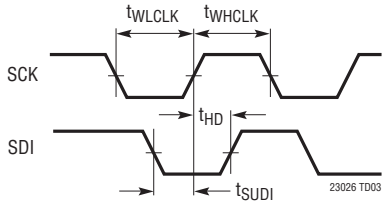
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

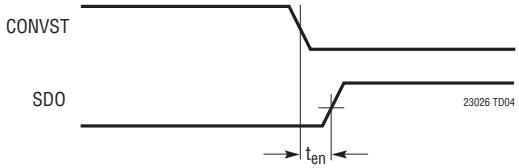
23026 TD02

TIMING DIAGRAMS

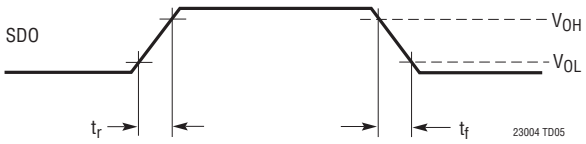
t_{WLCLK} (SCK Low Time)
t_{WHCLK} (SCK High Time)
t_{HD} (Hold Time SDI After SCK↑)
t_{SUDI} (Setup Time SDI Stable Before SCK↑)



Voltage Waveforms for t_{en}



Voltage Waveforms for SDO Rise and Fall Times t_r, t_f



APPLICATIONS INFORMATION

Overview

The LTC2302/LTC2306 are low noise, 500ksps, 1-/2-channel, 12-bit successive approximation register (SAR) A/D converters. The LTC2306 includes a 2-channel analog input multiplexer (MUX) while the LTC2302 includes an input MUX that allows the polarity of the differential input to be selected. Both ADCs include an SPI-compatible serial port for easy data transfers and can operate in either unipolar or bipolar mode. Unipolar mode should be used for single-ended operation with the LTC2306, since single-ended input signals are always referenced to GND. The LTC2302/LTC2306 can be put into a power-down sleep mode during idle periods to save power.

Conversions are initiated by a rising edge on the CONVST input. Once a conversion cycle has begun, it cannot be restarted. Between conversions, a 6-bit input word (D_{IN}) at the SDI input configures the MUX and programs various modes of operation. As the D_{IN} bits are shifted in, data from the previous conversion is shifted out on SDO. After the 6 bits of the D_{IN} word have been shifted in, the ADC begins acquiring the analog input in preparation for the next conversion as the rest of the data is shifted out.

The acquire phase requires a minimum time of 240ns for the sample-and-hold capacitors to acquire the analog input signal.

During the conversion, the internal 12-bit capacitive charge-redistribution DAC output is sequenced through a successive approximation algorithm by the SAR starting from the most significant bit (MSB) to the least significant bit (LSB). The sampled input is successively compared with binary weighted charges supplied by the capacitive DAC using a differential comparator. At the end of a conversion, the DAC output balances the analog input. The SAR contents (a 12-bit data word) that represent the sampled analog input are loaded into 12 output latches that allow the data to be shifted out.

Programming the LTC2306 and LTC2302

The software compatible LTC2302/LTC2306/LTC2308 family features a 6-bit D_{IN} word to program various modes of operation. Don't care bits (X) are ignored. The SDI data bits are loaded on the rising edge of SCK, with the S/D bit loaded on the first rising edge (see Figure 6 in the Timing

APPLICATIONS INFORMATION

and Control section). The input data word for the LTC2306 is defined as follows:

S/D	O/S	X	X	UNI	X

S/D = SINGLE-ENDED/$\overline{\text{DIFFERENTIAL}}$ BIT

O/S = ODD/$\overline{\text{SIGN}}$ BIT

UNI = UNIPOLAR/$\overline{\text{BIPOLAR}}$ BIT

X = DON'T CARE

For the LTC2302, the input data word is defined as:

X	O/S	X	X	UNI	X

Analog Input Multiplexer

The analog input MUX is programmed by the S/D and O/S bits of the D_{IN} word for the LTC2306 and the O/S bit of the D_{IN} word for the LTC2302. Table 1 and Table 2 list MUX configurations for all combinations of the configuration bits. Figure 1a shows several possible MUX configurations and Figure 1b shows how the MUX can be reconfigured from one conversion to the next.

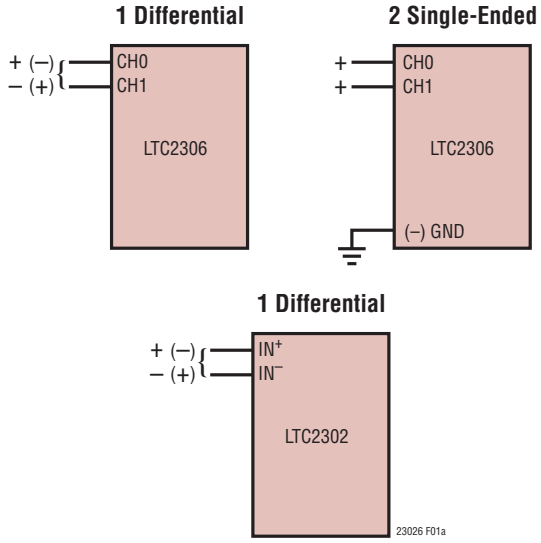


Figure 1a. Example MUX Configurations

Table 1. Channel Configuration for the LTC2306

S/D	O/S	CH0	CH1	
0	0	+	–	
0	1	–	+	
1	0	+		WITH RESPECT TO GND
1	1		+	

NOTE: UNIPOLAR MODE SHOULD BE USED FOR SINGLE-ENDED OPERATION, SINCE INPUT SIGNALS ARE ALWAYS REFERENCED TO GND

Table 2. Channel Configuration for the LTC2302

O/S	IN+	IN–
0	+	–
1	–	+

Driving the Analog Inputs

The analog inputs of the LTC2302/LTC2306 are easy to drive. Each of the analog inputs of the LTC2306 (CH0 and CH1) can be used as a single-ended input relative to GND or as a differential pair. The analog inputs of the LTC2302 (IN+, IN–) are always configured as a differential pair. Regardless of the MUX configuration, the "+" and "–" inputs are sampled at the same instant. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while

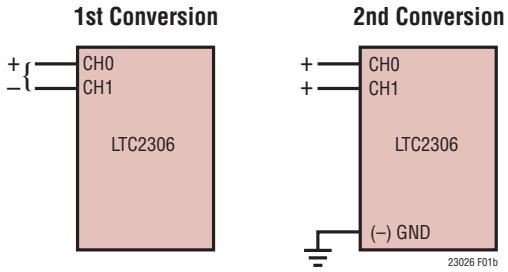


Figure 1b. Changing the MUX Assignment "On the Fly"

APPLICATIONS INFORMATION

charging the sample-and-hold capacitors during the acquire mode. In conversion mode, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, the ADC inputs can be driven directly. Otherwise, more acquisition time should be allowed for a source with higher impedance.

Reference

A low noise, stable reference is required to ensure full performance. The LT®1790 and LT6660 are adequate for most applications. The LT6660 is available in 2.5V, 3V, 3.3V and 5V versions, and the LT1790 is available in 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V and 5V versions. The exceptionally low input noise allows the input range to be optimized for the application by changing the reference voltage. The V_{REF} input must be decoupled with a 10µF capacitor in parallel with a 0.1µF capacitor, so verify that the device providing the reference voltage is stable with capacitive loads.

If the voltage reference is 5V and can supply 5mA, it can be used for both V_{REF} and V_{DD}. V_{DD} must be connected to a clean analog supply, and a quiet 5V reference voltage makes a convenient supply for this purpose.

Input Filtering

The noise and distortion of the input amplifier and other circuitry must be considered since they will add to the ADC noise and distortion. Therefore, noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

The analog inputs of the LTC2302/LTC2306 can be modeled as a 55pF capacitor (C_{IN}) in series with a 100Ω resistor (R_{ON}) as shown in Figure 2a. C_{IN} gets switched to the selected input once during each conversion. Large filter RC time constants will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle to 12-bit resolution within the acquisition time (t_{ACQ}) if DC accuracy is important.

When using a filter with a large C_{FILTER} value (e.g., 1µF), the inputs do not completely settle and the capacitive input switching currents are averaged into a net DC current (I_{DC}). In this case, the analog input can be modeled by an equivalent resistance ($R_{EQ} = 1/(f_{SMPL} \bullet C_{IN})$) in series with an ideal voltage source ($V_{REF}/2$) as shown in Figure 2b. The magnitude of the DC current is then approximately $I_{DC} = (V_{IN} – V_{REF}/2)/R_{EQ}$, which is roughly proportional to V_{IN}. To prevent large DC drops across the resistor R_{FILTER}, a filter with a small resistor and large capacitor should be chosen. When running at the minimum cycle time of 2µs, the input current equals 106µA at V_{IN} = 5V, which amounts to a full-scale error of 0.5LSB when using a filter resistor (R_{FILTER}) of 4.7Ω. Applications requiring lower sample rates can tolerate a larger filter resistor for the same amount of full-scale error.

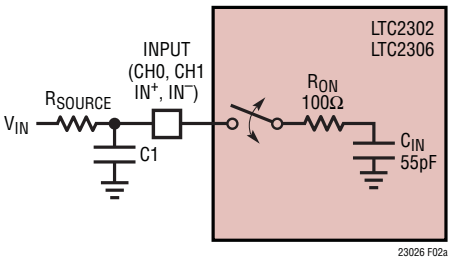


Figure 2a. Analog Input Equivalent Circuit

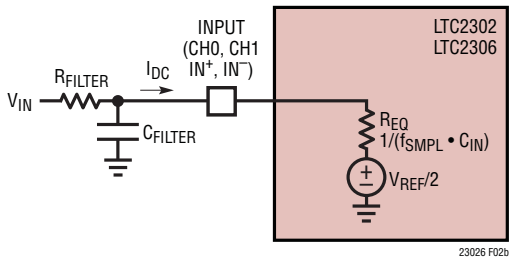


Figure 2b. Analog Input Equivalent Circuit for Large Filter Capacitances

APPLICATIONS INFORMATION

Figures 3a and 3b show respective examples of input filtering for single-ended and differential inputs. For the single-ended case in Figure 3a, a 50Ω source resistor and a 2000pF capacitor to ground on the input will limit the input bandwidth to 1.6MHz. High quality capacitors and resistors should be used in the RC filter since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Dynamic Performance

FFT (fast fourier transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental.

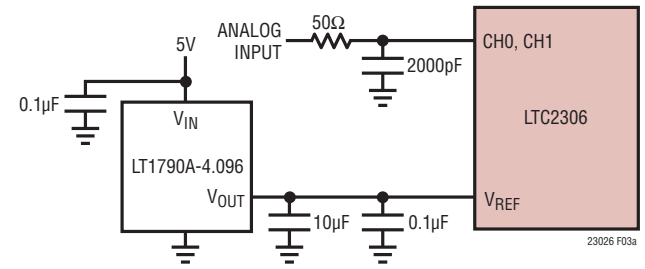


Figure 3a. Optional RC Input Filtering for Single-Ended Input

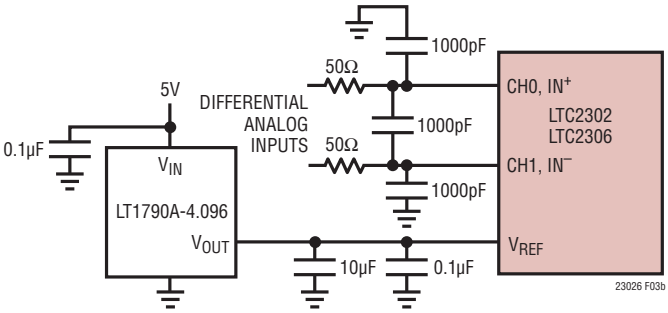


Figure 3b. Optional RC Input Filtering for Differential Inputs

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 4 shows a typical SINAD of 72.8dB with a 500kHz sampling rate and a 1kHz input. A SNR of 73.2dB can be achieved with the LTC2302/LTC2306.

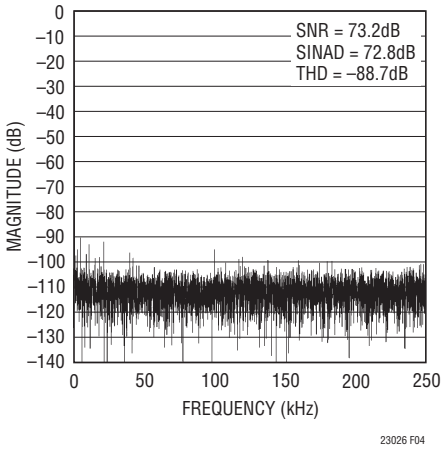


Figure 4. 1kHz Sine Wave 8192 Point FFT Plot (LTC2306)

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

APPLICATIONS INFORMATION

Internal Conversion Clock

The internal conversion clock is factory trimmed to achieve a typical conversion time (t_{CONV}) of 1.3µs and a maximum conversion time of 1.6µs over the full operating temperature range. With a minimum acquisition time of 240ns, a throughput sampling rate of 500ksps is tested and guaranteed.

Digital Interface

The LTC2302/LTC2306 communicate via a standard 4-wire SPI compatible digital interface. The rising edge of CONVST initiates a conversion. After the conversion is finished, pull CONVST low to enable the serial output (SDO). The ADC then shifts out the digital data in 2's complement format when operating in bipolar mode or in straight binary format when in unipolar mode, based on the setting of the UNI bit.

For best performance, ensure that CONVST returns low within 40ns after the conversion starts (i.e., before the first bit decision) or after the conversion ends. If CONVST is low when the conversion ends, the MSB bit will appear at SDO at the end of the conversion and the ADC will remain powered up.

Timing and Control

The start of a conversion is triggered by the rising edge of CONVST. Once initiated, a new conversion cannot be restarted until the current conversion is complete. Figures 6 and 7 show the timing diagrams for two different examples of CONVST pulses. Example 1 (Figure 6) shows CONVST staying HIGH after the conversion ends. If CONVST is high after the t_{CONV} period, the LTC2302/LTC2306 enter sleep mode (see Sleep Mode for more details).

When CONVST returns low, the ADC wakes up and the most significant bit (MSB) of the output data sequence at SDO becomes valid after the serial data bus is enabled. All other data bits from SDO transition on the falling edge of each SCK pulse. Configuration data (D_{IN}) is loaded into the LTC2302/LTC2306 at SDI, starting with the first SCK rising edge after CONVST returns low. The S/D bit is loaded on the first SCK rising edge.

Example 2 (Figure 7) shows CONVST returning low before the conversion ends. In this mode, the ADC and all internal circuitry remain powered up. When the conversion is complete, the MSB of the output data sequence at SDO becomes valid after the data bus is enabled. At this point(t_{CONV} 1.3µs after the rising edge of CONVST), pulsing SCK will shift data out at SDO and load configuration data (D_{IN}) into the LTC2302/LTC2306 at SDI. The first SCK rising edge loads the S/D bit. SDO transitions on the falling edge of each SCK pulse.

Figures 8 and 9 are the transfer characteristics for the bipolar and unipolar modes. Data is output at SDO in 2's complement format for bipolar readings or in straight binary for unipolar readings.

Sleep Mode

The ADC enters sleep mode when CONVST is held high after the conversion is complete (t_{CONV}). The supply current decreases to 7µA in sleep mode between conversions, thereby reducing the average power dissipation as the sample rate decreases. For example, the LTC2302/LTC2306 draw an average of 14µA with a 1ksps sampling rate. The LTC2302/LTC2306 power down all circuitry when in sleep mode.

Board Layout and Bypassing

To obtain the best performance, a printed circuit board with a solid ground plane is required. Layout for the printed circuit board should ensure digital and analog signal lines are separated as much as possible. Care should be taken not to run any digital signal alongside an analog signal. All analog inputs should be shielded by GND. V_{REF} and V_{DD} should be bypassed to the ground plane as close to the pin as possible. Maintaining a low impedance path for the common return of these bypass capacitors is essential to the low noise operation of the ADC. These traces should be as wide as possible. See Figure 5 for a suggested layout.

APPLICATIONS INFORMATION

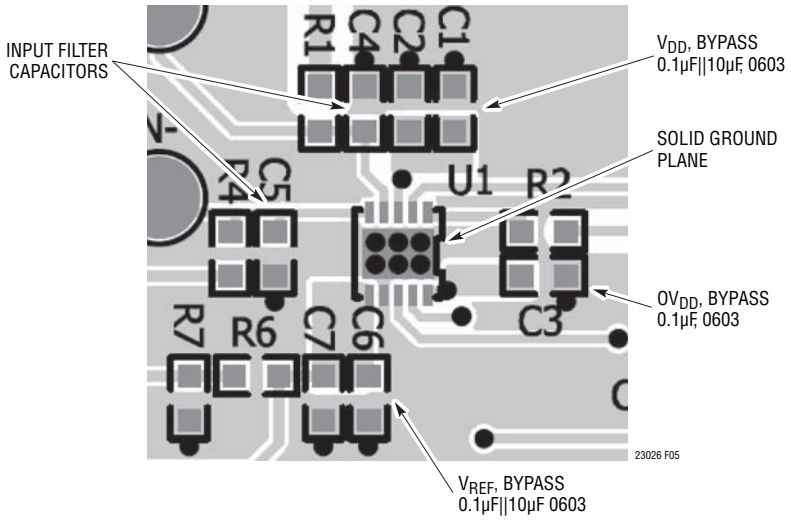


Figure 5. Suggested Layout

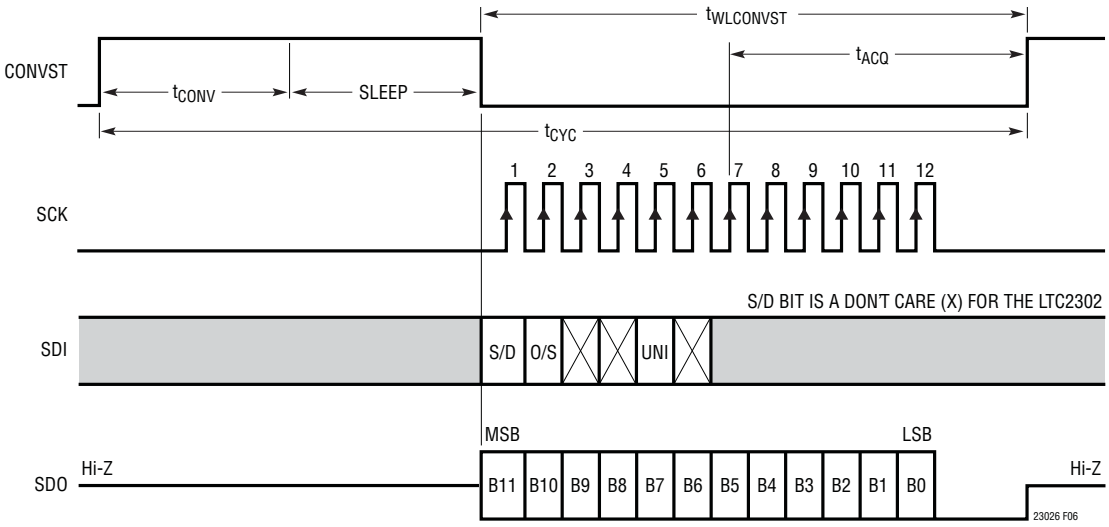


Figure 6. LTC2302/LTC2306 Timing with a Long CONVST Pulse

APPLICATIONS INFORMATION

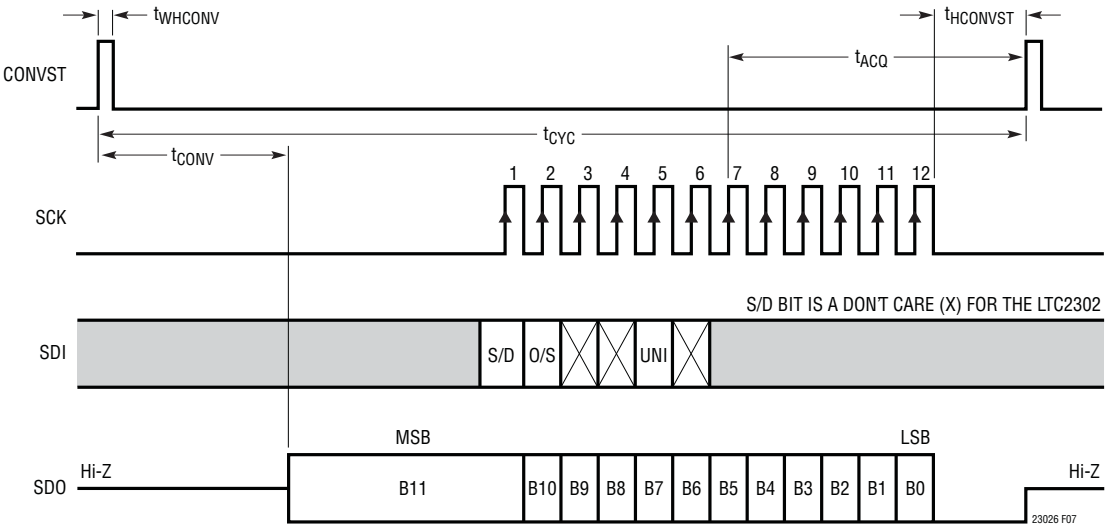


Figure 7. LTC2302/LTC2306 Timing with a Short CONVST Pulse

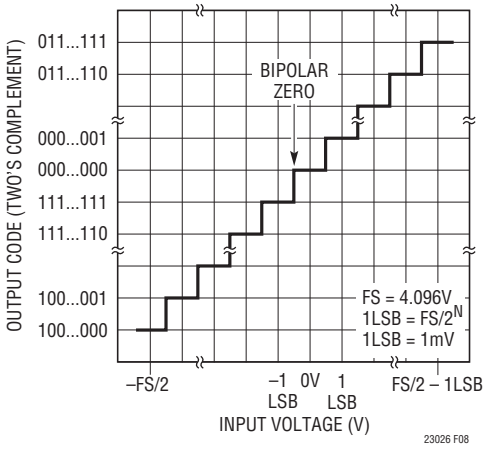


Figure 8. LTC2302/LTC2306 Bipolar Transfer Characteristics (2's Complement)

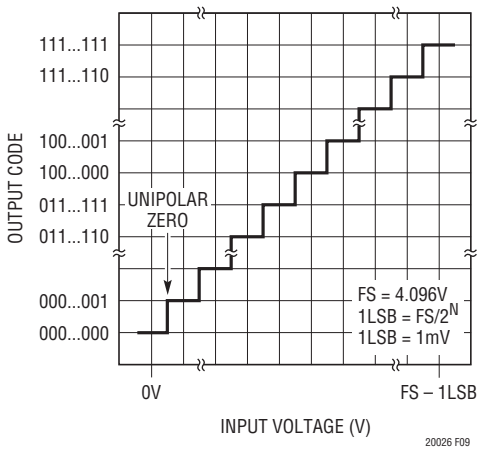
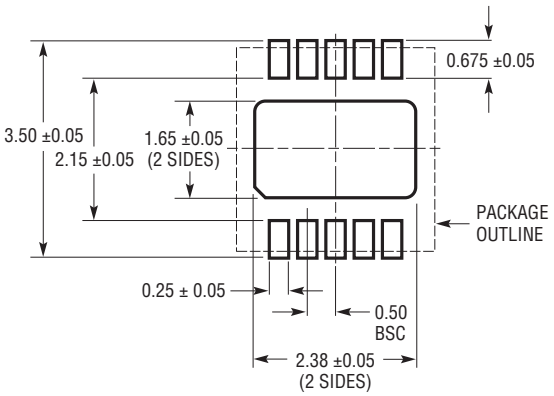


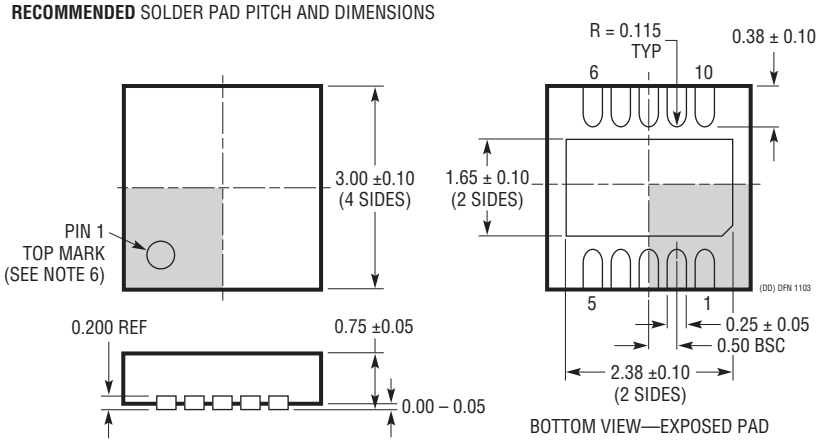
Figure 9. LTC2302/LTC2306 Unipolar Transfer Characteristics (Straight Binary)

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

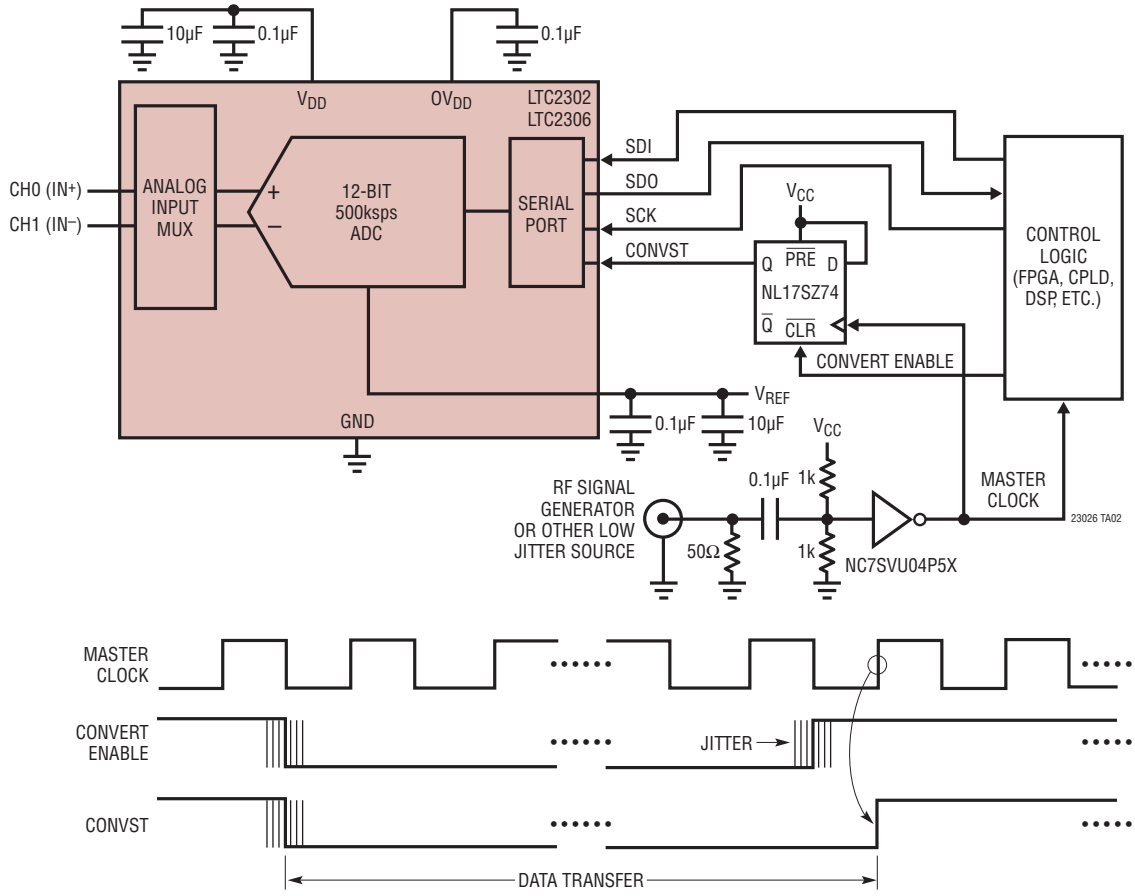


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Clock Squaring/Level Shifting Circuit Allows Testing with RF Sine Generator, Convert Re-Timing Flip-Flop Preserves Low Jitter Clock Timing



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1417	14-Bit, 400ksps Serial ADC	20mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1468/LT1469	Single/Dual 90MHz, 22V/µs, 16-Bit Accurate Op Amps	Low Input Offset: 75µV/125µV
LTC1609	16-Bit, 200ksps Serial ADC	65mW, Configurable Bipolar and Unipolar Input Ranges, 5V Supply
LTC1790	Micropower Low Dropout Reference	60µA Supply Current, 10ppm/°C, SOT-23 Package
LTC1850/LTC1851	10-Bit/12-Bit, 8-channel, 1.25Msps ADCs	Parallel Output, Programmable MUX and Sequencer, 5V Supply
LTC1852/LTC1853	10-Bit/12-Bit, 8-channel, 400ksps ADCs	Parallel Output, Programmable MUX and Sequencer, 3V or 5V Supply
LTC1860/LTC1861	12-Bit, 1-/2-Channel 250ksps ADCs in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	3V, 12-bit, 1-/2-Channel 150ksps ADCs	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC1863/LTC1867	12-/16-Bit, 8-Channel 200ksps ADCs	6.5mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1863L/LTC1867L	3V, 12-/16-bit, 8-Channel 175ksps ADCs	2mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LTC1864/LTC1865	16-Bit, 1-/2-Channel 250ksps ADCs in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	3V, 16-Bit, 1-/2-Channel 150ksps ADCs in MSOP	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC2308	12-Bit, 8-Channel 500ksps ADC	5V, Internal Reference, 4mm × 4mm QFN Packages

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