Complete SO-8, 12-Bit, 600ksps ADC with Shutdown

FEATURES

- **Complete 12-Bit ADC in SO-8**
- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 600ksps**
- Power Dissipation: 75mW (Typ)
- 72dB S/(N + D) and –80dB THD at Nyquist
- No Missing Codes over Temperature
- Nap Mode with Instant Wake-Up: 7.5mW
- Sleep Mode: 60µW
- High Impedance Analog Input
- Input Range (1mV/LSB): 0V to 4.096V or ±2.048V
- Internal Reference Can Be Overdriven Externally
- 3-Wire Interface to DSPs and Processors (SPI and MICROWIRE™ Compatible)

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Digital Radio
- Spectrum Analysis
- Low Power and Battery-Operated Systems
- Handheld or Portable Instruments

DESCRIPTION

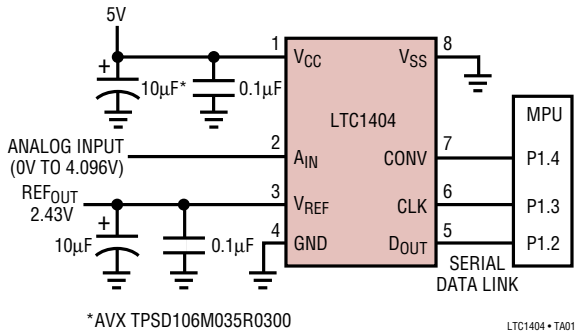
The LTC®1404 is a complete 600ksps, 12-bit A/D converter which draws only 75mW from a 5V or ± 5V supplies. This easy-to-use device comes complete with a 160ns sample-and-hold and a precision reference. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The LTC1404 has two power saving modes: Nap and Sleep. In Nap mode, it consumes only 7.5mW of power and can wake up and convert immediately. In the Sleep mode, it consumes 60µW of power typically. Upon power-up from Sleep mode, a reference ready (REFRDY) signal is available in the serial data word to indicate that the reference has settled and the chip is ready to convert.

The LTC1404 converts 0V to 4.096V unipolar inputs from a single 5V supply and ±2.048V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL, ±1LSB DNL and 45ppm/°C full-scale drift over temperature. Guaranteed AC performance includes 69dB S/(N + D) and –76dB THD at an input frequency of 100kHz over temperature.

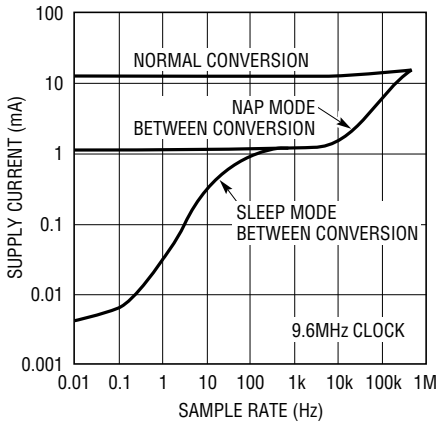
The 3-wire serial port allows compact and efficient data transfer to a wide range of microprocessors, microcontrollers and DSPs.

TYPICAL APPLICATION

Single 5V Supply, 600kHz, 12-Bit Sampling A/D Converter



Power Consumption vs Sample Rate

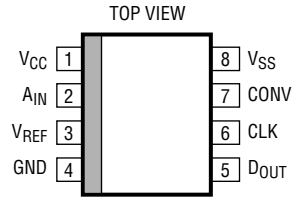


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Negative Supply Voltage (V_{SS}) ..... –6V to GND
Total Supply Voltage (V_{CC} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... –0.3V to (V_{CC} + 0.3V)
  Bipolar Operation ..... (V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Digital Input Voltage (Note 4)
  Unipolar Operation ..... –0.3V to 12V
  Bipolar Operation ..... (V_{SS} – 0.3V) to 12V
Digital Output Voltage
  Unipolar Operation ..... –0.3V to (V_{CC} + 0.3V)
  Bipolar Operation ..... (V_{SS} – 0.3V) to (V_{CC} + 0.3V)
Power Dissipation 300mW
Operating Ambient Temperature Range
  LTC1404C ..... 0°C to 70°C
  LTC1404I ..... –40°C to 85°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1404CS8 LTC1404IS8
S8 PART MARKING
1404 1404I

Consult factory for PDIP packages and Military grade parts.

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	Unipolar Bipolar		4.75 4.75		5.25 5.25	V V
V_{SS}	Negative Supply Voltage	Bipolar Only		–2.45		–5.25	V
I_{CC}	Positive Supply Current	f_{SAMPLE} = 600ksps Nap Mode Sleep Mode	● ● ●		15 1.3 8.0	30 3.0 20.0	mA mA µA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 600ksps, V_{SS} = –5V Nap Mode Sleep Mode	● ● ●		0.2 0.2 4	0.6 0.5 10	mA mA µA
P_D	Power Dissipation	f_{SAMPLE} = 600ksps Nap Mode Sleep Mode	● ● ●		75 7.5 60	160 20 150	mW mW µW

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range	4.75V ≤ V_{CC} ≤ 5.25V (Unipolar) 4.75V ≤ V_{CC} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –2.45V (Bipolar)			0 to 4.096 0 to ±2.048		V V
I_{IN}	Analog Input Leakage Current	During Conversions (Hold Mode)	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			45 5		pF pF

CONVERTER CHARACTERISTICS With internal reference (Notes 5, 7)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 8)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Offset Error	(Note 9)	 ●			±6 ±8	LSB LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

DYNAMIC ACCURACY V_{CC} = 5V, V_{SS} = –5V, f_{SAMPLE} = 600kHz

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise	100kHz Input Signal 300kHz Input Signal	●	69	72 72		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	100kHz Input Signal 300kHz Input Signal	●		–82 –80	–76	dB dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal 300kHz Input Signal	●		–84 –82	–76	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 99.17kHz, f_{IN2} = 102.69kHz f_{IN1} = 298.68kHz, f_{IN2} = 304.83kHz			–82 –70		dB dB
	Full Power Bandwidth				5		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)				1		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.410	2.430	2.450	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{CC} ≤ 5.25V –5.25V ≤ V_{SS} ≤ 0V			0.5 0.01		LSB/V LSB/V
V_{REF} Load Regulation	0 ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA			1		LSB/mA
V_{REF} Wake-Up Time from Sleep Mode	C_{VREF} = 10µF			2.5		ms

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = –10µA V_{CC} = 4.75V, I_O = –200µA	 ●	 4.0	4.7		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 160µA V_{CC} = 4.75V, I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V to V_{CC}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT}				15		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			10		mA

TIMING CHARACTERISTICS (Note 5, see Figures 12, 13, 14)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	600			kHz
t_{CONV}	Conversion Time	f_{CLK} = 9.6MHz			1.36		µs
t_{ACQ}	Acquisition Time (Unipolar Mode) (Bipolar Mode V_{SS} = –5V)				200 160		ns ns
f_{CLK}	CLK Frequency		●	0.1		9.6	MHz
t_{CLK}	CLK Pulse Width	(Note 6)	●	40			ns
$t_{WK(NAP)}$	Time to Wake Up from Nap Mode				350		ns
t_1	CLK Pulse Width to Return to Active Mode		●	40			ns
t_2	CONV↑ to CLK↑ Setup Time		●	70			ns
t_3	CONV↑ After Leading CLK↑		●	0			ns
t_4	CONV Pulse Width	(Note 10)	●	40			ns
t_5	Time from CLK↑ to Sample Mode				60		ns
t_6	Aperture Delay of Sample-and-Hold	Jitter < 50ps			40		ns
t_7	Minimum Delay Between Conversion (Unipolar Mode) (Bipolar Mode V_{SS} = –5V)	(Note 6)	● ●		220 180	310 300	ns ns
t_8	Delay Time, CLK↑ to D_{OUT} Valid	C_{LOAD} = 20pF	●		40	70	ns
t_9	Delay Time, CLK↑ to D_{OUT} Hi-Z	C_{LOAD} = 20pF	●		40	70	ns
t_{10}	Time from Previous Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	10	30		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals apply to T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: When these pin voltages are taken below V_{SS} (ground for unipolar mode) or above V_{CC}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA without latch-up if the pin is driven below V_{SS} (ground for unipolar mode) or above V_{CC}.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 60mA without latch-up if the pin is driven below V_{SS} (ground for unipolar mode). These pins are not clamped to V_{CC}.

Note 5: V_{CC} = 5V, f_{SAMPLE} = 600kHz, t_r = t_f = 5ns unless otherwise specified.

Note 6: Guaranteed by design, not subject to test.

Note 7: Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

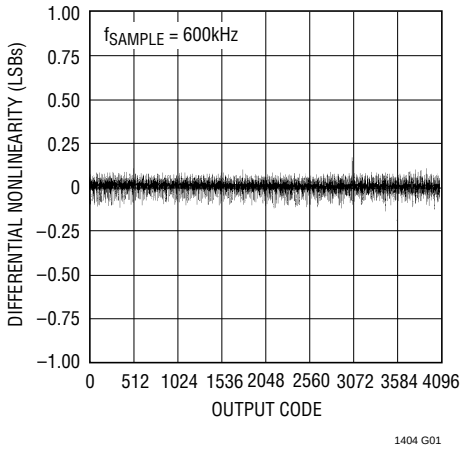
Note 8: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 9: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

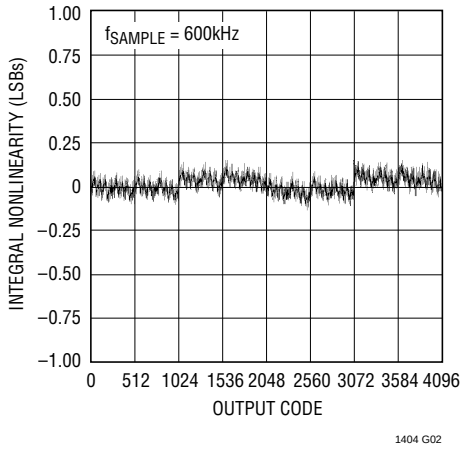
Note 10: The rising edge of CONV starts a conversion. If CONV returns low at a bit decision point during the conversion, it can create small errors. For best performance, ensure that CONV returns low either within 100ns after the conversion starts (i.e., before the first bit decision) or after the 14 clock cycles. (Figure 13 Timing Diagram).

TYPICAL PERFORMANCE CHARACTERISTICS

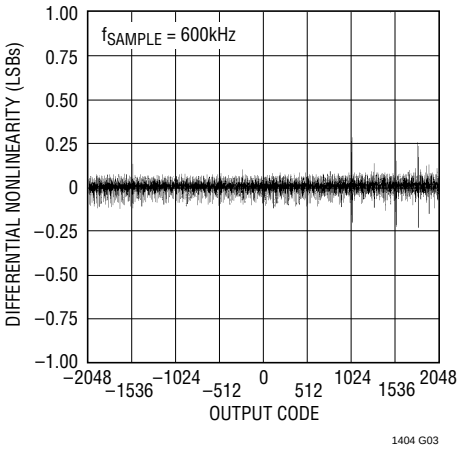
Unipolar Mode Differential Nonlinearity vs Output Code



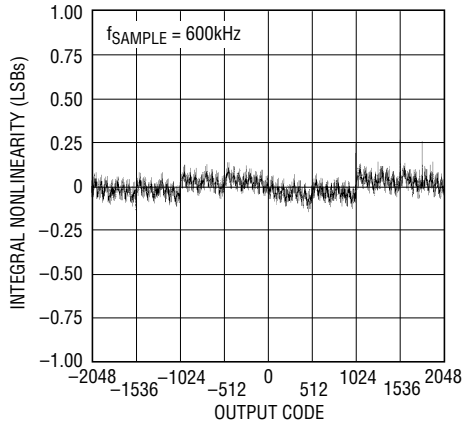
Unipolar Mode Integral Nonlinearity vs Output Code



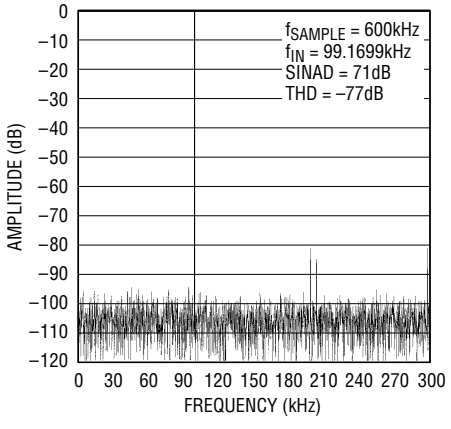
Bipolar Mode Differential Nonlinearity vs Output Code



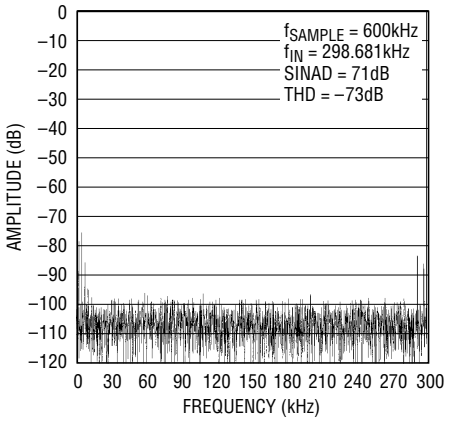
Bipolar Mode Integral Nonlinearity vs Output Code



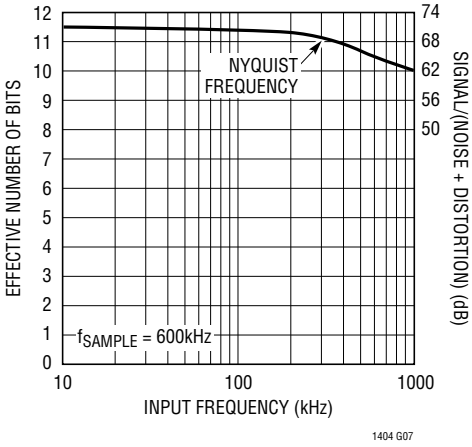
Unipolar Mode 4096 Nonaverage FFT with 100kHz Signal



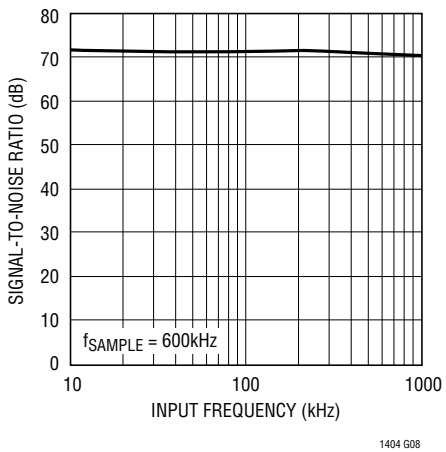
Unipolar Mode 4096 Nonaverage FFT with 300kHz Signal



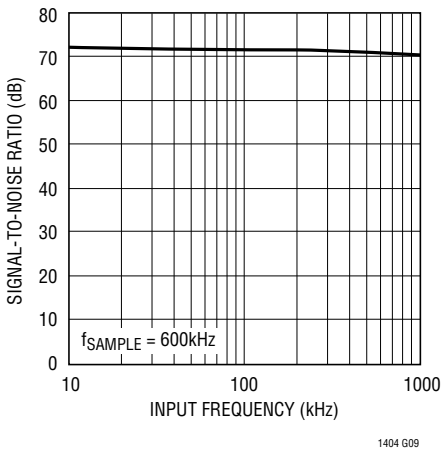
Unipolar Mode ENOB and Signal/(Noise + Distortion) vs Input Frequency



Unipolar Mode Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency

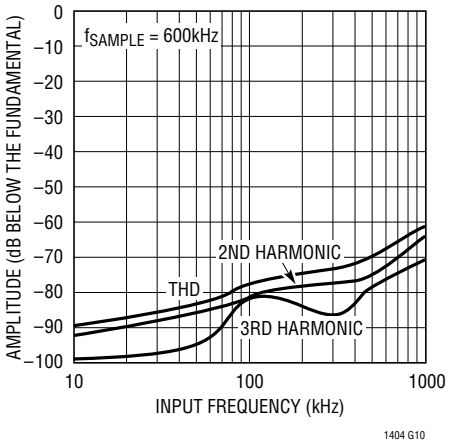


Bipolar Mode Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency

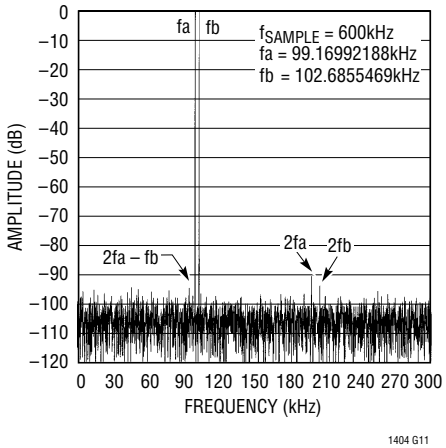


TYPICAL PERFORMANCE CHARACTERISTICS

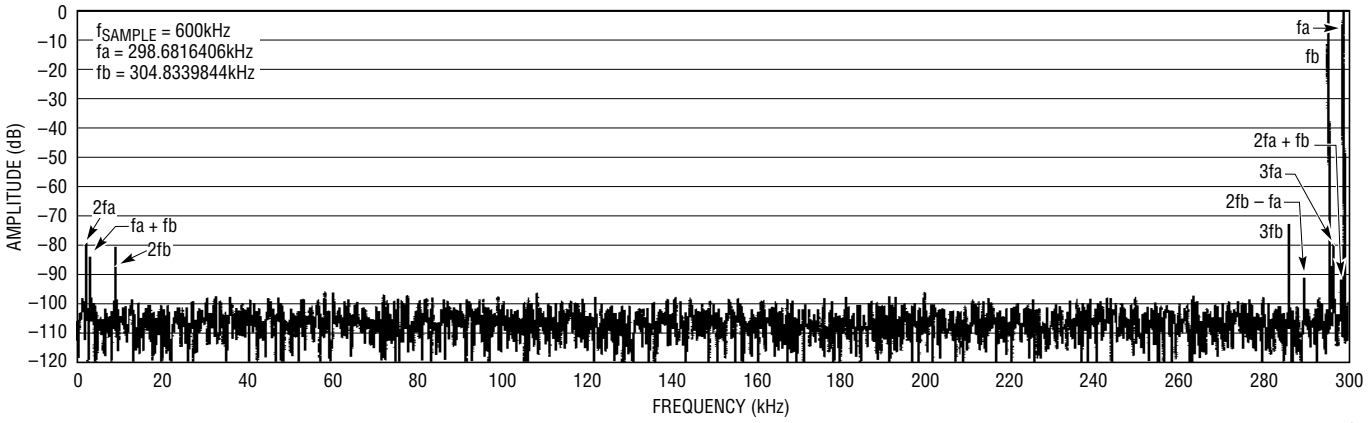
Unipolar Mode Distortion vs Input Frequency



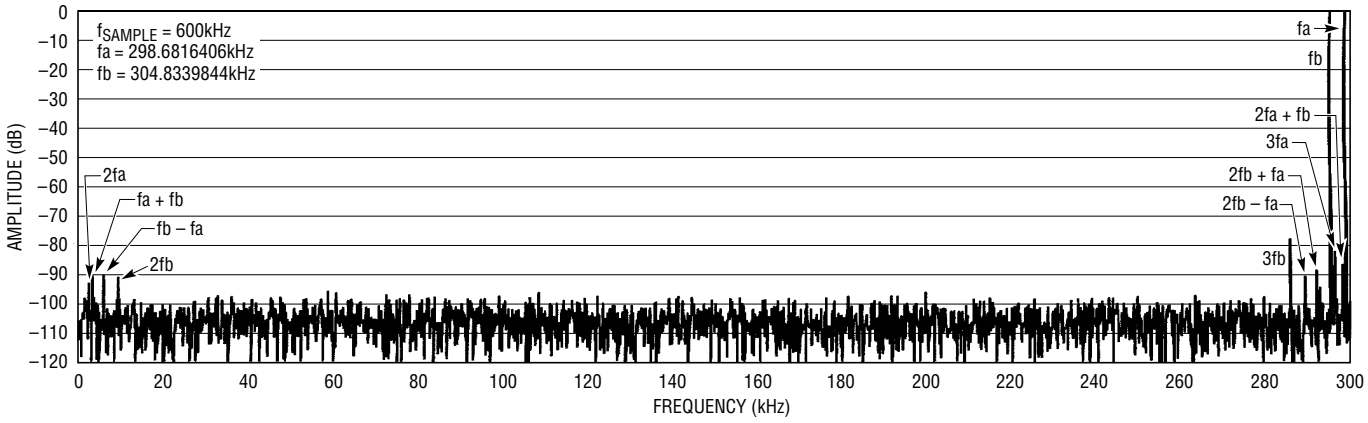
Unipolar Mode Intermodulation Distortion Plot at 100kHz



Unipolar Mode Intermodulation Distortion Plot at 300kHz

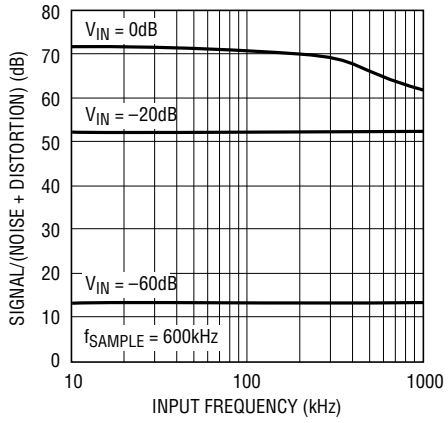


Bipolar Mode Intermodulation Distortion Plot at 300kHz



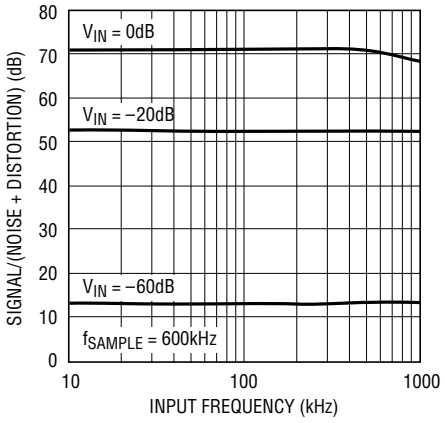
TYPICAL PERFORMANCE CHARACTERISTICS

Unipolar Mode S/(N + D) vs Input Frequency and Amplitude



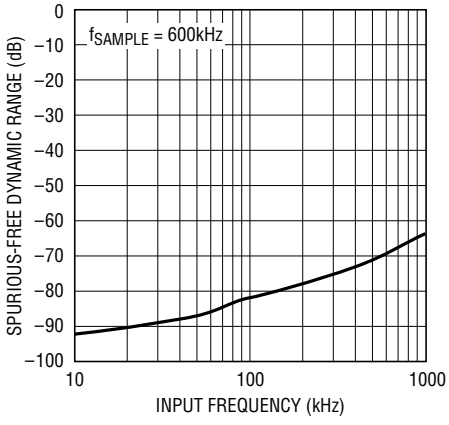
1404 G14

Bipolar Mode S/(N + D) vs Input Frequency and Amplitude



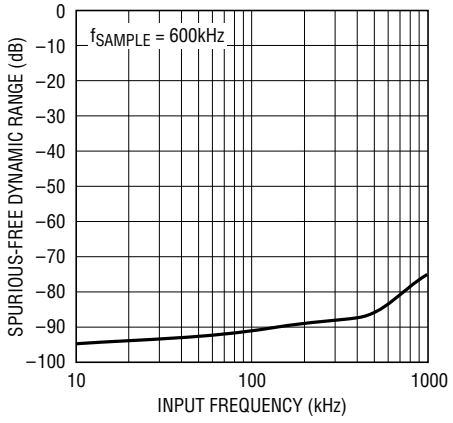
1404 G15

Unipolar Mode Peak Harmonic or Spurious Noise vs Input Frequency



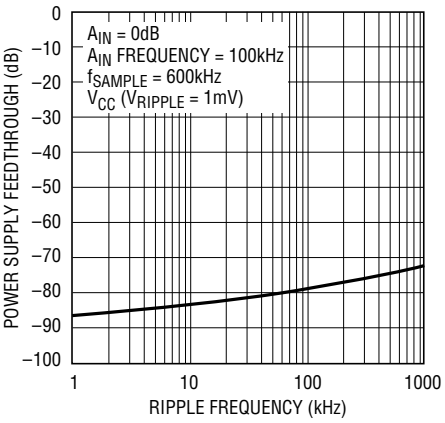
1404 G16

Bipolar Mode Peak Harmonic or Spurious Noise vs Input Frequency



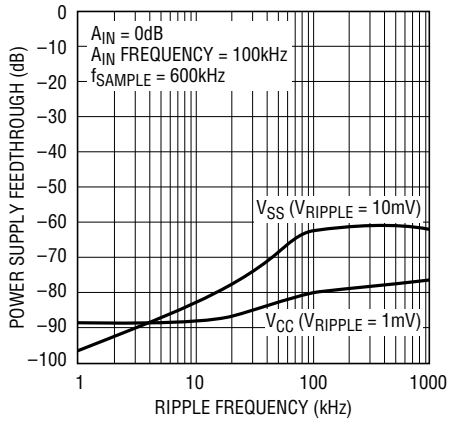
1404 G17

Unipolar Mode Power Supply Feedthrough vs Ripple Frequency



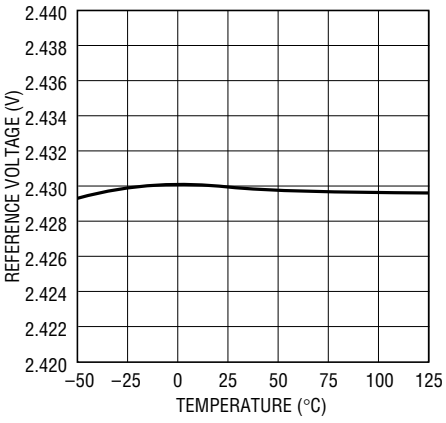
1404 G18

Bipolar Mode Power Supply Feedthrough vs Ripple Frequency



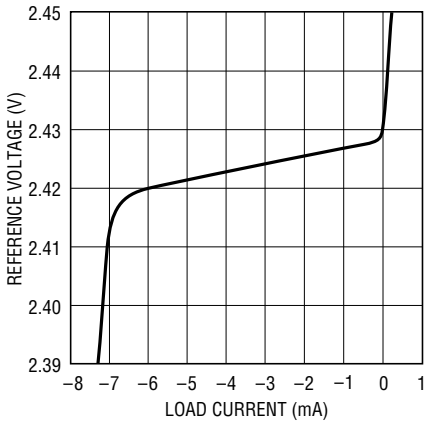
1404 G19

Reference Voltage vs Temperature



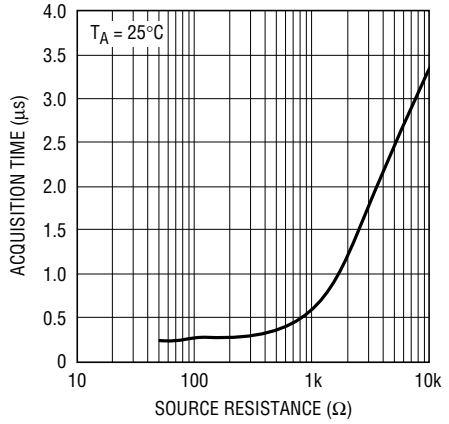
1404 G20

Reference Voltage vs Load Current



1404 G21

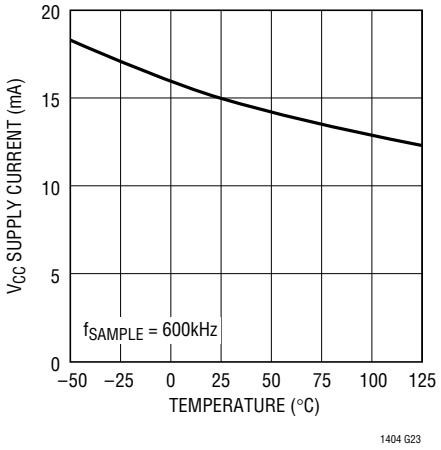
Acquisition Time vs Source Impedance



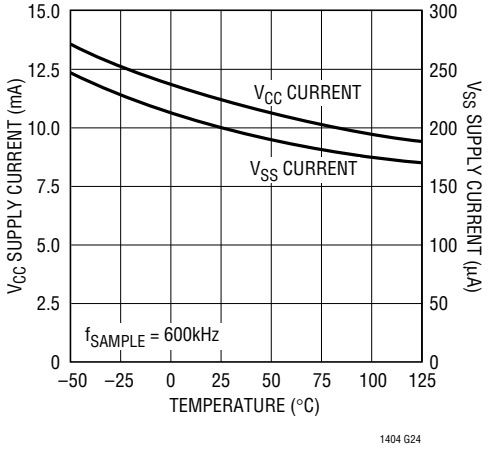
1404 G22

TYPICAL PERFORMANCE CHARACTERISTICS

Unipolar Mode V_{CC} Supply Current vs Temperature



Bipolar Mode Supply Current vs Temperature



PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply, 5V. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

A_{IN} (Pin 2): Analog Input. 0V to 4.096V (Unipolar), ±2.048V (Bipolar).

V_{REF} (Pin 3): 2.43V Reference Output. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 4): Ground. GND should be tied directly to an analog ground plane.

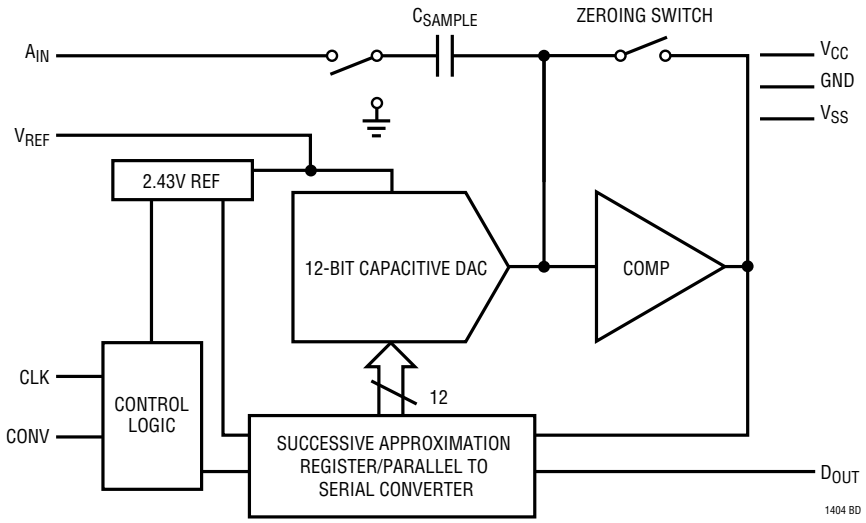
D_{OUT} (Pin 5): The A/D conversion result is shifted out from this pin.

CLK (Pin 6): Clock. This clock synchronizes the serial data transfer. A minimum CLK pulse of 40ns signals the ADC to wake up from Nap or Sleep mode.

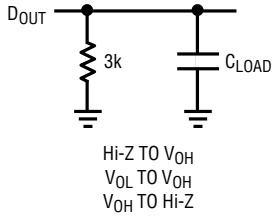
CONV (Pin 7): Conversion Start Signal. This active high signal starts a conversion on its rising edge. Keeping CLK low and pulsing CONV two/four times will put the ADC into Nap/Sleep mode.

V_{SS} (Pin 8): Negative Supply. –5V for bipolar operation. Bypass to GND with 10µF tantalum in parallel with 0.1µF ceramic. V_{SS} should be tied to GND for unipolar operation.

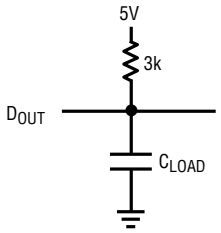
FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS



Hi-Z TO V_{OH}
V_{OL} TO V_{OH}
V_{OH} TO Hi-Z



Hi-Z TO V_{OL}
V_{OH} TO V_{OL}
V_{OL} TO Hi-Z

1404 TC01

APPLICATIONS INFORMATION

Conversion Details

The LTC1404 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit serial output based on a precision internal reference. The control logic provides easy interface to microprocessors and DSPs through 3-wire connections.

A rising edge on the CONV input starts a conversion. At the start of a conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun, it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquired phase and the comparator offset is nulled by the feedback switch. In this acquire phase, it typically takes 160ns for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switches connect C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the input voltage, are presented through the serial pin D_{OUT}.

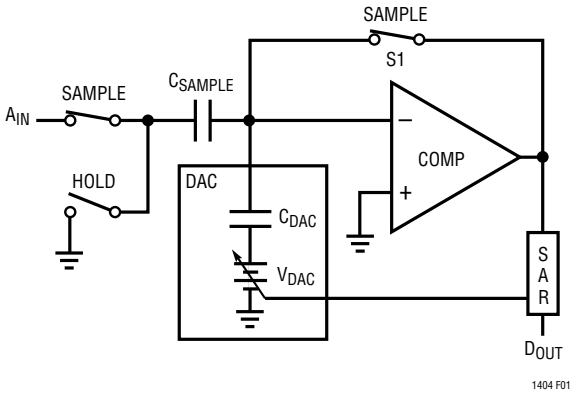


Figure 1. A_{IN} Input

Dynamic Performance

The LTC1404 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2a shows a typical LTC1404 FFT plot.

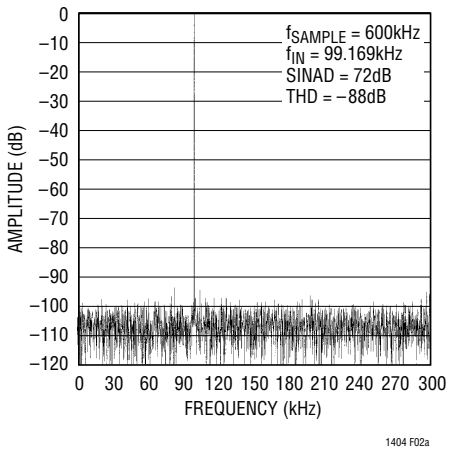


Figure 2a. LTC1404 Nonaveraged, 4096 Point FFT Plot with 100kHz Input Frequency in Bipolar Mode

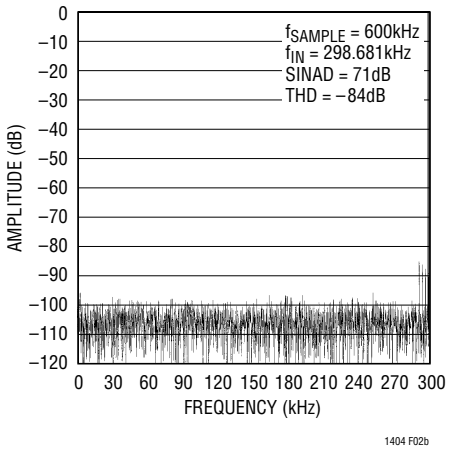


Figure 2b. LTC1404 Nonaveraged, 4096 Point FFT Plot with 300kHz Input Frequency in Bipolar Mode

APPLICATIONS INFORMATION

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from DC to half the sampling frequency. Figure 2a shows a typical spectral content with a 600kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 300kHz as shown in Figure 2b.

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the effective resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = \frac{S/(N+D) - 1.76}{6.02}$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 600kHz, the LTC1404 maintains very good ENOBs up to the Nyquist input frequency of 300kHz (refer to Figure 3).

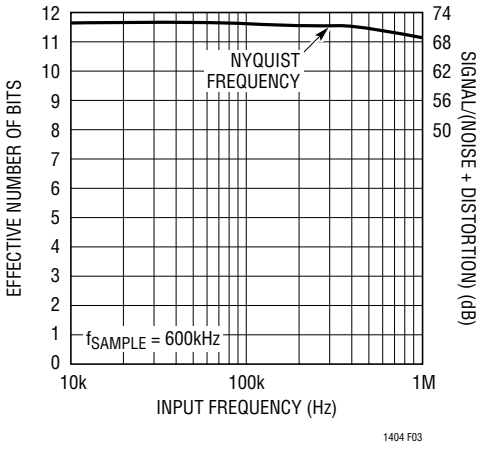


Figure 3. Effective Bits and Signal-to-Noise + Distortion vs Input Frequency in Bipolar Mode

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. THD vs input frequency is shown in Figure 4. The LTC1404 has good distortion performance up to the Nyquist frequency and beyond.

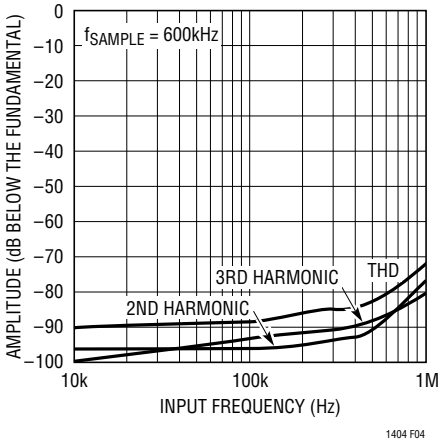


Figure 4. Distortion vs Input Frequency in Bipolar Mode

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

APPLICATIONS INFORMATION

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms includes (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula.

$$IMD(fa \pm fb) = 20\log\frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 100kHz input.

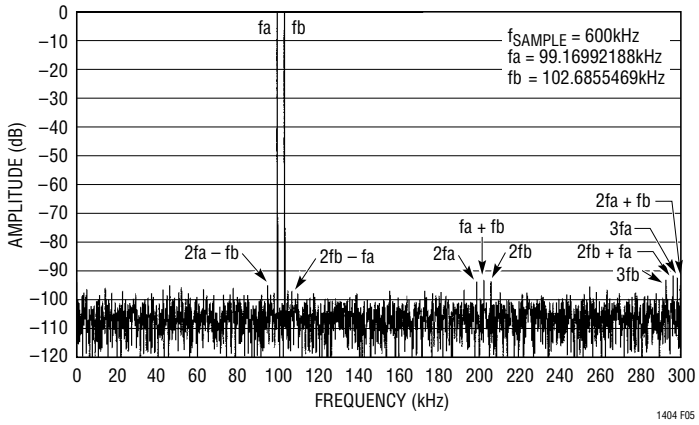


Figure 5. Intermodulation Distortion Plot in Bipolar Mode

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is the input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1404 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The analog input of the LTC1404 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of a conversion. During conversion, the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 160ns to small load current transient will allow maximum speed operation. If a slower op amp is used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include the LT®1360 and the LT1363 op amps.

The LTC1404 comes with a built-in unipolar/bipolar detection circuit. If the V_{SS} potential is forced below GND, the internal circuitry will automatically switch to bipolar mode.

The following list is a summary of the op amps that are suitable for driving the LTC1404, more detailed information is available in the Linear Technology databooks and the LinearView™ CD-ROM.

LT1215/LT1216: Dual and quad 23MHz, 50V/µs single supply op amps. Single 5V to ±15V supplies, 6.6mA specifications, 90ns settling to 0.5LSB.

LT1223: 100MHz video current feedback amplifier. ±5V to ±15V supplies, 6mA supply current. Low distortion up to and above 600kHz. Low noise. Good for AC applications.

LT1227: 140MHz video current feedback amplifier. ±5V to ±15V supplies, 10mA supply current. Lowest distortion at frequencies above 600kHz. Low noise. Best for AC applications.

APPLICATIONS INFORMATION

LT1229/LT1230: Dual and quad 100MHz current feedback amplifiers. ±2V to ±15V supplies, 6mA supply current each amplifier. Low noise. Good AC specs.

LT1360: 37MHz voltage feedback amplifier. ±5V to ±15V supplies. 3.8mA supply current. Good AC and DC specs. 70ns settling to 0.5LSB.

LT1363: 50MHz, 450V/µs op amps. ±5V to ±15V supplies. 6.3mA supply current. Good AC and DC specs. 60ns settling to 0.5LSB.

LT1364/LT1365: Dual and quad 50MHz, 450V/µs op amps. ±5V to ±15V supplies, 6.3mA supply current per amplifier. 60ns settling to 0.5LSB.

Internal Reference

The LTC1404 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.43V. It is internally connected to the DAC and is available at Pin 3 to provide up to 1mA of current to an external load. For minimum code transition noise, the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic). The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The V_{REF} pin must be driven to at least 2.46V to prevent conflict with the internal reference. The reference should not be driven to more than 5V. Figure 6 shows an LT1360 op amp driving the reference pin. Figure 7 shows a typical reference, the LT1019A-5 connected to the LTC1404. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-5) and a ±4.215V full scale. If V_{REF} is forced lower than 2.43V, the REFRDY bit in the serial data output will be forced to low.

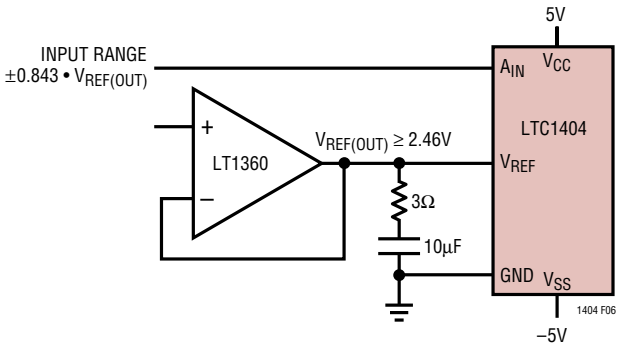


Figure 6. Driving the V_{REF} with the LT1360 Op Amp

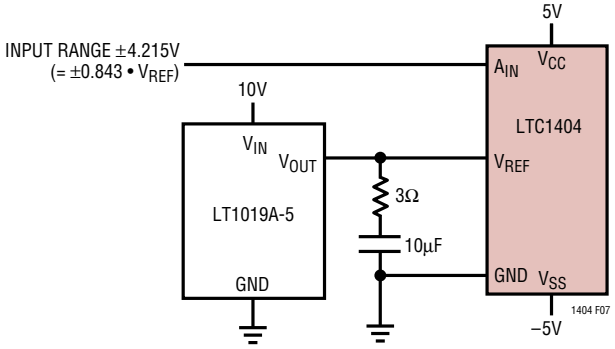


Figure 7. Supplying a 5V Reference Voltage to the LTC1404 with the LT1019A-5

UNIPOLAR / BIPOLAR OPERATION AND ADJUSTMENT

Figure 8 shows the ideal input/output characteristics for the LTC1404. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, … FS – 1.5LSB). The output code is natural binary with 1LSB = 4.096/4096 = 1mV. Figure 9 shows the input/output transfer characteristics for the bipolar mode in two's complement format.

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Figure 10a shows the extra components required for full-scale error adjustment. Figure 10b shows offset and full-scale adjustment. Offset error must be adjusted before full-scale error. Zero offset is achieved by applying 0.5mV (i.e., 0.5LSB) at the input and adjusting the offset trim until the LTC1404 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error, apply an analog input of 4.0945V (FS – 1.5LSB or last code transition) at the input and adjust R5 until the LTC1404 output code flickers between 1111 1111 1110 and 1111 1111 1111.

APPLICATIONS INFORMATION

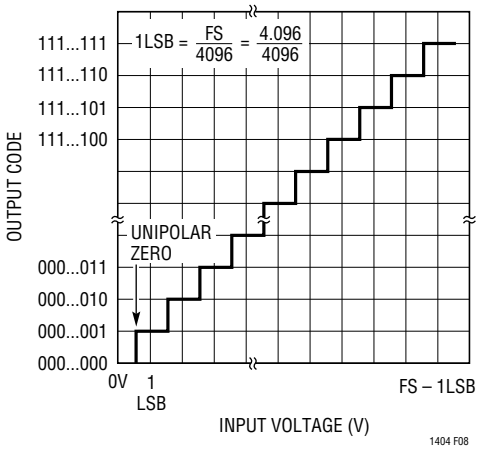


Figure 8. LTC1404 Unipolar Transfer Characteristics

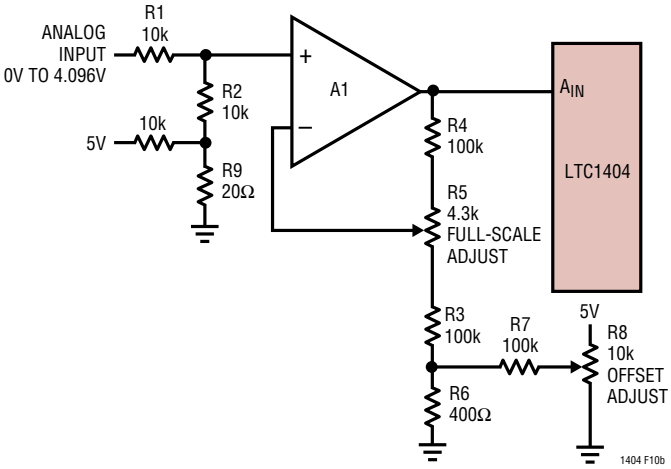


Figure 10b. LTC1404 Offset and Full-Scale Adjust Circuit

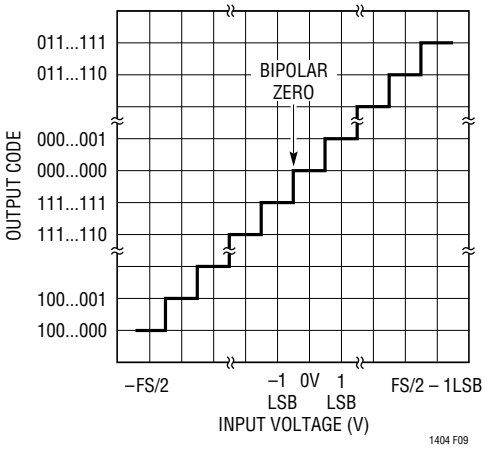


Figure 9. LTC1404 Bipolar Transfer Characteristics

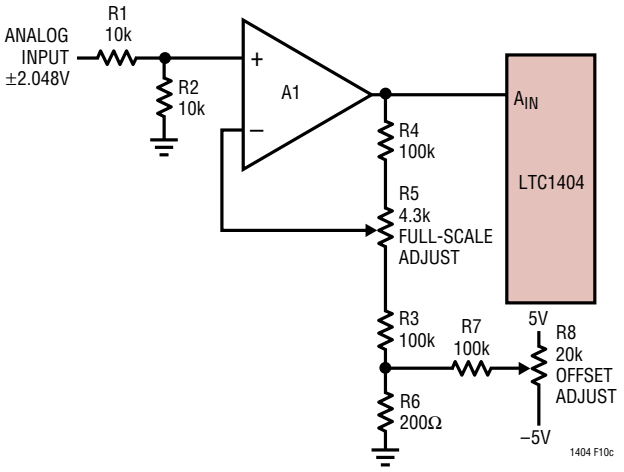


Figure 10c. LTC1404 Bipolar Offset and Full-Scale Adjust Circuit

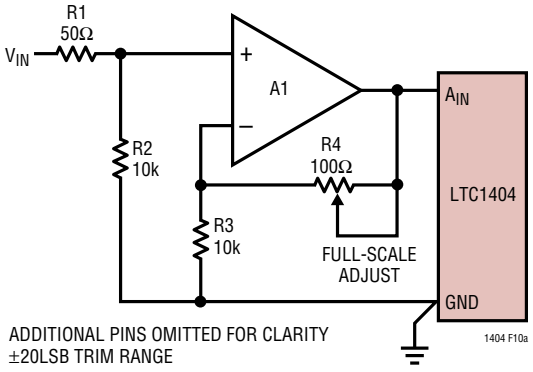


Figure 10a. LTC1404 Full-Scale Adjust Circuit

Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Bipolar offset error adjustment is achieved by applying an input voltage of –0.5mV (–0.5LSB) to the input in Figure 10c and adjusting the op amp until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

APPLICATIONS INFORMATION

BOARD LAYOUT AND BYPASSING

To obtain the best performance from the LTC1404, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital traces alongside an analog signal trace or underneath the ADC. The analog input should be screened by GND.

High quality 10µF surface mount AVX capacitor with a 0.1µF ceramic should be used at the V_{CC}, V_{SS} and V_{REF} pins. For better results, another 10µF AVX capacitor can be added to the V_{CC} pin. At 600ksps, the CLK frequency can be as high as 9.6MHz. A poor quality capacitor can lose more than 80% of its capacitance at this frequency range. Therefore, it is important to consult the manufacturer's data sheet before the capacitor is used. For the LTC1404, at 600ksps, every bit decision must be determined within 104ns (9.6MHz). During this short time interval, the supply disturbance due to a CLK transition needs to settle. The ADC must update its DAC, make a comparator decision based on sub-mV overdrive, latch the new DAC information and output the serial data. This ADC provides one power supply, V_{CC}, which is connected to both the internal analog and digital circuitry. Any ringing due to poor supply or reference bypassing, inductive trace runs, CLK and CONV over- or undershoot, or unnecessary D_{OUT} loading can cause ADC errors. Therefore, the bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible. In unipolar mode operation, V_{SS} must be connected to the GND pin directly.

Input signal leads to A_{IN} and signal return leads from GND (Pin 4) should be kept as short as possible to minimize noise coupling. In applications where this is not possible, a shielded cable between the analog input signal and the ADC is recommended. Also, any potential difference in grounds between the analog signal and the ADC appears as an error voltage in series with the analog input signal. Attention should be paid to reducing the ground circuit impedance as much as possible.

Figure 11 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC1404 GND pin. The ground return from the LTC1404 Pin 4 to the power supply should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common. As an alternative, instead of a direct short between the digital and analog circuitry, a 10Ω or a ferrite bead jumper helps reduce the digital noise.

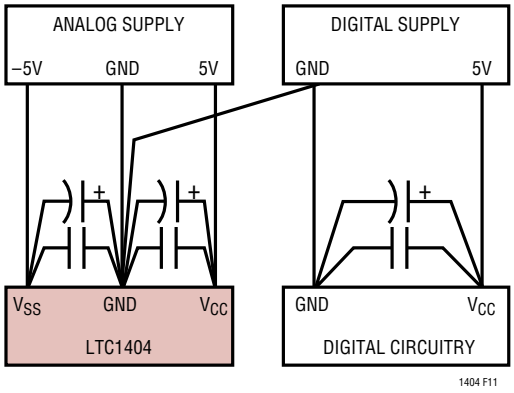


Figure 11. Power Supply Connection

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

Power-Down Mode

Upon power-up, the LTC1404 is initialized to the active state and is ready for conversion. However, the chip can be easily placed into Nap or Sleep mode by exercising the right combination of CLK and CONV signals. In Nap mode, all power is off except for the internal reference, which is still active and provides 2.43V output voltage to the other circuitry. In this mode, the ADC draws only 7.5mW of power instead of 75mW (for minimum power, the logic

APPLICATIONS INFORMATION

inputs must be within 500mV of the supply rails). In Sleep mode, power consumption is reduced to a minimum by cutting off power to all internal circuitry including the reference. Figure 12 illustrates power-down modes for the LTC1404. The chip enters Nap mode by keeping the CLK signal low and pulsing the CONV signal twice. For Sleep mode operation, the CONV signal should be pulsed four times while CLK is kept low. Nap and Sleep modes are activated on the falling edge of the CONV pulse.

The LTC1404 returns to active mode easily. The rising edge of CLK wakes up the LTC1404. From Nap mode, wake-up occurs within 350ns. During the transition from Sleep mode to active mode, the V_{REF} voltage ramp-up time is a function of its loading conditions. With a 10µF bypass capacitor, the wake-up time from Sleep mode is typically 2.5ms. A REFRDY signal is activated once the reference has settled and is ready for an A/D conversion. This REFRDY bit is sent to the D_{OUT} pin as the first bit followed by the 12-bit data word (refer to Figure 13). To save power during wake-up from Sleep mode, the chip is designed to enter Nap mode automatically until the reference is ready. Once REFRDY goes high, the comparator powers up immediately and is ready for a conversion. During the Nap interval, any attempt to perform an analog-to-digital conversion will result in an all-zero output code, including the REFRDY bit. If no conversion is attempted, the D_{OUT} pin remains in a high impedance state. If the ADC wakes from Sleep mode, this can be determined by monitoring the state of the REFRDY bit at the D_{OUT} pin.

DIGITAL INTERFACE

The digital interface requires only three digital lines. CLK and CONV are both inputs, and the D_{OUT} output provides the conversion result in serial form.

Figure 13 shows the digital timing diagram of the LTC1404 during the A/D conversion. The CONV rising edge starts the conversion. Once initiated, it can not be restarted until the conversion is completed. If the time from CONV signal to CLK rising edge is less than t_2, the digital output will be delayed by one clock cycle.

The digital output data is updated on the rising edge of the CLK line. The digital output data consists of a REFRDY bit followed by a valid 12-bit data word. D_{OUT} data should be captured by the receiving system on the rising CLK edge. Data remains valid for a minimum time of t_{10} after the rising CLK edge to allow capture to occur.

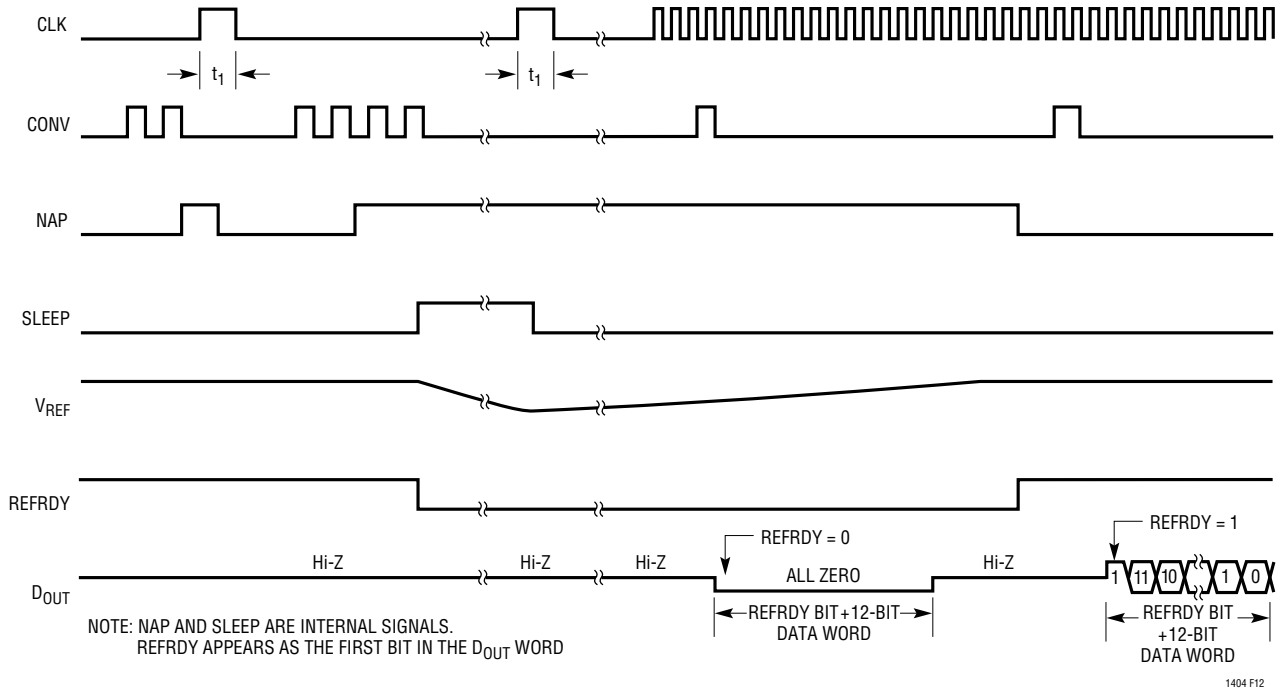


Figure 12. Nap Mode and Sleep Mode Waveforms

APPLICATIONS INFORMATION

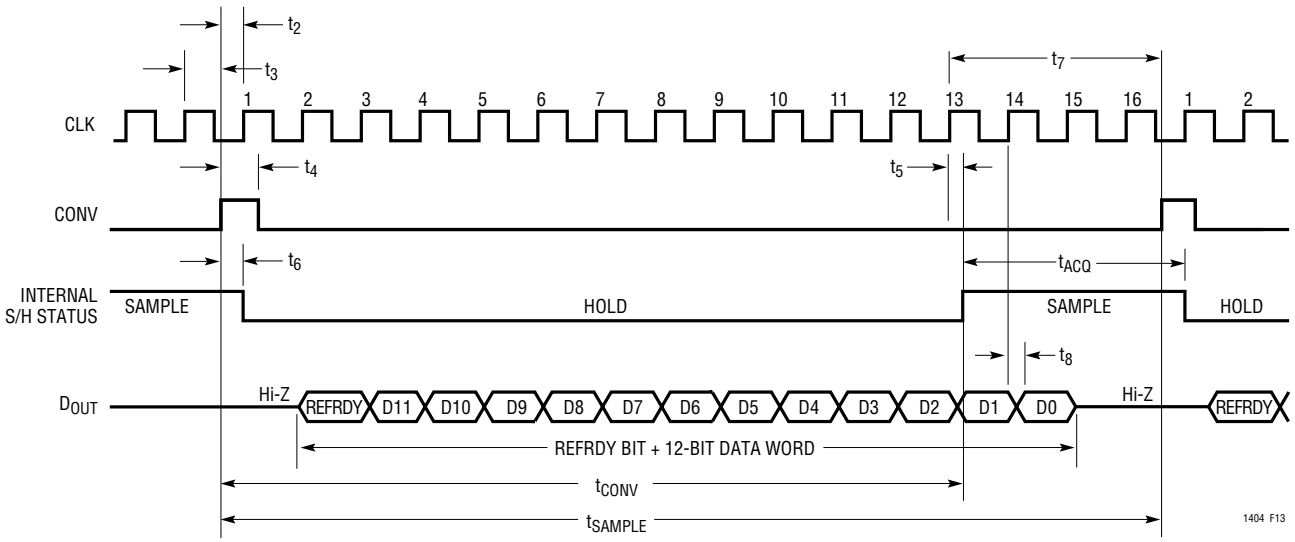


Figure 13. ADC Digital Timing Diagram

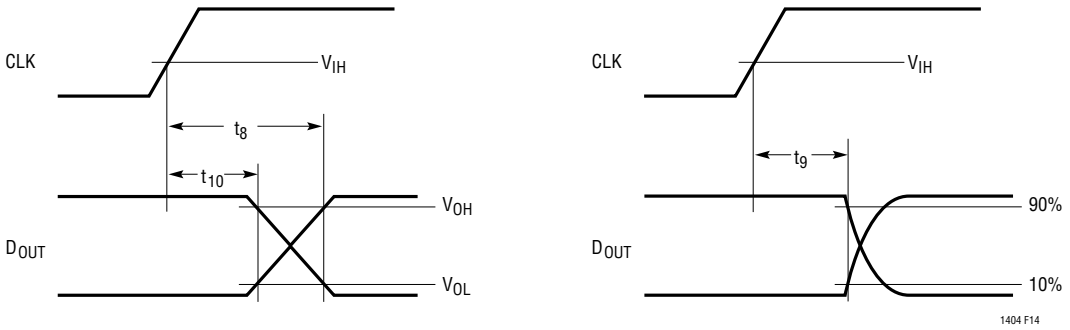
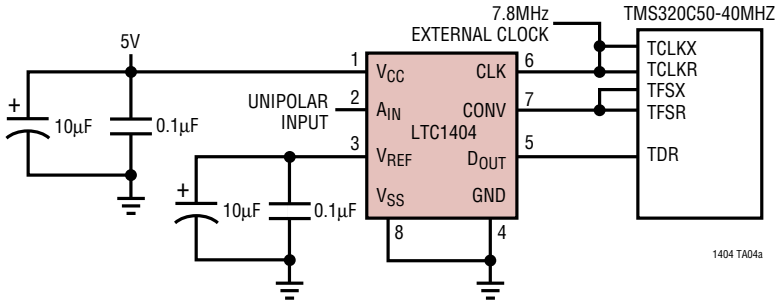


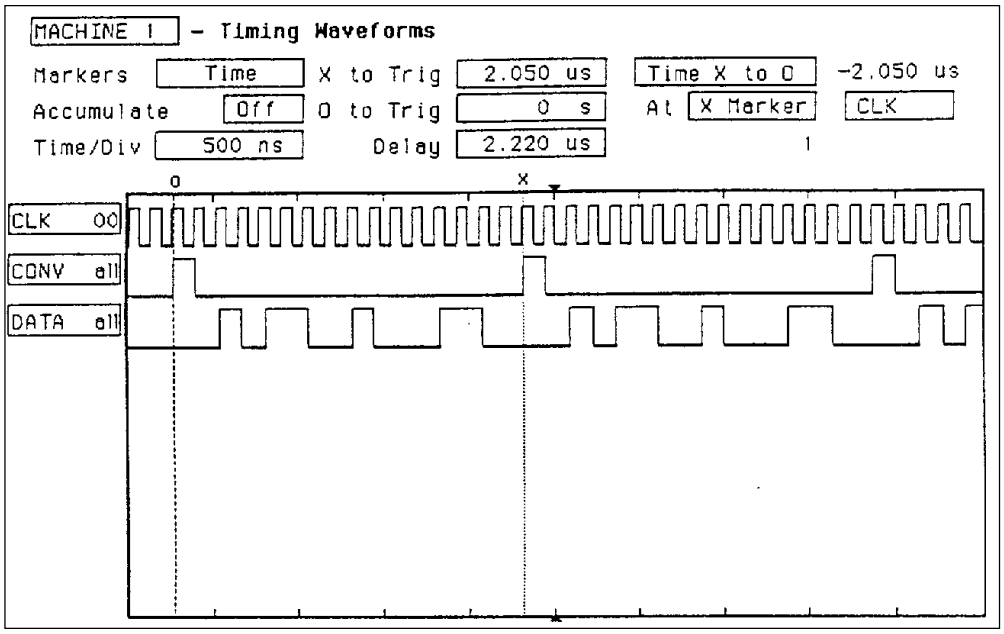
Figure 14. CLK to D_{OUT} Delay

TYPICAL APPLICATIONS

Hardware Interface to the TMS320C50's TDM Serial Port (Frame Sync is Generated from TFSX)



Logic Analyzer Waveforms Show 2.05µs Throughput Rate (Input Voltage = 1.606V, Output Code = 0110 0100 0110 = 1606_{10})



NOTE: THE TMS320C50-40MHz HAS A LIMITED SERIAL PORT CLOCK SPEED OF 7.8MHz. TO ALLOW THE LTC1404 TO RUN AT ITS MAXIMUM SPEED OF 9.6MHz, THE TMS320C50-57 OR TMS320C50-80MHz IS NEEDED

1404T A04B

Data from the LTC1404 Loaded into the TMS320C50's TRCV Register

X	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

1404 TA04c

Data Stored in the TMS320C50's Memory (in Right Justified Format)

0	0	0	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1404 TA04d

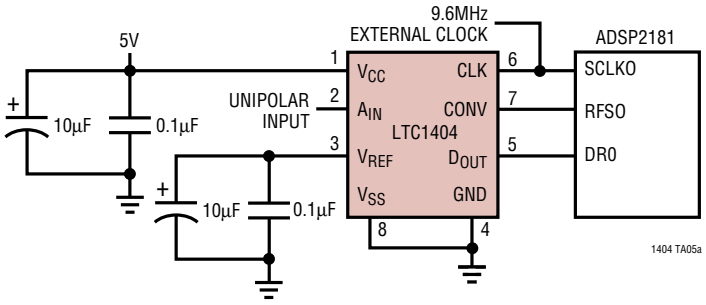
TYPICAL APPLICATIONS

TMS320C50 Code for Circuit

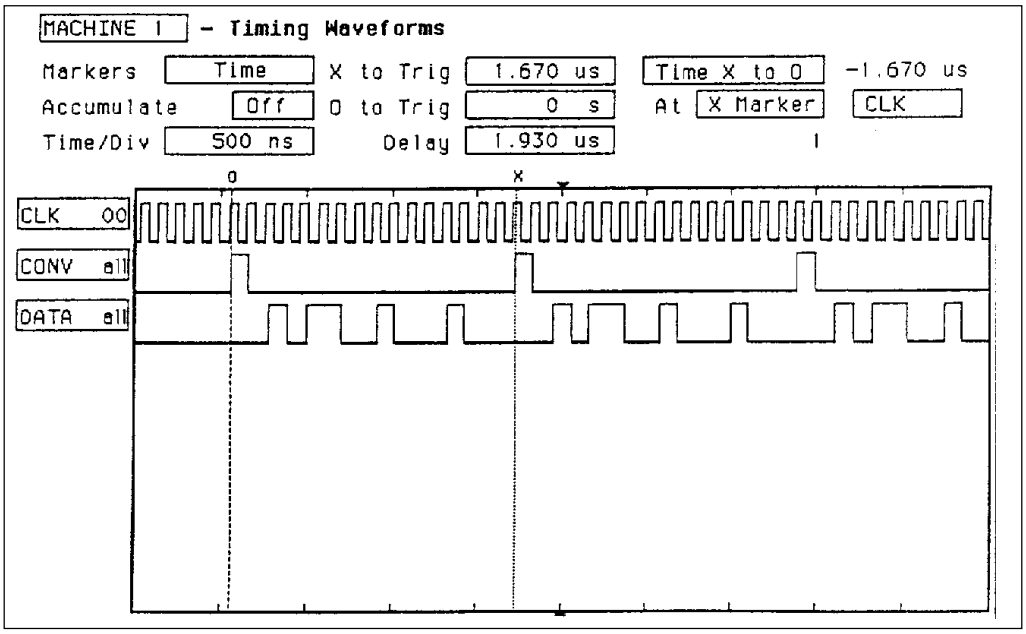
```
*THIS PROGRAM DEMONSTRATES THE LTC1404 INTERFACE TO THE
*TMS320C50. FRAME SYNC PULSE IS GENERATED FROM TFSX.
*DATA SHIFT CLOCK IS EXTERNALLY GENERATED.

*Initialization*
    .mmregs                         ; Defines global symbolic names
;- - Initialized data memory to zero
            .ds     0F00h           ; Initialize data to zero
DATA0       .word   0               ; Begin sample data location
DATA1       .word   0               ; .
DATA2       .word   0               ; Location of data
DATA3       .word   0               ; .
DATA4       .word   0               ; .
DATA5       .word   0               ; End sample data location
;- - Set up the ISR vector
            .ps     080Ah           ; Serial ports interrupts
rint :      B       RECEIVE         ; 0A;
xint :      B       TRANSMIT        ; 0C;
trnt :      B       TREC            ; 0E;
txnt :      B       TTRANX          ; 10;
;- - Setup the reset vector
    .ps 0A00h
    .entry
START:

*TMS320C50 Initialization*
    SETC   INTM             ; Temporarily disable all interrupts
    LDP    #0               ; Set data page pointer to zero
    OPL    #0834h, PMST     ; Set up the PMST status and control register
    LACC   #0
    SAMM CWSR               ; Set software wait state to 0
    SAMM PDWSR              ;

*Configure Serial Port*
    SPLK   #0028h, TSPC     ; Set TDM Serial Port
                            ; TDM = 0 Stand Alone mode
                            ; DLB=0 Not loop back
                            ; FO=0 16  Bits
                            ; FSM=1 Burst Mode
                            ; MCM=0 CLKR is generated externally
                            ; TXM=1 FSX as output pin
                            ; Put serial port into reset
                            ; (XRST=RRST=0)
    SPLK   #00E8h, TSPC     ; Take Serial Port out of reset
                            ; (XRST=RRST=1)
    SPLK   #0FFFFh, IFR     ; Clear all the pending interrupts

*Start Serial Communication*
    SACL   TDXR             ; Generate frame sync pulse
    SPLK   #040h, IMR       ; Turn on TRNT receiver interrupt
    CLRC   INTM             ; Enable interrupt
    CLRC   SXM              ; For Unipolar input, set for right shift
                            ; with no sign extension
    MAR    *, AR7           ; Load the auxiliary register pointer with seven
    LAR    AR7, #0F00h      ; Load the auxiliary register seven with #0F00h
                            ; as the begin address for data storage
WAIT:   NOP                 ; Wait for a receive interrupt
            NOP             ;
            NOP             ;
    SACL   TDXR             ; !! Regenerate the frame sync pulse
    B      WAIT             ;
; - - - - - - - end of main program - - - - - - - - - - ;

*Receiver Interrupt Service Routine*
TREC:
    LAMM TRCV               ; Load the data received from LTC1404
    SFR                     ; Shift right two times
    SFR                     ;
    AND    #1FFFh, 0        ; ANDed with #1FFFh
                            ; For converting the data to right
                            ; justified format
                            ;
    SACL   *+, 0            ; Write to data memory pointed by AR7 and
                            ; increase the memory address by one
    LACC   AR7              ;
    SUB    #0F05h,0         ; Compare to end sample address #0F05h
    BCND   END_TRCV,GEQ     ; If the end sample address has exceeded jump
                              to END_TRCV
                            ;
    SPLK   #040h, IMR       ; Else Re-enable the TRNT receive interrupt
    RETE                    ; Return to main program and enable interrupt

*After Obtained the Data from LTC1404, Program Jump to END_TRCV*
END_TRCV:
    SPLK   #002h, IMR       ; Enable INT2 for program to halt
    CLRC   INTM
SUCCESS:
    B      SUCCESS

*Fill the Unused Interrupt with RETE, to avoid program get "lost"*
TTRANX:
    RETE
RECEIVE:
    RETE
TRANSMIT:
    RETE
INT2:
    B halt                  ; Halts the running CPU
```

TYPICAL APPLICATIONS

LTC1404 Interface to the ADSP2181's SPORT0 (Frame Sync is Generated from RFS0)



Logic Analyzer Waveforms Show 1.67µs Throughput Rate (Input Voltage = 1.604V, Output Code = 0110 0100 0100 = 1604_{10})



NOTE: WITHOUT THE EXTERNAL CLOCKING SIGNAL, THE ADSP2181 SCLK0 CAN BE PROGRAMMED TO RUN AT 8.3MHz

1404 TA05b

Data from the LTC1404 (Normal Mode)

X	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X

1404 TA05c

Data Stored in the ADSP2181's Memory (Normal Mode, SLEN = D)

0	0	0	RDY	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1404 TA05d

TYPICAL APPLICATIONS

ADSP2181 Code for Circuit

```
/*Section 1: Initialization*/
.module/ram/abs = 0 adspltc;    /*define the program module*/
    jump start;             /*jump over interrupt vectors*/
    nop; nop; nop;
    rti; rti; rti; rti;     /*code vectors here upon IRQ2 int*/
    rti; rti; rti; rti;     /*code vectors here upon IRQL1 int*/
    rti; rti; rti; rti;     /*code vectors here upon IRQL0 int*/
    rti; rti; rti; rti;     /*code vectors here upon SPORT0 TX int*/
    ax0 = rx0;              /*Section 5*/
    dm (0x2000) = ax0;      /*begin of SPORT0 receive interrupt*/
    rti;                    /* */
                            /* */
                            /*end of SPORT0 receive interrupt*/
    rti; rti; rti; rti;     /*code vectors here upon /IRQE int*/
    rti; rti; rti; rti;     /*code vectors here upon BDMA interrupt*/
    rti; rti; rti; rti;     /*code vectors here upon SPORT1 TX (IRQ1) int*/
    rti; rti; rti; rti;     /*code vectors here upon SPORT1 RX (IRQ0) int*/
    rti; rti; rti; rti;     /*code vectors here upon TIMER int*/
    rti; rti; rti; rti;     /*code vectors here upon POWER DOWN int*/
```

THIS PROGRAM DEMONSTRATES THE LTC1404 INTERFACE TO THE ADSP-2181. FRAME SYNC PULSE IS GENERATED FROM RFS. DATA SHIFT CLOCK IS EXTERNALLY GENERATED.

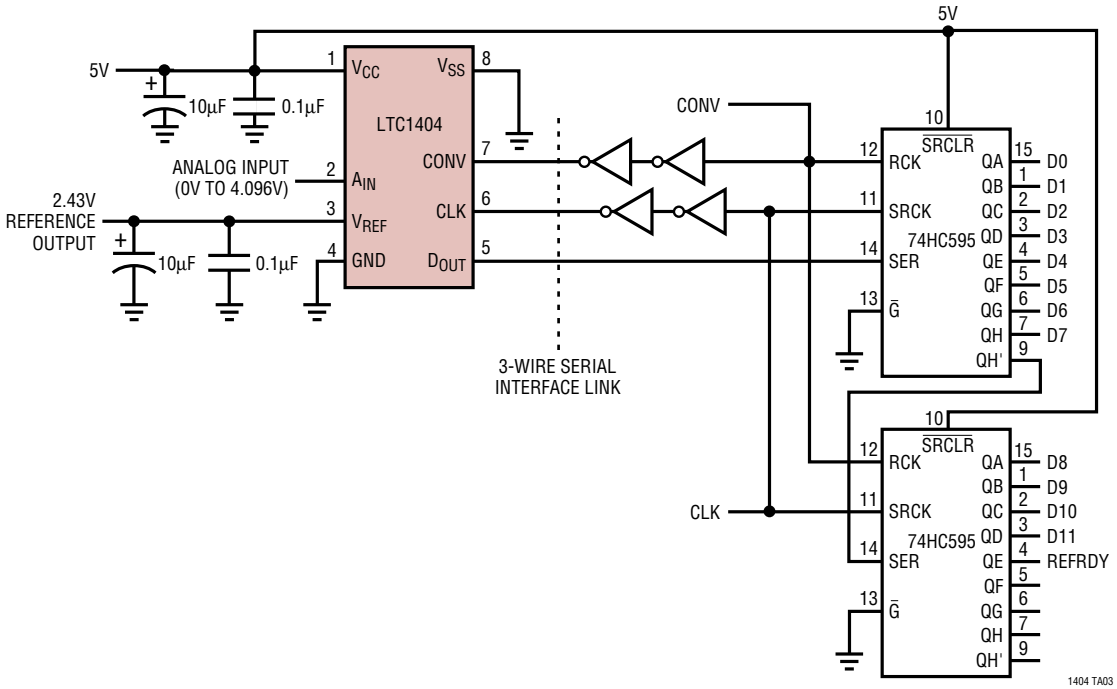
```
/*Section 2: Configure SPORT0*/
start:
/*to configure SPORT0 control reg*/
                            /*SPORT0 address = 0X3FF6*/
                            /*RFS is used for frame sync generation*/
                            /*RFS is internal, TFS is not used*/
                            /*bit 0-3 = Slen*/
                            /*F = 15 = 1111*/
                            /*E = 14 = 1110*/
                            /*D = 13 = 1101*/
                            /*bit 4,5 data type right justified zero filled MSB*/
                            /*bit 6 INVRFS = 0*/
                            /*bit 7 INVTFS = 0*/
                            /*bit 8 IRFS=1 receive internal frame sync*/
                            /*bit 9,10,11 are for TFS (don't care)*/
                            /*bit 12 RFSW=0 receive is Normal mode*/
                            /*bit 13 RTFS=1 receive is framed mode*/
                            /*bit 14 ISCLK=0 SCLK is external */
                            /*bit 15 multichannel mode = 0*/
    ax0 = 0x2F0D;           /*normal mode, bit 12=0*/
                            /*if alternate mode bit 12=1, ax0=0x3F0E*/
    dm (0x3FF6) =ax0;
```

```
/*Section 3: configure CLKDIV and RFSDIV, setup interrupts*/
/*Using an external clock source=9.6MHz*/
/*Does not need to configure CLKDIV*/
/*to Configure RFSDIV*/
    ax0 = 15;               /*set the RFSDIV reg = 15*/
                            /*=> the frame sync pulse for every 16 SCLK*/
                            /*if frame sync pulse in every 15 SCLK, ax0=14*/
    dm(0x3FF4) =ax0;
/*to setup interrupt*/
    ifc= 0x0066;            /*clear any extraneous SPORT interrupts*/
    icntl= 0;               /*IRQXB = level sensitivity*/
                            /*disable nesting interrupt*/
    imask= 0x0020;          /*bit 0 = timer int = 0*/
                            /*bit 1 = SPORT1 or IRQ0B int = 0*/
                            /*bit 2 = SPORT1 or IRQ1B int = 0*/
                            /*bit 3 = BDMA int = 0*/
                            /*bit 4 = IRQEB int = 0*/
                            /*bit 5 = SPORT0 receive int = 1*/
                            /*bit 6 = SPORT0 transmit int = 0*/
                            /*bit 7 = IRQ2B int = 0*/
                            /*enable SPORT0 receive interrupt*/
```

```
/*Section 4: Configure System Control Register and Start Communication*/
/*to configure system control reg*/
    ax0 = dm(0x3FFF);       /*read the system control reg*/
    ay0 = 0xFFF0;
    ar = ax0 AND ay0;       /*set wait state to zero*/
    ay0 = 0x1000;
    ar = ar OR ay0;         /*bit 12 = 1, enable SPORT0*/
    dm(0x3FFF) = ar;
/*frame sync pulse regenerated automatically*/
    cntr = 5000;
do waitloop until ce;
    nop;
    nop;
    nop;
    nop;
    nop;
    nop;
waitloop: nop;
    rts;
.endmod;
```

TYPICAL APPLICATIONS

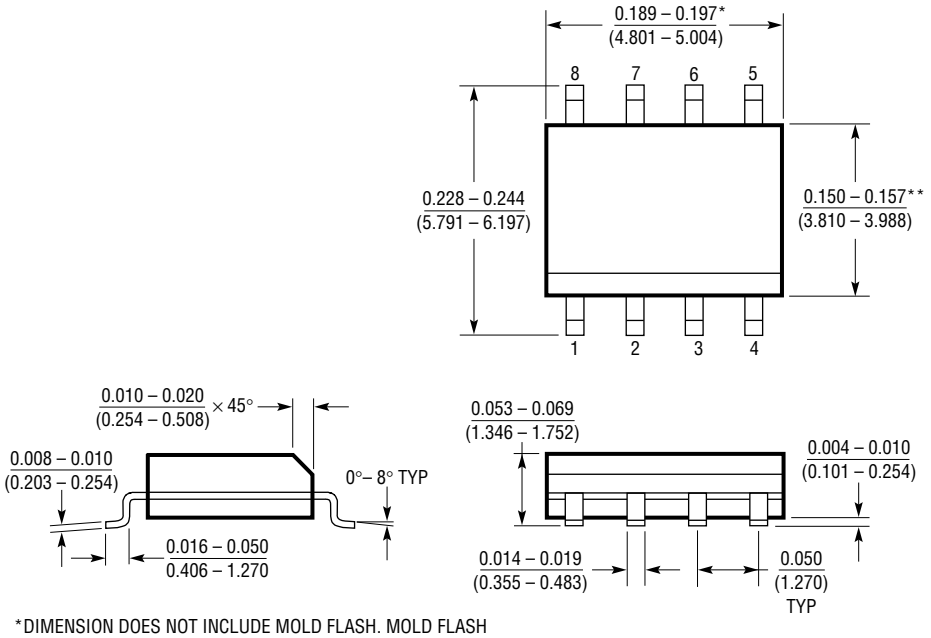
Quick Look Circuit for Converting Data to Parallel Format



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



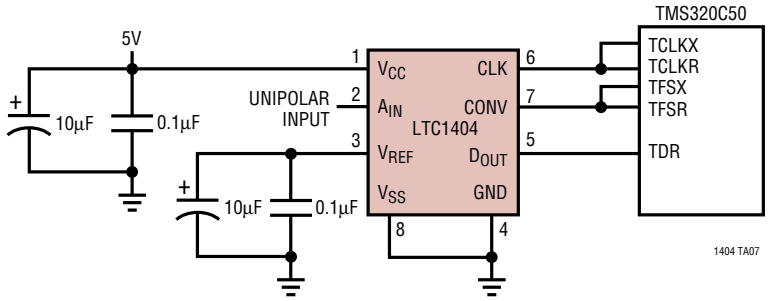
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

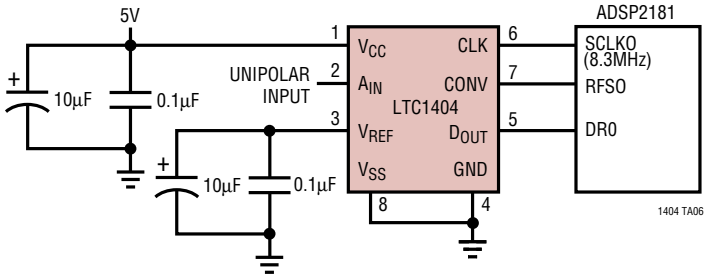
SO8 0996

TYPICAL APPLICATIONS

LTC1404 Interface to TMS320C50 Running at 5MHz without External Clock



LTC1404 Interface to ADSP2181 Running at 8.3MHz without External Clock



RELATED PARTS

12-Bit Parallel Output ADCs

PART NUMBER	DESCRIPTION	COMMENTS
LTC1273/LTC1275/ LTC1276	Complete 5V Sampling 12-Bit ADCs with 70dB SINAD at Nyquist	Lower Power and Cost Effective for $f_{SAMPLE} \leq 300$ksps
LTC1274/LTC1277	Low Power 12-Bit ADCs with Nap and Sleep Mode Shutdown	Lowest Power (10mW) for $f_{SAMPLE} \leq 100$ksps
LTC1278/LTC1279	High Speed Sampling 12-Bit ADCs with Shutdown	Cost Effective 12-Bit ADCs with Convert Start Input Best for 300ksps < $f_{SAMPLE} \leq 600$ksps
LTC1282	Complete 3V 12-Bit ADCs with 12mW Power Dissipation	Fully Specified for 3V Powered Applications, $f_{SAMPLE} \leq 140$ksps
LTC1409	Low Power 12-Bit, 800ksps Sampling ADC	Best Dynamic Performance $f_{SAMPLE} \leq 800$ksps, 80mW Dissipation
LTC1410	12-Bit, 1.25Msps Sampling ADC with Shutdown	Best Dynamic Performance, THD = 84 and SINAD = 71 at Nyquist

12-Bit Serial Output ADCs

PART NUMBER	V_{CC}	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
LTC1285/LTC1288	3V	7.5/6.6ksps	0.48mW	3V, One or Two Input, Micropower, SO-8
LTC1286/LTC1298	5V	12.5/11.1ksps	1.25mV	One or Two Input, Micropower, SO-8
LTC1290	5/±5V	50ksps	30mW	8 Input, Full-Duplex Serial I/O
LTC1296	5/±5V	46.5ksps	30mW	8 Input, Half-Duplex Serial I/O, Power Shutdown Output
LTC1400	5/±5V	400ksps	75mW	Complete 12-Bit, 400ksps, SO-8 ADC with Shutdown
LTC1401	3V	200ksps	15mW	Complete 12-Bit, 200ksps, SO-8 ADC with Shutdown

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