

## FEATURES

- **Tight Load Regulation with Highly Resistive Cables without Requiring Remote Sense Wiring**
- Compatible with Isolated and Nonisolated Power Supplies
- $\pm 1\%$  Internal Voltage Reference
- 5mA Sink Current Capability
- Soft-Correct Reduces Turn-On Transients
- Undervoltage and Overvoltage Protection
- Pin-Programmable Dither Frequency
- Optional Spread Spectrum Dither
- Wide  $V_{IN}$  Range: 3.1V to 50V
- 24-Pin SSOP Package

## APPLICATIONS

- 12V High Intensity Lamps
- 28V Industrial Systems
- High Power (>40 Watts) CAT5 Cable Systems
- Wiring Drop Cancellation for Notebook Computer Battery Charging
- AC and DC Adaptors
- Well-Logging and Other Remote Instrumentation
- Surveillance Equipment

## DESCRIPTION

The LT<sup>®</sup>4180 solves the problem of providing tight load regulation over long, highly resistive cables without requiring an additional pair of remote sense wires. This Virtual Remote Sense™ device continuously interrogates the line impedance and corrects the power supply output voltage via its feedback loop to maintain a steady voltage at the load regardless of current changes.

The LT4180 is a full-featured controller with 5mA optoisolator sink capability, under/overvoltage lockout, soft-start and a  $\pm 1\%$  internal voltage reference. The Virtual Remote Sense feature set includes user-programmable dither frequency and optional spread spectrum dither.

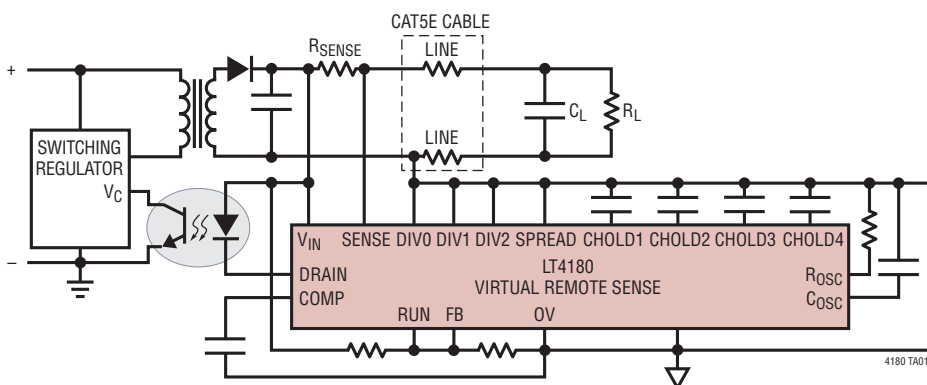
The LT4180 works with any topology and type of isolated or nonisolated power supply, including DC/DC converters and adjustable linear regulators.

The LT4180 is available in a 24-pin, SSOP package.

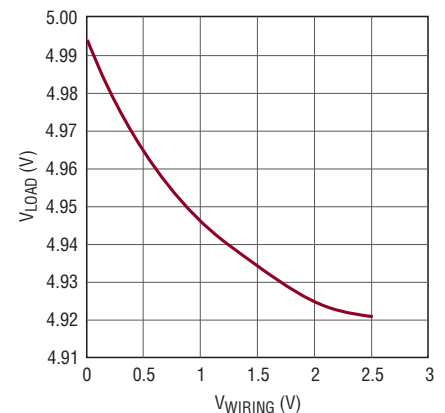
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## TYPICAL APPLICATION

Isolated Power Supply with Virtual Remote Sense



$V_{LOAD}$  vs  $V_{WIRE}$



4180 TA01b

4180fp

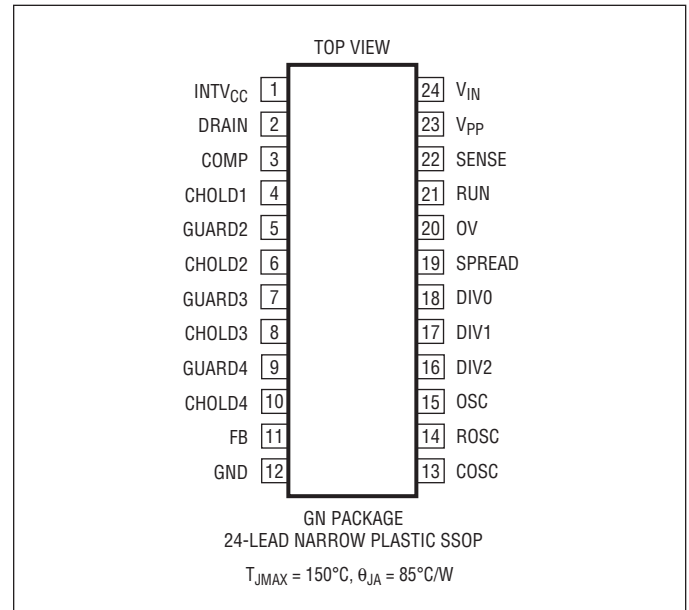
# LT4180

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ .....	-0.3V to 52V
SENSE.....	$V_{IN} - 0.3V$ to $V_{IN}$
INTVCC, RUN, FB, OV, ROSC, OSC, DIV0, DIV1, DIV2, SPREAD, CHOLD1, CHOLD2, CHOLD3, CHOLD4, DRAIN, COMP, GUARD2, GUARD3, GUARD4, $V_{PP}$ .....	-0.3V to 5.5V
$V_{IN}$ Pin Current.....	10mA
INTVCC Pin Current .....	-10mA
COSC Pin Current.....	3.3mA
Maximum Junction Temperature .....	125°C
Operating Junction Temperature Range (Note 2)	
E-, I-Grades .....	-40°C to 125°C
MP-Grade .....	-55°C to 125°C
Storage Temperature Range .....	-65°C to 125°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4180EGN#PBF	LT4180EGN#TRPBF	LT4180GN	24-Lead Narrow Plastic SSOP	-40°C to 125°C
LT4180IGN#PBF	LT4180IGN#TRPBF	LT4180GN	24-Lead Narrow Plastic SSOP	-40°C to 125°C
LT4180MPGN#PBF	LT4180MPGN#TRPBF	LT4180GN	24-Lead Narrow Plastic SSOP	-55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = \text{SENSE} = 5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{IN}$	Operating Supply Voltage		● 3.10		50	V	
$I_{VIN}$	Input Quiescent Current	ROSC Open, COSC Open, SENSE = $V_{IN}$	●	1	2	mA	
$V_{REF}$	Reference Voltage	$V_{CHOLD2} = V_{CHOLD3} = 1.2\text{V}$ , Measured at $C_{HOLD4}$ During Track $\Delta V_{OUT}$ Clock Phase	● 1.209	1.221	1.233	V	
			1.197	1.221	1.245	V	
$I_{LIM}$	Open-Drain Current Limit	With $\text{FB} = V_{REF} + 200\text{mV}$ , OSC Stopped with Voltage Feedback Loop Closed		5	10	15	mA
$V_{OL}$	DRAIN Low Voltage	$V_{IN} = 3\text{V}$			0.3	V	
$V_{INTVCC}$	LDO Regulator Output Voltage	$V_{IN} = 5\text{V}$		3.15		V	

4180fp

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{INTVCC}$	LDO Regulator Output Voltage in Dropout	$V_{IN} = 2.5\text{V}$	2.2			V
$V_{OV}$	Overvoltage Threshold	Rising		1.21		V
$V_{OHYST}$	Overvoltage Input Hysteresis	$V_{RISING} - V_{FALLING}$	20		80	mV
$V_{RUN}$	Run Threshold	Falling		1.21		V
$V_{RHYST}$	Run Input Hysteresis	$V_{RISING} - V_{FALLING}$	20		80	mV
$I_{FB}$	Input Bias Current		-0.2		0.2	$\mu\text{A}$
$V_{OS}$	Current Amplifier Offset Voltage	$V_{IN} = 3.5\text{V}$ $V_{IN} = 5\text{V}$ $V_{IN} = 48\text{V}$	-4 -3 -4		4 3 4	mV mV mV
$A_V(\text{RATIO})$	Current Amplifier Gain Ratio	$A_{VL}/A_{VH}$ , $A_V$ Measured in V/V	0.891	0.9	0.909	
$I_{SENSE}$	Current Amplifier Input Bias Current	Measured at SENSE with $\text{SENSE} = V_{IN}$	-1		1	$\mu\text{A}$
$A_V$	$\Delta V_{FB}$ Amplifier Gain		9.7	10	10.3	V/V
$I_{CHOLD1}$	Track/Hold Charging Current	Measured at CHOLD1 with $V_{CHOLD1} = 1.2\text{V}$		$\pm 60$		$\mu\text{A}$
$I_{CHOLD2}$	Track/Hold Charging Current	Measured at CHOLD2 with $V_{CHOLD2} = 1.2\text{V}$		$\pm 25$		$\mu\text{A}$
$I_{CHOLD3}$	Track/Hold Charging Current	Measured at CHOLD3 with $V_{CHOLD3} = 1.2\text{V}$		$\pm 25$		$\mu\text{A}$
$I_{CHOLD4}$	Track/Hold Charging Current	Measured at CHOLD4 with $V_{CHOLD4} = 1.5\text{V}$ , $V_{CHOLD2} = 1\text{V}$ , $V_{CHOLD3} = 1.2\text{V}$		10		$\mu\text{A}$
		Measured at CHOLD4 with $V_{CHOLD4} = 1.5\text{V}$ , $V_{CHOLD2} = 1.4\text{V}$ , $V_{CHOLD3} = 1.2\text{V}$		-200		$\mu\text{A}$
$I_{SC}$	Soft-Correct Current	Measured at CHOLD4			$\pm 1.5$	$\mu\text{A}$
$I_{LKG1}$	Track/Hold Leakage Current	Measured at CHOLD1 with $V_{CHOLD1} = 1.2\text{V}$			$\pm 1$	$\mu\text{A}$
$I_{LKG2}$	Track/Hold Leakage Current	Measured at CHOLD2 with $V_{CHOLD2} = 1.2\text{V}$			$\pm 1$	$\mu\text{A}$
$I_{LKG3}$	Track/Hold Leakage Current	Measured at CHOLD3 with $V_{CHOLD3} = 1.2\text{V}$			$\pm 1$	$\mu\text{A}$
$I_{LKG4}$	Track/Hold Leakage Current	Measured at CHOLD4 with $V_{CHOLD4} = 1.2\text{V}$			$\pm 1$	$\mu\text{A}$
$f_{OSC}$	Oscillator Frequency	$R_{OSC} = 20\text{k}$ , $C_{OSC} = 1\text{nF}$	170	200	230	kHz
$g_{mFB}$	Voltage Error Amplifier Transconductance	Measured from FB to COMP, $V_{COMP} = 2\text{V}$ , OSC Stopped with Voltage Feedback Loop Closed		110		$\mu\text{mho}$
$g_{mIAMP}$	Current Amplifier Transconductance	Measured from SENSE to COMP, $V_{COMP} = 2\text{V}$ , OSC Stopped with Current Feedback Loop Closed		750		$\mu\text{mho}$

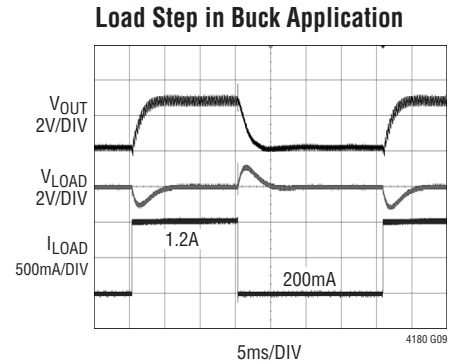
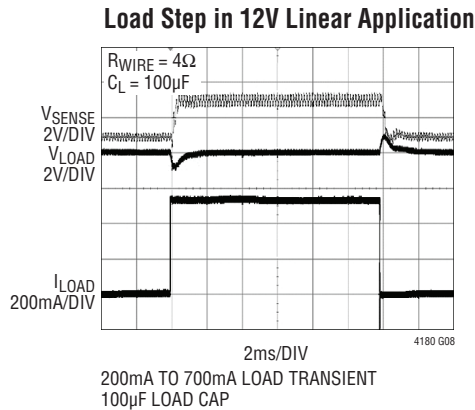
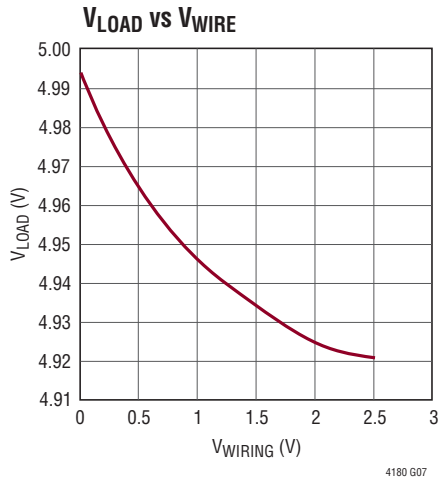
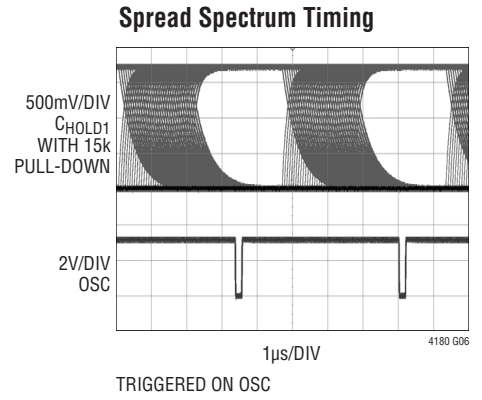
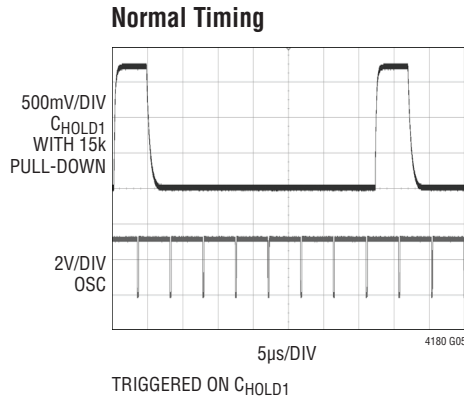
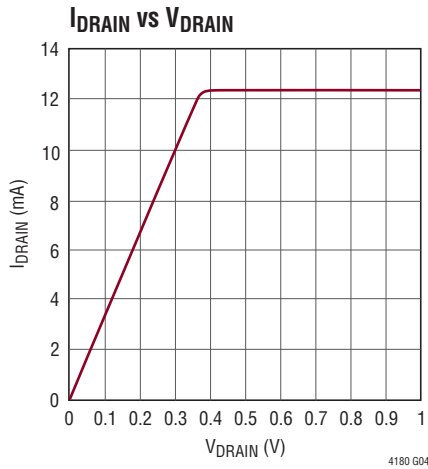
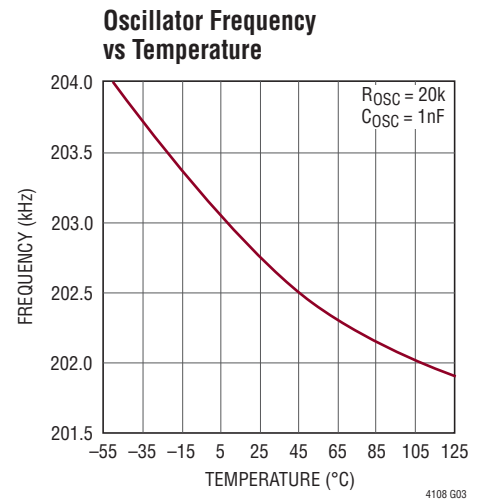
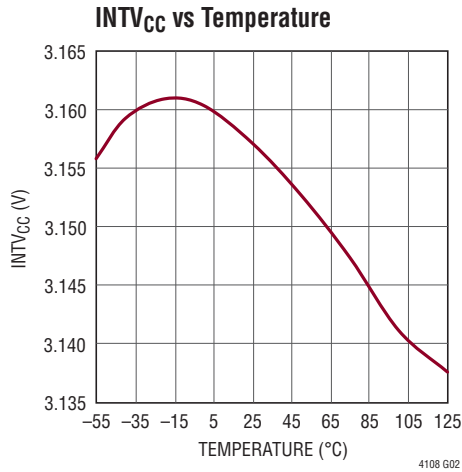
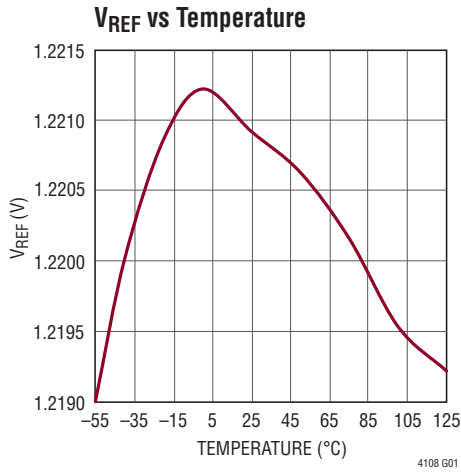
**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT4180E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature. Specifications over the  $-40^\circ\text{C}$

to  $125^\circ\text{C}$  operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LT4180I is guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range. The LT4180MP is guaranteed over the full  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range.

**Note 3:** Positive current is defined as flowing into a pin.

## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**INTVCC (Pin 1):** The LDO Output. A low ESR ceramic capacitor provides decoupling and output compensation. 1 $\mu$ F or more should be used.

**DRAIN (Pin 2):** Open-Drain of the Output Transistor. This pin drives either the LED in an opto-isolator, or pulls down on the regulator control pin.

**COMP (Pin 3):** Gate of the Output Transistor. This pin allows additional compensation. It must be left open if unused.

**CHOLD1 (Pin 4):** Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

**GUARD2 (Pin 5):** Guard Ring Drive for CHOLD2.

**CHOLD2 (Pin 6):** Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

**GUARD3 (Pin 7):** Guard Ring Drive for CHOLD3.

**CHOLD3 (Pin 8):** Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

**GUARD4 (Pin 9):** Guard Ring Drive for CHOLD4.

**CHOLD4 (Pin 10):** Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

**FB (Pin 11):** Receives the feedback voltage from an external resistor divider across the main output. An (optional) capacitor to ground may be added to eliminate high frequency noise. The time constant for this RC network should be no greater than 0.1 times the dither frequency. For example, with  $f_{\text{DITHER}} = 1\text{kHz}$ ,  $\tau = 0.1\text{ms}$ .

**GND (Pin 12):** Ground.

**COSC (Pin 13):** Oscillator Timing Capacitor. Oscillator frequency is set by this capacitor and ROsc. For best accuracy, the minimum recommended capacitance is 100pF.

**ROSC (Pin 14):** Oscillator Timing Resistor. Oscillator frequency is set by this resistor and COSC.

**OSC (Pin 15):** Oscillator Output. This output may be used to synchronize the switching regulator to the

Virtual Remote Sense. This is a high current output capable of driving opto-isolators. Other isolation methods may also be used with this output.

**DIV2 (Pin 16):** Dither Division Ratio Programming Pin.

**DIV1 (Pin 17):** Dither Division Ratio Programming Pin.

**DIV0 (Pin 18):** Dither Division Ratio Programming Pin.

Use the following table to program the dither division ratio ( $f_{\text{OSC}}/f_{\text{DITHER}}$ )

**Table 1. Programming the Dither Division Ratio ( $f_{\text{OSC}}/f_{\text{DITHER}}$ )**

DIV2	DIV1	DIV0	DIVISION RATIO
0	0	0	8
0	0	1	16
0	1	0	32
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

For example,  $f_{\text{DITHER}} = f_{\text{OSC}}/128$  with  $\text{DIV2} = 1$  and  $\text{DIV1} = \text{DIV0} = 0$ .

**SPREAD (Pin 19):** Spread Spectrum Enable Input. Dither phasing is pseudo-randomly adjusted when SPREAD is tied high.

**OV (Pin 20):** Overvoltage Comparator Input. This prevents line drop correction when wiring drops would cause excessive switching power supply output voltage. Set OV so  $V_{\text{REG(MAX)}} \leq 1.50V_{\text{LOAD}}$ .

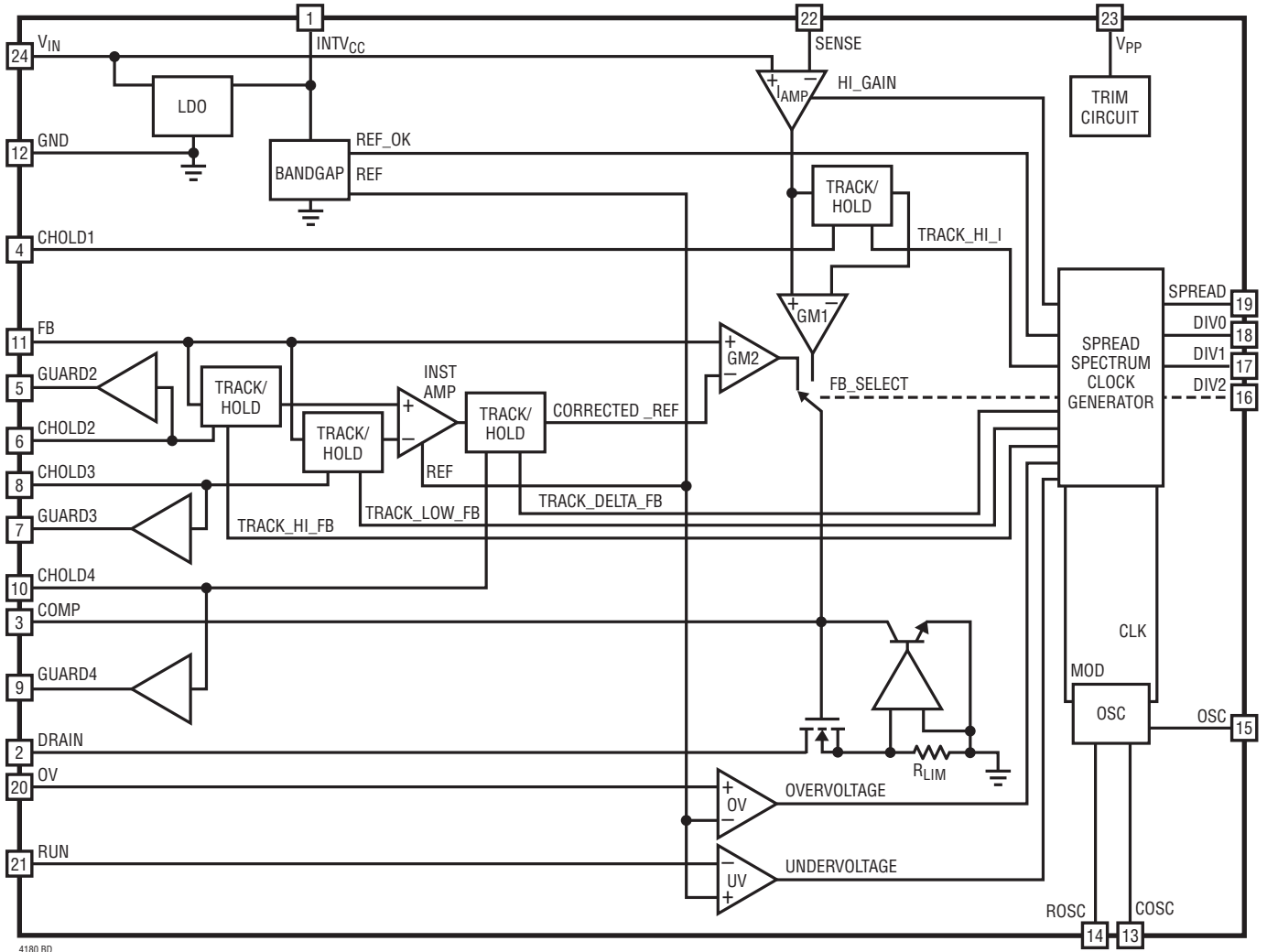
**RUN (Pin 21):** The RUN pin provides the user with an accurate means for sensing the input voltage and programming the start-up threshold for the line drop corrector.

**SENSE (Pin 22):** Current Sense Input. This input connects to the current sense resistor. Kelvin connect to  $R_{\text{SENSE}}$ .

**V<sub>PP</sub> (Pin 23):** Connect this pin to INTVCC.

**V<sub>IN</sub> (Pin 24):** Main Supply Pin.  $V_{\text{IN}}$  must be locally bypassed to ground. Kelvin connect the current sense resistor to this pin and minimize interconnect resistance.

## BLOCK DIAGRAM



4180 BD

## OPERATION

Voltage drops in wiring can produce considerable load regulation errors in electrical systems (Figure 1). As load current,  $I_L$ , increases the voltage drop in the wiring ( $I_L \cdot RW$ ) increases and the voltage delivered to the system ( $V_L$ ) drops. The traditional approach to solving this problem, remote sensing, regulates the voltage at the load, increasing the power supply voltage ( $V_{OUT}$ ) to compensate for voltage drops in the wiring. While remote sensing works well, it does require an additional pair of wires to measure at the load, which may not always be practical.

The LT4180 eliminates the need for a pair of remote sense wires by creating a Virtual Remote Sense. Virtual remote sensing is achieved by measuring the incremental change in voltage that occurs with an incremental change in current in the wiring (Figure 2). This measurement can then be used to infer the total DC voltage drop in the wiring, which can then be compensated for. The Virtual Remote Sense takes over control of the power supply via the feedback

pin (VFB) of the power supply maintaining tight regulation of load voltage,  $V_L$ .

Figure 3 shows the timing diagram for virtual remote sensing (VRS). A new cycle begins when the power supply and VRS close the loop around  $V_{OUT}$  (regulate  $V_{OUT} = H$ ). Both  $V_{OUT}$  and  $I_{OUT}$  slew and settle to a new value, and these values are stored in the Virtual Remote Sense (track  $V_{OUT}$  high = L and track  $I_{OUT} = L$ ). The  $V_{OUT}$  feedback loop is opened and a new feedback loop is set up commanding the power supply to deliver 90% of the previously measured current ( $0.9I_{OUT}$ ).  $V_{OUT}$  drops to a new value as the power supply reaches a new steady state, and this information is also stored in the Virtual Remote Sense. At this point, the change in output voltage ( $\Delta V_{OUT}$ ) for a  $-10\%$  change in output current has been measured and is stored in the Virtual Remote Sense. This voltage is used during the next VRS cycle to compensate for voltage drops due to wiring resistance.

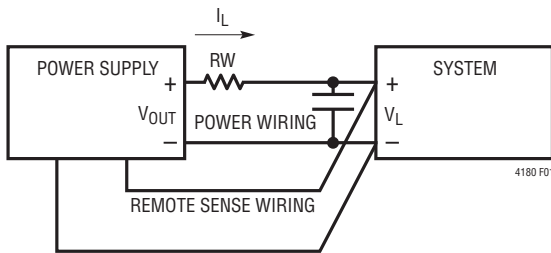


Figure 1. Traditional Remote Sensing

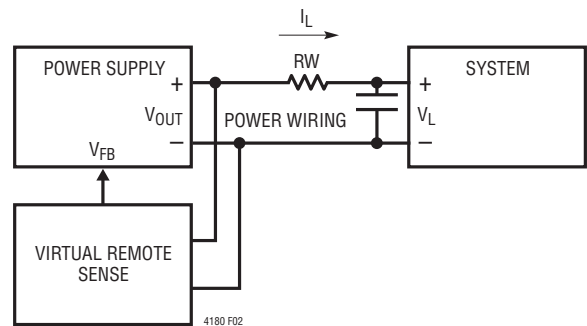


Figure 2. Virtual Remote Sensing

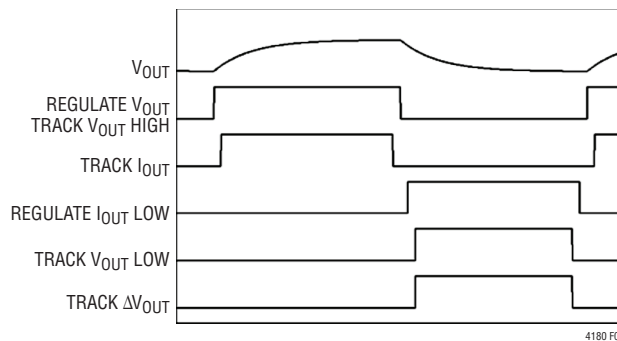


Figure 3. Simplified Timing Diagram, Virtual Remote Sense

## APPLICATIONS INFORMATION

### INTRODUCTION

The LT4180 is designed to interface with a variety of power supplies and regulators having either an external feedback or control pin. In Figure 4, the regulator error amplifier (which is a  $g_m$  amplifier) is disabled by tying its inverting input to ground. This converts the error amplifier into a constant-current source which is then controlled by the drain pin of the LT4180. This is the preferred method of interfacing because it eliminates the regulator error amplifier from the control loop which simplifies compensation and provides best control loop response.

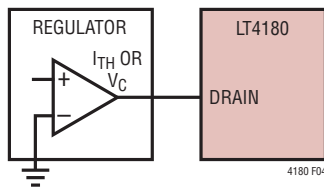


Figure 4. Nonisolated Regulator Interface

For proper operation, increasing control voltage should correspond to increasing regulator output. For example, in the case of a current mode switching power supply, the control pin ITH should produce higher peak currents as the ITH pin voltage is made more positive.

Isolated power supplies and regulators may also be used by adding an opto-coupler (Figure 5). LT4180 output voltage INTV<sub>CC</sub> supplies power to the opto-coupler LED. In situations where the control pin V<sub>C</sub> of the regulator may exceed 5V, a cascode may be added to keep the DRAIN pin of the LT4180 below 5V (Figure 6). Use a Low V<sub>T</sub> MOSFET for the cascode transistor.

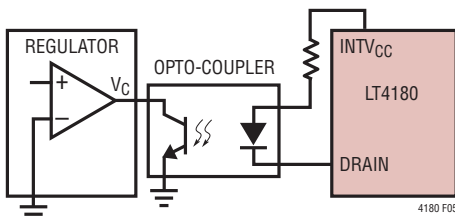


Figure 5. Isolated Power Supply Interface

### DESIGN PROCEDURE

The first step in the design procedure is to determine whether the LT4180 will control a linear or switching supply/regulator. If using a switching power supply or regulator, it is recommended that the supply be synchronized to the LT4180 by connecting the OSC pin to the SYNC pin (or equivalent) of the supply.

If the power supply is synchronized to the LT4180, the power supply switching frequency is determined by:

$$f_{osc} = \frac{4}{R_{osc} \cdot C_{osc}}$$

Recommended values for R<sub>OSC</sub> are between 20k and 100k (with 30.1k the optimum for best accuracy) and greater than 100pF for C<sub>OSC</sub>. C<sub>OSC</sub> may be reduced to as low as 50pF, but oscillator frequency accuracy will be somewhat degraded.

The following example synchronizes a 250kHz switching power supply to the LT4180. In this example, start with R<sub>OSC</sub> = 30.1k:

$$C_{osc} = \frac{4}{250\text{kHz} \cdot 30.1\text{k}} = 531\text{pF}$$

This example uses 470pF. For 250kHz:

$$R_{osc} = \frac{4}{250\text{kHz} \cdot 470\text{pF}} = 34.04\text{k}$$

The closest standard 1% value is 34k.

The next step is to determine the highest practical dither frequency. This may be limited either by the response time of the power supply or regulator, or by the propagation time of the wiring connecting the load to the power supply or regulator.

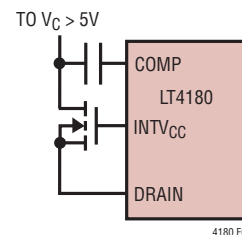


Figure 6. Cascoded DRAIN Pin for Isolated Supplies



## APPLICATIONS INFORMATION

First determine the settling time (to 1% of final value) of the power supply. The settling time should be the worst-case value (over the whole operating envelope:  $V_{IN}$ ,  $I_{LOAD}$ , etc.).

$$F1 = \frac{1}{2 \cdot t_{SETTLING}} \text{ Hz}$$

For example, if the power supply takes 1ms to settle (worst-case) to within 1% of final value:

$$F1 = \frac{1}{2 \cdot 1e-3} = 500\text{Hz}$$

Next, determine the propagation time of the wiring. In order to ignore transmission line effects, the dither period should be approximately twenty times longer than this. This will limit dither frequency to:

$$F2 = \frac{V_F}{20 \cdot 1.017\text{ns/ft} \cdot L} \text{ Hz}$$

Where  $V_F$  is the velocity factor (or velocity of propagation), and  $L$  is the length of the wiring (in feet).

For example, assume the load is connected to a power supply with 1000ft of CAT5 cable. Nominal velocity of propagation is approximately 70%.

$$F2 = \frac{0.7}{20 \cdot 1.017e-9 \cdot 1000} = 34.4\text{kHz}$$

The maximum dither frequency should not exceed  $F1$  or  $F2$  (whichever is less):

$$f_{DITHER} < \min(F1, F2).$$

Continuing this example, the dither frequency should be less than 500Hz (limited by the power supply).

With the dither frequency known, the division ratio can be determined:

$$D_{RATIO} = \frac{f_{OSC}}{f_{DITHER}} = \frac{250,000}{500} = 500$$

The nearest division ratio is 512 (set  $DIV0 = L$ ,  $DIV1 = DIV2 = H$ ). Based on this division ratio, nominal dither frequency will be:

$$f_{DITHER} = \frac{f_{OSC}}{D_{RATIO}} = \frac{250,000}{512} = 488\text{Hz}$$

After the dither frequency is determined, the minimum load decoupling capacitor can be determined. This load capacitor must be sufficiently large to filter out the dither signal at the load.

$$C_{LOAD} = \frac{2.2}{R_{WIRE} \cdot 2 \cdot f_{DITHER}}$$

Where  $C_{LOAD}$  is the minimum load decoupling capacitance,  $R_{WIRE}$  is the minimum wiring resistance of one conductor of the wiring pair, and  $f_{DITHER}$  is the minimum dither frequency.

Continuing the example, our CAT5 cable has a maximum  $9.38\Omega/100\text{m}$  conductor resistance.

Maximum wiring resistance is:

$$R_{WIRE} = 2 \cdot 1000\text{ft} \cdot 0.305\text{m/ft} \cdot 0.0938\Omega/\text{m}$$

$$R_{WIRE} = 57.2\Omega$$

## APPLICATIONS INFORMATION

With an oscillator tolerance of  $\pm 15\%$ , the minimum dither frequency is 414.8Hz, so the minimum decoupling capacitance is:

$$C_{LOAD} = \frac{2.2}{57.2\Omega \cdot 2 \cdot 414.8\text{Hz}} = 46.36\mu\text{F}$$

This is the minimum value. Select a nominal value to account for all factors which could reduce the nominal, such as initial tolerance, voltage and temperature coefficients and aging.

### CHOLD Capacitor Selection and Compensation

With dither frequency determined, use the following equations to determine CHOLD values:

$$C_{HOLD1} = \frac{11.9\text{nF}}{f_{DITHER}(\text{kHz})}$$

and

$$C_{HOLD2} = C_{HOLD3} = \frac{2.5\text{nF}}{f_{DITHER}(\text{kHz})}$$

So, with a dither frequency of 488Hz:

$$C_{HOLD1} = \frac{11.9\text{nF}}{0.488\text{kHz}} = 24.4\text{nF}$$

and

$$C_{HOLD2} = C_{HOLD3} = \frac{2.5\text{nF}}{0.488(\text{kHz})} = 5.12\text{nF}$$

NPO ceramic or other capacitors with low leakage and dielectric absorption should be used for all hold capacitors.

Set  $C_{HOLD4}$  to  $1\mu\text{F}$ .

Start with a 47pF capacitor between the COMP and DRAIN pins of the LT4180. Add an RC network in parallel with the 47pF capacitor. 10k and 10nF are good starting values. Connect a DC load corresponding to full-scale load current and verify that  $V_{OUT}$  produces a rounded squarewave without any noticeable overshoot or ringing (similar to the  $V_{OUT}$  waveform in Figure 3). If overshoot or ringing

is observed, decrease the value of the resistor until it just disappears. If overshoot or ringing is not observed, increase the value of the resistor until it is observed, then slightly decrease the value of the resistor so that overshoot and ringing disappear. Check for proper voltage drop correction and converter behavior (start-up, regulation etc.), over the load range, and repeat the above procedure with a smaller value of the compensation capacitor, if necessary. Decrease  $C_{HOLD4}$  capacitance until  $V_{OUT}$  exhibits slight low frequency instability, then increase  $C_{HOLD4}$  slightly from this value.

### Setting Output Voltage, Undervoltage and Overvoltage Thresholds

The RUN pin has accurate rising and falling thresholds which may be used to determine when Virtual Remote Sense operation begins. Undervoltage threshold should never be set lower than the minimum operating voltage of the LT4180 (3.1V).

The overvoltage threshold should be set slightly greater than the highest voltage which will be produced by the power supply or regulator:

$$V_{OUT(MAX)} = V_{LOAD(MAX)} + V_{WIRE(MAX)}$$

$V_{OUT(MAX)}$  should never exceed  $1.5 \cdot V_{LOAD}$

Since the RUN and OV pins connect to MOSFET input comparators, input bias currents are negligible and a common voltage divider can be used to set both thresholds (Figure 7).

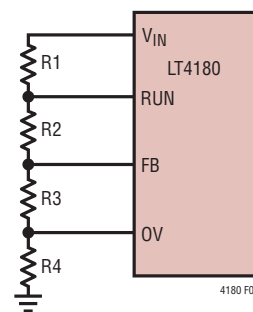


Figure 7. Voltage Divider for Output Voltage, UVL and OVL

## APPLICATIONS INFORMATION

The voltage divider resistors can be calculated from the following equations:

$$R_T = \frac{V_{OV}}{200\mu A}, R_4 = \frac{1.22V}{200\mu A}$$

Where  $R_T$  is the total divider resistance and  $V_{OV}$  is the overvoltage set point.

Find the equivalent series resistance for R2 and R3 ( $R_{SERIES}$ ). This resistance will determine the RUN voltage level.

$$R_{SERIES} = \left( \frac{1.22 \cdot R_T}{V_{UVL}} \right) - R_4$$

$$R_1 = R_T - R_{SERIES} - R_4$$

$$R_3 = \frac{1.22V - \left( V_{OUT(NOM)} \cdot \frac{R_4}{R_T} \right)}{\frac{V_{OUT(NOM)}}{R_T}}$$

$$R_2 = R_{SERIES} - R_3$$

Where  $V_{UVL}$  is the RUN voltage and  $V_{OUT(NOM)}$  is the nominal output voltage desired.

For example, with  $V_{UVL} = 4V$ ,  $V_{OV} = 7.5V$  and  $V_{OUT(NOM)} = 5V$ ,

$$R_T = \frac{7.5V}{200\mu A} = 37.5k$$

$$R_4 = \frac{1.22V}{200\mu A} = 6.1k$$

$$R_{SERIES} = \left( \frac{1.22V \cdot 37.5k}{4V} \right) - 6.1k = 5.34k$$

$$R_1 = 37.5k - 5.34k - 6.1k = 26.06k$$

$$R_3 = \frac{1.22V - \left( \frac{5V \cdot 6.1k}{37.5k} \right)}{\frac{5V}{37.5k}} = 3.05k$$

$$R_2 = R_{SERIES} - R_3 = 2.29k$$

### R<sub>SENSE</sub> SELECTION

Select the value of  $R_{SENSE}$  so that it produces a 100mV voltage drop at maximum load current. For best accuracy,  $V_{IN}$  and SENSE should be Kelvin connected to this resistor.

### Soft-Correct Operation

The LT4180 has a soft-correct function which insures orderly start-up. When the RUN pin rising threshold is first exceeded (indicating  $V_{IN}$  has crossed its undervoltage lockout threshold), power supply output voltage is set to a value corresponding to zero wiring voltage drop (no correction for wiring). Over a period of time (determined by  $CHOLD4$ ), the power supply output voltage ramps up to account for wiring voltage drops, providing best load-end voltage regulation. A new soft-correct cycle is also initiated whenever an overvoltage condition occurs.

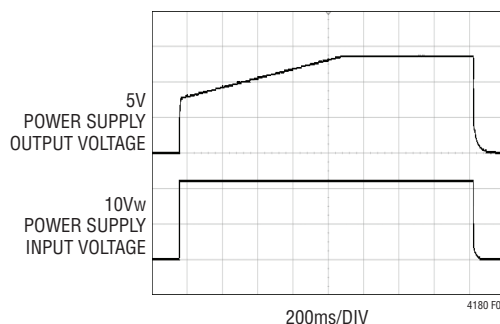


Figure 8. Soft-Correct Operation,  $C_{HOLD4} = 1\mu F$

## APPLICATIONS INFORMATION

### Using Guard Rings

The LT4180 includes a total of four track/holds in the Virtual Remote Sense path. For best accuracy, all leakage sources on the CHOLD pins should be minimized.

At very low dither frequencies, the circuit board layout may include guard rings which should be tied to their respective guard ring drivers.

To better understand the purpose of guard rings, a simplified model of hold capacitor leakage (with and without guard rings) is shown in Figure 9. Without guard rings, a large difference voltage may exist between the hold capacitor (Pin 1) node and adjacent conductors (Pin 2) producing substantial leakage current through the leakage resistance ( $R_{LKG}$ ). By adding a guard ring driver with approximately the same voltage as the voltage on the hold capacitor node, the difference voltage across  $R_{LKG1}$  is reduced substantially thereby reducing leakage current on the hold capacitor.

### Synchronization

Linear and switching power supplies and regulators may be used with the LT4180. In most applications regulator interference should be negligible. For those applications where accurate control of interference spectrum is desirable, an oscillator output has been provided so that

switching supplies may be synchronized to the LT4180 (Figure 10). The OSC pin was designed so that it may directly connect to most regulators, or drive opto-isolators (for isolated power supplies).

### Spread Spectrum Operation

Virtual remote sensing relies on sampling techniques. Because switching power supplies are commonly used, the LT4180 uses a variety of techniques to minimize potential interference (in the form of beat notes which may occur between the dither frequency and power supply switching frequency). Besides several types of internal filtering, and the option for VRS/power supply synchronization, the LT4180 also provides spread spectrum operation.

By enabling spread spectrum operation, low modulation index pseudo-random phasing is applied to Virtual Remote Sense timing. This has the effect of converting any remaining narrow-band interference into broadband noise, reducing its effect.

### Increasing Voltage Correction Range

Correction range may be slightly improved by regulating  $INTV_{CC}$  to 5V. This may be done by placing an LDO between  $V_{IN}$  and  $INTV_{CC}$ . Contact Linear Technology Applications for more information.

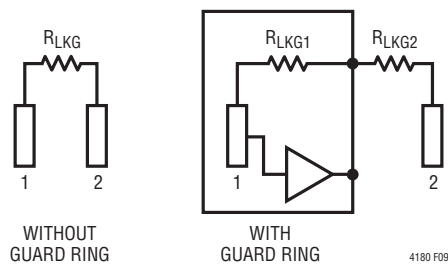


Figure 9. Simplified Leakage Models (with and without Guard Rings)

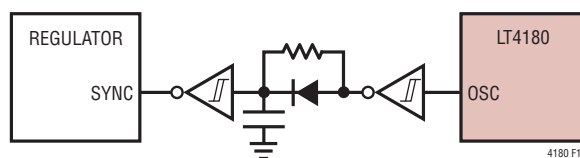
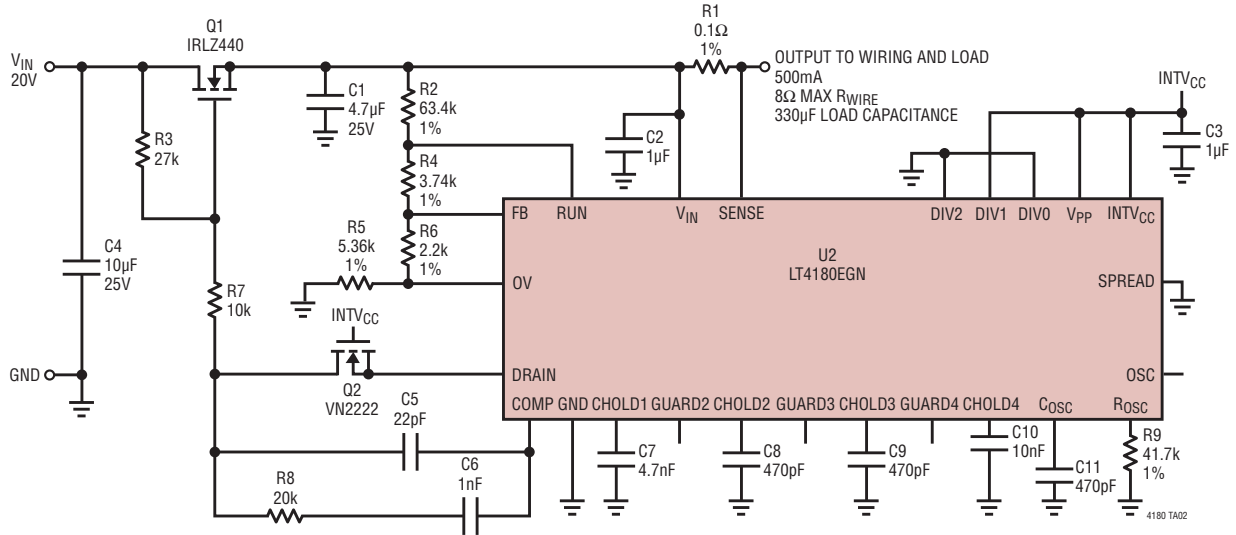


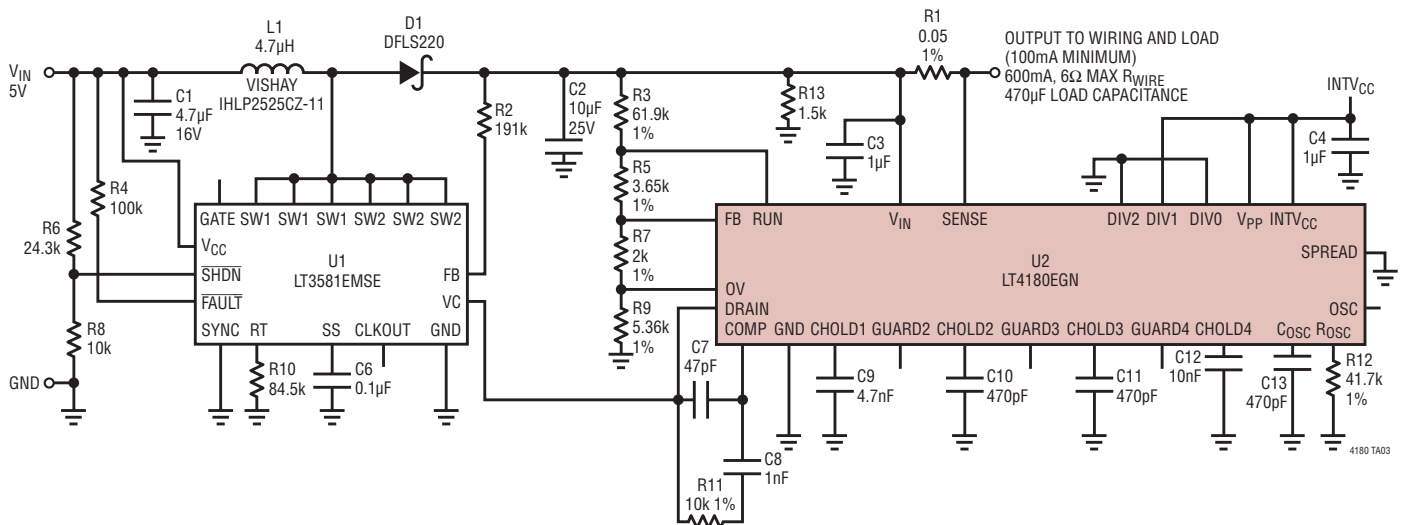
Figure 10. Clock Interface for Synchronization

TYPICAL APPLICATIONS

12V, 500mA Linear Regulator

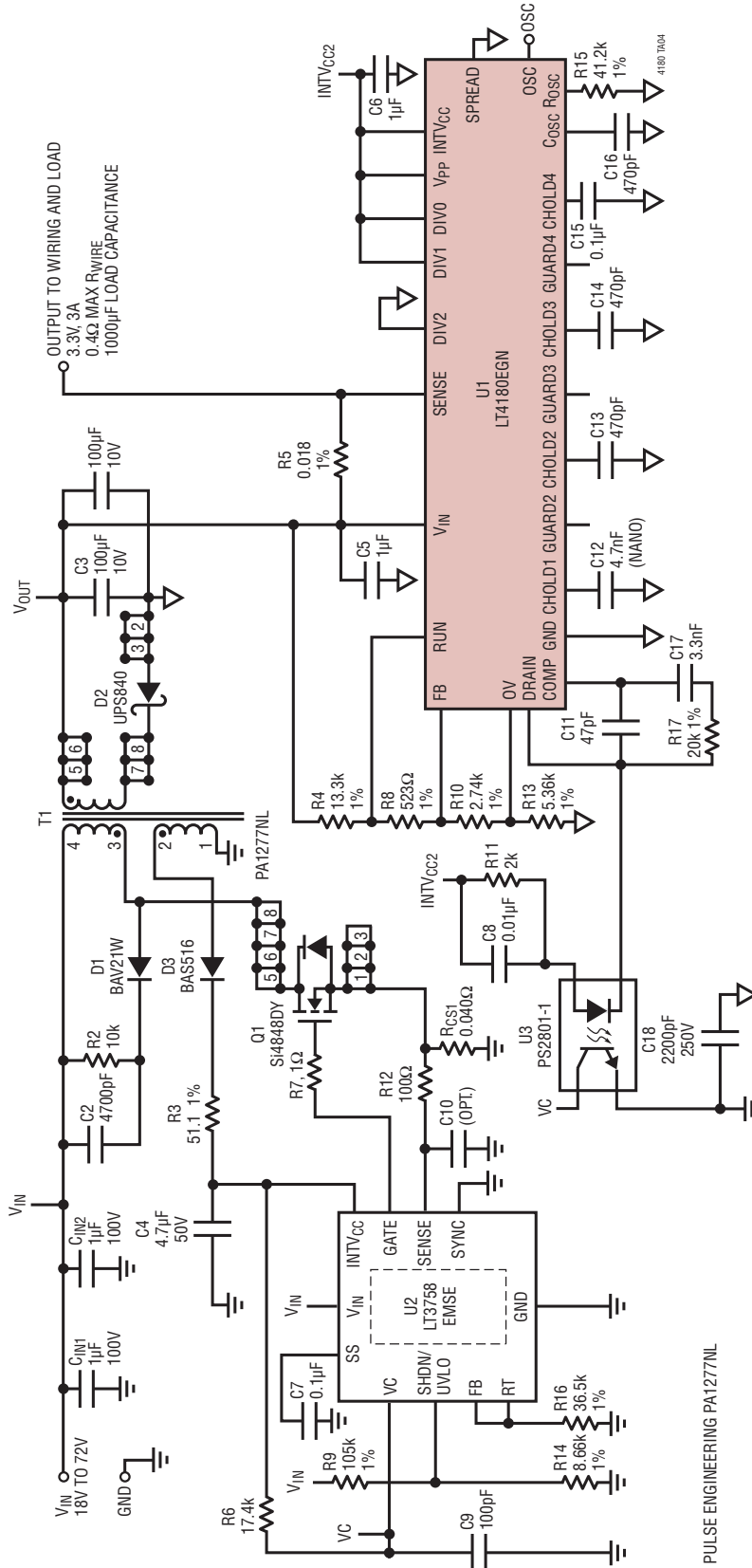


12V, 600mA Boost Regulator



TYPICAL APPLICATIONS

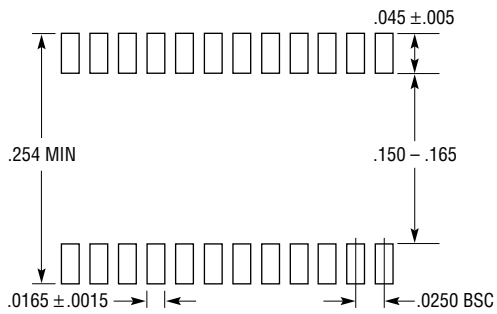
3.3V Isolated Flyback Regulator



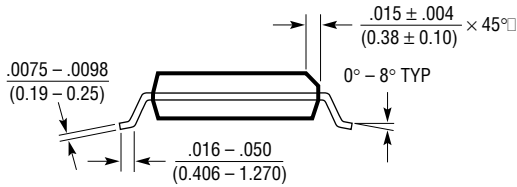
PULSE ENGINEERING PA1277NL

# PACKAGE DESCRIPTION

**GN Package**  
**24-Lead Plastic SSOP (Narrow .150 Inch)**  
 (Reference LTC DWG # 05-08-1641)

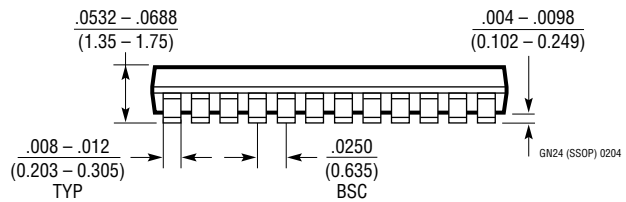
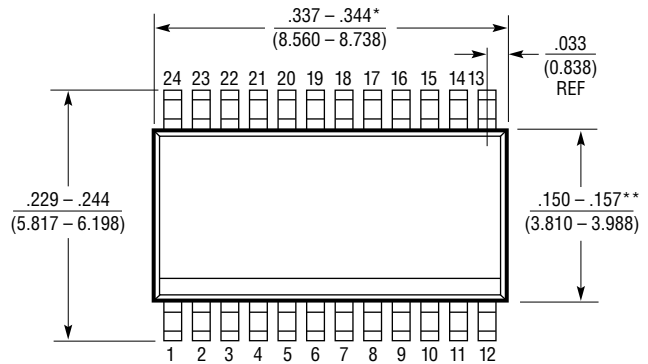


RECOMMENDED SOLDER PAD LAYOUT



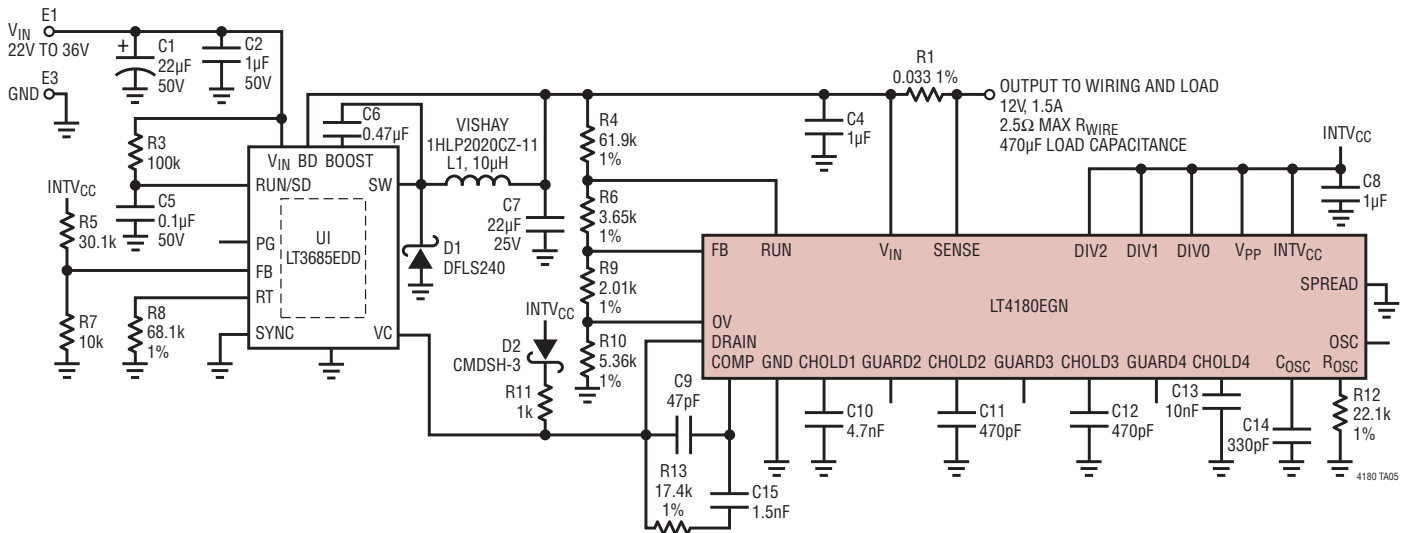
NOTE:

1. CONTROLLING DIMENSION: INCHES
  2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
  3. DRAWING NOT TO SCALE
- \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006\* (0.152mm) PER SIDE
- \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010\* (0.254mm) PER SIDE



## TYPICAL APPLICATION

### 12V 1.5A Buck Regulator



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3581	Boost/Inverting DC/DC Converter with 3.3A Switch, Soft-Start and Synchronization	$2.5V \leq V_{IN} \leq 22V$ , Current Mode Control, 200kHz to 2.5MHz, MSOP-16E and 3mm × 4mm DFN-14 Packages
LT3685	36V, 2A, 2.4MHz Step-Down Switching Regulator	$3.6V \leq V_{IN} \leq 36V$ (60V <sub>PK</sub> ), Integrated Boost Diode, MSOP-10E and 3mm × 3mm DFN Packages
LT3573	Isolated Flyback Switching Regulator with 60V Integrated Switch	$3V \leq V_{IN} \leq 40V$ , Up to 7W, No Opto-Isolator or Third Winding Required, MSOP-16E Package
LT3757	Boost, Flyback, SEPIC and Inverting Controller	$2.9V \leq V_{IN} \leq 40V$ , Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, MSOP-10E and 3mm × 3mm DFN-10 Packages
LT3758	Boost, Flyback, SEPIC and Inverting Controller	$5.5V \leq V_{IN} \leq 100V$ , Current Mode Control, 100kHz to 1MHz Programmable Operation Frequency, MSOP-10E and 3mm × 3mm DFN-10 Packages
LTC3805/ LTC3805-5	Adjustable Fixed 70kHz to 700kHz Operating Frequency Flyback Controller	$V_{IN}$ and $V_{OUT}$ Limited Only by External Components, MSOP-10E and 3mm × 3mm DFN-10 Packages