LT1055/LT1056

Precision, High Speed, JFET Input Operational Amplifiers

FEATURES

- *Guaranteed* Offset Voltage: 150µV Max
  - −55°C to 125°C: 500µV Max
- *Guaranteed* Drift: 4µV/°C Max
- *Guaranteed* Bias Current
  - 70°C: 150pA Max
  - 125°C: 2.5nA Max
- *Guaranteed* Slew Rate: 12V/µs Min
- Available in 8-Pin PDIP and SO Packages

APPLICATIONS

- Precision, High Speed Instrumentation
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters
- Fast, Precision Sample-and-Hold

DESCRIPTION

The LT®1055/LT1056 JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/µs slew rate and 6.5MHz gain bandwidth product are simultaneously achieved with offset voltage of typically 50µV, 1.2µV/°C drift, bias currents of 40pA at 70°C and 500pA at 125°C.

The 150µV maximum offset voltage specification is the best available on any JFET input operational amplifier.

The LT1055 and LT1056 are differentiated by their operating currents. The lower power dissipation LT1055 achieves lower bias and offset currents and offset voltage. The additional power dissipation of the LT1056 permits higher slew rate, bandwidth and faster settling time with a slight sacrifice in DC performance.

The voltage-to-frequency converter shown below is one of the many applications which utilize both the precision and high speed of the LT1055/LT1056.

For a JFET input op amp with 23V/µs guaranteed slew rate, refer to the LT1022 data sheet.

TYPICAL APPLICATION

1Hz to 10kHz Voltage-to-Frequency Converter

THE LOW OFFSET VOLTAGE OF LT1056 CONTRIBUTES ONLY 0.1Hz OF ERROR WHILE ITS HIGH SLEW RATE PERMITS 10kHz OPERATION.

= 1N4148

*1% FILM

LT1055/56 TA01

Distribution of Input Offset Voltage (H Package)

$V_S = \pm15V$
$T_A = 25°C$
634 UNITS TESTED FROM THREE RUNS
50% TO ±60µV
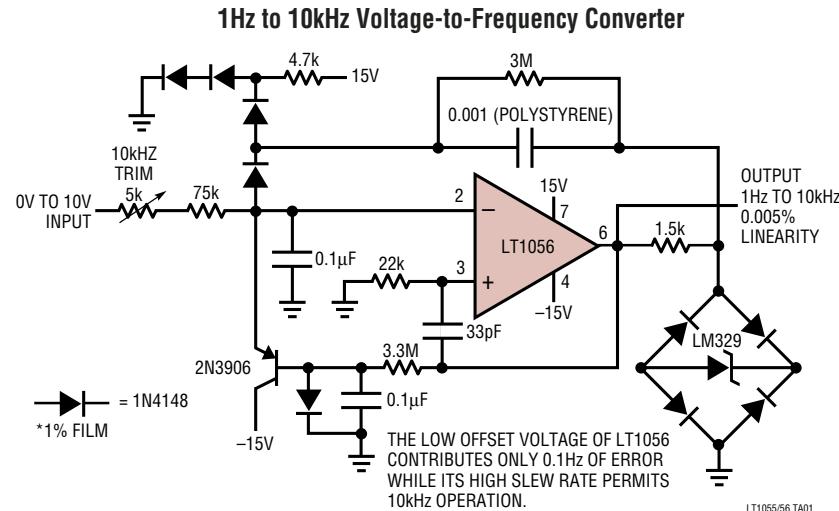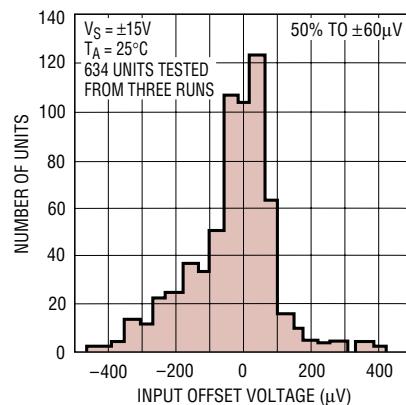
LT1055/56 TA02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage .... ±20V
Differential Input Voltage .... ±40V
Input Voltage .... ±20V
Output Short-Circuit Duration .... Indefinite
Operating Temperature Range
　LT1055AM/LT1055M/LT1056AM/
　LT1056M **(OBSOLETE)** .... −55°C to 125°C

LT1055AC/LT1055C/LT1056AC/
　LT1056C .... 0°C to 70°C
Storage Temperature Range
　All Devices .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER
BAL 1 ☐ ☐ 8 N/C −IN 2 ☐ ☐ 7 V⁺ +IN 3 ☐ ☐ 6 OUT V⁻ 4 ☐ ☐ 5 BAL N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 150°C$, $\theta_{JA} = 130°C/W$	LT1055CN8 LT1056CN8

TOP VIEW	ORDER PART NUMBER
BAL 1 ☐ ☐ 8 N/C −IN 2 ☐ ☐ 7 V⁺ +IN 3 ☐ ☐ 6 OUT V⁻ 4 ☐ ☐ 5 BAL S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150°C$, $\theta_{JA} = 150°C/W$	LT1055S8 LT1056S8
	S8 PART MARKING 1055 1056

TOP VIEW	ORDER PART NUMBER	
NC 8 BALANCE 1　7 V⁺ −IN 2　6 OUT +IN 3　5 BALANCE 4 V⁻ H PACKAGE 8-LEAD TO-5 METAL CAN $T_{JMAX} = 150°C$, $\theta_{JA} = 150°C/W$, $\theta_{JC} = 45°C/W$	LT1055ACH LT1055CH LT1055AMH LT1055MH	LT1056ACH LT1056CH LT1056AMH LT1056MH
	OBSOLETE PACKAGE Consider the N8 Package for Alternate Source	

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF　Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $T_A = 25°C$. $V_S = ±15V$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM/LT1056AM LT1055AC/LT1056AC			LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 2)	LT1055 H Package	—	50	150	—	70	400	μV
		LT1056 H Package	—	50	180	—	70	450	μV
		LT1055 N8 Package	—	—	—	—	120	700	μV
		LT1056 N8 Package	—	—	—	—	140	800	μV
I_{OS}	Input Offset Current	Fully Warmed Up	—	2	10	—	2	20	pA

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ELECTRICAL CHARACTERISTICS $T_A = 25°C$. $V_S = ±15V$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1055AM/LT1056AM LT1055AC/LT1056AC			LT1055M/LT1056M LT1055CH/LT1056CH LT1055CN8/LT1056CN8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_B	Input Bias Current	Fully Warmed Up	—	±10	±50	—	±10	±50	pA
		$V_{CM} = 10V$	—	30	130	—	30	150	pA
	Input Resistance:Differential		—	10^{12}	—	—	10^{12}	—	Ω
	Common Mode	$V_{CM} = -11V$ to $8V$	—	10^{12}	—	—	10^{12}	—	Ω
		$V_{CM} = 8V$ to $11V$	—	10^{11}	—	—	10^{11}	—	Ω
	Input Capacitance		—	4	—	—	4	—	pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1055	—	1.8	—	—	2.0	—	μV_{P-P}
		LT1056	—	2.5	—	—	2.8	—	μV_{P-P}
	Input Noise Voltage Density	$f_0 = 10Hz$ (Note 3)	—	28	50	—	30	60	$nV/\sqrt{Hz}$
		$f_0 = 1kHz$ (Note 4)	—	14	20	—	15	22	$nV/\sqrt{Hz}$
I_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$ (Note 5)	—	1.8	4	—	1.8	4	$fA/\sqrt{Hz}$
A_{VOL}	Large-Signal Voltage Gain	$V_0 = ±10V$ $R_L = 2k$	150	400	—	120	400	—	V/mV
		$R_L = 1k$	130	300	—	100	300	—	V/mV
	Input Voltage Range		±11	±12	—	±11	±12	—	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±11V$	86	100	—	83	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = ±10V$ to $±18V$	90	106	—	88	104	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±12	±13.2	—	±12	±13.2	—	V
SR	Slew Rate	LT1055	10	13	—	7.5	12	—	V/μs
		LT1056	12	16	—	9.0	14	—	V/μs
GBW	Gain Bandwidth Product	$f = 1MHz$ LT1055	—	5.0	—	—	4.5	—	MHz
		LT1056	—	6.5	—	—	5.5	—	MHz
I_S	Supply Current	LT1055	—	2.8	4.0	—	2.8	4.0	mA
		LT1056	—	5.0	6.5	—	5.0	7.0	mA
	Offset Voltage Adjustment Range	$R_{POT} = 100k$	—	±5	—	—	±5	—	mV

The ● denotes the specifications which apply over the temperature range $0°C \leq T_A \leq 70°C$.
$V_S = ±15V$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055AC LT1056AC			LT1055CH/LT1056CH LT1055CN8/LT1056CN8			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage (Note 2)	LT1055 H Package	●	—	100	330	—	140	750	μV
		LT1056 H Package	●	—	100	360	—	140	800	μV
		LT1055 N8 Package	●	—	—	—	—	250	1250	μV
		LT1056 N8 Package	●	—	—	—	—	280	1350	μV
	Average Temperature Coefficient of Input Offset Voltage	H Package (Note 6)	●	—	1.2	4.0	—	1.6	8.0	μV/°C
		N8 Package (Note 6)	●	—	—	—	—	3.0	12.0	μV/°C
I_{OS}	Input Offset Current	Warmed Up LT1055	●	—	10	50	—	16	80	pA
		$T_A = 70°C$ LT1056	●	—	14	70	—	18	100	pA
I_B	Input Bias Current	Warmed Up LT1055	●	—	±30	±150	—	±40	±200	pA
		$T_A = 70°C$ LT1056	●	—	±40	±80	—	±50	±240	pA
A_{VOL}	Large-Signal Voltage Gain	$V_0 = ±10V$, $R_L = 2k$	●	80	250	—	60	250	—	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = ±10.5V$	●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = ±10V$ to $±18V$	●	89	105	—	87	103	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.1	—	±12	±13.1	—	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range −55°C ≤ T_A ≤ 125°C. V_S = ±15V, V_{CM} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			LT1055AM LT1056AM MIN	TYP	MAX	LT1055M LT1056M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 2)	LT1055		●	—	180	500	—	250	1200	μV
		LT1056		●	—	180	550	—	250	1250	μV
	Average Temperature Coefficient of Input Offset Voltage	(Note 6)		●	—	1.3	4.0	—	1.8	8.0	μV/°C
I_{OS}	Input Offset Current	Warmed Up	LT1055	●	—	0.20	1.2	—	0.25	1.8	nA
		T_A = 125°C	LT1056	●	—	0.25	1.5	—	0.30	2.4	nA
I_B	Input Bias Current	Warmed Up	LT1055	●	—	±0.4	±2.5	—	±0.5	±4.0	nA
		T_A = 125°C	LT1056	●	—	±0.5	±3.0	—	±0.6	±5.0	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V, R_L = 2k		●	40	120	—	35	120	—	V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10.5V		●	85	100	—	82	98	—	dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±17V		●	88	104	—	86	102	—	dB
V_{OUT}	Output Voltage Swing	R_L = 2k		●	±12	±12.9	—	±12	±12.9	—	V

T_A = 25°C. V_S = ±15V, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055CS8/LT1056CS8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 2)				500	1500	μV
I_{OS}	Input Offset Current	Fully Warmed Up			5	30	pA
I_B	Input Bias Current	Fully Warmed Up			±30	±100	pA
		V_{CM} = 10V			30	150	pA
	Input Resistance Differential				0.4		TΩ
	Common Mode	V_{CM} = −11V to 8V			0.4		TΩ
		V_{CM} = 8V to 11V			0.05		TΩ
	Input Capacitance				4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz	LT1055		2.5		μV$_{P-P}$
			LT1056		3.5		μV$_{P-P}$
	Input Noise Voltage Density	f_O = 10Hz (Note 4)			35	70	nV/√Hz
		f_O = 1kHz (Note 4)			15	22	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, 1kHz (Note 5)			2.5	10	fA/√Hz
A_{VOL}	Large-Signal Voltage Gain	V_O = ±10V	R_L = 2k	120	400		V/mV
			R_L = 1k	100	300		V/mV
	Input Voltage Range			±11	±12		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±11V		83	98		dB
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V		88	104		dB
V_{OUT}	Output Voltage Swing	R_L = 2K		±12	±13.2		V
SR	Slew Rate		LT1055	7.5	12		V/μs
			LT1056	9.0	14		V/μs
GBW	Gain Bandwidth Product	f = 1MHz	LT1055		4.5		MHz
			LT1056		5.5		MHz
I_S	Supply Current		LT1055		2.8	4.0	mA
			LT1056		5.0	7.0	mA
	Offset Voltage Adjustment Range	R_{POT} = 100k			±5		mV

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $0°C \leq T_A \leq 70°C$. $V_S = \pm15V$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1055CS8/LT1056CS8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (Note 2)		●		800	2200	μV
	Average Temperature Coefficient of Input Offset Voltage		●		4	15	μV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70°C$	●		18	150	pA
I_B	Input Bias Current	Warmed Up, $T_A = 70°C$	●		±60	±400	pA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm10V$, $R_L = 2k$	●	60	250		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm10.5V$	●	82	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm10V$ to $\pm18V$	●	87	103		dB
V_{OUT}	Output Voltage Swing	$R_L = 2K$	●	±12	±13.1		V

For MIL-STD components, please refer to LTC883 data sheet for test listing and parameters.

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power; (b) at $T_A = 25°C$ only, with the chip heated to approximately 38°C for the LT1055 and to 45°C for the LT1056, to account for chip temperature rise when the device is fully warmed up.

Note 3: 10Hz noise voltage density is sample tested on every lot of A grades. Devices 100% tested at 10Hz are available on request.

Note 4: This parameter is tested on a sample basis only.

Note 5: Current noise is calculated from the formula: $i_n = (2qI_B)^{1/2}$, where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 6: Offset voltage drift with temperature is practically unchanged when the offset voltage is trimmed to zero with a 100k potentiometer between the balance terminals and the wiper tied to V^+. Devices tested to tighter drift specifications are available on request.

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TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias and Offset Currents vs Temperature
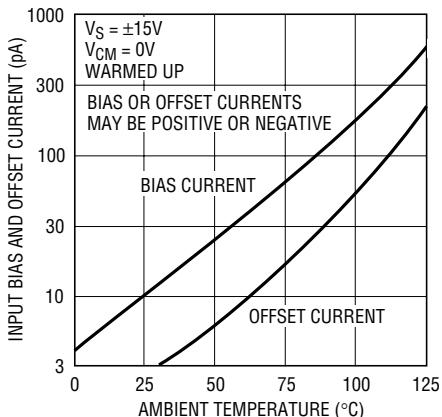
LT1055/56 G01

Input Bias Current Over the Common Mode Range

A = POSITIVE INPUT CURRENT
B = NEGATIVE INPUT CURRENT
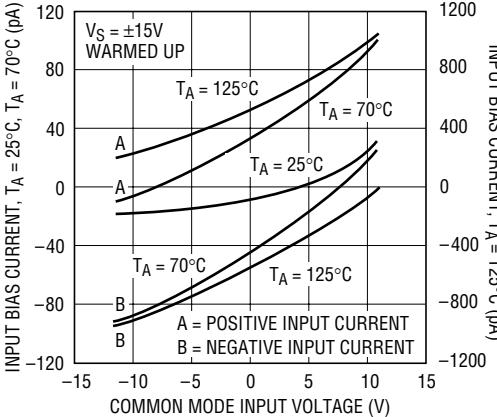
LT1055/56 G02

Distribution of Input Offset Voltage (N8 Package)
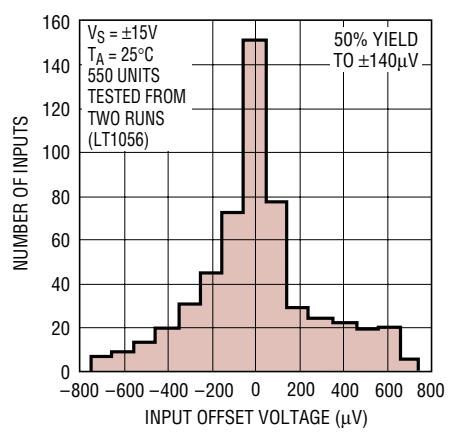
LT1055/56 G03

Distribution of Offset Voltage Drift with Temperature (H Package)*

OFFSET VOLTAGE DRIFT WITH TEMPERATURE (µV/°C)
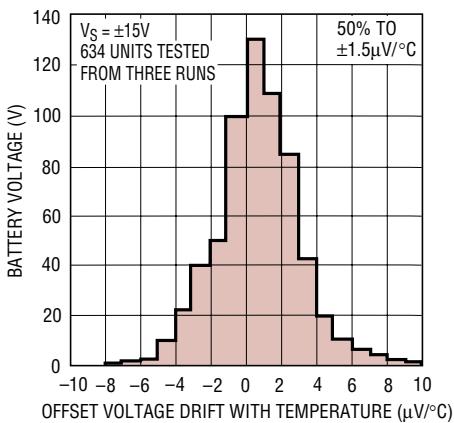
*DISTRIBUTION IN THE PLASTIC (N8) PACKAGE IS SIGNIFICANTLY WIDER.

LT1055/56 G04

Warm-Up Drift
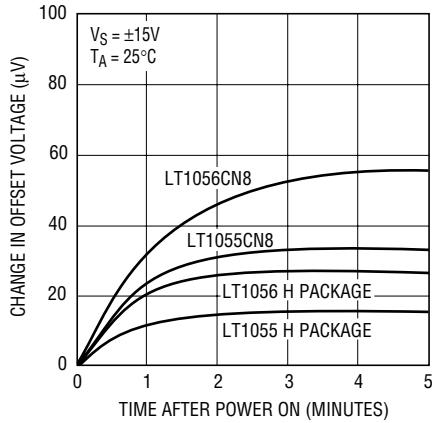
LT1055/56 G05

Long Term Drift of Representative Units
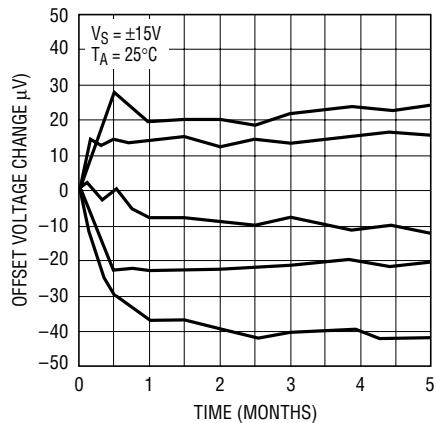
LT1055/56 G06

0.1Hz to 10Hz Noise
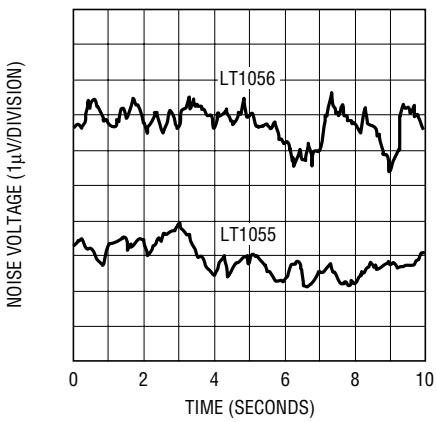
LT1055/56 G07

Noise vs Chip Temperature
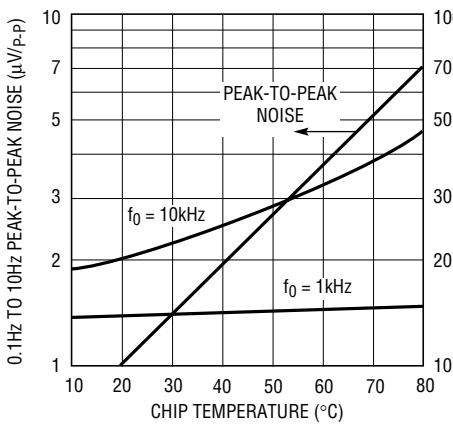
LT1055/56 G08

Voltage Noise vs Frequency

LT1055/56 G09

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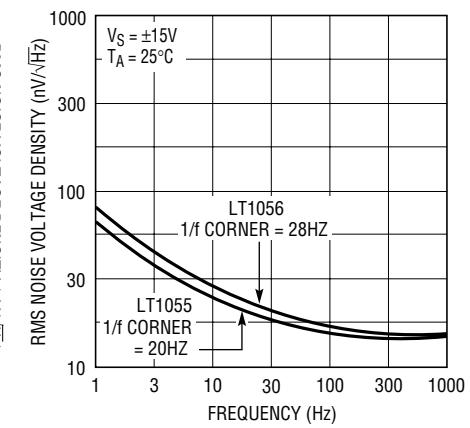
TYPICAL PERFORMANCE CHARACTERISTICS

LT1056 Large-Signal Response
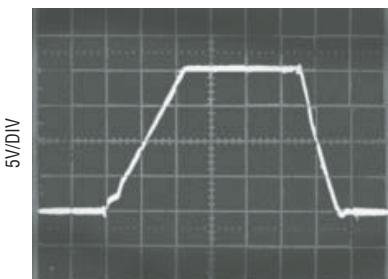
$A_V = 1$, $C_L = 100pF$, $0.5\mu s$/DIV

LT1055/56 G10

**Small-Signal Response**
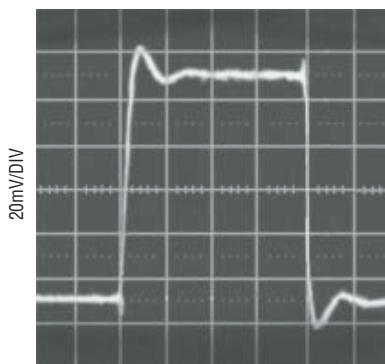
$A_V = 1$, $C_L = 100pF$, $0.2\mu s$/DIV

LT1055/56 G11

LT1055 Large-Signal Response
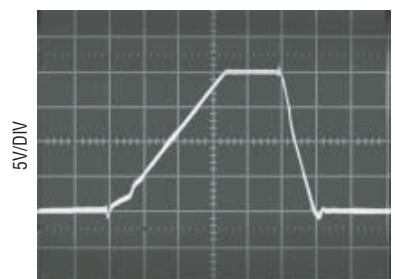
$A_V = 1$, $C_L = 100pF$, $0.5\mu s$/DIV

LT1055/56 G12

Undistorted Output Swing vs Frequency
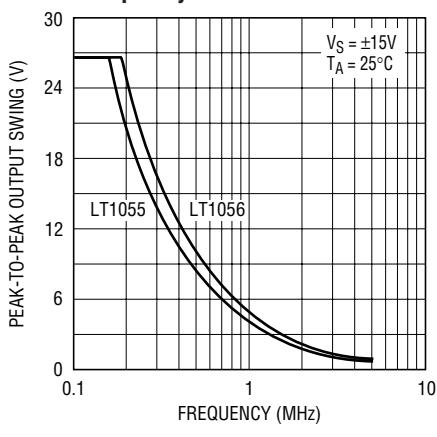
LT1055/56 G13

Slew Rate, Gain Bandwidth vs Temperature
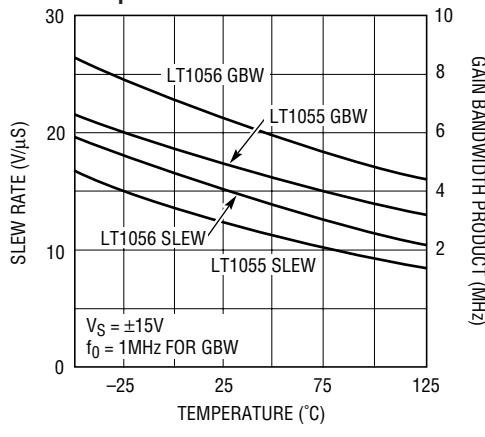
LT1055/56 G14

Output Impedence vs Frequency
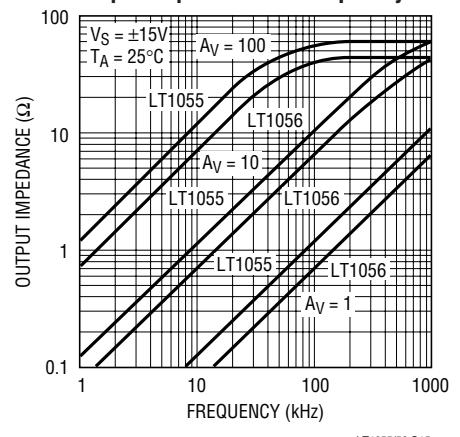
LT1055/56 G15

Gain vs Frequency
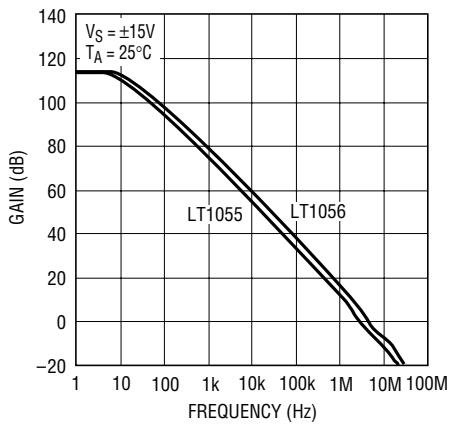
LT1055/56 G16

Gain, Phase Shift vs Frequency
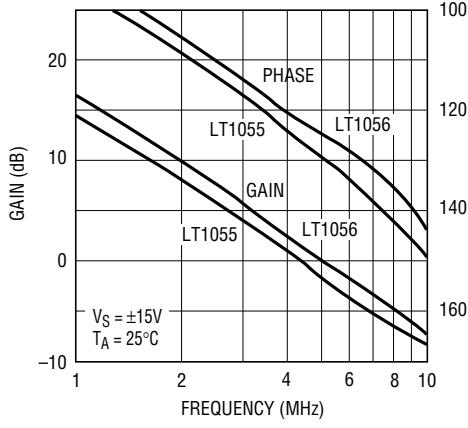
LT1055/56 G17

Voltage Gain vs Temperature
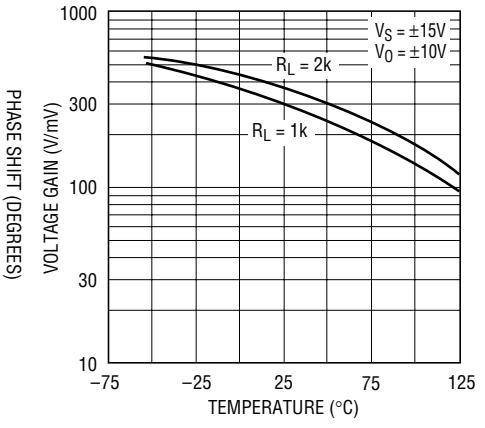
LT1055/56 G18

TYPICAL PERFORMANCE CHARACTERISTICS

LT1055 Settling Time

LT1055/56 G19
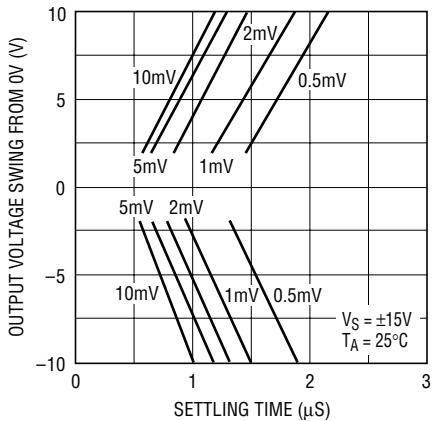
LT1056 Settling Time

LT1055/56 G20
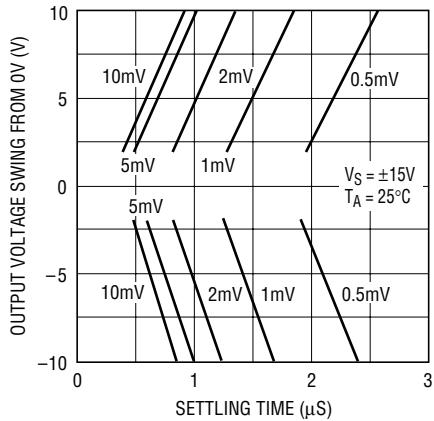
Common Mode Range vs Temperature

LT1055/56 G21
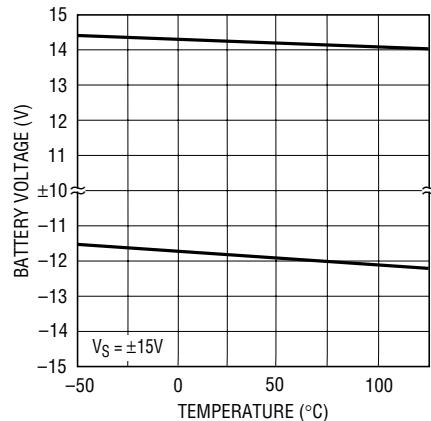
Common Mode and Power Supply Rejections vs Temperature
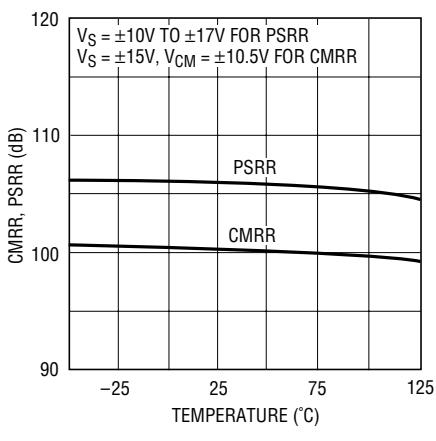
LT1055/56 G22

Common Mode Rejection Ratio vs Frequency

LT1055/56 G23

Power Supply Rejection Ratio vs Frequency

LT1055/56 G24
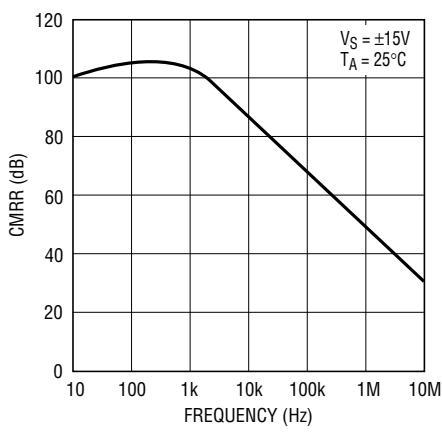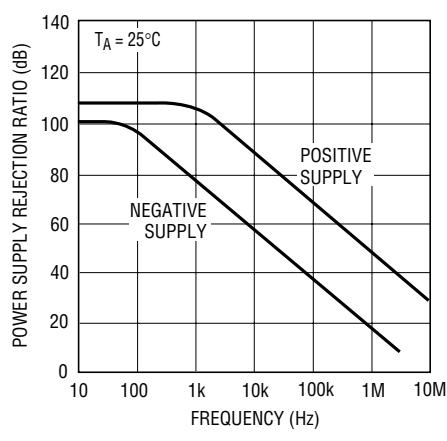
Supply Current vs Supply Voltage

LT1055/56 G25
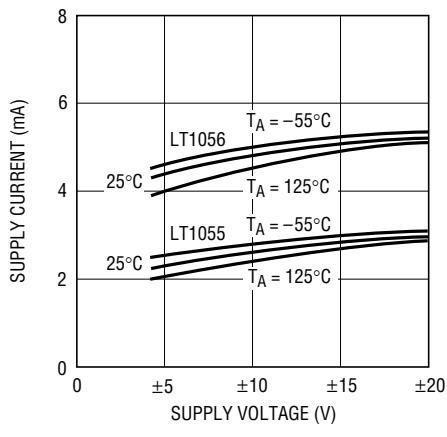
Output Swing vs Load Resistance

LT1055/56 G26
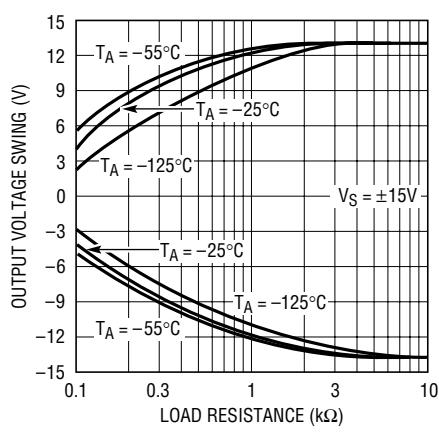
Short-Circuit Current vs Time

LT1055/56 G27
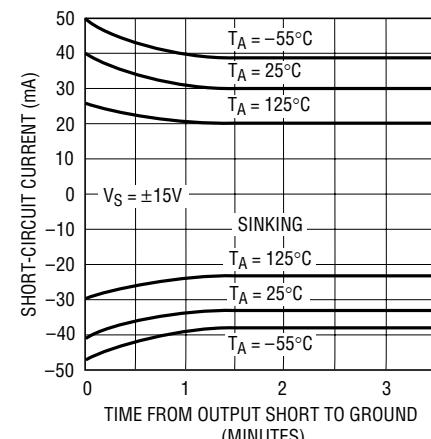
APPLICATIONS INFORMATION

The LT1055/LT1056 may be inserted directly into LF155A/ LT355A, LF156A/LT356A, OP-15 and OP-16 sockets. Off-set nulling will be compatible with these devices with the wiper of the potentiometer tied to the positive supply.

Offset Nulling

LT1055/56 AI1

LT1055/56 AI2
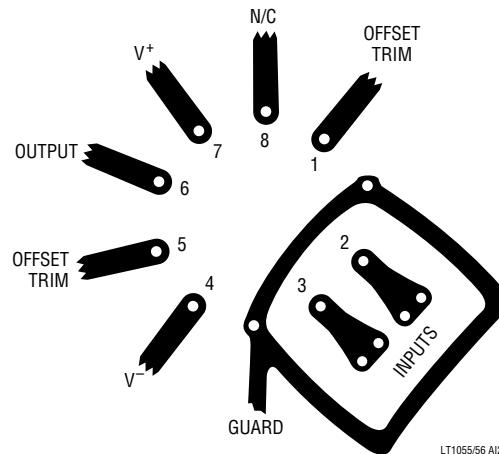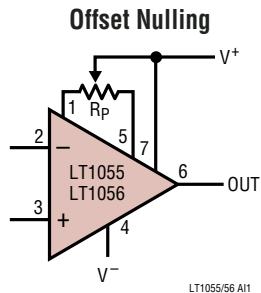
No appreciable change in offset voltage drift with temperature will occur when the device is nulled with a potentiometer, R_P, ranging from 10k to 200k.

The LT1055/LT1056 can also be used in LF351, LF411, AD547, AD611, OPA-111, and TL081 sockets, provided that the nulling cicuitry is removed. Because of the LT1055/ LT1056's low offset voltage, nulling will not be necessary in most applications.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere-microvolt level accuracy of the LT1055/LT1056 proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g. Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground, in noninverting connnections to the inverting input at pin 2. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Teflon is a trademark of Dupont.

The LT1055/LT1056 has the lowest offset voltage of any JFET input op amp available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers because the transconductance of FETs is considerably lower than that of bipolar transistors. Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 20μV hysteresis (30μV on the M grades) when cycled over the −55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than 10μV) hysteresis effect.

The offset voltage and drift performance are also affected by packaging. In the plastic N8 package the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device matching and drift are degraded. Consequently, for best DC performance, as shown in the typical performance distribution plots, the TO-5 H package is recommended.

Noise Performance

The current noise of the LT1055/LT1056 is practically immeasurable at 1.8fA/√Hz. At 25°C it is negligible up to 1G of source resistance, R_S (compound to the noise of R_S). Even at 125°C it is negligible to 100M of R_S.

APPLICATIONS INFORMATION

The voltage noise spectrum is characterized by a low 1/f corner in the 20Hz to 30Hz range, significantly lower than on other competitive JFET input op amps. Of particular interest is the fact that with any JFET IC amplifier, the frequency location of the 1/f corner is proportional to the square root of the internal gate leakage currents and, therefore, noise doubles every 20°C. Furthermore, as illustrated in the noise versus chip temperature curves, the 0.1Hz to 10Hz peak-to-peak noise is a strong function of temperature, while wideband noise (f_0 = 1kHz) is practically unaffected by temperature.

Consequently, for optimum low frequency noise, chip temperature should be minimized. For example, operating an LT1056 at ±5V supplies or with a 20°C/W case-to-ambient heat sink reduces 0.1Hz to 10Hz noise from typically 2.5μV$_{P-P}$ (±15V, free-air) to 1.5μV$_{P-P}$. Similiarly, the noise of an LT1055 will be 1.8μV$_{P-P}$ typically because of its lower power dissipation and chip temperature.

High Speed Operation

Settling time is measured in the test circuit shown. This test configuration has two features which eliminate problems common to settling time measurments: (1) probe

capacitance is isolated from the "false summing" node, and (2) it does not require a "flat top" input pulse since the input pulse is merely used to steer current through the diode bridges. For more details, please see Application Note 10.

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed-loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With R_S ($C_S + C_{IN}$) = $R_F C_F$, the effect of the feedback pole is completely removed.
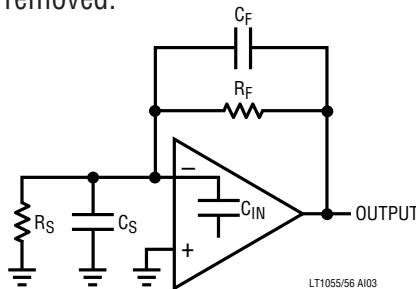
Settling Time Test Circuit
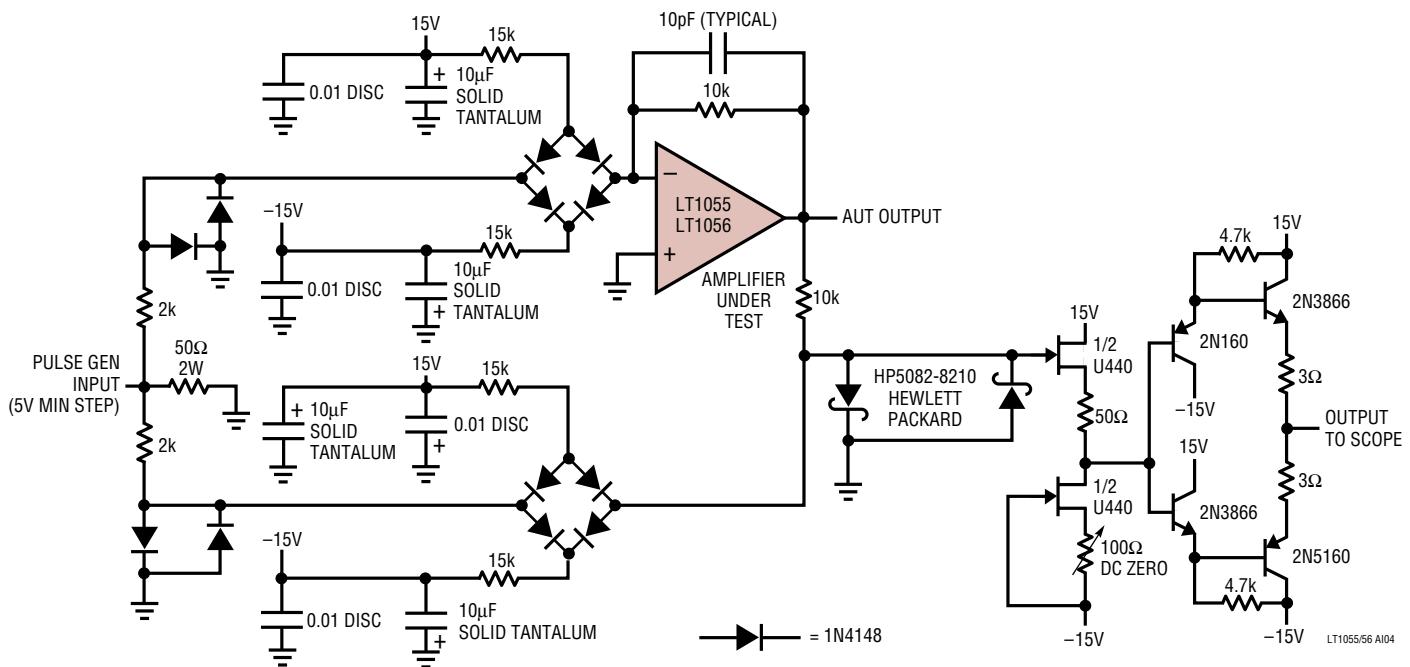
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APPLICATIONS INFORMATION

Phase Reversal Protection

Most industry standard JFET input op amps (e.g., LF155/LF156, LF351, LF411, OP15/16) exhibit phase reversal at the output when the negitive common mode limit at the input is exceeded (i.e., from −12V to −15V with ±15V supplies). This can cause lock-up in servo systems. As shown below, the LT1055/LT1056 does not have this problem due to unique phase reversal protection circuitry (Q1 on simplified schematic).
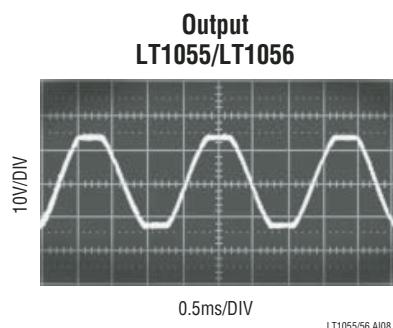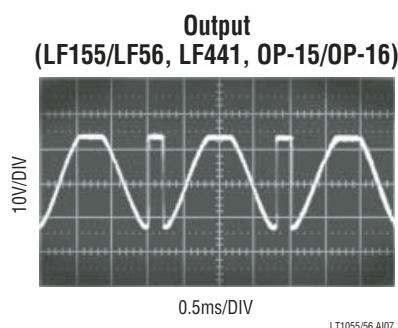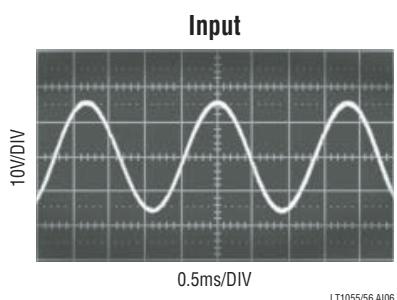
Voltage Follower with Input Exceeding the Negative Common Mode Range

LT1055/56 AI05

Input

10V/DIV

0.5ms/DIV

LT1055/56 AI06

**Output
(LF155/LF56, LF441, OP-15/OP-16)**

10V/DIV

0.5ms/DIV

LT1055/56 AI07

**Output
LT1055/LT1056**

10V/DIV

0.5ms/DIV

LT1055/56 AI08
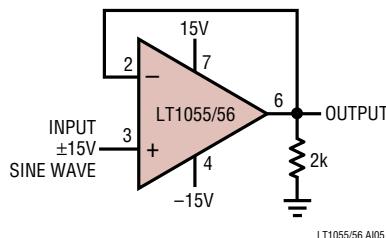
TYPICAL APPLICATIONS †

Exponential Voltage-to-Frequency Converter for Music Synthesizers

SCALE FACTOR
1V IN OCTAVE OUT
*1% METAL FILM RESISTOR
PIN NUMBERED TRANSISTORS = CA3096 ARRAY

TEMPERATURE CONTROL LOOP
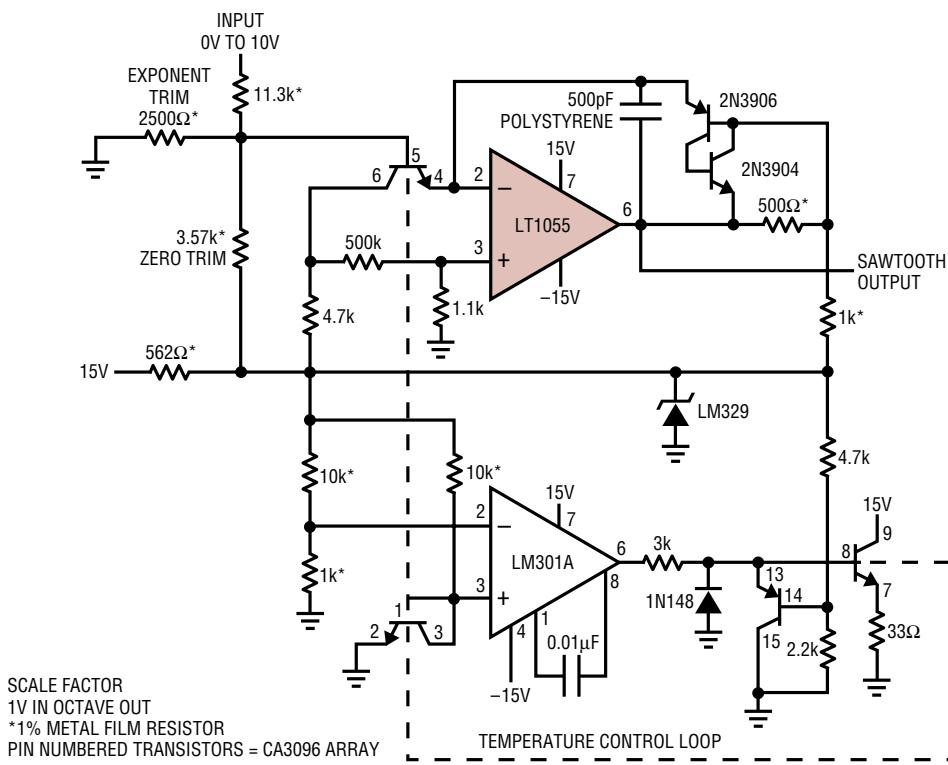
†For ten additional applications utilizing the LT1055 and LT1056, please see the LTC1043 data sheet and Application Note 3.

LT1055/56 TA03

10556fc

11

TYPICAL APPLICATIONS

12-Bit Charge Balance A/D Converter

74C00

28k   14k   0.003μF

0.01

LT1055

2   −   15V   7

3   +   6   1N4148

4   −15V

1N4148

CLK OUTPUT (B)

10k

CLK   74C74

D   Q

P   CL   Q̄

15V   2N3904

OUTPUT (A)

10k

249k*

0V TO 10V INPUT

1N4148   1N4148

33k

COUPLE THERMALLY

LM329

10k

15V

15V   7

6   −   2

LT1001

33k   4   −15V   +   3

CIRCUIT OUTPUT

RATIO $\dfrac{f_{OUT}\ (A)}{f_{CLK}\ (B)}$

1N4148
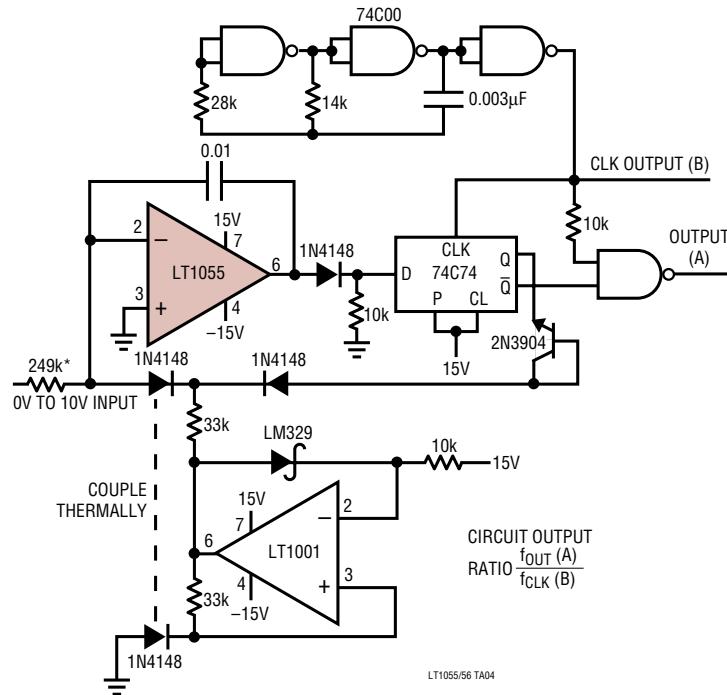
LT1055/56 TA04

Fast "No Trims" 12-Bit Multiplying CMOS DAC Amplifier

REFERENCE IN

TYPICAL 12-BIT CMOS DAC

$R_{FEEDBACK}$

I_{OUT1}

I_{OUT2}

LT1055   −   +

OUTPUT

LT1055/56 TA05

Fast, 16-Bit Current Comparator

HP5082-2810

DELAY = 250ns
* = 1% FILM RESISTOR

15V   4.7k   50k*   2   −   15V   7

INPUT   100k*

LT1056   6   2   +   8

3   +   4   −15V   1   LT1011   7

LT1009 2.5V

15V   3k

OUTPUT

3   −   4   −15V

LT1055/56 TA06

LINEAR TECHNOLOGY

TYPICAL APPLICATIONS

Temperature-to-Frequency Converter

560Ω
15V
1k* 1k*
2N2222
LM329
6.2k*
2N2907
0.01µF
POLYSTYRENE
510pF
2.7k
15V
10k
TTL OUTPUT
0kHz TO 1kHz =
0°C TO 100°C
2N2222
4.7k
500Ω
0°C ADJ
2k
100°C
ADJ
2
−
15V
7
6
LT1055
10k
6.2k*
3
+
4
−15V
820Ω*
LM134
510Ω
2V
137Ω*
*1% FILM RESISTOR

LT1055/56 TA07

100kHz Voltage Controlled Oscillator

*1% FILM RESISTOR
=1N4148
FREQUENCY LINEARITY = 0.1%
FREQUENCY STABILITY = 150ppm/°C
SETTLING TIME = 1.7µs
DISTORTION = 0.25% AT 100kHz,
0.07% AT 10zHz

2
−
15V
7
6
LT1056
3
+
4
−15V
X1 +V +15V
X2 CC SINE OUT
U1 W 2V_RMS
U2 AD639 Z1 0kHs TO 100kHs
COM Z2
VR GT
Y1 UP
Y2 −V −15

22.1k 4.5k
1k
FINE
DISTORTION
TRIMS
68k
10k
68k
−15V

100kHz
DISTORTION
TRIM
9.09k*
2k
10k*
0V TO 10V
INPUT
2
−
15V
7
6
LT1056
3
+
4
−15V
50k
15V
10Hz
DISTORTION
TRIM
−15V
22M
POLYSTYRENE
500pF
15pF
2N4391 2N4391
5k*
2
−
15V
7
6
LT1056
3
+
4
−15V
2.5k*
2N4391
20pF
10k
22k
HP5082-
2810
5k
FREQUENCY
TRIM
10k*
2
+
15V
8
7
LT1011
3
−
4
1
−15V
15V
1k
1k
10k
0.01µF
LM329
4.7k
−15V
4.7k
15V

LT1055/56 TA08

TYPICAL APPLICATIONS

12-Bit Voltage Output D/A Converter

12-BIT CURRENT OUTPUT D/A
CONVERTER (e.g., 6012,565
OR DAC-80)

C_F

2

LT1056

3

15V
7

6

OUTPUT
0V TO 10V

4
−15V

0 TO 2
OR 4mA

C_F = 15pF TO 33pF
SETTLING TIME TO 2mV
(0.8 LSB) = 1.5μs TO 2μs

LT1055/56 TA09

SIMPLIFIED SCHEMATIC

NULL
5

NULL 1

7k   7k

J5   J6

Q7

Q8

7 V⁺

−INPUT 2

+INPUT 3

J1   J2

300Ω

7.5pF   J7

Q9

Q12

Q11

Q15

20Ω

6 OUTPUT

J8

Q1
8k

Q2

200Ω   Q3

Q13

Q14

Q10

J3

J4

Q5

Q16

14k   14k   9pF

Q4

120μA*
(160)

120μA*
(160)

800μA*
(1000)

400μA*
(1100)

3k   50Ω

4 V⁻

*CURRENTS AS SHOWN FOR LT1055. (X) = CURRENTS FOR LT1056.

LT1055/56 SCHM

10556fc

14

PACKAGE DESCRIPTION

H Package
8-Lead TO-5 Metal Can (.200 Inch PCD)
(Reference LTC DWG # 05-08-1320)

0.335 – 0.370
(8.509 – 9.398)
DIA

0.305 – 0.335
(7.747 – 8.509)

0.040
(1.016)
MAX

0.050
(1.270)
MAX

0.165 – 0.185
(4.191 – 4.699)

REFERENCE
PLANE

SEATING
PLANE

GAUGE
PLANE

0.500 – 0.750
(12.700 – 19.050)

0.010 – 0.045*
(0.254 – 1.143)

0.016 – 0.021**
(0.406 – 0.533)

0.027 – 0.045
(0.686 – 1.143)

45°TYP

0.028 – 0.034
(0.711 – 0.864)

PIN 1

0.200
(5.080)
TYP

0.110 – 0.160
(2.794 – 4.064)
INSULATING
STANDOFF

*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE
AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

H8(TO-5) 0.200 PCD 1197

OBSOLETE PACKAGE

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)

.400*
(10.160)
MAX

8 7 6 5

.255 ± .015*
(6.477 ± 0.381)

1 2 3 4

.300 – .325
(7.620 – 8.255)

.045 – .065
(1.143 – 1.651)

.130 ± .005
(3.302 ± 0.127)

.065
(1.651)
TYP

.008 – .015
(0.203 – 0.381)

.120
(3.048)
MIN

.020
(0.508)
MIN

$.325 \begin{smallmatrix} +.035 \\ -.015 \end{smallmatrix}$

$\left(8.255 \begin{smallmatrix} +0.889 \\ -0.381 \end{smallmatrix}\right)$

.100
(2.54)
BSC

.018 ± .003
(0.457 ± 0.076)

N8 1002

NOTE:
1. DIMENSIONS ARE $\frac{INCHES}{MILLIMETERS}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

TYPICAL APPLICATION

±120V Output Precision Op Amp

LT1055/56 TA10
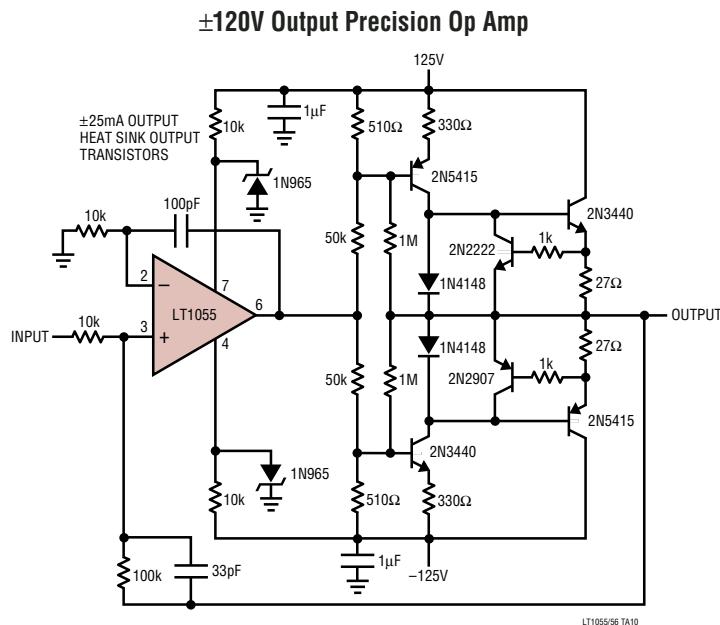
PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN $\frac{INCHES}{(MILLIMETERS)}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303
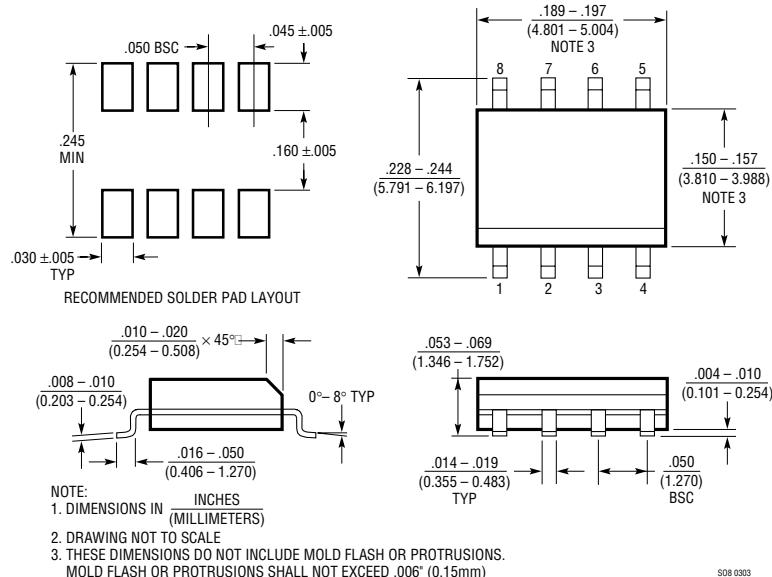
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1122	Fast Settling JFET Op Amp	340ns Settling Time, GBW = 14MHz, SR = 60V/µs
LT1792	Low Noise JFET Op Amp	e_n = 6nV/√Hz Max at f = 1kHz

10556fc

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