LMZM33606 3.5-V to 36-V Input, 1-V to 20-V Output, 6-A Power Module

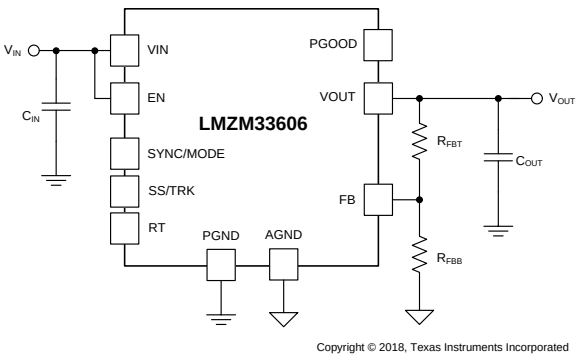
1 Features

- Small Complete Solution Size: < 250 mm^2
  - Requires as few as 4 External Components
  - 16 mm × 10 mm × 4 mm QFN Package
- Supports 5-V, 12-V, 24-V, 28-V Input Rails
  - 3.5-V to 36-V Input Voltage Range
  - 1-V to 20-V Output Voltage Range
- Meets EN55011 Radiated Emissions
- Configurable as Negative Output Voltage
- Adjustable Features for Design Flexibility
  - Switching Frequency (350 kHz to 2.2 MHz)
  - Synchronization to an External Clock
  - Selectable Auto Mode or FPWM Mode
    - Auto: Boost Efficiency at Light Loads
    - FPWM: Fixed Frequency Over Entire Load
  - Adjustable Soft Start and Tracking Input
  - Precision Enable to Program System UVLO
- Protection Features
  - Hiccup Mode Current Limit
  - Overtemperature Protection
  - Power-Good Output
- Operate in Rugged Environments
  - Up to 50-W Output Power at 85°C, No Airflow
  - Operating Junction Range: –40°C to +125°C
  - Operating Ambient Range: –40°C to +105°C
  - Shock and Vibration Tested to Mil-STD-883D

2 Applications

- Industrial Distributed Power
- Medical and Test Equipment
- General Purpose Wide VIN Regulation

Simplified Schematic



3 Description

The LMZM33606 power module is an easy-to-use integrated power solution that combines a 6-A DC/DC converter with power MOSFETs, a shielded inductor, and passives into a low-profile package. This power solution requires as few as four external components and eliminates the loop compensation and magnetics part selection from the design process.

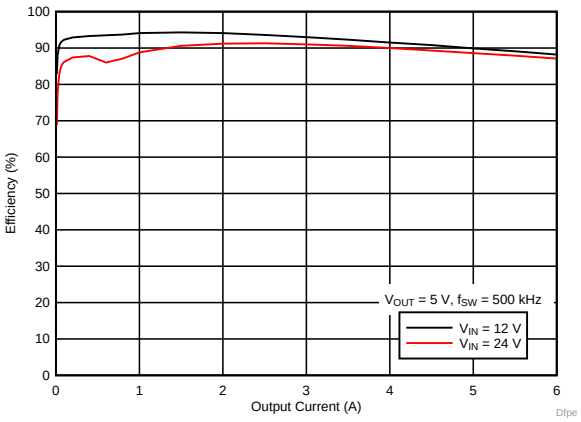
The 16 mm × 10 mm × 4 mm, 41-pin, QFN package is easy to solder onto a printed circuit board and allows a compact, low-profile point-of-load design. The full feature set including power good, adjustable soft start, tracking, synchronization, programmable UVLO, prebias start-up, selectable auto or FPWM modes, as well as overcurrent and overtemperature protection makes the LMZM33606 ideal for powering a wide range of applications.

Device Information

DEVICE NUMBER	PACKAGE	BODY SIZE (NOM)
LMZM33606	QFN (41)	16.00 mm × 10.00 mm

Minimum Solution Size

Typical Efficiency (Auto Mode)



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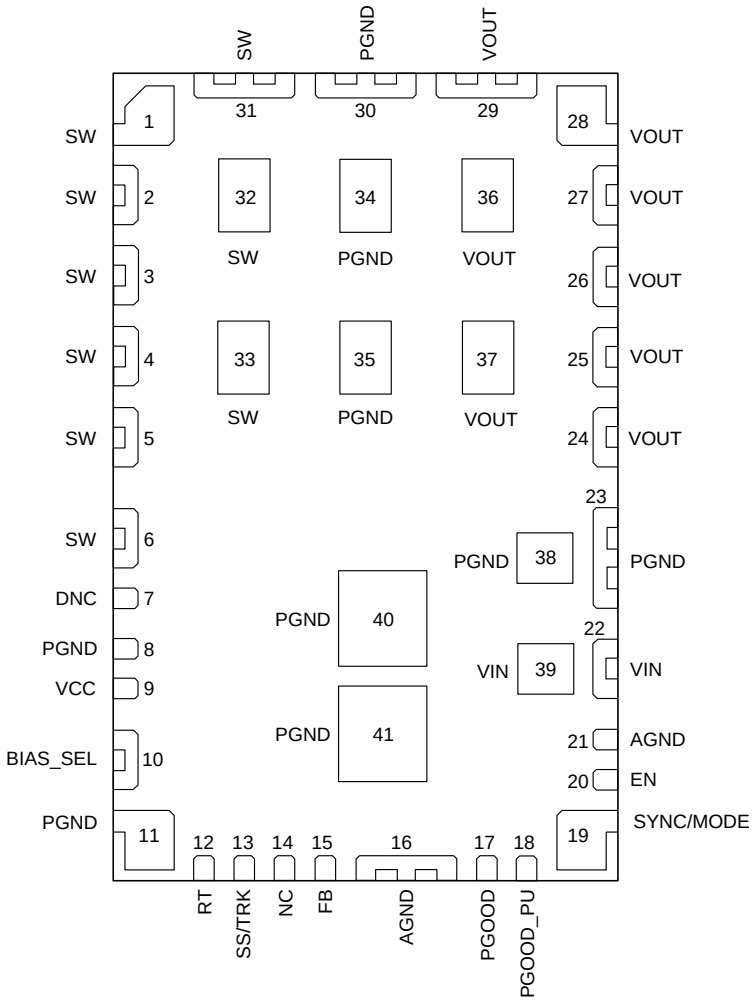
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2018	*	Initial release

5 Pin Configuration and Functions

RLX Package
41-Pin QFN
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	16, 21	G	Analog ground. Zero voltage reference for internal references and logic. These pins are not connected to one another internal to the device and must be connected to one another externally. Do not connect these pins to PGND; the AGND to PGND connection is made internal to the device. See the *Layout* section of the datasheet for a recommended layout.
BIAS_SEL	10		Optional BIAS LDO supply input. An internal 470 nF capacitor is placed between this pin and PGND. Do not float; tie to PGND if not used.
DNC	7	—	Do not connect. This pin is connect to internal circuitry. Do not connect this pin to AGND, PGND, or any other voltage. **This pin must be soldered to an isolated pad.**.
EN	20	I	Precision enable input to regulator. Do not float. High = ON, Low = OFF. Can be tied to VIN. Precision enable input allows adjustable system UVLO using external resistor divider.
FB	15	I	Feedback input. Connect the center point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND.
NC	14	—	Not internally connected.
PGND	8, 11, 23, 30, 34, 35, 38, 40, 41	G	Power ground. This is the return current path for the power stage of the device. Connect these pins to the low side of the input source, load, and bypass capacitors associated with VIN and VOUT using power ground planes on the PCB. Not all pins are connected to PGND internal to the device; connections must be made externally. Connect pad 40 and 41 to the ground planes using multiple vias for good thermal performance.
PGOOD	17	O	Open drain output for power-good flag. Internal to the device, a 100-kΩ pullup resistor is placed between this pin and the PGOOD_PU pin.
PGOOD_PU	18	I	Power-good pullup supply. Connect to logic rail or other DC voltage no higher than 20 V.
RT	12	I	An external timing resistor connected between this pin and AGND adjusts the switching frequency of the device. If floating, the default switching frequency is 500 kHz. Do not short to ground.
SS/TRK	13	I	Soft start / tracking control pin. Leave this pin floating to use the 5-ms internal soft-start ramp. An external capacitor can be connected from this pin to ground to extend the internal soft start ramp. A 2-μA current sourced from this pin can charge the capacitor to provide the ramp. Connect to external ramp for tracking. Do not connect to ground.
SW	1, 2, 3, 4, 5, 6, 31, 32, 33	O	Switch node. Connect these pins to a small copper island under the device for thermal relief. Do not place any external component on these pins or tie them to a pin of another function.
SYNC/MODE	19	I	Synchronization input and Mode setting pin. Do not float; tie to AGND or logic high if not used. Connect to an external clock to synchronize (see *Synchronization (SYNC/MODE)*). Connect to AGND to select Auto mode or connect to logic high to select FPWM mode. (see *Mode Select (Auto or FPWM)*).
VCC	9	O	Output of internal bias supply. Used to supply internal control circuits and drivers. Do not place any external component on this pin or tie it to a pin of another function.
VIN	22, 39	I	Input supply voltage. Connect external input capacitors between these pins and PGND.
VOUT	24, 25, 26, 27, 28, 29, 36, 37	O	Output voltage. These pins are connected to the output of the internal inductor. Connect these pins to the output VOUT load and connect external bypass capacitors between these pins and PGND.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	-0.3	42	V
	EN to AGND	-0.3	V_{IN} + 0.3	V
	FB, RT, SS/TRK to AGND	-0.3	5	V
	PGOOD to AGND	-0.1	20	V
	SYNC/MODE to AGND	-0.3	5.5	V
	BIAS_SEL to AGND	-0.3	Lower of (V_{IN}+0.3) and 20	V
	AGND to PGND	-0.3	0.3	V
Output voltage	VOUT to PGND	-0.3	V_{IN}	V
	SW to PGND	-0.3	V_{IN} + 0.3	V
	SW to PGND (<10 ns transients)	-3.5	42	V
	VCC to PGND	-0.3	5	V
Temperature	Maximum junction temperature, T_J (2)	-40	125	°C
	Storage temperature, T_{stg}	-55	150	°C
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		tbd	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		tbd	G

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under the recommended operating conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the typical characteristics sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input voltage, V_{IN}	3.5 (1)	36	V
Output voltage, V_{OUT}	1	20	V
EN voltage, V_{EN}	0	VIN	V
PGOOD pullup voltage, V_{PGOOD}	0	15	V
PGOOD sink current	0	5	mA
BIAS_SEL	3.3	Lower of VIN and 18	V
Output current, I_{OUT}	0	6	A
Switching frequency, F_{SW}	350	1200	kHz
Operating ambient temperature, T_A	–40	105	°C
Input Capacitance, C_{IN}	20 (2)		µF
Output Capacitance, C_{OUT}	min (3)	700	µF

(1) For output voltages ≤ 5 V, the recommended minimum V_{IN} is 3.5 V or (VOUT + 1 V), whichever is greater. For output voltages > 5 V, the recommended minimum V_{IN} is (1.1 × VOUT). See *Voltage Dropout* for more information.
(2) A minimum of 20 µF ceramic input capacitance is required for proper operation. An additional 100 µF of bulk capacitance is recommended for applications with transient load requirements. (see *Input Capacitor Selection*).
(3) The minimum amount of required output capacitance varies depending on the output voltage (see *Output Capacitor Selection*).

6.4 Thermal Information

THERMAL METRIC (1)		LMZM33606 RLX(B2QFN) 41 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	13.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter (3)	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter (4)	6.2	°C/W
T_{SHDN}	Thermal Shutdown Temperature	160	°C
	Thermal Shutdown Hysteresis	25	°C

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 75 mm x 75 mm double-sided PCB with 2 oz. copper and natural convection cooling. Additional airflow reduces $R_{\theta JA}$.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times Pdis + T_T$; where Pdis is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times Pdis + T_B$; where Pdis is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

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6.5 Electrical Characteristics

Limits apply at T_A = 25°C, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = I_{OUT} maximum, f_{sw} = 500 kHz, FPWM mode (unless otherwise noted); C_{IN1} = 3x 10 µF, 50-V, 1210 ceramic; C_{IN2} = 2x 4.7 µF, 50-V, electrolytic; C_{OUT} = 6x 22 µF, 25-V, 1210 ceramic. Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (V_{IN})						
V_{IN}	Input voltage range	Over I_{OUT} range, V_{OUT} = 2.5 V, f_{SW} = 350 kHz	3.5(1)		36	V
	V_{IN} turn on	V_{IN} increasing		3.12		V
	V_{IN} turn off	V_{IN} decreasing		2.62		V
I_{SHDN}	Shutdown supply current	V_{IN} = 12 V, V_{EN} = 0 V, I_{OUT} = 0 A		0.8	10	µA
INTERNAL LDO (VCC, BIAS_SEL)						
V_{CC}	Internal V_{CC} voltage	CCM		3.27		V
		DCM		3.1		V
I_{BIAS_SEL}	BIAS_SEL quiescent current (non-switching)	V_{IN} = 12 V, FB =1.5 V, EN = 2 V, BIAS_SEL = 3.3 V		21	50	µA
FEEDBACK						
V_{FB}	Feedback voltage(2)	–40°C ≤ T_J = T_A ≤ 125°C, I_{OUT} = 0 A, Over V_{IN} range	0.987	1.006	1.017	V
	Load regulation	Over I_{OUT} range, T_A = 25°C		0.35%		
I_{FB}	Feedback leakage current	V_{FB} = 1 V		0.2	65	nA
CURRENT						
I_{OUT}	Output current	Natural convection, T_A = 25°C	0		6	A
	Overcurrent threshold			9		A
PERFORMANCE						
η	Efficiency	I_{OUT} = 3 A		91%		
SOFT START						
T_{SS}	Internal soft start time	SS pin open		5		ms
I_{SS}	Soft-start charge current		1.8	2	2.2	µA
ENABLE (EN)						
V_{EN-H}	EN rising threshold		1.14	1.2	1.25	V
V_{EN-HYS}	EN hysteresis voltage			-100		mV
I_{EN}	EN Input leakage current	V_{EN} = 2 V		1.4	200	nA
POWER GOOD (PGOOD)						
V_{PGOOD}	PGOOD thresholds	Overvoltage	106%	110%	113%	
		Undervoltage	86%	90%	93%	
	Minimum V_{IN} for valid PGOOD	50-µA pullup, V_{EN} = 0 V, T_J = T_A = 25°C		1.3	2	V
V_{PGOOD}	PGOOD low voltage	0.5-mA pullup, V_{EN} = 0 V			0.3	V

(1) For output voltages ≤ 5 V, the recommended minimum V_{IN} is 3.5 V or (V_{OUT} + 1 V), whichever is greater. For output voltages > 5 V, the recommended minimum V_{IN} is (1.1 × V_{OUT}). See *Voltage Dropout* for more information.
(2) The overall output voltage tolerance will be affected by the tolerance of the external R_{FBT} and R_{FBB} resistors.

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6.6 Switching Characteristics

Limits apply at T_A = 25°C, V_{IN} = 24 V, V_{OUT} = 5 V, FPWM mode (unless otherwise noted);
Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm, and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY (RT) and SYNCHRONIZATION (EN/SYNC)						
f_{SW}	Default switching frequency	RT pin = open, I_{OUT} = 0 A	440	500	560	kHz
	Switching frequency range	I_{OUT} = 0 A	350		2200	kHz
V_{SYNC}	High Threshold				2	V
	Low Threshold		0.4			V
T_{S-MIN}	Minimum SYNC ON/OFF time			80		ns

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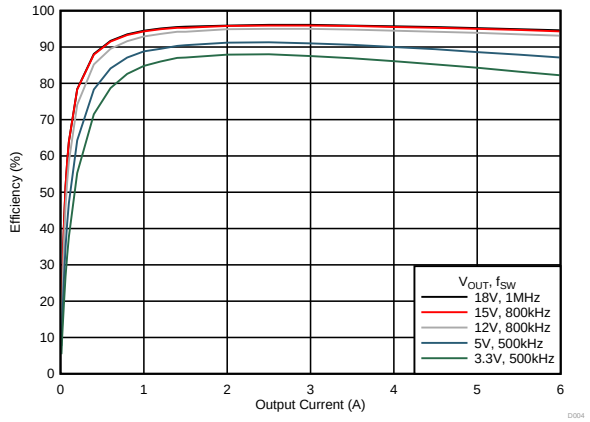
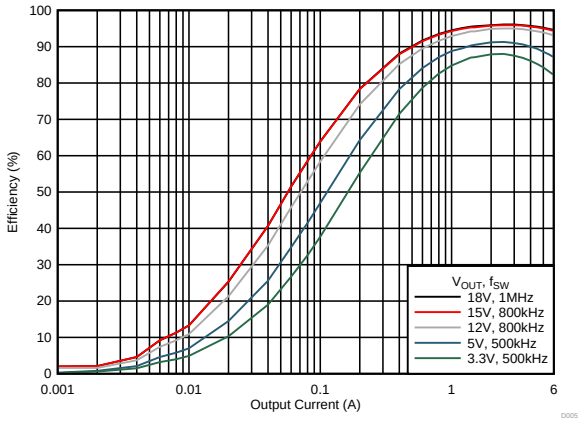
6.7 Typical Characteristics (V_{IN} = 24 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



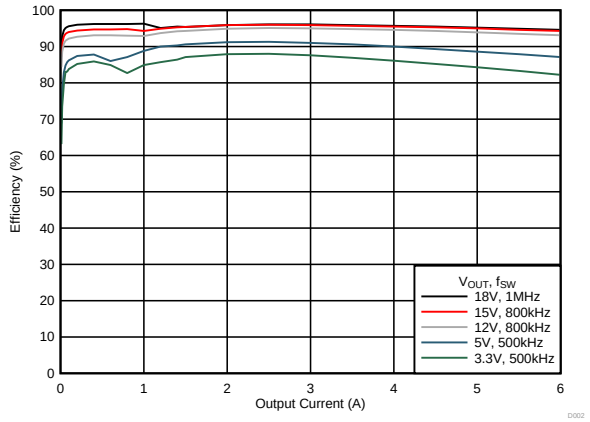
FPWM Mode Linear Scale

Figure 1. Efficiency vs Output Current



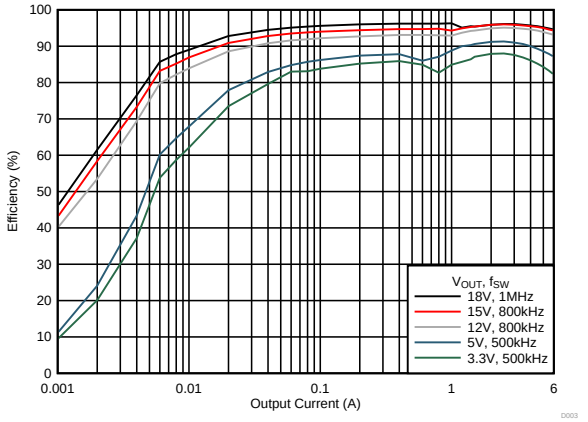
FPWM Mode Log Scale

Figure 2. Efficiency vs Output Current



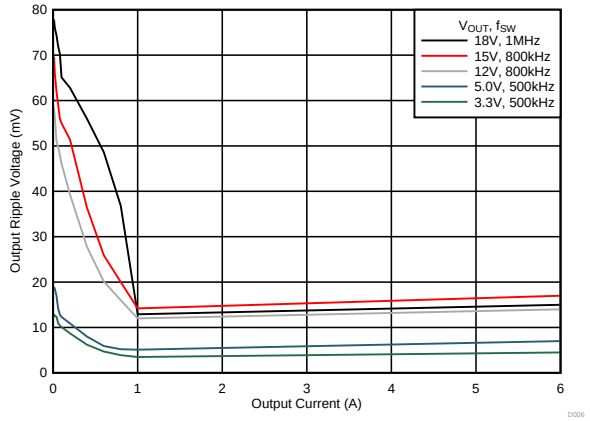
Auto Mode Linear Scale

Figure 3. Efficiency vs Output Current



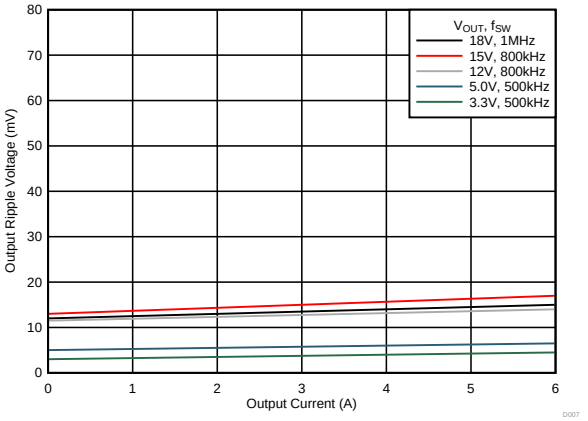
Auto Mode Log Scale

Figure 4. Efficiency vs Output Current



Auto Mode

Figure 5. Output Voltage Ripple



FPWM Mode

Figure 6. Output Voltage Ripple

ADVANCE INFORMATION

Typical Characteristics (V_{IN} = 24 V) (continued)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.

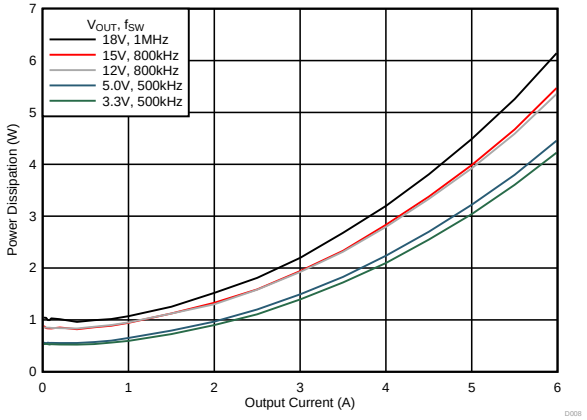
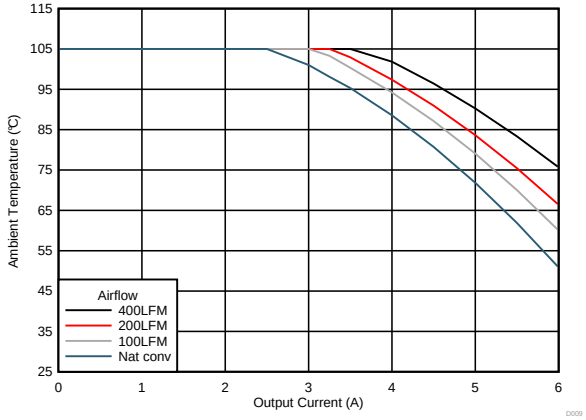
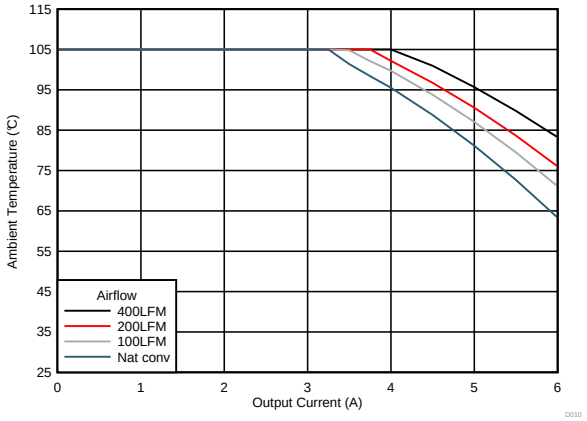


Figure 7. Power Dissipation



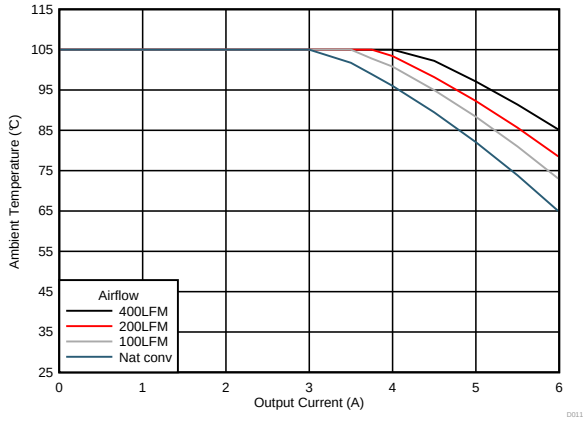
V_{OUT} = 12 V f_{SW} = 800 kHz

Figure 8. Safe Operating Area



V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 9. Safe Operating Area



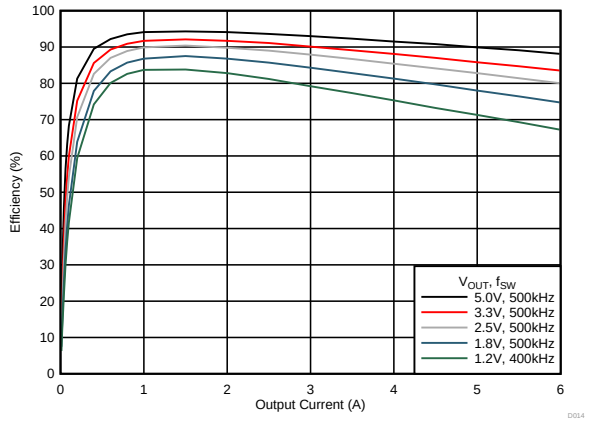
V_{OUT} =3.3 V f_{SW} = 500 kHz

Figure 10. Safe Operating Area

ADVANCE INFORMATION

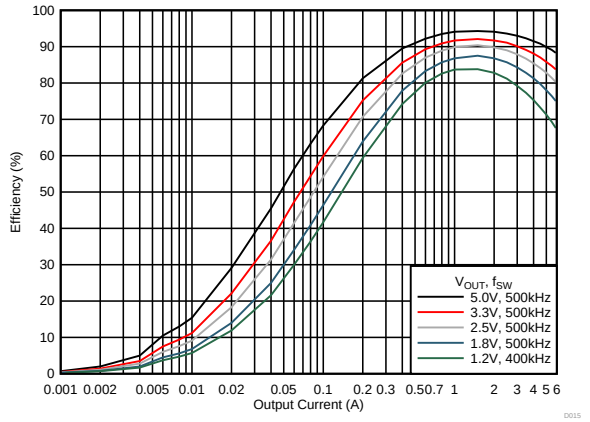
6.8 Typical Characteristics (V_{IN} = 12 V)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.



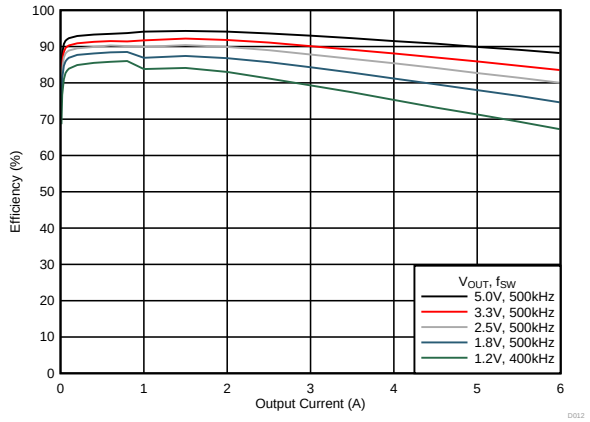
FPWM Mode Linear Scale

Figure 11. Efficiency vs Output Current



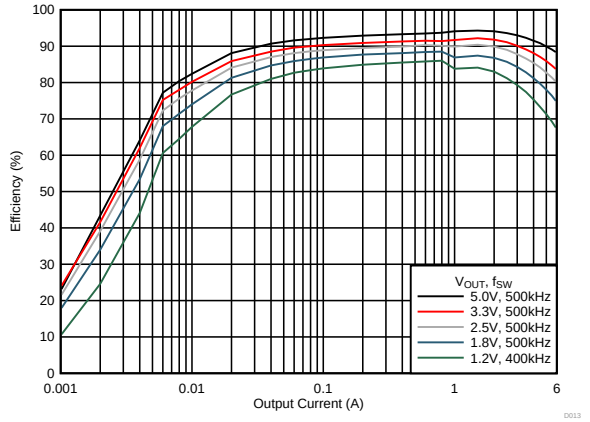
FPWM Mode Log Scale

Figure 12. Efficiency vs Output Current



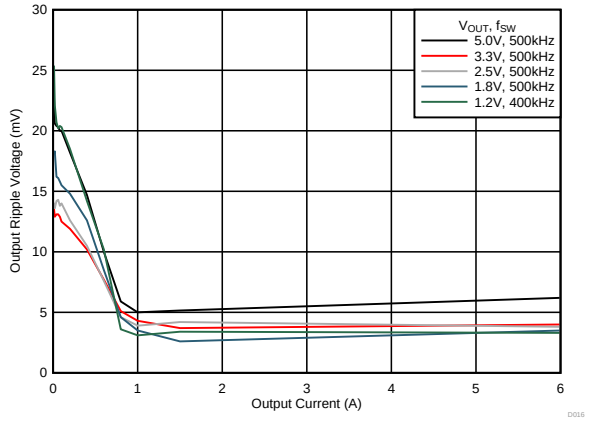
Auto Mode Linear Scale

Figure 13. Efficiency vs Output Current



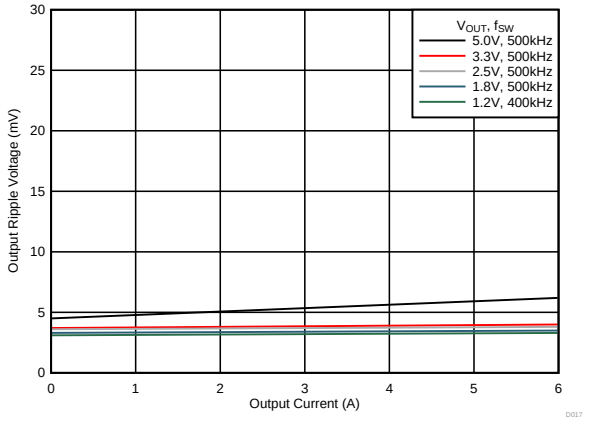
Auto Mode Log Scale

Figure 14. Efficiency vs Output Current



Auto Mode

Figure 15. Voltage Ripple vs Output Current



FPWM Mode

Figure 16. Voltage Ripple vs Output Current

ADVANCE INFORMATION

Typical Characteristics (V_{IN} = 12 V) (continued)

The typical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the device.

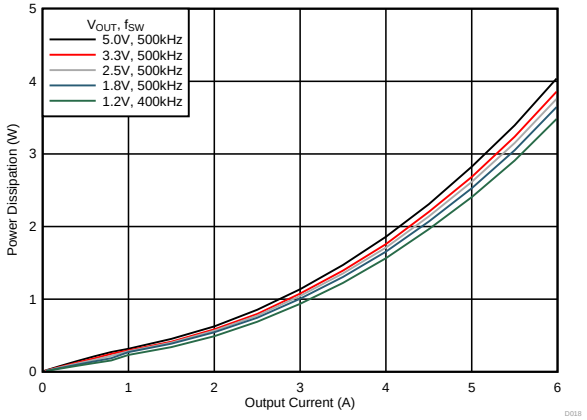
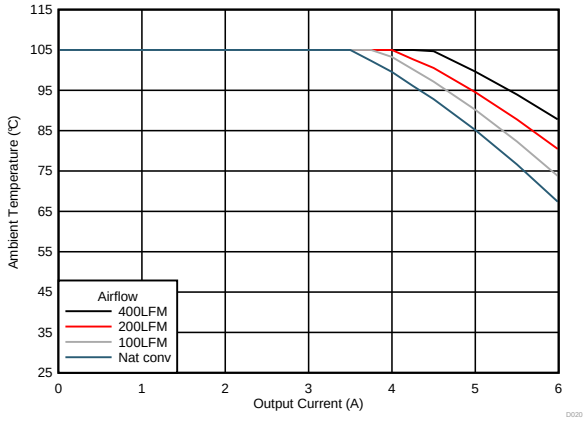
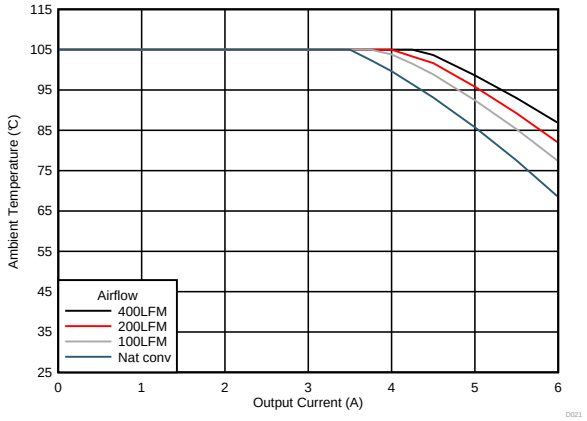


Figure 17. Power Dissipation vs Output Current



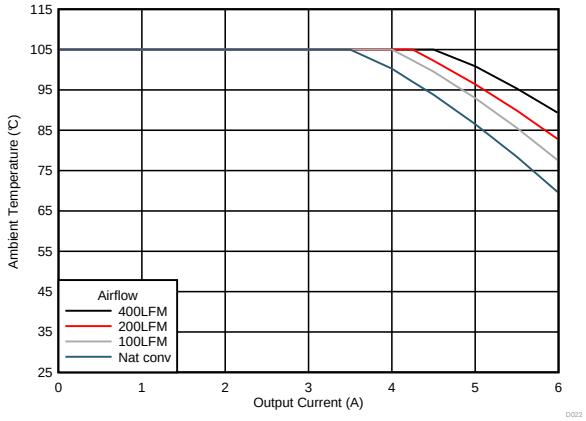
V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 18. Safe Operating Area



V_{OUT} = 3.3 V f_{SW} = 500 kHz

Figure 19. Safe Operating Area



V_{OUT} = 1.8 V f_{SW} = 500 kHz

Figure 20. Safe Operating Area

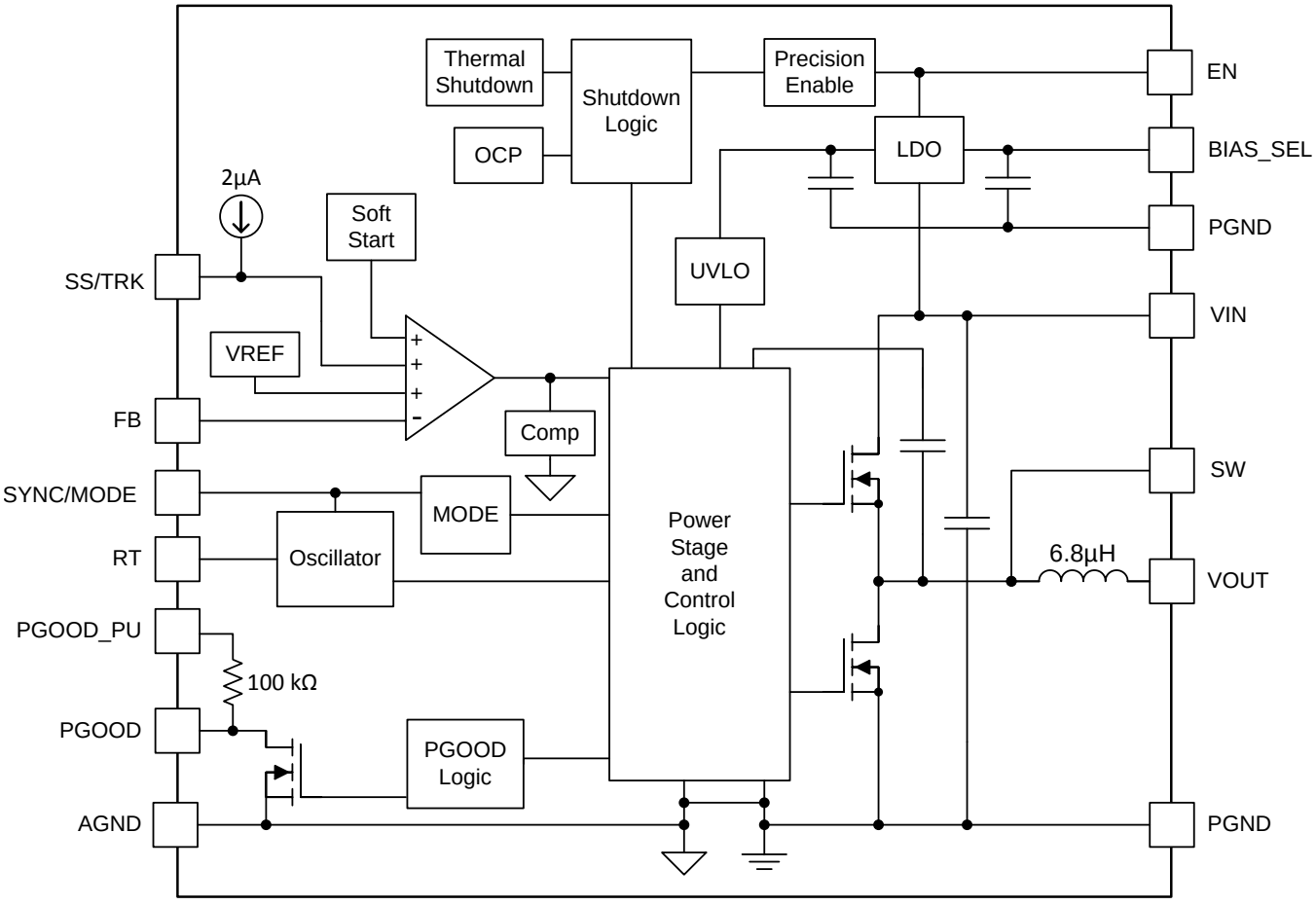
ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The LMZM33606 is a full-featured 36-V input, 6-A synchronous step-down converter with controller, MOSFETs, shielded inductor, and control circuitry integrated into a low-profile, overmolded package. The device integration enables small designs, while providing the ability to adjust key parameters to meet specific design requirements. The LMZM33606 provides an output voltage range of 1 V to 20 V. An external resistor divider is used to adjust the output voltage to the desired value. The switching frequency can also be adjusted, by either an external resistor or a sync signal, which allows the LMZM33606 to accommodate a variety of input and output voltage conditions as well as to optimize efficiency. The device provides accurate voltage regulation over a wide load range by using a precision internal voltage reference. The EN pin can be pulled low to disable the device as well as the system undervoltage lockout can be adjusted using a resistor divider on the EN pin. A power-good signal is provided to indicate when the output is within its nominal voltage range. Thermal shutdown and current limit features protect the device during an overload condition. A 41-pin, QFN package that includes exposed bottom pads provides a thermally enhanced solution for space-constrained applications.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Adjusting the Output Voltage

A resistor divider connected to the FB pin (pin 15) programs the output voltage of the LMZM33606. The output voltage adjustment range is from 1 V to 20 V. Figure 21 shows the feedback resistor connection for setting the output voltage. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using Equation 1.

Table 1 lists the standard external R_{FBT} values for several standard output voltages along with the recommended switching frequency (F_{SW}) and the frequency setting resistor (R_{RT}) for each of the output voltages listed. (See *Voltage Dropout* for the allowable output voltage as a function of input voltage.)

$$R_{FBT} = 10 \times \left(V_{OUT} - V_{FB} \right) (k\Omega) \quad (1)$$

where

- V_{FB} (typical) = 1.006 V

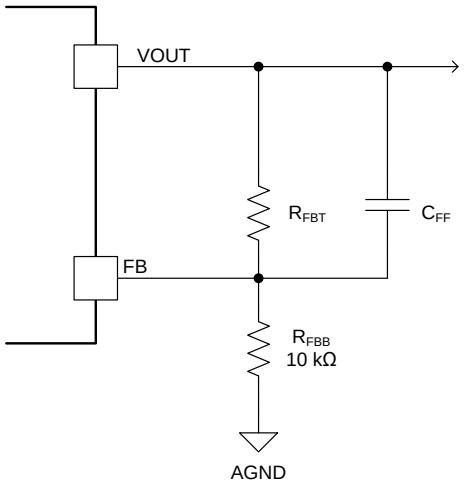


Figure 21. Setting the Output Voltage

Table 1. Standard Component Values

V_{OUT} (V)	R_{FBT} (kΩ)(1)	f_{SW} (kHz)	R_{RT} (kΩ)
1.2	1.96	400	100
1.8	7.87	500	78.7 or open
2.5	15.0	500	78.7 or open
3.3	22.6	500	78.7 or open
5	40.2	500	78.7 or open
7.5	64.9	500	78.7 or open
12	110	800	47.5
15	140	800	47.5
20	191	1000	38.3

(1) R_{FBB} = 10 kΩ.

ADVANCE INFORMATION

7.3.2 Input Capacitor Selection

The LMZM33606 requires a minimum of 20 µF of ceramic type input capacitance. Use only high-quality ceramic type X5R or X7R capacitors with sufficient voltage rating. TI recommends an additional 100 µF of non-ceramic capacitance for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. At worst case, when operating at 50% duty cycle and maximum load, the combined ripple current rating of the input capacitors must be at least 3 A_{RMS}. Table 2 includes a preferred list of capacitors by vendor.

Table 2. Recommended Input Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			WORKING VOLTAGE (V)	CAPACITANCE (2) (µF)	ESR (3) (mΩ)
TDK	X5R	C3225X5R1H106K	50	10	3
Murata	X7R	GRM32ER71H106K	50	10	2
Murata	X7R	GRM32ER71J106K	63	10	2
Panasonic	ZA	EEHZA1H101P	50	100	28
Panasonic	ZA	EEHZA1J560P	63	56	30

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR at 100 kHz, 25°C.

7.3.3 Output Capacitor Selection

The minimum amount of required output capacitance for the LMZM33606 varies depending on the output voltage. Table 3 lists the minimum output capacitance for several output voltage ranges. The required output capacitance must be comprised of all ceramic capacitors or a combination of ceramic and polymer-type capacitors. The effects of temperature and capacitor voltage rating must be considered when selecting capacitors to meet the minimum required capacitance.

When adding additional output capacitance, ceramic capacitors or a combination of ceramic and polymer-type capacitors can be used. The required capacitance above the minimum is determined by actual transient deviation requirements. See Table 4 for a preferred list of output capacitors by vendor.

Table 3. Minimum Required Output Capacitance

V_{OUT} RANGE (V)		MINIMUM REQUIRED C_{OUT}	
MIN	MAX	CAPACITANCE VALUE	VOLTAGE RATING
1	5	282 µF (6 × 47 µF)(1)	≥ 6.3 V
> 5.0	12	188 µF (4 × 47 µF)(1)	≥ 16 V
> 12	20	88 µF (4 × 22 µF)(1)	≥ 25 V

(1) The minimum required output capacitance must be made up of ceramic type capacitors. Additional capacitance above the minimum can be either ceramic or low-ESR polymer type.

ADVANCE INFORMATION

Table 4. Recommended Output Capacitors(1)

VENDOR	SERIES	PART NUMBER	CAPACITOR CHARACTERISTICS		
			VOLTAGE (V)	CAPACITANCE (µF)(2)	ESR (mΩ)(3)
TDK	X5R	C3225X5R1C106K	16	10	2
Murata	X5R	GRM32ER61C106K	16	10	2
TDK	X5R	C3225X5R1C226M	16	22	2
Murata	X5R	GRM32ER61C226K	16	22	2
Murata	X6S	GRM31CC81E226K	25	22	2
Murata	X7R	GRM32ER71E226M	25	22	2
TDK	X5R	C3225X5R1A476M	10	47	2
Murata	X5R	GRM32ER61C476K	16	47	2
Murata	X5R	GRM31CR61E476M	25	47	2
TDK	X5R	C3225X5R0J107M	6.3	100	2
Murata	X5R	GRM32ER60J107M	6.3	100	2
Murata	X5R	GRM32ER61A107M	10	100	2
Kemet	X5R	C1210C107M4PAC7800	16	100	2
Panasonic	POSCAP	6TPF220M9L	6.3	220	9
Panasonic	POSCAP	6TPE220ML	6.3	220	12

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table.
(2) Specified capacitance values.
(3) Maximum ESR at 100 kHz, 25°C.

7.3.4 Feed-Forward Capacitor

The LMZM33606 is internally compensated to be stable over the operating range of the device. However, depending on the output voltage, an additional feed-forward capacitor, C_{FF}, may be added for optimum performance. Adding additional output capacitance above the minimum reduces the output voltage ripple of the device. However, adding additional output capacitance also reduces the cross-over frequency of the device, slowing the response to load transients. Adding a feed-forward capacitor when adding more output capacitance helps to restore the cross-over frequency of the device, improving the transient response. The feed-forward capacitor must be placed in parallel with the top resistor divider, R_{FBT} as shown in Figure 22. See Table 5 for recommended C_{FF} capacitor values.

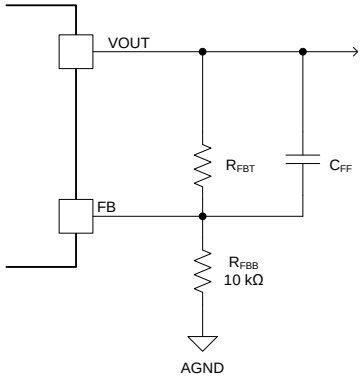


Figure 22. Feed-Forward Capacitor

Table 5. C_{FF} Capacitance

V_{OUT} RANGE	C_{FF} (pF)
1 V to < 2 V	470
2 V to < 4 V	220
4 V to < 6 V	100
≥ 6 V	open

7.3.5 Switching Frequency (RT)

The switching frequency range of the LMZM33606 is 350 kHz to 2.2 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Additionally, the RT pin can be left floating, and the LMZM33606 operates at 500 kHz default switching frequency. Use Equation 2 to calculate the R_{RT} value for a desired frequency or simply select from Table 6.

The switching frequency must be selected based on the output voltage setting of the device. See Table 6 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for several common input voltages. For the most efficient solution, always select the lowest allowable frequency.

$$R_{RT} = \frac{1}{f_{SW}(kHz) \times (2.675 \times 10^{-5}) - 0.0007} \quad (k\Omega) \tag{2}$$

Table 6. Switching Frequency vs Output Voltage

SWITCHING FREQUENCY (kHz)	R_{RT} RESISTOR (kΩ)	V_{IN} = 5 V (±0.25 V)		V_{IN} = 12 V (±0.5 V)		V_{IN} = 24 V (±0.5 V)	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX
350	115	1	4	1	8.2	1	8.4
400	100	1	4	1	8.8	1	9.9
500	78.7 or open	1	4	1	9.9	1.1	13.9
600	64.9	1	4	1	9.9	1.3	15.6
700	54.9	1	3.5	1	9.7	1.5	16.9
800	47.5	1	3.4	1	9.6	1.7	18
1000	38.3	1	3.4	1.1	9.3	2.1	20
1200	31.6	1	3.3	1.3	9.1	2.5	19.1

7.3.6 Synchronization (SYNC/MODE)

The LMZM33606 switching frequency can also be synchronized to an external clock from 350 kHz to 2.2 MHz. TI recommends connecting the external clock to the SYNC/MODE pin with an appropriate termination resistor.

Before the external clock is present, the device switches at the frequency programmed by the R_{RT} resistor. Select R_{RT} to set the frequency to be the same as the external synchronization frequency. Once the external clock is present, the device transitions to SYNC mode within 1 ms (typical) and overrides the RT mode. If the external clock is removed, the device continues to switch at the SYNC frequency for 10 µs (typ) before returning to the switching frequency set by the RT resistor, resulting in minimal disturbance to the output voltage during the transitions.

Recommendations for the external clock include a high level no lower than 2 V, low level no higher than 0.4 V, duty cycle between 10% and 90%, and both positive and negative pulse width no shorter than 80 ns.

When synchronizing to an external clock, the device operation mode is FPWM. If synchronization is not needed, connect this pin to AGND or logic high to select either Auto mode or FPWM mode. Do not leave this pin open.

The synchronization frequency must be selected based on the output voltages of the devices being synchronized. Table 6 and show the allowable frequencies for a given range of output voltages. For the most efficient solution, always select the lowest allowable frequency.

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7.3.7 Output Enable (EN)

The voltage on the EN pin provides electrical ON/OFF control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low quiescent current state.

The EN pin cannot be open circuit or floating. The simplest way to enable the operation of the LMZM33606 is to connect the EN pin to VIN directly as shown in Figure 23. This allows self-start-up of the LMZM33606 when VIN reaches the turnon threshold.

If an application requires controlling the EN pin, an external logic signal can be used to drive EN/SYNC pin as shown in Figure 24. Applications using an open drain/collector device to interface with this pin require a pullup resistor to a voltage above the enable threshold.

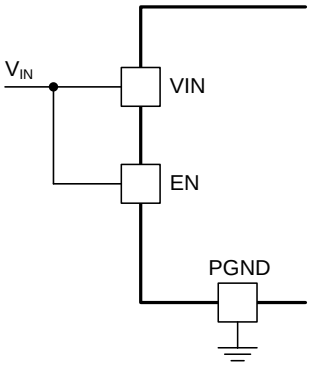


Figure 23. Enabling the Device

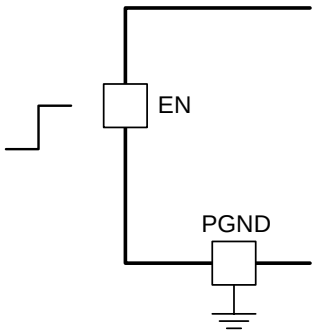


Figure 24. Typical Enable Control

7.3.8 Programmable System UVLO (EN)

Many applications benefit from employing an enable divider to establish a customized system UVLO. This can be used either for sequencing, system timing requirement, or to reduce the occurrence of deep discharge of a battery power source. Figure 25 shows how to use a resistor divider to set a system UVLO level. An external logic output can also be used to drive the EN pin for system sequencing.

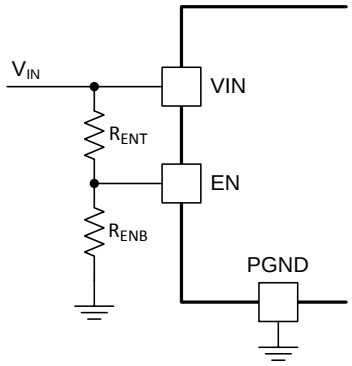


Figure 25. System UVLO

Table 7 lists recommended resistor values for R_{ENT} and R_{ENB} to adjust the system UVLO voltage. TI recommends to set the system UVLO turn-on threshold to approximately 80% to 85% of the minimum expected input voltage.

Table 7. Resistor Values for Setting System UVLO

UVLO (V)	6.5	10	15	20	25
R_{ENT} (kΩ)	100	100	100	100	100
R_{ENB} (kΩ)	22.6	13.7	8.66	6.34	4.99

7.3.9 Power Good (PGOOD) and Power Good Pullup (PGOOD_PU)

The LMZM33606 has a built-in power-good signal (PGOOD) that indicates whether the output voltage is within its regulation range. The PGOOD pin is an open-drain output that requires a pullup resistor to a nominal voltage source of 15 V or less. The maximum recommended PGOOD sink current is 5 mA. A typical pullup resistor value is between 10 kΩ and 100 kΩ.

Once the output voltage rises above 90% (typical) of the set voltage, the PGOOD pin rises to the pullup voltage level. The PGOOD pin is pulled low when the output voltage drops lower than 90% (typical) or rises higher than 110% (typ) of the nominal set voltage.

Internal to the device, a 100-kΩ pullup resistor is placed between the PGOOD pin and the PGOOD_PU pin. Applying a pullup voltage directly to the PGOOD_PU pin, eliminates the need to place an external pullup resistor.

7.3.10 Mode Select (Auto or FPWM)

The LMZM33606 has configurable auto mode or FPWM mode options. Connect the SYNC/MODE pin (pin 19) to AGND to select Auto mode, or connect the SYNC/MODE pin to logic high to select FPWM mode.

In auto mode, the device operates in discontinuous conduction mode (DCM) at light load. In DCM, the inductor current stops flowing when it reaches 0 A. In auto mode, the switching frequency reduces to regulate the required load current improving efficiency by reducing switching losses. At heavier load, when the inductor current valley is above 0 A, the device operates in continuous conduction mode (CCM), where the switching frequency is fixed and set by the RT pin.

In forced PWM (FPWM) mode, the device operates in CCM regardless of load with the frequency set by the RT pin or the synchronization input. Inductor current can go negative at light loads. At light loads, the efficiency in FPWM mode is lower than Auto mode, due to higher conduction losses and switching losses. In FPWM, the device has fixed switching frequency over the entire load range, which is beneficial to noise sensitive applications.

7.3.11 Soft Start and Voltage Tracking

The soft-start and tracking features control the output voltage ramp during start-up. The soft-start feature reduces inrush current during start-up and improves system performance and reliability. If the SS/TRK pin is floating, the LMZM33606 starts up following the fixed, 5-ms internal soft-start ramp. Use C_{SS} to extend soft-start time when there are a large amount of output capacitors, or the output voltage is high, or the output is heavily loaded during start-up.

If longer soft-start time is desired, an external capacitor can be added from SS/TRK pin to AGND. There is a 2-µA (typical) internal current source, I_{SSC}, to charge the external capacitor. For a desired soft-start time t_{SS}, capacitance of C_{SS} can be found by Equation 3.

$$C_{SS} = I_{SSC} \times t_{SS} \quad (3)$$

where

- C_{SS} = soft-start capacitor value (F)
- I_{SSC} = soft-start charging current (A)
- t_{SS} = desired soft-start time(s)

LMZM33606 can track an external voltage ramp applied to the SS/TRK pin, if the ramp is slower than the internal soft-start ramp. The external ramp final voltage after start-up must be greater than 1.5 V to avoid noise interfering with the reference voltage. Figure 26 shows how to use resistor divider to set V_{OUT} to follow an external ramp.

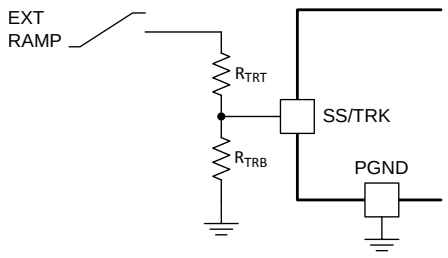


Figure 26. Soft-Start Tracking External Ramp

7.3.12 Voltage Dropout

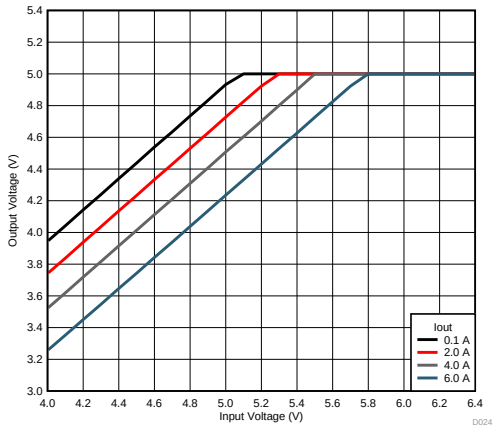
Voltage dropout is the difference between the input voltage and output voltage that is required to maintain output voltage regulation while providing the rated output current.

To ensure the LMZM33606 maintains output voltage regulation at the recommended switching frequency, over the operating temperature range, the following requirements apply:

For output voltages ≤ 5 V, the minimum V_{IN} is 3.5 V or (V_{OUT} + 1 V), whichever is greater.

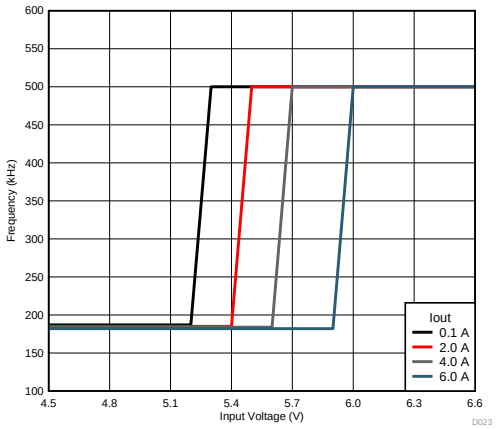
For output voltages > 5 V, the minimum V_{IN} is (1.1 × V_{OUT}).

However, if fixed switching frequency operation is not required, the LMZM33606 operates in a frequency foldback mode when the dropout voltage is less than the recommendations above. Frequency foldback reduces the switching frequency to allow the output voltage to maintain regulation as input voltage decreases. Figure 27 through Figure 30 show typical dropout voltage and frequency foldback curves for 5 V and 12 V outputs at T_A = 25°C. (As ambient temperature increases, dropout voltage and frequency foldback occur at higher input voltage.)



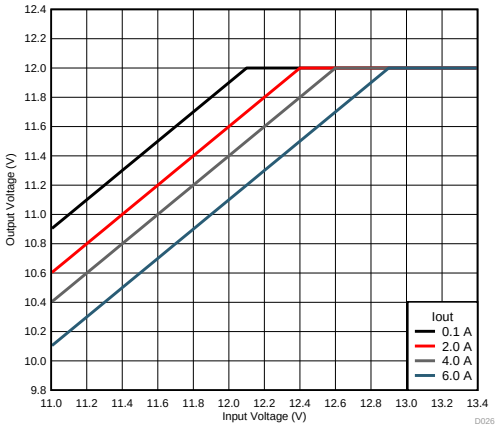
V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 27. Voltage Dropout



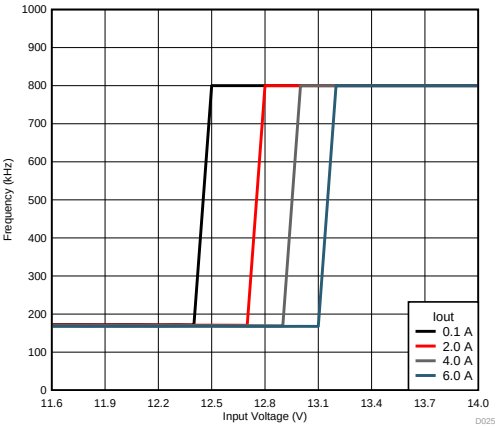
V_{OUT} = 5 V f_{SW} = 500 kHz

Figure 28. Frequency Foldback



V_{OUT} = 12 V f_{SW} = 800 kHz

Figure 29. Voltage Dropout



V_{OUT} = 12 V f_{SW} = 800 kHz

Figure 30. Frequency Foldback

ADVANCE INFORMATION

7.3.13 Overcurrent Protection (OCP)

The LMZM33606 is protected from overcurrent conditions. Hiccup mode is activated if a fault condition persists to prevent overheating. In hiccup mode, the regulator is shut down and kept off for 10 ms typically before the LMZM33606 tries to start again. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

7.3.14 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. The device reinitiates the power-up sequence when the junction temperature drops below 135°C typically.

7.4 Device Functional Modes

7.4.1 Active Mode

The LMZM33606 is in active mode when VIN is above the turnon threshold and the EN pin voltage is above the EN high threshold. The simplest way to enable the LMZM33606 is to connect the EN pin to VIN. This allows self start-up of the LMZM33606 when the input voltage is in the operation range of 3.5 V to 36 V.

7.4.2 Auto Mode

In Auto mode, the LMZM33606 operates in discontinuous conduction mode (DCM) at light load. In auto mode, the switching frequency reduces to regulate the required load current, improving efficiency by reducing switching losses. At heavier load, when the inductor current valley is above 0 A, the device operates in continuous conduction mode (CCM), where the switching frequency is fixed and set by the RT pin.

7.4.3 FPWM Mode

In forced PWM (FPWM) mode, the LMZM33606 operates in continuous conduction mode (CCM) regardless of load current at the switching frequency set by the RT pin or the synchronization input. In FPWM, the device has fixed switching frequency over the entire load range, which is beneficial to noise sensitive applications.

7.4.4 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMZM33606. When the EN pin voltage is below the EN low threshold, the device is in shutdown mode. In shutdown mode the standby current is 0.8 μA typical. Also, if V_{IN} falls below the turn-off threshold, the output of the regulator is turned off.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZM33606 is a synchronous step-down DC/DC power module. It is used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 6 A. The following design procedure can be used to select components for the LMZM33606. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH® software utilizes an iterative design procedure and accesses comprehensive databases of components. See www.ti.com for more details.

8.2 Typical Application

The LMZM33606 only requires a few external components to convert from a wide input-voltage-supply range to a wide range of output voltages. Figure 31 shows a basic LMZM33606 schematic with only the minimum required components.

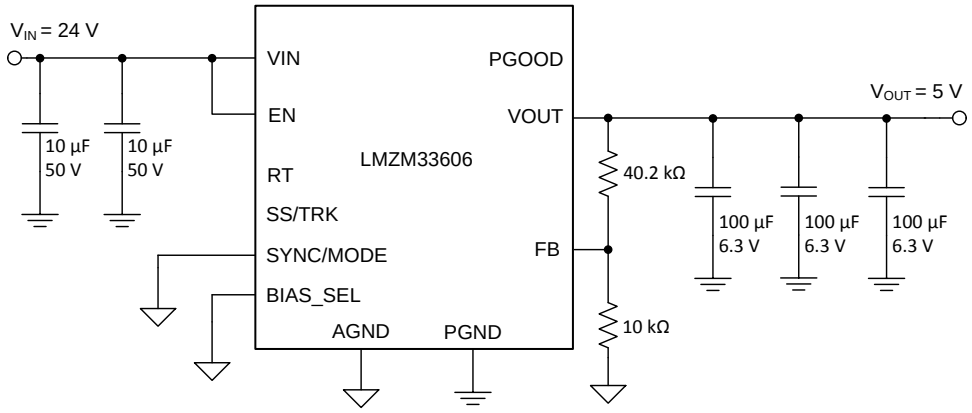


Figure 31. LMZM33606 Typical Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8 as the input parameters and follow the design procedures in *Detailed Design Procedure*.

Table 8. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	24 V typical
Output voltage V_{OUT}	5 V
Output current rating	6 A
Operating frequency	500 kHz

ADVANCE INFORMATION

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Setpoint

The output voltage of the LMZM33606 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be selected from Table 1 or calculated using the Equation 4:

$$R_{FBT} = 10 \times \left(V_{OUT} - V_{FB} \right) \text{ (k}\Omega\text{)} \quad (4)$$

For the desired output voltage of 5 V, the formula yields a value of 40 kΩ. Choose the closest available value of 40.2 kΩ for R_{FBT}.

8.2.2.2 Setting the Switching Frequency

The recommended switching frequency for a 5-V application is 500 kHz. To set the switching frequency to 500 kHz, the RT pin can be left open to operate at the default 500-kHz switching frequency.

8.2.2.3 Input Capacitors

The LMZM33606 requires a minimum input capacitance of 20-µF ceramic type. High-quality ceramic type X5R or X7R capacitors with sufficient voltage rating are recommended. An additional 100 µF of non-ceramic capacitance is recommended for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, 2x 10-µF, 50-V ceramic capacitors are selected.

8.2.2.4 Output Capacitor Selection

The LMZM33606 requires a minimum amount of output capacitance for proper operation. The minimum amount of required output varies depending on the output voltage. See *Table 3* for the required output capacitance.

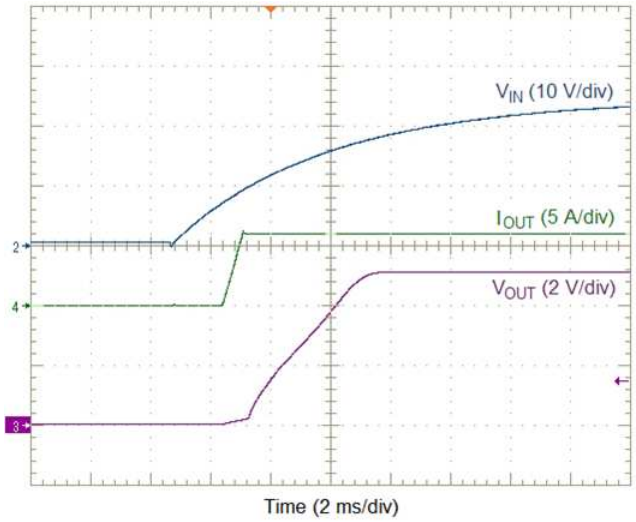
For this design example, 3 × 100-µF, 6.3-V ceramic capacitors are used.

8.2.2.5 Feed-Forward Capacitor (C_{FF})

For typical applications, an external feed-forward capacitor, C_{FF} is not required. Applications requiring optimum transient performance can benefit from placing a C_{FF} capacitor in parallel with the top resistor divider, R_{FBT}. The value for C_{FF} can be selected from Table 5. The recommended C_{FF} value for 5-V application is 100 pF.

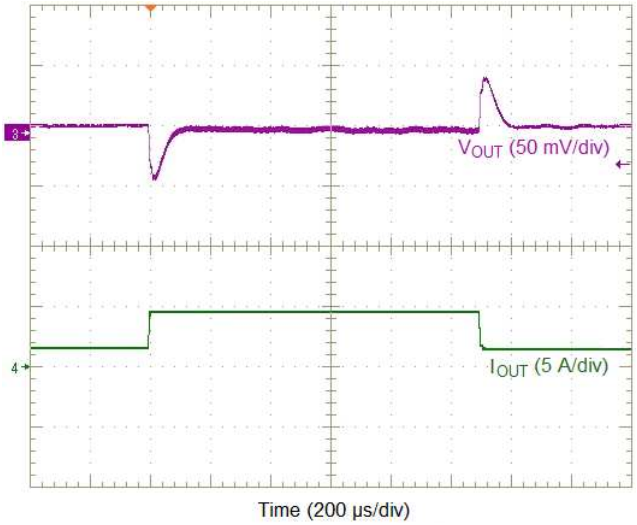
ADVANCE INFORMATION

8.2.2.6 Application Curves



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 6 A

Figure 32. Start-up Waveforms



V_{IN} = 24 V V_{OUT} = 5 V I_{OUT} = 1.5 A to 4.5 A
C_{OUT} = 300 µF Slew rate: 1 A/µs

Figure 33. Transient Response

ADVANCE INFORMATION

9 Power Supply Recommendations

The LMZM33606 is designed to operate from an input voltage supply range between 3.5 V and 36 V. This input supply must be able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMZM33606 supply voltage that can cause a turn-off and system reset.

If the input supply is located more than a few inches from the LMZM33606 additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The typical amount of bulk capacitance is a 100-µF electrolytic capacitor.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimized generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 34 thru Figure 37, shows a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- **Connect all PGND pins together using copper plane or thick copper traces.**
- Connect the SW pins together using a small copper island under the device for thermal relief.
- Place ceramic input and output capacitors close to the device pins to minimize high frequency noise.
- Locate additional output capacitors between the ceramic capacitor and the load.
- Keep AGND and PGND separate from one another. AGND and PGND are connected internal to the device.
- Place R_{FBT}, R_{FBB}, R_{RT}, and C_{FF} as close as possible to their respective pins.
- Use multiple vias to connect the power planes to internal layers.

ADVANCE INFORMATION

10.2 Layout Example

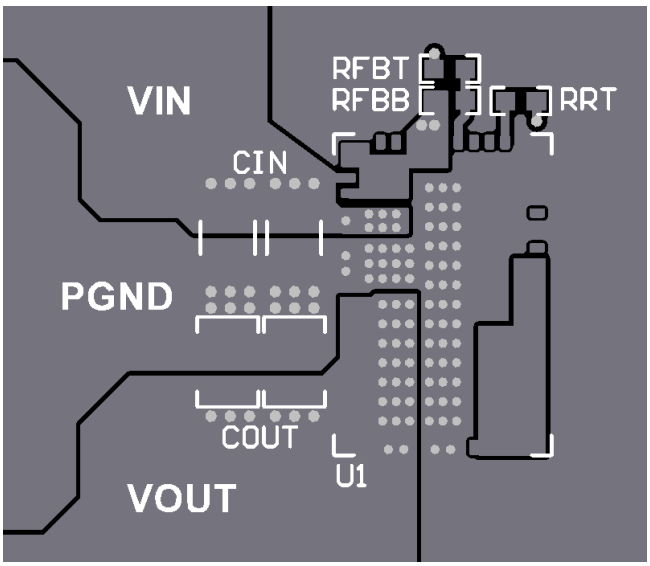


Figure 34. Typical Top-Layer Layout

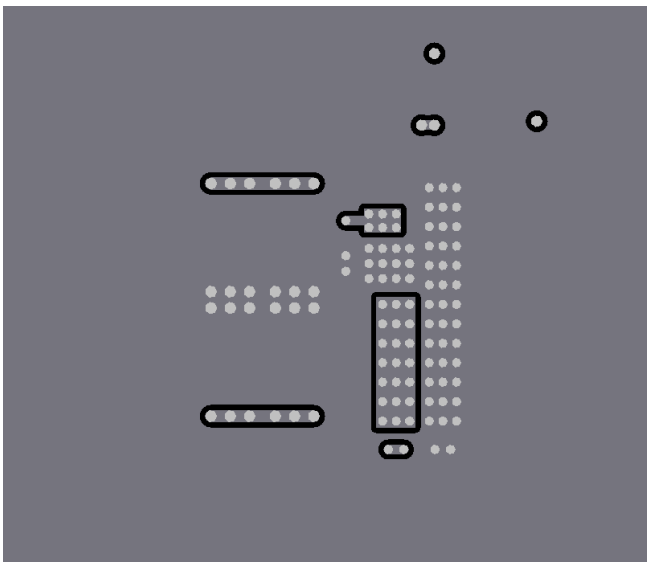


Figure 35. Typical Layer-2 Layout

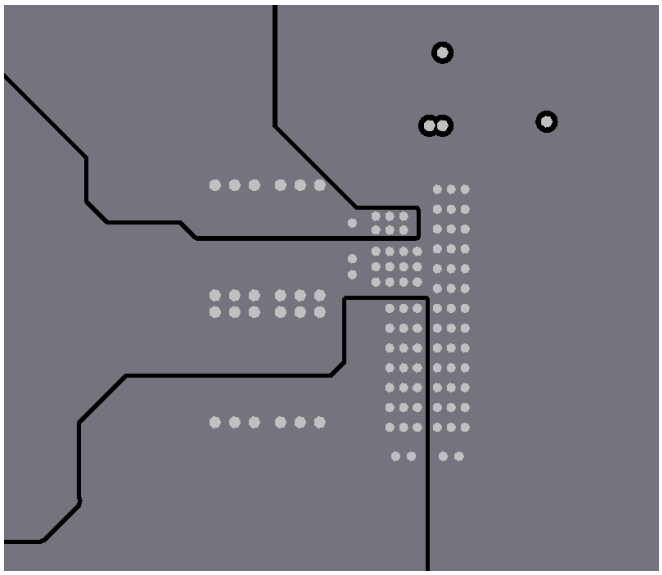


Figure 36. Typical Layer 3 Layout

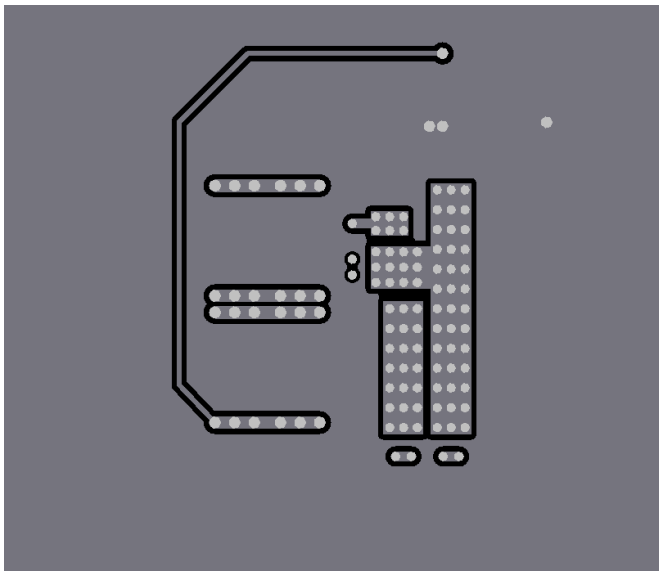


Figure 37. Typical Bottom-Layer Layout

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

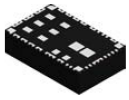
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

ADVANCE INFORMATION

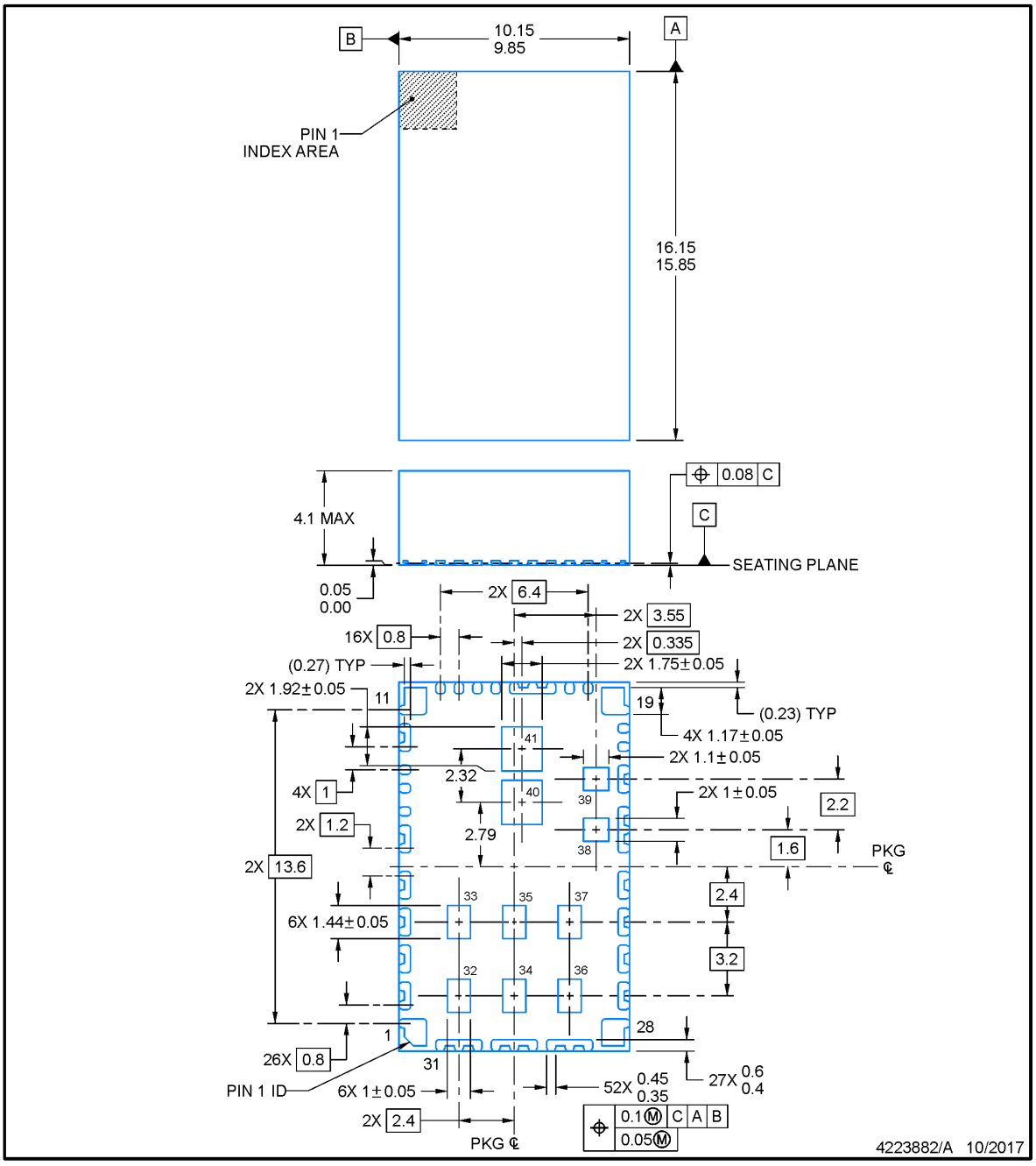
PACKAGE OUTLINE

RLX0041A



B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

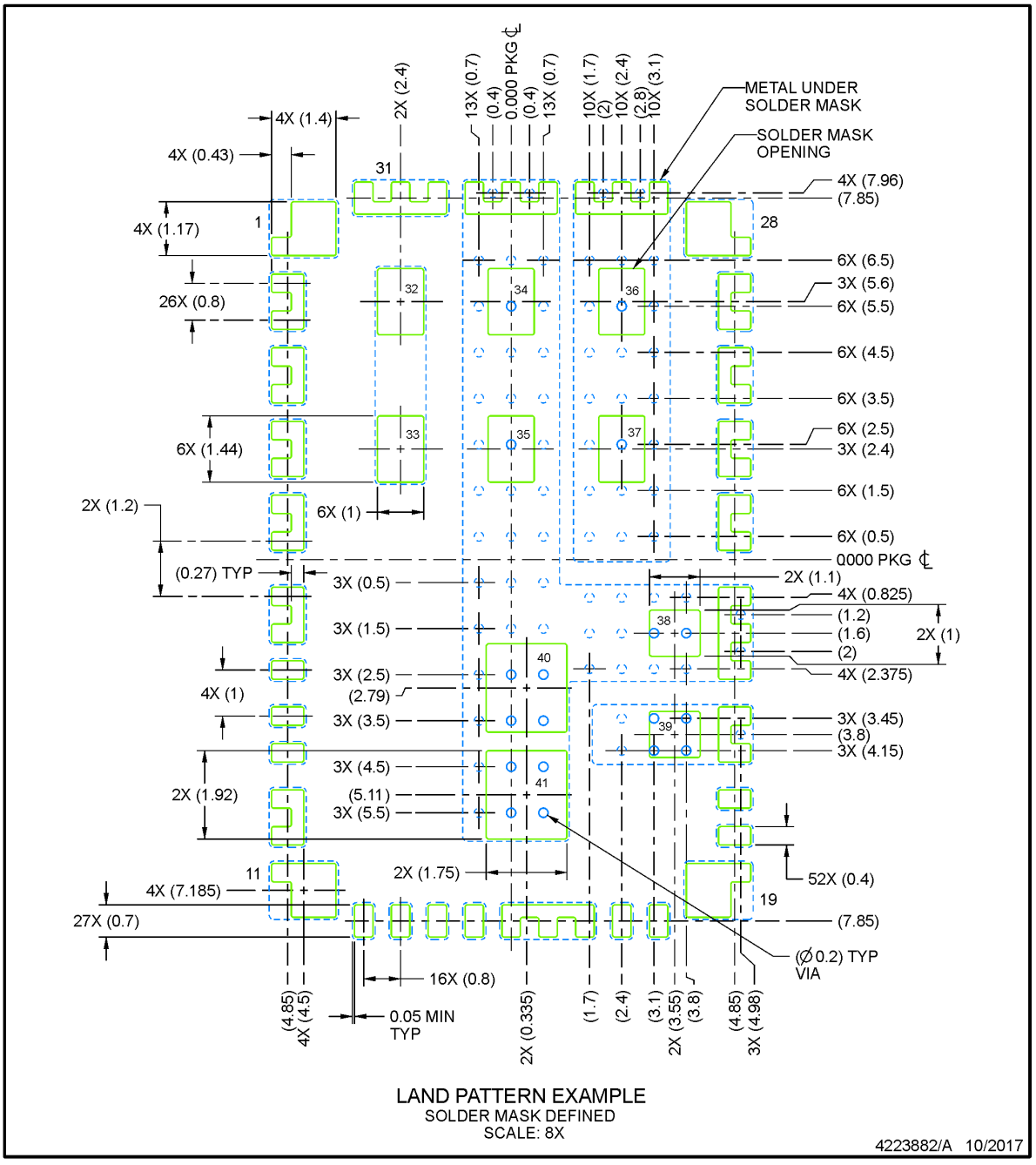
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RLX0041A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 8X

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NOTES: (continued)

4. This package designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

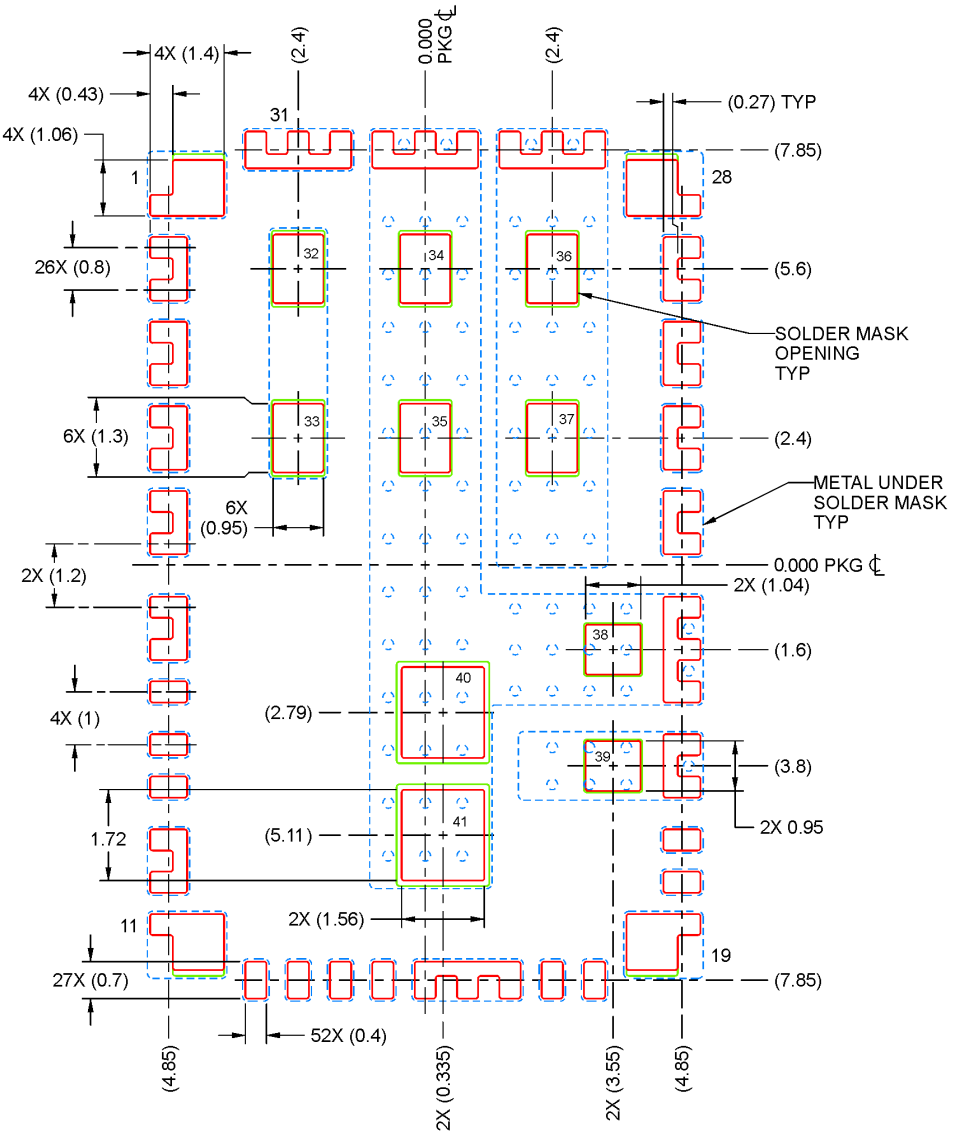
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RLX0041A — **B3QFN - 4.1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA
PADS 1,11,19,28,38 & 39: 90%; PADS 32-37: 86%; PADS 40 & 41: 80%
SCALE: 8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZM33606RLXR	PREVIEW	B2QFN	RLX	41	500	TBD	Call TI	Call TI	-40 to 105	LMZM33606	
PLMZM33606RLXR	ACTIVE	B2QFN	RLX	41	400	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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