LMX2491 6.4-GHz Low Noise RF PLL With Ramp/Chirp Generation

1 Features

- –227-dBc/Hz Normalized PLL Noise
- 500-MHz to 6.4-GHz Wideband PLL
- 3.15-V to 5.25-V Charge Pump PLL Supply
- Versatile Ramp / Chirp Generation
- 200-MHz Maximum Phase Detector Frequency
- FSK / PSK Modulation Pin
- Digital Lock Detect
- Single 3.3-V Supply Capability

2 Applications

- FMCW Radars
- Military Radars
- Microwave Backhaul
- Test and Measurement
- Satellite Communications
- Wireless Infrastructure
- Sampling Clock for High-Speed ADC/DAC

3 Description

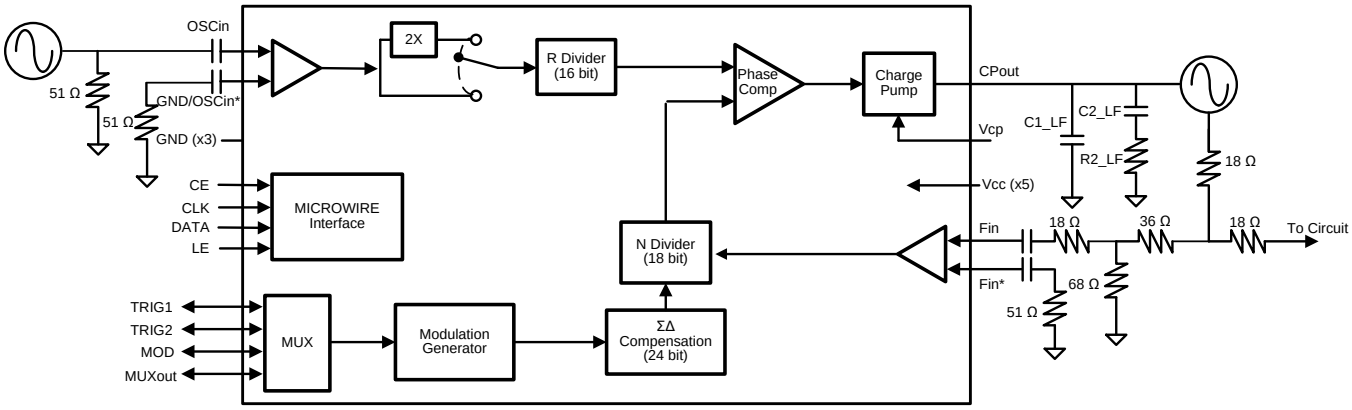
The LMX2491 device is a low-noise, 6.4-GHz wideband delta-sigma fractional N PLL with ramp and chirp generation. It consists of a phase frequency detector, programmable charge pump, and high frequency input for the external VCO. The LMX2491 supports a broad and flexible class of ramping capabilities, including FSK, PSK, and configurable piecewise linear FM modulation profiles of up to 8 segments. It supports fine PLL resolution and fast ramp with up to a 200-MHz phase detector rate. The LMX2491 allows any of its registers to be read back. The LMX2491 can operate with a single 3.3-V supply. Moreover, supporting up to 5.25-V charge pump can eliminate the need of external amplifier, leading to a simpler solution with improved phase noise performance.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMX2491	WQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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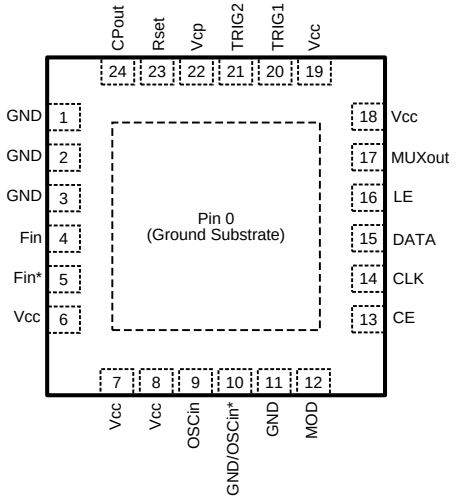
4 Revision History

DATE	REVISION	NOTES
October 2016	*	Initial release.

5 Pin Configuration and Functions

RTW Package
24-Pin VQFN
Top View



Pin Functions

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
0	DAP	GND	Die Attach Pad. Connect to PCB ground plane.
1	GND	GND	Ground for charge pump.
2, 3	GND	GND	Ground for Fin Buffer
4, 5	Fin Fin*	Input	Complimentary high frequency input pins. Should be AC-coupled. If driving single-ended, impedance as seen from Fin and Fin* pins looking outwards from the part should be roughly the same.
6	Vcc	Supply	Power Supply for Fin Buffer
7	Vcc	Supply	Supply for On-chip LDOs
8	Vcc	Supply	Supply for OSCin Buffer
9	OSCin	Input	Reference Frequency Input
10	GND/ OSCin*	GND/Input	Complimentary input for OSCin. If not used, it is recommended to match the termination as seen from the OSCin terminal looking outwards. However, this may also be grounded as well.
11	GND	GND	Ground for OSCin Buffer
12	MOD	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
13	CE	Input	Chip Enable
14	CLK	GND	Serial Programming Clock.
15	DATA	GND	Serial Programming Data
16	LE	Input	Serial Programming Latch Enable
17	MUXout	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
18	Vcc	Supply	Supply for delta sigma engine.
19	Vcc	Supply	Supply for general circuitry.
20	TRIG1	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
21	TRIG2	Input/Output	Multiplexed Input/Output Pins for Ramp Triggers, FSK/PSK Modulation, FastLock, and Diagnostics
22	Vcp	Supply	Power Supply for the charge pump.
23	Rset	NC	No connect.
24	CPout	Output	Charge Pump Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CP}	Supply voltage for charge pump	V_{CC}	5.5	V
CPout	Charge pump output pin	–0.3	V_{CP}	V
Vcc	All V_{CC} pins	–0.3	3.6	V
	All other I/O pins	–0.3	V_{CC} + 0.3	V
T_{Solder}	Lead temperature (solder 4 seconds)		260	°C
$T_{Junction}$	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	–65	150	°C
T_{DP}	Storage dew point		3	°C

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	PLL supply voltage	3.15	3.3	3.45	V
V_{CP}	Charge pump supply voltage	V_{CC}		5.25	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC (1)		LMX2491 RTW (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

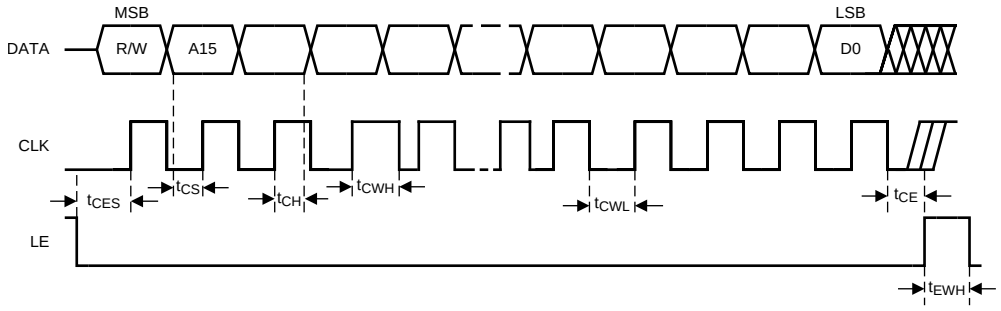
3.15 V ≤ V_{CC} ≤ 3.45 V, V_{CC} ≤ V_{CP} ≤ 5.25 V, –40 °C ≤ T_A ≤ 85 °C, except as specified. Typical values are at V_{CC} = V_{CP} = 3.3 V, 25 °C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Icc	Current consumption	All V_{CC} pins	Fpd = 10 MHz		45		mA
			Fpd = 100 MHz		50		
			Fpd = 200 MHz		55		
		V_{CP} pin	Kpd = 0.1 mA		2		
			Kpd = 1.6 mA		10		
			Kpd = 3.1 mA		19		
IccPD	Current	POWERDOWN			3		
f_{OSCin}	Frequency for OSCin terminal	OSC_DIFFR=0, doubler disabled		10		600	MHz
		OSC_DIFFR=0, doubler enabled		10		300	
		OSC_DIFFR=1, doubler disabled		10		1200	
		OSC_DIFFR=1, doubler enabled		10		600	
v_{OSCin}	Voltage for OSCin pin(1)			0.5		Vcc – 0.5	Vpp
f_{Fin}	Frequency for Fin pin			500		6400	MHz
p_{Fin}	Power for Fin pin	Single-ended operation		–5		5	dBm
f_{PD}	Phase detector frequency					200	MHz
PN1Hz	PLL figure of merit(2)				–227		dBc/Hz
PN10kHz	Normalized PLL 1/f noise(2)	Normalized to 10-kHz offset for a 1-GHz carrier.			–120		dBc/Hz
I_{CPout}TRI	Charge pump leakage tri-state leakage					10	nA
I_{CPout}MM	Charge pump mismatch(3)	V_{CPout} = V_{CP} / 2			5%		
I_{CPout}	Charge pump current	V_{CPout} = V_{CP} / 2	CPG=1X		0.1		mA
			…				
			CPG=31X		3.1		
LOGIC OUTPUT TERMINALS (MUXout,TRIG1,TRIG2,MOD)							
V_{OH}	Output high voltage			0.8 × Vcc	Vcc		V
V_{OL}	Output low voltage				0	0.2 × Vcc	V
LOGIC INPUT TERMINALS (CE,CLK,DATA,LE,MUXout,TRIG1,TRIG2,MOD)							
V_{IH}	Input high voltage			1.4		Vcc	V
V_{IL}	Input low voltage			0		0.6	V
I_{IH}	Input leakage			–5	1	5	µA
T_{CE}LOW	Chip enable low time			5			µs
T_{CE}HIGH	Chip enable high time			5			µs

(1) For optimal phase noise performance, higher input voltage and a slew rate of at least 3 V/ns is recommended
(2) PLL Noise Metrics are measured with a clean OSCin signal with a high slew rate using a wide loop bandwidth. The noise metrics model the PLL noise for an infinite loop bandwidth as:
PLL_Total = 10 × log($10^{PLL\_Flat/10}$ + $10^{PLL\_Flicker(Offset)/10}$)
PLL_Flat = PN1Hz + 20×log(N) + 10 × log(Fpd/1Hz)
PLL_Flicker = PN10kHz - 10 × log(Offset/10kHz) + 20 × log(Fvco/1GHz)
(3) Charge pump mismatch varies as a function of charge pump voltage. Consult typical performance characteristics to see this variation.

6.7 Timing Requirements, Programming Interface (CLK, DATA, LE)

		MIN	TYP	MAX	UNIT
t_{CE}	Clock to LE low time	10			ns
t_{CS}	Data to clock setup time	4			ns
t_{CH}	Data to clock hold time	4			ns
t_{CWH}	Clock pulse width high	10			ns
t_{CWL}	Clock pulse width low	10			ns
t_{CES}	Enable to clock setup time	10			ns
t_{EWH}	Enable pulse width high	10			ns

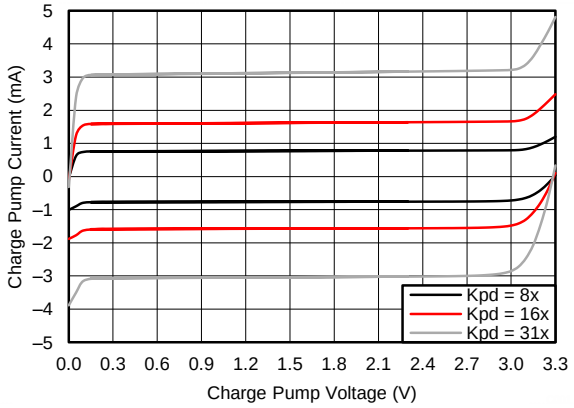


There are several other considerations for programming:

- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift register to an actual counter.
- If no LE signal is given after the last data bit and the clock is kept toggling, then these bits are read into the next lower register. This eliminates the need to send the address each time.
- A slew rate of at least 30 V/µs is recommended for the CLK, DATA, and LE signals
- Timing specs also apply to readback. Readback can be done through the MUXout, TRIG1, TRIG2, or MOD terminals.

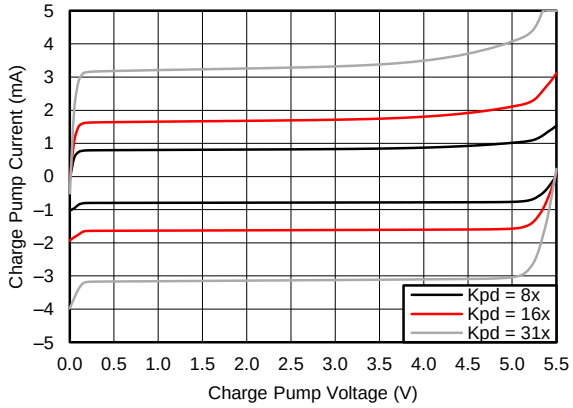
Figure 1. Serial Data Input Timing

6.8 Typical Characteristics



For a charge pump supply of 3.3 V, optimal performance is for a typical charge pump output voltage between 0.5 and 2.8 volts.

Figure 2. Charge Pump Current for Vcp = 3.3 V



For a charge pump supply voltage of 5 volts or higher, optimal performance is typically for a charge pump output voltage between 0.5 and 4.5 volts.

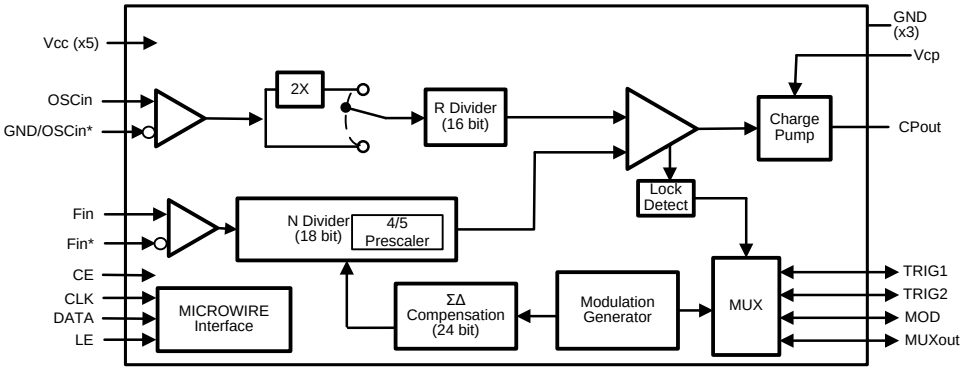
Figure 3. Charge Pump Current for Vcp = 5.5 V

7 Detailed Description

7.1 Overview

The LMX2491 is a microwave PLL, consisting of a reference input and divider, high frequency input and divider, charge pump, ramp generator, and other digital logic. The Vcc power supply pins run at a nominal 3.3 volts, while the charge pump supply pin, Vcp, operates anywhere from Vcc to 5 volts. The device is designed to operate with an external loop filter and VCO. Modulation is achieved by manipulating the MASH engine.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 OSCin Input

The reference can be applied in several ways. If using a differential input, this must be terminated differentially with a 100-Ω resistance and AC-coupled to the OSCin and GND/OSCin* terminals. If driving this single-ended, then the GND/OSCin* terminal may be grounded, although better performance is attained by connecting the GND/OSCin* terminal through a series resistance and capacitance to ground to match the OSCin terminal impedance.

7.3.2 OSCin Doubler

The OSCin doubler allows the input signal to the OSCin to be doubled to have higher phase detector frequencies. This works by clocking on both the rising and falling edges of the input signal, so it therefore requires a 50% input duty cycle.

7.3.3 R Divider

The R counter is 16 bits divides the OSCin signal from 1 to 65535. If DIFF_R = 0, then any value can be chosen in this range. If DIFF_R=1, then the divide is restricted to 2,4,8, and 16, but allows for higher OSCin frequencies.

7.3.4 PLL N Divider

The 16-bit N divider divides the signal at the Fin terminal down to the phase detector frequency. It contains a 4/5 prescaler that creates minimum divide restrictions, but allows the N value to increment in values of one.

Table 1. Allowable Minimum N Divide for Delta Sigma Modulation Order

MODULATOR ORDER	MINIMUM N DIVIDE
Integer Mode, 1st-Order Modulator	16
2nd-Order Modulator	17
3rd-Order Modulator	19
4th-Order Modulator	25

7.3.5 Fractional Circuitry

The fractional circuitry controls the N divider with delta sigma modulation that supports a programmable first, second, third, and fourth-order modulator. The fractional denominator is a fully programmable 24-bit denominator that can support any value from 1,2,..., 2^{24}, with the exception when the device is running one of the ramps, and in this case it is a fixed size of 2^{24}.

7.3.6 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the R and N dividers and generates a correction voltage corresponding to the phase error. This voltage is converted to a correction current by the charge pump. The phase detector frequency, f_{PD}, can be calculated as follows: $f_{PD} = f_{OSCin} \times OSC\_2X / R$.

The charge pump supply voltage on this device, Vcp, can be either run at the Vcc voltage, or up to 5.25 volts to get higher tuning voltages to present to the VCO.

7.3.7 External Loop Filter

The loop filter is external to the device and is application specific. Texas Instruments website has details on this at Vcc on www.ti.com.

7.3.8 Fastlock and Cycle Slip Reduction

This PLL has a Fastlock and a cycle slipping reduction feature. The user can enable these two features by programming FL_TOC to a non-zero value. Every time PLL_N (the feedback divider, register R17 and R16) is written, the Fastlock feature engages for the prescribed time set in FL_TOC. There are 3 actions that can be enabled while the counter is running:

1. Change the charge pump current to the desired higher value FL_CPG. Typically this value would be set to the maximum at 31x. This increases the loop bandwidth and hence reduces lock time.
2. Change the phase detector frequency with FL_CSR to reduce cycle slipping. The phase detector frequency can be reduced by a factor 2 or 4 to reduce cycle slipping.
3. The loop filter can be configured to have a switchable R2 resistor to increase loop bandwidth and hence reduce lock time. A resistor R2pLF is added in parallel to R2_LF and connected to the a terminal on the PLL to use the internal switch. Any of the terminal MUXout, MOD, TRIG1,or TRIG2 can be configured for the function. The terminal configuration is set as *Output TOC Running*. Also set the terminal as *output inverted OD* (OD for open-drain) so the output will be high impedance in normal operation and act as ground in Fastlock. The suggested schematic for that feature is shown in Figure 4.

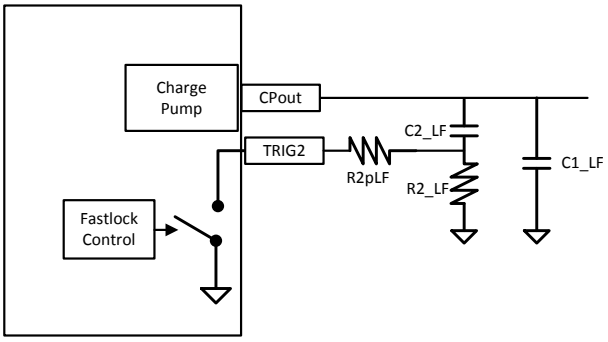


Figure 4. Suggested Schematic to Enable the Variable Loop Bandwidth Filter In Fastlock Mode

Table 2. Fastlock Settings: Charge Pump Gain and Fastlock Pin Status

PARAMETER	NORMAL OPERATION	FASTLOCK OPERATION
Charge Pump Gain	CPG	FL_CPG
Device Pin (TRIG1, TRIG2, MOD, or MUXout)	High Impedance	Grounded

The resistor and the charge pump current are changed simultaneously so that the phase margin remains the same while the loop bandwidth is by a factor of K as shown in the following table:

Table 3. Suggested Equations to Calculate R2pLF

PARAMETER		CALCULATION
FL_CPG	Charge Pump Gain in Fastlock	Typically use the highest value.
K	Loop Bandwidth Multiplier	K=sqrt(FL_CPG/CPG)
R2pLF	External Resistor	R2 / (K-1)

Cycle slip reduction is another method that can also be used to speed up lock time by reducing cycle slipping. Cycle slipping typically occurs when the phase detector frequency exceeds about 100x the loop bandwidth of the PLL. Cycle slip reduction works in a different way than fastlock. To use this, the phase detector frequency is decreased while the charge pump current is simultaneously increased by the same factor. Although the loop bandwidth is unchanged, the ratio of the phase detector frequency to the loop bandwidth is, and this is helpful for cases when the phase detector frequency is high. Because cycle slip reduction changes the phase detector rate, it also impacts other things that are based on the phase detector rate, such as the fastlock timeout-counter and ramping controls.

7.3.9 Lock Detect and Charge Pump Voltage Monitor

The LMX2491 offers two methods to determine if the PLL is in lock: charge pump voltage monitoring and digital lock detect. These features can be used individually or in conjunction to give a reliable indication of when the PLL is in lock. The output of this detection can be routed to the TRIG1, TRIG2, MOD, or MUXout terminals.

7.3.9.1 Charge Pump Voltage Monitor

The charge pump voltage monitor allows the user to set low (CMP_THR_LOW) and high (CMP_THR_HIGH) thresholds for a comparator that monitors the charge pump output voltage.

Table 4. Desired Comparator Threshold Register Settings for Two Charge Pump Supplies

V_{CP}	THRESHOLD	SUGGESTED LEVEL
3.3 V	CPM_THR_LOW = (Vthresh + 0.08) / 0.085	6 for 0.5-V limit
	CPM_THR_HIGH = (Vthresh - 0.96) / 0.044	42 for 2.8-V limit
5.0 V	CPM_THR_LOW = (Vthresh + 0.056) / 0.137	4 for 0.5-V limit
	CPM_THR_HIGH = (Vthresh -1.23) / 0.071	46 for 4.5-V limit

7.3.9.2 Digital Lock Detect

Digital lock detect works by comparing the phase error as presented to the phase detector. If the phase error plus the delay as specified by the PFD_DLY bit is outside the tolerance as specified by DLD_TOL, then this comparison would be considered to be an error, otherwise passing. The DLD_ERR_CNT specifies how may errors are necessary to cause the circuit to consider the PLL to be unlocked. The DLD_PASS_CNT specifies how many passing comparisons are necessary to cause the PLL to be considered to be locked and also resets the count for the errors. The DLD_TOL value should be set to no more than half of a phase detector period plus the PFD_DLY value. The DLD_ERR_CNT and DLD_PASS_CNT values can be decreased to make the circuit more sensitive. If the circuit is too sensitive, then chattering can occur and the DLD_ERR_CNT, DLD_PASS_CNT, or DLD_TOL values should be increased.

NOTE

If the OSCin signal goes away and there is no noise or self-oscillation at the OSCin pin, then it is possible for the digital lock detect to indicate a locked state when the PLL really is not in lock. If this is a concern, then digital lock detect can be combined with charge pump voltage monitor to detect this situation.

7.3.10 FSK/PSK Modulation

Two-level FSK or PSK modulation can be created whenever a trigger event, as defined by the FSK_TRIG field is detected. This trigger can be defined as a transition on a terminal (TRIG1, TRIG2, MOD, or MUXout) or done purely in software. The RAMP_PM_EN bit defines the modulation to be either FSK or PSK and the FSK_DEV register determines the amount of the deviation. Remember that the FSK_DEV[32:0] field is programmed as the 2's complement of the actual desired FSK_DEV value. This modulation can be added to the modulation created from the ramping functions as well.

Table 5. How to Obtain Deviation for Two Types of Modulation

RAMP_PM_EN	MODULATION TYPE	DEVIATION
0	2 Level FSK	Fpd × FSK_DEV / 2^{24}
1	2 Level PSK	360° × FSK_DEV / 2^{24}

7.3.11 Ramping Functions

The LMX2491 supports a broad and flexible class of FMCW modulation formed by up to 8 linear ramps. When the ramping function is running, the denominator is fixed to a forced value of 2^{24} = 16777216. The waveform always starts at RAMP0 when the LSB of the PLL_N (R16) is written to. After it is set up, it starts at the initial frequency and have piecewise linear frequency modulation that deviates from this initial frequency as specified by the modulation. Each of the eight ramps can be individually programmed. Various settings are as follows:

Table 6. Register Descriptions of the Ramping Function

RAMP CHARACTERISTIC	PROGRAMMING FIELD NAME	DESCRIPTION
Ramp Length	RAMPx_LEN RAMPx_DLY	The user programs the length of the ramp in phase detector cycles. If RAMPx_DLY=1, then each count of RAMPx_LEN is actually two phase detector cycles.
Ramp Slope	RAMPx_LEN RAMPx_DLY RAMPx_INC	The user does not directly program slope of the line, but rather this is done by defining how long the ramp is and how much the fractional numerator is increased per phase detector cycle. The value for RAMPx_INC is calculated by taking the total expected increase in the frequency, expressed in terms of how much the fractional numerator increases, and dividing it by RAMPx_LEN. The value programmed into RAMPx_INC is actually the two's complement of the desired mathematical value.
Trigger for Next Ramp	RAMPx_NEXT_TRIG	The event that triggers the next ramp can be defined to be the ramp finishing or can wait for a trigger as defined by TRIG A, TRIG B, or TRIG C.
Next Ramp	RAMPx_NEXT	This sets the ramp that follows. Waveforms are constructed by defining a chain ramp segments. To make the waveform repeat, make RAMPx_NEXT point to the first ramp in the pattern.
Ramp Fastlock	RAMPx_FL	This allows the ramp to use a different charge pump current or use Fastlock
Ramp Flags	RAMPx_FLAG	This allows the ramp to set a flag that can be routed to external terminals to trigger other devices.

7.3.11.1 Ramp Count

If it is desired that the ramping waveform keep repeating, then all that is needed is to make the RAMPx_NEXT of the final ramp equal to the first ramp. This runs until the RAMP_EN bit is set to zero. If this is not desired, then one can use the RAMP_COUNT to specify how may times the specified pattern is to repeat.

7.3.11.2 Ramp Comparators and Ramp Limits

The ramp comparators and ramp limits use programable thresholds to allow the device to detect whenever the modulated waveform frequency crosses a limit as set by the user. The difference between these is that comparators set a flag to alert the user while a ramp limits prevent the frequency from going beyond the prescribed threshold. In either case, these thresholds are expressed by programming the Extended_Fractional_Numerator.

$$\text{Extended\_Fractional\_Numerator} = \text{Fractional\_Numerator} + (N\text{-}N^*) \times 2^{24} \quad (1)$$

Equation 1, N is the PLL feedback value without ramping and N* is the instantaneous value during ramping. The actual value programmed is the 2's complement of Extended_Fractional_Numerator.

Table 7. Register Descriptions of Ramp Comparators and Limits

TYPE	PROGRAMMING BIT	THRESHOLD
Ramp Limits	RAMP_LIMIT_LOW	Lower Limit
	RAMP_LIMIT_HIGH	Upper Limit
Ramp Comparators	RAMP_CMP0 RAMP_CMP1	For the ramp comparators, if the ramp is increasing and exceeds the value as specified by RAMP_CMPx, then the flag goes high, otherwise it is low. If the ramp is decreasing and goes below the value as specified by RAMP_CMPx, then the flag goes high, otherwise it is low.

7.3.12 Power-on-reset (POR)

The power-on-reset circuitry sets all the registers to a default state when the device is powered up. This same reset can be done by programming SWRST=1. In the programming section, the power on reset state is given for all the programmable fields.

7.4 Device Functional Modes

The two primary ways to use the LMX2491 are to run it to generate a set of frequencies

7.4.1 Continuous Frequency Generator

In this mode, the LMX2491 generates a single frequency that only changes when the N divider is programmed to a new value. In this mode, the RAMP_EN bit is set to 0 and the ramping controls are not used. The fractional denominator can be programmed to any value from 1 to 16777216. In this kind of application, the PLL is tuned to different channels, but at each channel, the goal is to generate a stable fixed frequency.

7.4.1.1 Integer Mode Operation

In integer mode operation, the VCO frequency needs to be an integer multiple of the phase detector frequency. This can be the case when the output frequency or frequencies are nicely related to the input frequency. As a rule of thumb, if this an be done with a phase detector of as high as the lesser of 10 MHz or the OSCin frequency, then this makes sense. To operate the device in integer mode, disable the fractional circuitry by programming the fractional order (FRAC_ORDER), dithering (FRAC_DITH), and numerator (FRAC_NUM) to zero.

7.4.1.2 Fractional Mode Operation

In fractional mode, the output frequency does not need to be an integer multiple of the phase detector frequency. This makes sense when the channel spacing is more narrow or the input and output frequencies are not nicely related. There are several programmable controls for this such as the modulator order, fractional dithering, fractional numerator, and fractional denominator. There are many trade-offs with choosing these, but here are some guidelines

Table 8. Fractional Mode Register Descriptions and Recommendations

PARAMETER	FIELD NAME	HOW TO CHOOSE
Fractional Numerator and Denominator	FRAC_NUM FRAC_DEN	The first step is to find the fractional denominator. To do this, find the frequency that divides the phase detector frequency by the channel spacing. For instance, if the output ranges from 5000 to 5050 in 5-MHz steps and the phase detector is 100 MHz, then the fractional denominator is 100 MHz/5 = 20. So for a an output of 5015 MHz, the N divider would be 50 + 3/20. In this case, the fractional numerator is 3 and the fractional denominator is 20. Sometimes when dithering is used, it makes sense to express this as a larger equivalent fraction. Note that if ramping is active, the fractional denominator is forced to 2^{24}.
Fractional Order	FRAC_ORDER	There are many trade-offs, but in general try either the 2nd or 3rd-order modulator as starting points. The 3rd-order modulator may give lower main spurs, but may generate others. Also if dithering is involved, it can generate phase noise.
Dithering	FRAC_DITH	Dithering can reduce some fractional spurs, but add noise. Consult application note *AN-1879 Fractional N Frequency Synthesis* for more details on this.

7.4.2 Modulated Waveform Generator

In this mode, the device can generate a broad class of frequency sweeping waveforms. The user can specify up to 8 linear segments to generate these waveforms. When the ramping function is running, the denominator is fixed to a forced value of 2^{24} = 16777216

In addition to the ramping functions, there is also the capability to use a terminal to add phase or frequency modulation that can be done by itself or added on top of the waveforms created by the ramp generation functions.

7.5 Programming

7.5.1 Loading Registers

The device is programmed using several 24 bit registers. The first 16 bits of the register are the address, followed by the next 8 bits of data. The user has the option to pull the LE terminal high after this data, or keep sending data and it applies this data to the next lower register. So instead of sending three registers of 24 bits each, one could send a single 40-bit register with the 16 bits of address and 24 bits of data. For that matter, the entire device could be programmed as a single register if desired.

7.6 Register Maps

Registers are programmed in REVERSE order from highest to lowest. Registers NOT shown in this table or marked as reserved can be written as all 0s unless otherwise stated. The POR value is the power on reset value that is assigned when the device is powered up or the SWRST bit is asserted.

Table 9. Register Map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0	POR
0	0	0	0	0	1	1	0	0	0	0x18
1	0x1	Reserved								0x00
2	0x2	0	0	0	0	0	SWRST	POWERDOWN[1:0]		0x00
3-15	0x3 - 0xF	Reserved								-
16	0x10	PLL_N[7:0]								0x64
17	0x11	PLL_N[15:8]								0x00
18	0x12	0	FRAC_ORDER[2:0]			FRAC_DITHER[1:0]		PLL_N[17:16]		0x00
19	0x13	FRAC_NUM[7:0]								0x00
20	0x14	FRAC_NUM[15:8]								0x00
21	0x15	FRAC_NUM[23:16]								0x00
22	0x16	FRAC_DEN[7:0]								0x00
23	0x17	FRAC_DEN[15:8]								0x00
24	0x18	FRAC_DEN[23:16]								0x00
25	0x19	PLL_R[7:0]								0x04
26	0x1A	PLL_R[15:8]								0x00
27	0x1B	0	FL_CSR[1:0]		PFD_DLY[1:0]		PLL_R_DIFF	0	OSC_2X	0x08
28	0x1C	0	0	CPPOL	CPG[4:0]					0x00
29	0x1D	FL_TOC[10:8]			FL_CPG[4:0]					0x00
30	0x1E	0	CPM_FLAGL	CPM_THR_LOW[5:0]						0x0a
31	0x1F	0	CPM_FLAGH	CPM_THR_HIGH[5:0]						0x32
32	0x20	FL_TOC[7:0]								0x00
33	0x21	DLD_PASS_CNT[7:0]								0x0f
34	0x22	DLD_TOL[2:0]			DLD_ERR_CNTR[4:0]					0x00
35	0x23	MOD_MUX[5]	1	MUXout_MUX[5]	TRIG2_MUX[5]	TRIG1_MUX[5]	0	0	1	0x41

Register Maps (continued)

Table 9. Register Map (continued)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0	POR
36	0x24	TRIG1_MUX[4:0]					TRIG1_PIN[2:0]			0x08
37	0x25	TRIG2_MUX[4:0]					TRIG2_PIN[2:0]			0x10
38	0x26	MOD_MUX[4:0]					MOD_PIN[2:0]			0x18
39	0x27	MUXout_MUX[4:0]					MUXout_PIN[2:0]			0x38
40-57	0x28-0x39	Reserved								-
58	0x3A	RAMP_TRIG_A[3:0]				0	RAMP_ PM_EN	RAMP_ CLK	RAMP_EN	0x00
59	0x3B	RAMP_TRIG_C[3:0]				RAMP_TRIG_B[3:0]				0x00
60	0x3C	RAMP_CMP0[7:0]								0x00
61	0x3D	RAMP_CMP0[15:8]								0x00
62	0x3E	RAMP_CMP0[23:16]								0x00
63	0x3F	RAMP_CMP0[31:24]								0x00
64	0x40	RAMP_CMP0_EN[7:0]								0x00
65	0x41	RAMP_CMP1[7:0]								0x00
66	0x42	RAMP_CMP1[15:8]								0x00
67	0x43	RAMP_CMP1[23:16]								0x00
68	0x44	RAMP_CMP1[31:24]								0x00
69	0x45	RAMP_CMP1_EN[7:0]								0x00
70	0x46	0	FSK_TRIG[1:0]		RAMP_ LIMH[32]	RAMP_ LIML[32]	FSK_ DEV[32]	RAMP_ CMP1[32]	RAMP_ CMP0[32]	0x08
71	0x47	FSK_DEV[7:0]								0x00
72	0x48	FSK_DEV[15:8]								0x00
73	0x49	FSK_DEV[23:16]								0x00
74	0x4A	FSK_DEV[31:24]								0x00
75	0x4B	RAMP_LIMIT_LOW[7:0]								0x00
76	0x4C	RAMP_LIMIT_LOW[15:8]								0x00
77	0x4D	RAMP_LIMIT_LOW[23:16]								0x00
78	0x4E	RAMP_LIMIT_LOW[31:24]								0x00
79	0x4F	RAMP_LIMIT_HIGH[7:0]								0xff
80	0x50	RAMP_LIMIT_HIGH[15:8]								0xff
81	0x51	RAMP_LIMIT_HIGH[23:16]								0xff
82	0x52	RAMP_LIMIT_HIGH[31:24]								0xff
83	0x53	RAMP_COUNT[7:0]								0x00
84	0x54	RAMP_TRIG_INC[1:0]		RAMP_ AUTO	RAMP_COUNT[12:8]					0x00
85	0x55	Reserved								0x00
86	0x56	RAMP0_INC[7:0]								0x00
87	0x57	RAMP0_INC[15:8]								0x00
88	0x58	RAMP0_INC[23:16]								0x00
89	0x59	RAMP0_ DLY	RAMP0_ FL	RAMP0_INC[29:24]						0x00
90	0x5A	RAMP0_LEN[7:0]								0x00
91	0x5B	RAMP0_LEN[15:8]								0x00
92	0x5C	RAMP0_NEXT[2:0]			RAMP0_ NEXT_TRIG[1:0]		RAMP0_ RST	RAMP0_FLAG[1:0]		0x00
93	0x5D	RAMP1_INC[7:0]								0x00
94	0x5E	RAMP1_INC[15:8]								0x00

Register Maps (continued)

Table 9. Register Map (continued)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0	POR
95	0x5F	RAMP1_INC[23:16]								0x00
96	0x60	RAMP1_ DLY	RAMP1_ FL	RAMP1_INC[29:24]						0x00
97	0x61	RAMP1_LEN[7:0]								0x00
98	0x62	RAMP1_LEN[15:8]								0x00
99	0x63	RAMP1_NEXT[2:0]			RAMP1_ NEXT_TRIG[1:0]		RAMP1_ RST	RAMP1_FLAG[1:0]		0x00
100	0x64	RAMP2_INC[7:0]								0x00
101	0x65	RAMP2_INC[15:8]								0x00
102	0x66	RAMP2_INC[23:16]								0x00
103	0x67	RAMP2 DLY	RAMP2_ FL	RAMP2_INC[29:24]						0x00
104	0x68	RAMP2_LEN[7:0]								0x00
105	0x69	RAMP2_LEN[15:8]								0x00
106	0x6A	RAMP2_NEXT[2:0]			RAMP2_ NEXT_TRIG[1:0]		RAMP2_ RST	RAMP2_FLAG[1:0]		0x00
107	0x6B	RAMP3_INC[7:0]								0x00
108	0x6C	RAMP3_INC[15:8]								0x00
109	0x6D	RAMP3_INC[23:16]								0x00
110	0x6E	RAMP3_ DLY	RAMP3_ FL	RAMP3_INC[29:24]						0x00
111	0x6F	RAMP3_LEN[7:0]								0x00
112	0x70	RAMP3_LEN[15:8]								0x00
113	0x71	RAMP3_NEXT[2:0]			RAMP3_ NEXT_TRIG[1:0]		RAMP3_ RST	RAMP3_FLAG[1:0]		0x00
114	0x72	RAMP4_INC[7:0]								0x00
115	0x73	RAMP4_INC[15:8]								0x00
116	0x74	RAMP4_INC[23:16]								0x00
117	0x75	RAMP4_ DLY	RAMP4_ FL	RAMP4_INC[29:24]						0x00
118	0x76	RAMP4_LEN[7:0]								0x00
119	0x77	RAMP4_LEN[15:8]								0x00
120	0x78	RAMP4_NEXT[2:0]			RAMP4_ NEXT_TRIG[1:0]		RAMP4_ RST	RAMP4_FLAG[1:0]		0x00
121	0x79	RAMP5_INC[7:0]								0x00
122	0x7A	RAMP5_INC[15:8]								0x00
123	0x7B	RAMP5_INC[23:16]								0x00
124	0x7C	RAMP5_ DLY	RAMP5_ FL	RAMP5_INC[29:24]						0x00
125	0x7D	RAMP5_LEN[7:0]								0x00
126	0x7E	RAMP5_LEN[15:8]								0x00
127	0x7F	RAMP5_NEXT[2:0]			RAMP5_ NEXT_TRIG[1:0]		RAMP5_ RST	RAMP5_FLAG[1:0]		0x00
128	0x80	RAMP6_INC[7:0]								0x00
129	0x81	RAMP6_INC[15:8]								0x00
130	0x82	RAMP6_INC[23:16]								0x00
131	0x83	RAMP6_ DLY	RAMP6_ FL	RAMP6_INC[29:24]						0x00
132	0x84	RAMP6_LEN[7:0]								0x00

Register Maps (continued)

Table 9. Register Map (continued)

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0	POR
133	0x85	RAMP6_LEN[15:8]								0x00
134	0x86	RAMP6_NEXT[2:0]			RAMP6_ NEXT_TRIG[1:0]		RAMP6_ RST	RAMP6_FLAG[1:0]		0x00
135	0x87	RAMP7_INC[7:0]								0x00
136	0x88	RAMP7_INC[15:8]								0x00
137	0x89	RAMP7_INC[23:16]								0x00
138	0x8A	RAMP7_ DLY	RAMP7_ FL	RAMP7_INC[29:24]						0x00
139	0x8B	RAMP7_LEN[7:0]								0x00
140	0x8C	RAMP7_LEN[15:8]								0x00
141	0x8D	RAMP7_NEXT[2:0]			RAMP7_ NEXT_TRIG[1:0]		RAMP7_ RST	RAMP7_FLAG[1:0]		0x00
142-32767	0x8E-0x7fff	Reserved								0x00

7.6.1 Register Field Descriptions

The following sections go through all the programmable fields and their states. Additional information is also available in the applications and feature descriptions sections as well. The POR column is the power on reset state that this field assumes if not programmed.

7.6.1.1 POWERDOWN and Reset Fields

Table 10. POWERDOWN and Reset Fields

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
POWERDOWN [1:0]	R2[1:0]	0	POWERDOWN Control	**Value**	**POWERDOWN State**
				0	POWERDOWN, ignore CE
				1	Power Up, ignore CE
				2	Power State Defined by CE terminal state
				3	Reserved
SWRST	R2[2]	0	Software Reset. Setting this bit sets all registers to their POR default values.	**Value**	**Reset State**
				0	Normal Operation
				1	Register Reset

7.6.1.2 Dividers and Fractional Controls

Table 11. Dividers and Fractional Controls

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
PLL_N [17:0]	R18[1] to R16[0]	16	Feedback N counter Divide value. Minimum count is 16. Maximum is 262132. Writing of the register R16 begins any ramp execution when RAMP_EN=1.		
FRAC_ DITHER [1:0]	R18[3:2]	0	Dither used by the fractional modulator	**Value**	**Dither**
				0	Weak
				1	Medium
				2	Strong
				3	Disabled
FRAC_ ORDER [2:0]	R18[6:4]	0	Fractional Modulator order	**Value**	**Modulator Order**
				0	Integer Mode
				1	1st Order Modulator
				2	2nd Order Modulator
				3	3rd Order Modulator
				4	4th Order Modulator
				5-7	Reserved
FRAC_NUM [23:0]	R21[7] to R19[0]	0	Fractional Numerator. This value should be less than or equal to the fractional denominator.		
FRAC_DEN [23:0]	R24[7] to R22[0]	0	Fractional Denominator. If the RAMP_EN=1, this field is ignored and the denominator is fixed to 2^{24}.		
PLL_R [15:0]	R26[7] to R25[0]	1	Reference Divider value. Selecting 1 bypasses counter.		
OSC_2X	R27[0]	0	Enables the Doubler before the Reference divider	**Value**	**Doubler**
				0	Disabled
				1	Enabled
PLL_R _DIFF	R27[2]	0	Enables the Differential R counter. This allows for higher OSCin frequencies, but restricts PLL_R to divides of 2,4,8 or 16.	**Value**	**R Divider**
				0	Single-Ended
				1	Differential
PFD_DLY [1:0]	R27[4:3]	1	Sets the charge pump minimum pulse width. This could potentially be a trade-off between fractional spurs and phase noise. Setting 1 is recommended for general use.	**Value**	**Pulse Width**
				0	Reserved
				1	860 ps
				2	1200 ps
				3	1500 ps
CPG [4:0]	R28[4:0]	0	Charge pump gain	**Value**	**Charge Pump State**
				0	Tri-State
				1	100 µA
				2	200 µA
				…	…
				31	3100 µA
CPPOL	R28[5]	0	Charge pump polarity is used to accommodate VCO with either polarity so that feedback of the PLL is always correct. IF reference (R) output is faster than feedback (N) output, R28[5]==0 THEN charge pump will source current R28[5]==1 THEN charge pump will sink current	**Value**	**Charge Pump Polarity**
				0	Positive
				1	Negative

7.6.1.2.1 Speed Up Controls (Cycle Slip Reduction and Fastlock)

Table 12. FastLock and Cycle Slip Reduction

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
FL_ CSR [1:0]	R27[6:5]	0	Cycle Slip Reduction (CSR) reduces the phase detector frequency by multiplying both the R and N counters by the CSR value while either the FastLock Timer is counting or the RAMPx_FL=1 and the part is ramping. Care must be taken that the R and N divides remain inside the range of the counters. Cycle slip reduction is generally not recommended during ramping.	**Value**	**CSR Value**
				0	Disabled
				1	x 2
				2	x 4
				3	Reserved
FL_ CPG [4:0]	R29[4:0]	0	Charge pump gain only when Fast Lock Timer is counting down or a ramp is running with RAMPx_FL=1	**Value**	**Fastlock Charge Pump Gain**
				0	Tri-State
				1	100 µA
				2	200 µA
				…	…
				31	3100 µA
FL_ TOC [10:0]	R29[7:5] and R32[7:0]	0	Fast Lock Timer. This counter starts counting when the user writes the PLL_N(Register R16). During this time the FL_CPG gain is sent to the charge pump, and the FL_CSR shifts the R and N counters if enabled. When the counter terminates, the normal CPG is presented and the CSR undo's the shifts to give a normal PFD frequency.	**Value**	**Fastlock Timer Value**
				0	Disabled
				1	1 x 32 = 32
				...	
				2047	2047 x 32 = 65504

7.6.2 Lock Detect and Charge Pump Monitoring

Table 13. Lock Detect and Charge Pump Monitor

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
CPM_THR _LOW [5:0]	R30[5:0]	0x0A	Charge pump voltage low threshold value. When the charge pump voltage is below this threshold, the LD goes low.	**Value**	**Threshold**
				0	Lowest
				…	…
				63	Highest
CPM_FLAGL	R30[6]	-	This is a read only bit. Low indicates the charge pump voltage is below the minimum threshold.	**Value**	**Flag Indication**
				0	Charge pump is below CPM_THR_LOW threshold
				1	Charge pump is above CPM_THR_LOW threshold
CPM_THR _HIGH [5:0]	R31[5:0]	0x32	Charge pump voltage high threshold value. When the charge pump voltage is above this threshold, the LD goes low.	**Value**	**Threshold**
				0	Lowest
				…	…
				63	Highest
CPM_FLAGH	R31[6]	-	This is a read only bit. Charge pump voltage high comparator reading. High indicates the charge pump voltage is above the maximum threshold.	**Value**	**Threshold**
				0	Charge pump is below CPM_THR_HIGH threshold
				1	Charge pump is above CPM_THR_HIGH threshold
DLD_ PASS_CNT [7:0]	R33[7:0]	0xff	Digital Lock Detect Filter amount. There must be at least DLD_PASS_CNT good edges and less than DLD_ERR edges before the DLD is considered in lock. Making this number smaller speeds the detection of lock, but also allows a higher chance of DLD chatter.		
DLD_ ERR_CNT [4:0]	R34[4:0]	0	Digital Lock Detect error count. This is the maximum number of errors greater than DLD_TOL that are allowed before DLD is de-asserted. Although the default is 0, the recommended value is 4.		
DLD _TOL [2:0]	R34[7:5]	0	Digital Lock detect edge window. If both N and R edges are within this window, it is considered a “good” edge. Edges that are farther apart in time are considered “error” edges. Window choice depends on phase detector frequency, charge pump minimum pulse width, fractional modulator order and the users desired margin.	**Value**	**Window and Fpd Frequency**
				0	1 ns (Fpd > 130 MHz)
				1	1.7 ns (80 MHz , Fpd ≤ 130 MHz)
				2	3 ns (60 MHz , Fpd ≤ 80 MHz)
				3	6 ns (45 MHz , Fpd ≤ 60 MHz)
				4	10 ns (30 MHz < Fpd ≤ 45 MHz)
				5	18 ns (Fpd ≤ 30 MHz)
				6 and 7	Reserved

7.6.3 TRIG1,TRIG2,MOD, and MUXout Pins

Table 14. TRIG1, TRIG2, MOD, and MUXout Terminal States

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
TRIG1 _PIN [2:0]	R36[2:0]	0	This is the terminal drive state for the TRIG1, TRIG2, MOD, and MUXout Pins	**Value**	**Pin Drive State**
				0	TRISTATE (default)
				1	Open Drain Output
				2	Pullup / Pulldown Output
TRIG2 _PIN [2:0]	R37[2:0]	0		3	Reserved
MOD_ PIN [2:0]	R38[2:0]	0		4	GND
MUXout_ PIN [2:0]	R39[2:0]	0		5	Inverted Open Drain Output
				6	Inverted Pullup / Pulldown Output
				7	Input

Table 15. TRIG1, TRIG2, MOD, and MUXout Selections

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
TRIG1_MUX [5:0] TRIG2_MUX [5:0] MOD_MUX [5:0] MUXout_MUX [5:0]	R36[7:3], R37.3 R36[7:3], R35.3 R37[7:3], R35.4 R38[7:3], R35.7	1 2 3 7	These fields control what signal is muxed to or from the TRIG1,TRIG2, MOD, and MUXout pins. Some of the abbreviations used are: COMP0, COMP1: Comparators 0 and 1 LD, DLD: Lock Detect, Digital Lock Detect CPM: Charge Pump Monitor CPG: Charge Pump Gain CPUP: Charge Pump Up Pulse CPDN: Charge Pump Down Pulse	**Value**	**MUX State**
				0	GND
				1	Input TRIG1
				2	Input TRIG2
				3	Input MOD
				4	Output TRIG1 after synchronizer
				5	Output TRIG2 after synchronizer
				6	Output MOD after synchronizer
				7	Output Read back
				8	Output CMP0
				9	Output CMP1
				10	Output LD (DLD good AND CPM good)
				11	Output DLD
				12	Output CPMON good
				13	Output CPMON too High
				14	Output CPMON too low
				15	Output RAMP LIMIT EXCEEDED
				16	Output R Divide/2
				17	Output R Divide/4
				18	Output N Divide/2
				19	Output N Divide/4
				20	Reserved
				21	Reserved
				22	Output CMP0RAMP
				23	Output CMP1RAMP
				24	Reserved
				25	Reserved
				26	Reserved
				27	Reserved
				28	Output Faslock
				29	Output CPG from RAMP
				30	Output Flag0 from RAMP
				31	Output Flag1 from RAMP
				32	Output TRIGA
				33	Output TRIGB
				34	Output TRIGC
				35	Output R Divide
				36	Output CPUP
				37	Output CPDN
				38	Output RAMP_CNT Finished
				39 to 63	Reserved

7.6.4 Ramping Functions

Table 16. Ramping Functions

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
RAMP_EN	R58[0]	0	Enables the RAMP functions. When this bit is set, the Fractional Denominator is fixed to 2^{24}. RAMP execution begins at RAMP0 upon the PLL_N[7:0] write. The Ramp should be set up before RAMP_EN is set.	**Value**	**Ramp**
				0	Disabled
				1	Enabled
RAMP_CLK	R58[1]	0	RAMP clock input source. The ramp can be clocked by either the phase detector clock or the MOD terminal based on this selection.	**Value**	**Source**
				0	Phase Detector
				1	MOD Terminal
RAMP_PM_EN	R58[2]	0	Phase modulation enable.	**Value**	**Modulation Type**
				0	Frequency Modulation
				1	Phase Modulation
RAMP_TRIGA [3:0] RAMP_TRIGB [3:0] RAMP_TRIGC [3:0]	R58[7:4] R59[3:0] R59[7:4]	0	Trigger A,B, and C Sources	**Value**	**Source**
				0	Never Triggers (default)
				1	TRIG1 terminal rising edge
				2	TRIG2 terminal rising edge
				3	MOD terminal rising edge
				4	DLD Rising Edge
				5	CMP0 detected (level)
				6	RAMPx_CPG Rising edge
				7	RAMPx_FLAG0 Rising edge
				8	Always Triggered (level)
				9	TRIG1 terminal falling edge
				10	TRIG2 terminal falling edge
				11	MOD terminal falling edge
				12	DLD Falling Edge
				13	CMP1 detected (level)
				14	RAMPx_CPG Falling edge
				15	RAMPx_FLAG0 Falling edge
RAMP_CMP0 [32:0]	R70[0], R63[7] to R60[0]	0	Twos compliment of Ramp Comparator 0 value. Be aware of that the MSB is in Register R70.		
RAMP_CMP0_EN [7:0]	R64[7:0]	0	Comparator 0 is active during each RAMP corresponding to the bit. Place a 1 for ramps it is active in and 0 for ramps it should be ignored. RAMP0 corresponds to R64[0], RAMP7 corresponds to R64[7]		
RAMP_CMP1 [32:0]	R70[1], R68[7] to R65[0]	0	Twos compliment of Ramp Comparator 1 value. Be aware of that the MSB is in Register R70.		
RAMP_CMP1_EN [7:0]	R69[7:0]	0	Comparator 1 is active during each RAMP corresponding to the bit. Place a 1 for ramps it is active in and 0 for ramps it should be ignored. RAMP0 corresponds to R64[0], RAMP7 corresponds to R64[7].		
FSK_TRIG [1:0]	R76[4] to R75[3]	0	Deviation trigger source. When this trigger source specified is active, the FSK_DEV value is applied.	**Value**	**Trigger**
				0	Always Triggered
				1	Trigger A
				2	Trigger B
				3	Trigger C
FSK_DEV [32:0]	R70[2], R74[7] to R71[0]	0	Twos compliment of the deviation value for frequency modulation and phase modulation. This value should be written with 0 when not used. Be aware that the MSB is in Register R70.		

Table 16. Ramping Functions (continued)

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
RAMP_LIMIT_LOW [32:0]	R70[3], R78[7] to 75[0]	0	Twos compliment of the ramp lower limit that the ramp can not go below . The ramp limit occurs before any deviation values are included. Care must be taken if the deviation is used and the ramp limit must be set appropriately. Be aware that the MSB is in Register R70.		
RAMP_LIMIT_HIGH [32:0]	R70[4], R82[7] to 79.0[0]	0xffffffff	Twos compliment of the ramp higher limit that the ramp can not go above. The ramp limit occurs before any deviation values are included. Care must be taken if the deviation is used and the ramp limit must be set appropriately. Be aware that the MSB is in Register R70.		
RAMP_COUNT [12:0]	R84[4] to R83[0]	0	Number of RAMPs that is executed before a trigger or ramp enable is brought down. Load zero if this feature is not used. Counter is automatically reset when RAMP_EN goes from 0 to 1.		
RAMP_AUTO	R84[5]	0	Automatically clear RAMP_EN when RAMP Count hits terminal count.	**Value**	**Ramp**
				0	RAMP_EN unaffected by ramp counter (default)
				1	RAMP_EN automatically brought low when ramp counter terminal counts
RAMP_TRIG_INC [1:0]	R84[7:6]	0	Increment Trigger source for RAMP Counter. To disable ramp counter, load a count value of 0.	**Value**	**Source**
				0	Increments occur on each ramp transition
				1	Increment occurs on trigA
				2	Increment occurs on trigB
				3	Increment occurs on trigC

7.6.5 Individual Ramp Controls

These bits apply for all eight ramps. For the field names, x can be 0,1,2,3,4,5,6, or 7.

Table 17. Individual Ramp Controls

FIELD	LOCATION	POR	DESCRIPTION AND STATES		
RAMPx _INC[29:0]	Varies	0	Signed ramp increment.		
RAMPx _FL	Varies	0	This enables fastlock and cycle slip reduction for ramp x.	Value	CPG
				0	Disabled
				1	Enabled
RAMPx _DLY	Varies	0	During this ramp, each increment takes 2 PFD cycles per LEN clock instead of the normal 1 PFD cycle. Slows the ramp by a factor of 2.	Value	Clocks
				0	1 PFD clock per RAMP tick.(default)
				1	2 PFD clocks per RAMP tick.
RAMPx _LEN	Varies	0	Number of PFD clocks (if DLY is 0) to continue to increment RAMP. 1=>1 cycle, 2=>2 etc. Maximum of 65536 cycles.		
RAMPx _FLAG[1:0]	Varies	0	General purpose FLAGS sent out of RAMP.	Value	Flag
				0	Both FLAG1 and FLAG0 are zero. (default)
				1	FLAG0 is set, FLAG1 is clear
				2	FLAG0 is clear, FLAG1 is set
				3	Both FLAG0 and FLAG1 are set.
RAMP0 _RST	Varies	0	Forces a clear of the ramp accumulator. This is used to erase any accumulator creep that can occur depending on how the ramps are defined. Should be done at the start of a ramp pattern.	Value	Reset
				0	Disabled
				1	Enabled
RAMPx_ NEXT _TRIG [1:0]	Varies	0	Determines what event is necessary to cause the state machine to go to the next ramp. It can be set to when the RAMPx_LEN counter reaches zero or one of the events for Triggers A, B, or C.	Value	Operation
				0	RAMPx_LEN
				1	TRIG_A
				2	TRIG_B
				3	TRIG_C
RAMP0 _NEXT[2:0]	Varies	0	The next RAMP to execute when the length counter times out		

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMX2491 can be used in a broad class of applications such as generating a single frequency for a high frequency clock, generating a tunable range of frequencies, or generating swept waveforms that can be used in applications such as radar.

8.2 Typical Application

Figure 5 is an example of hat could be used in a typical application.

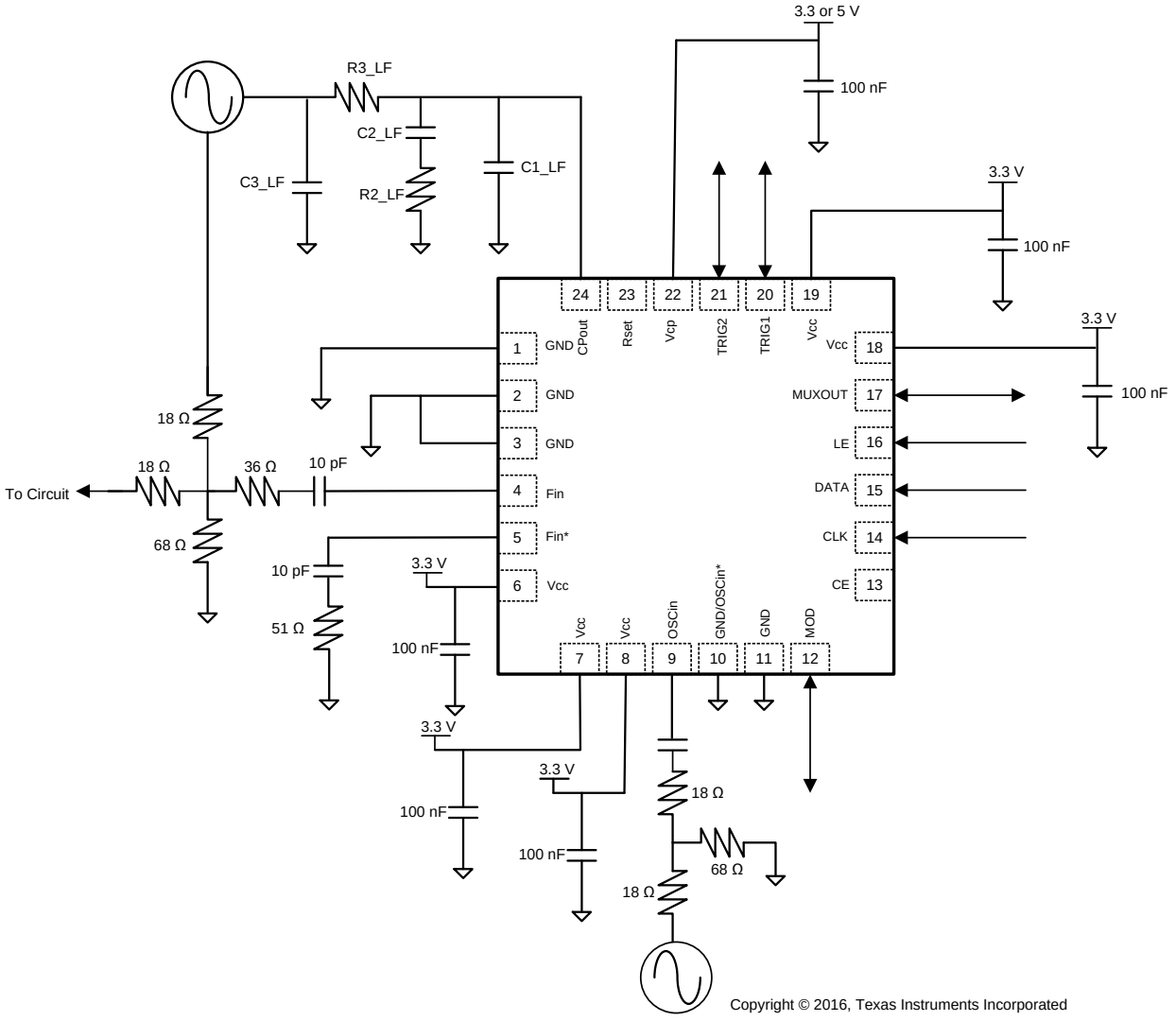


Figure 5. Typical Schematic

9 Power Supply Recommendations

For power supplies, TI recommends placing 100 nF close to each of the power supply pins. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree.

10 Layout

10.1 Layout Guidelines

For layout examples, the EVM instructions are the most comprehensive document. In general, the layout guidelines are similar to most other PLL devices. For the high frequency Fin pin, it is recommended to use 0402 components and match the trace width to these pad sizes. Also the same needs to be done on the Fin* pin. If layout is easier to route the signal to Fin* instead of Fin, then this is acceptable as well.

10.2 Layout Example

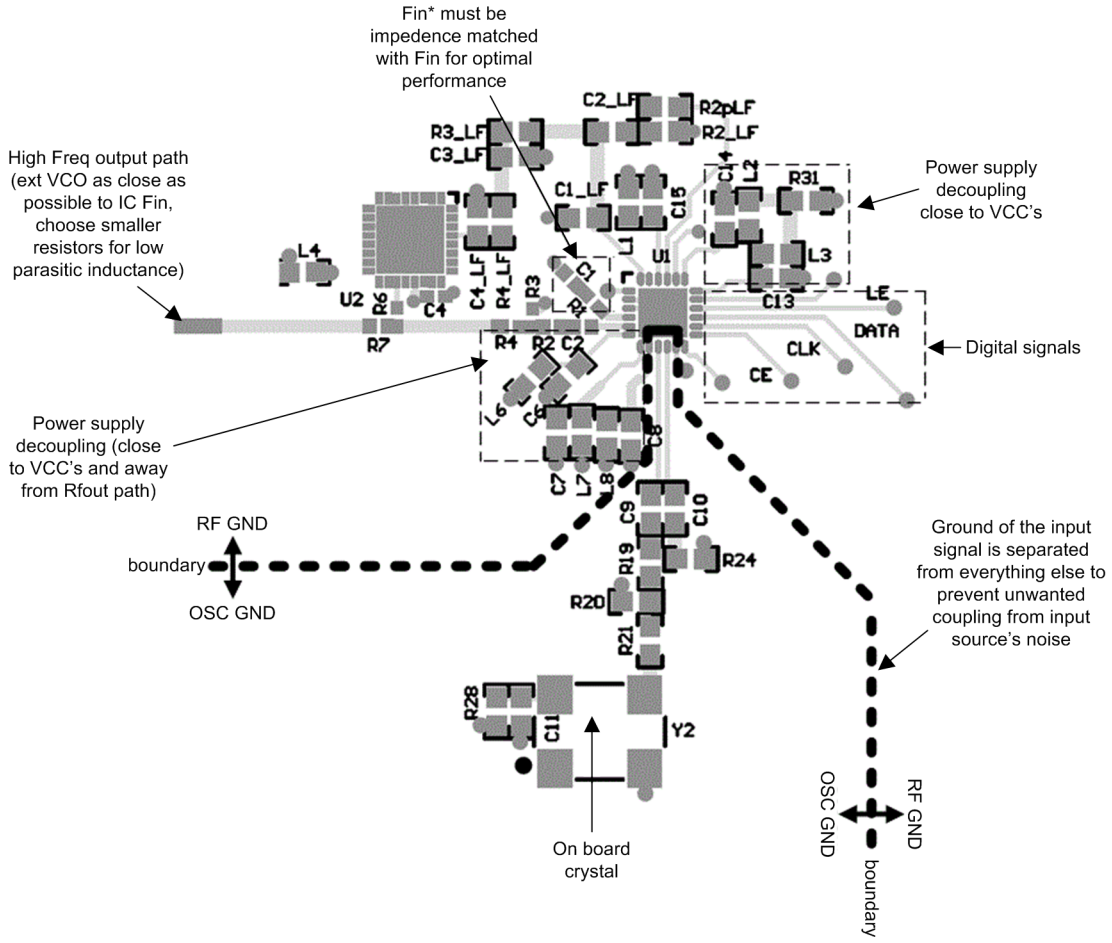


Figure 6. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

Texas Instruments has several software tools to aid in the development process including TICS Pro for programming, PLLatinum Simulator Tool for loop filter design and phase noise/spur simulation. All these tools are available at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- *AN-1879 Fractional N Frequency Synthesis* (SNAA062)
- *PLL Performance, Simulation, and Design*

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMX2491RTWR	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	X2491	Samples
LMX2491RTWT	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	X2491	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

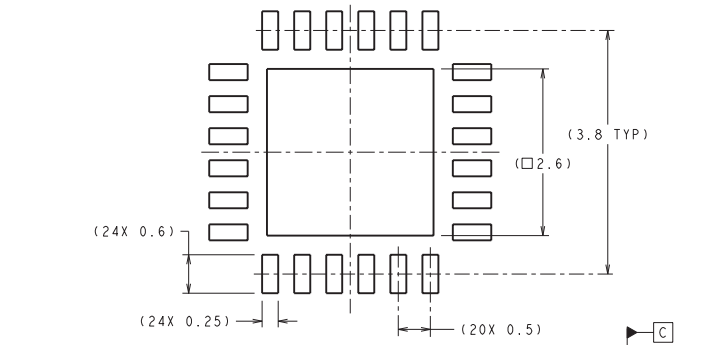
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

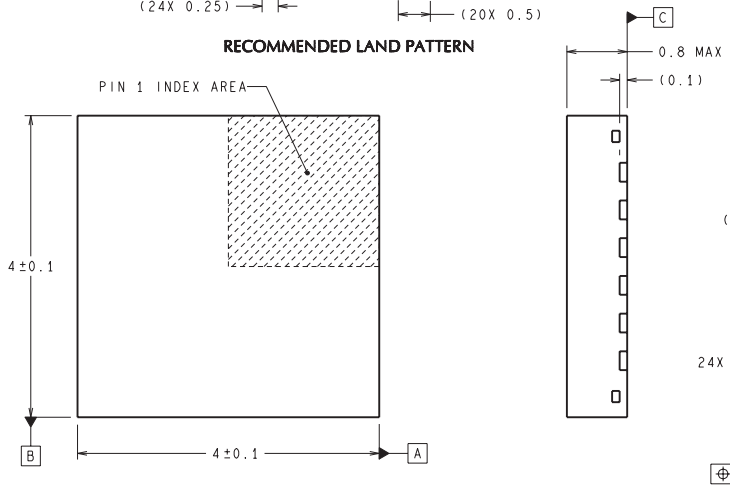
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

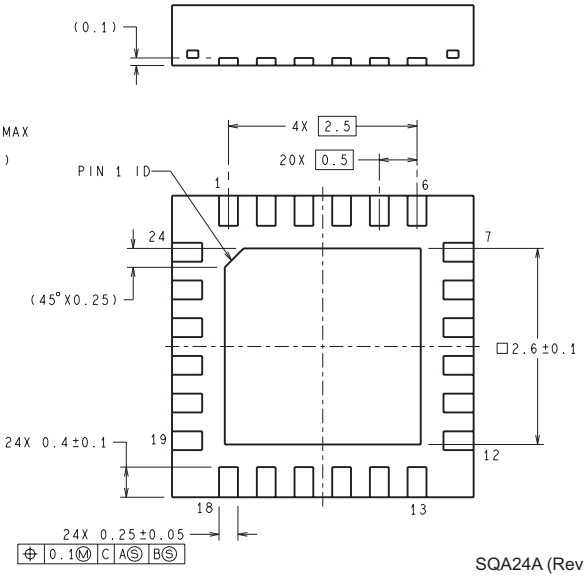
RTW0024A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





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