LMV751 Low Noise, Low Vos, Single Op Amp

Check for Samples: LMV751

FEATURES

- Low Noise 6.5nV/√Hz
- Low V_{OS} (0.05mV typ.)
- Wideband 4.5MHz GBP typ.
- Low Supply Current 500uA typ.
- Low Supply Voltage 2.7V to 5.0V
- Ground-Referenced Inputs
- Unity Gain Stable
- Small Package

APPLICATIONS

- Cellular Phones
- Portable Equipment
- Radio Systems

DESCRIPTION

The LMV751 is a high performance CMOS operational amplifier intended for applications requiring low noise and low input offset voltage. It offers modest bandwidth of 4.5MHz for very low supply current and is unity gain stable.

The output stage is able to drive high capacitance, up to 1000pF and source or sink 8mA output current.

It is supplied in the space saving SOT-23-5 Tiny package.

The LMV751 is designed to meet the demands of small size, low power, and high performance required by cellular phones and similar battery operated portable electronics.

Connection Diagram

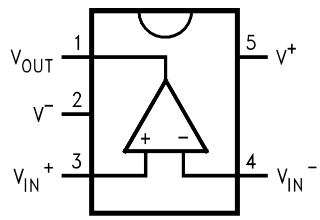

Figure 1. SOT-23-5 Top View

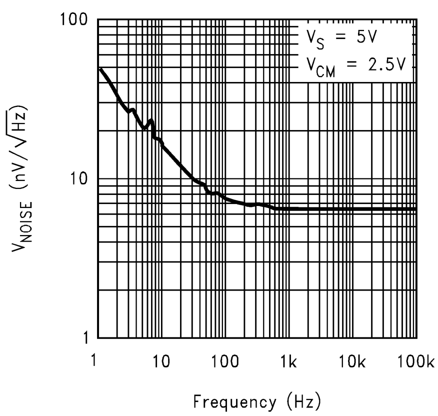

Figure 2. Voltage Noise

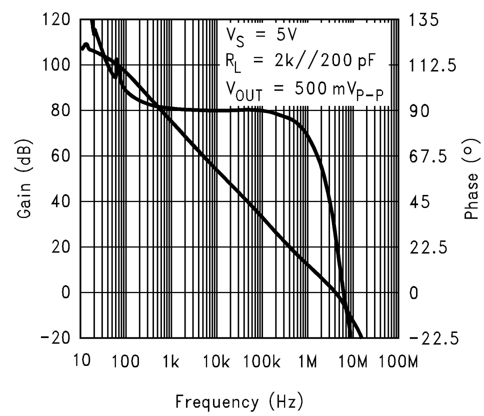

Figure 3. Gain/Phase

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1][2]

ESD Tolerance [3]	
Human Body Model	2000V
Machine Model	200V
Differential Input Voltage	±Supply Voltage
Supply Voltage (V^+ - V^-)	5.5V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature (T_J) [4]	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 1000pF.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions

Supply Voltage	2.7V to 5.0V
Temperature Range	−40°C ≤ T_J ≤ 85°C
Thermal Resistance (θ_{JA}) [1]	
DBV-5 Package, SOT-23-5	274°C/W

(1) All numbers are typical, and apply to packages soldered directly onto PC board in still air.

2.7V Electrical Characteristics

V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, T_A = 25°C unless otherwise stated. **Boldface limits** apply over the Temperature Range.

Symbol	Parameter	Condition	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		0.05	1.0 **1.5**	mV max
V_{CM}	Input common-Mode Voltage Range	For CMRR ≥ 50dB		0	V min
			1.4	1.3	V max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 1.3V	100	85 **70**	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5.0V	107	85 **70**	dB min
I_S	Supply Current		0.5	0.8 **0.85**	mA max
I_{IN}	Input Current		1.5	100	pA max
I_{OS}	Input Offset Current		0.2		pA
A_{VOL}	Voltage Gain	R_L = 10k Connect to $V^+/2$ V_O = 0.2V to 2.2V	120	110 **95**	dB min
		R_L = 2k Connect to $V^+/2$ V_O = 0.2V to 2.2V	120	100 **85**	

(1) Typical values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis

2.7V Electrical Characteristics (continued)

$V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.35V$, $T_A = 25°C$ unless otherwise stated. **Boldface limits** apply over the Temperature Range.

Symbol	Parameter	Condition	Typ (1)	Limit (2)	Units
V_O	Positive Voltage Swing	R_L = 10k Connect to $V^+/2$	2.62	2.54 **2.52**	V min
		R_L = 2k Connect to $V^+/2$	2.62	2.54 **2.52**	
V_O	Negative Voltage Swing	R_L = 10k Connect to $V^+/2$	78	140 **160**	mV max
		R_L = 2k Connect to $V^+/2$	78	160 **180**	
I_O	Output Current	Sourcing, V_O = 0V V_{IN} (diff) = ±0.5V	12	6.0 **1.5**	mA min
		Sinking, V_O = 2.7V V_{IN} (diff) = ±0.5V	11	6.0 **1.5**	
e_n (10Hz)	Input Referred Voltage Noise		15.5		nV/√Hz
e_n (1kHz)	Input Referred Voltage Noise		7		nV/√Hz
e_n (30kHz)	Input Referred Voltage Noise		7	10	nV/√Hz max
I_N(1kHz)	Input Referred Current Noise		0.01		pA/√Hz
GBW	Gain-Bandwidth Product		4.5	2	MHZ min
SR	Slew Rate		2		V/µs

5.0V Electrical Characteristics

$V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = 2.5V$, $T_A = 25°C$ unless otherwise stated.**Boldface limits** apply over the Temperature Range.

Symbol	Parameter		Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		0.05	1.0 **1.5**	mV max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 3.6V	103	85 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		0	V min
			3.7	3.6	V max
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5.0V	107	85 **70**	dB min
I_S	Supply Current		0.6	0.9 **0.95**	mA max
I_{IN}	Input Current		1.5	100	pA max
I_{OS}	Input offset Current		0.2		pA
A_{VOL}	Voltage Gain	R_L = 10k Connect to $V^+/2$ V_O = 0.2V to 4.5V	120	110 **95**	db min
		R_L = 2k Connect to $V^+/2$ V_O = 0.2V to 4.5V	120	100 **85**	
V_O	Positive Voltage Swing	R_L = 10k Connect to $V^+/2$	4.89	4.82 **4.80**	V min
		R_L = 2k Connect to $V^+/2$	4.89	4.82 **4.80**	
V_O	Negative Voltage Swing	R_L = 10k Connect to $V^+/2$	86	160 **180**	mV max
		R_L = 2k Connect to $V^+/2$	86	180 **200**	

(1) Typical values represent the most likely parametric norm.
(2) All limits are ensured by testing or statistical analysis

5.0V Electrical Characteristics (continued)

V^+ = 5.0V, V^- = 0V, V_{CM} = 2.5V, T_A = 25°C unless otherwise stated. **Boldface limits** apply over the Temperature Range.

Symbol	Parameter		Typ (1)	Limit (2)	Units
I_O	Output Current	Sourcing, V_O = 0V V_{IN} (diff) = ±0.5V	15	8.0 **2.5**	mA min
		Sinking, V_O = 5V V_{IN} (diff) = ±0.5V	20	8.0 **2.5**	
e_n (10Hz)	Input Referred Voltage Noise		15		nV/ √Hz
e_n (1kHz)	Input Referred Voltage Noise		6.5		nV/ √Hz
e_n (30kHz)	Input Referred Voltage Noise		6.5	10	nV/ √Hz max
I_N (1kHz)	Input Referred Current Noise		0.01		pA/√Hz
GBW	Gain-Bandwidth Product		5	2	MHz min
SR	Slew Rate		2.3		V/µs

Typical Performance Characteristics

Supply Current vs. Voltage

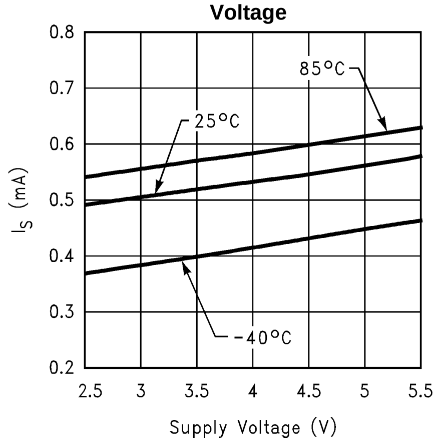

Figure 4.

V_{OS} vs. V_{CM}, V^+ = 2.7V

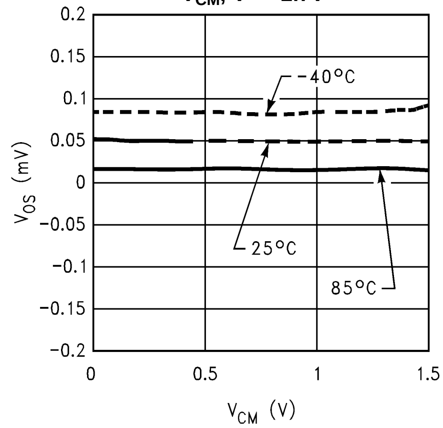

Figure 5.

V_{OS} vs. V_{CM}, V^+ = 5.0V

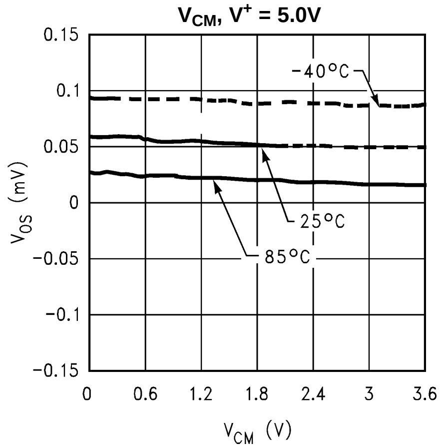

Figure 6.

Source Current vs. Out, V^+ = 2.7V

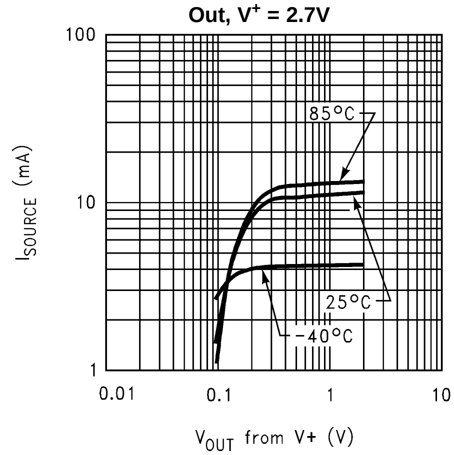

Figure 7.

Source Current vs. V_{OUT}, V^+ = 5.0V

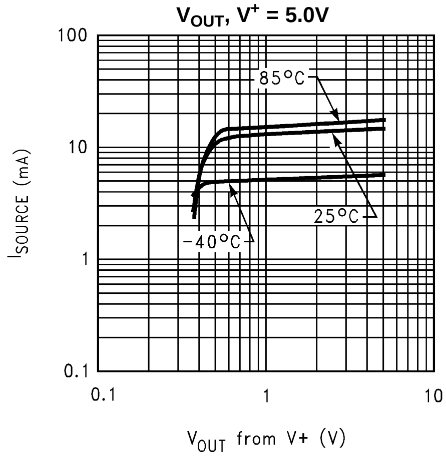

Figure 8.

Gain/Phase

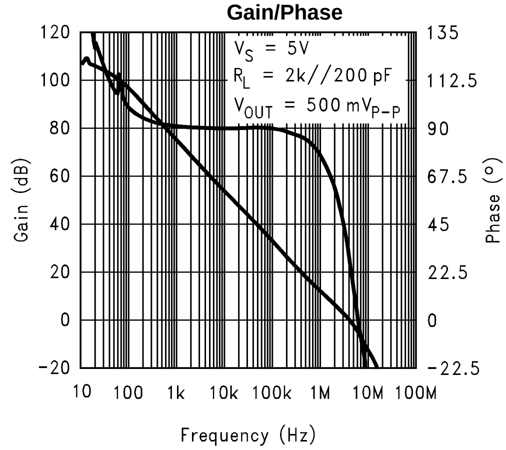

Figure 9.

Typical Performance Characteristics (continued)

Sinking Current vs. V_{OUT}, V^+ = 2.7V

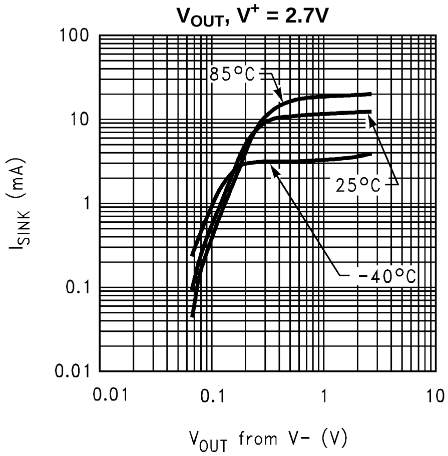

Figure 10.

Sinking Current vs. V_{OUT}, V^+ = 5.0V

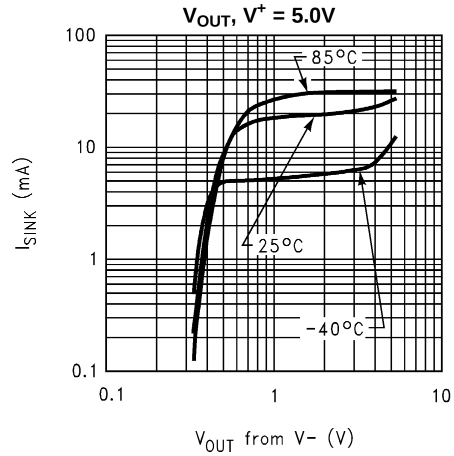

Figure 11.

V_{OS} vs. V^+

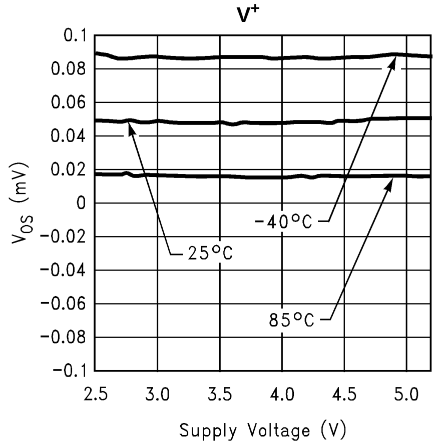

Figure 12.

V_{IN} vs. V_{OUT}, V^+ = 2.7V, R_L = 2k

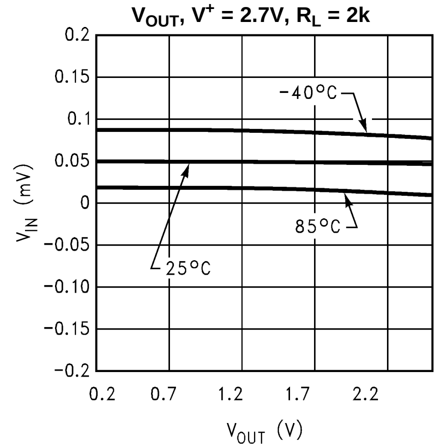

Figure 13.

V_{IN} vs. V_{OUT}, V^+ = 5.0V, R_L = 2k

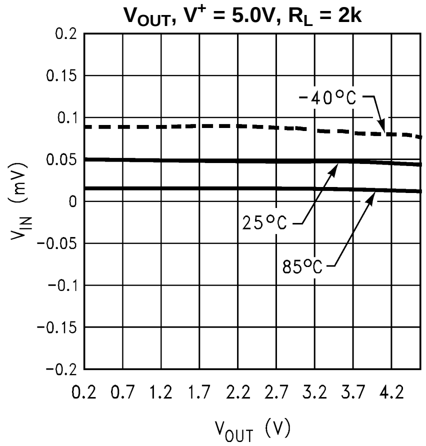

Figure 14.

Input Bias vs. V_{CM}, T_A = 25°C

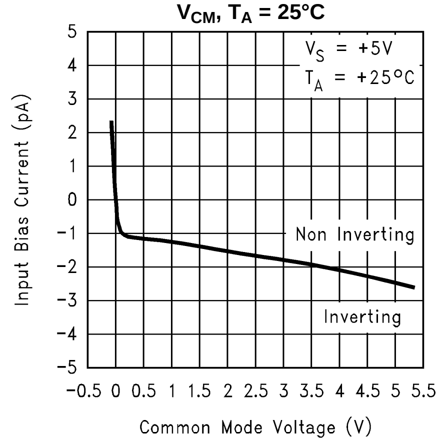

Figure 15.

Typical Performance Characteristics (continued)

Input Bias vs. V_{CM}, T_A = 85°C

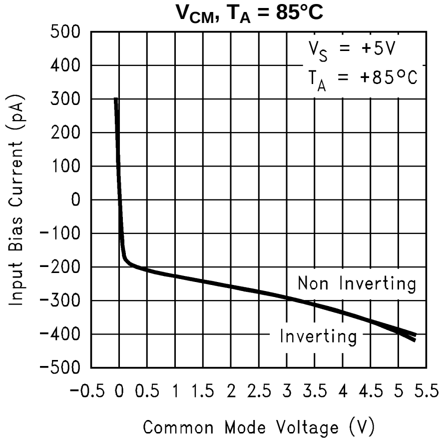

Figure 16.

PSRR +

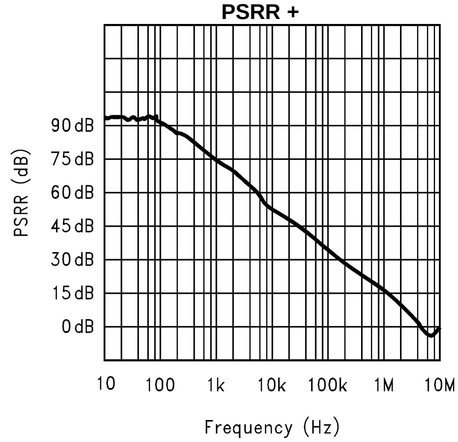

Figure 17.

PSRR −

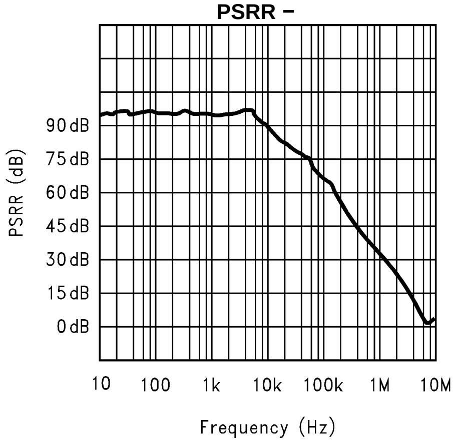

Figure 18.

Voltage Noise

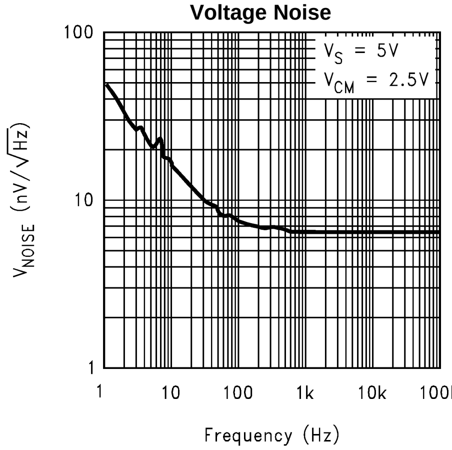

Figure 19.

CMRR

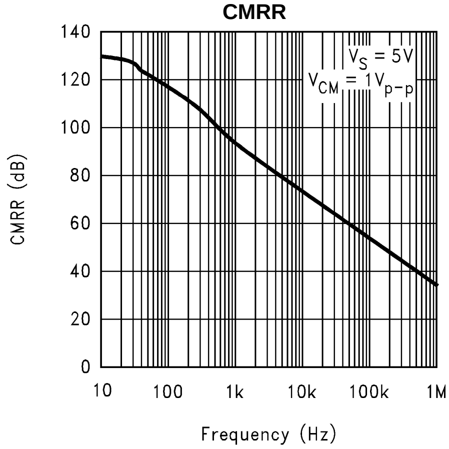

Figure 20.

APPLICATION HINTS

Noise

There are many sources of noise in a system: thermal noise, shot noise, 1/f, popcorn noise, resistor noise, just to name a few. In addition to starting with a low noise op amp, such as the LMV751, careful attention to detail will result in the lowest overall noise for the system.

To invert or not invert?

Both inverting and non-inverting amplifiers employ feedback to stabilize the closed loop gain of the block being designed. The loop gain (in decibels) equals the algebraic difference between the open loop and closed loop gains. Feedback improves the Total Harmonic Distortion (THD) and the output impedance. The various noise sources, when input referred, are amplified, not by the closed loop gain, but by the noise gain. For a non-inverting amplifier, the noise gain is equal to the closed loop gain, but for an inverting amplifier, the noise gain is equal to the closed loop gain plus one. For large gains, e.g., 100, the difference is negligible, but for small gains, such as one, the noise gain for the inverting amplifier would be two. This implies that non-inverting blocks are preferred at low gains.

Source impedance

Because noise sources are uncorrelated, the system noise is calculated by taking the RMS sum of the various noise sources, that is, the square root of the sum of the squares. At very low source impedances, the voltage noise will dominate; at very high source impedances, the input noise current times the equivalent external resistance will dominate. For a detailed example calculation, refer to Note 1.

Bias current compensation resistor

In CMOS input op amps, the input bias currents are very low, so there is no need to use R_{COMP} (see Figure 21 and Figure 22) for bias current compensation that would normally be used with early generation bipolar op amps. In fact, inclusion of the resistor would act as another thermal noise source in the system, increasing the overall noise.

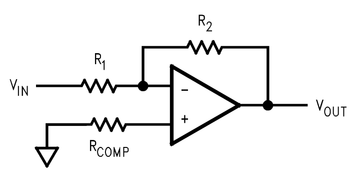

Figure 21. Bias Current Compensation Resistor

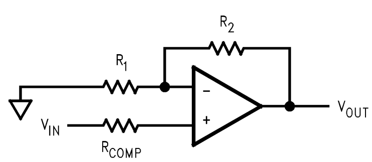

Figure 22. Bias Current Compensation Resistor

Resistor types

Thermal noise is generated by any passive resistive element. This noise is "white"; meaning it has a constant spectral density. Thermal noise can be represented by a mean-square voltage generator e_R^2 in series with a noiseless resistor, where e_R^2 is given by: Where:

e_R^2 = 4K TRB (volts)^2

where

- T = temperature in °K
- R = resistor value in ohms
- B = noise bandwidth in Hz
- K = Boltzmann's constant (1.38 x 10-23 W-sec/°K) (1)

Actual resistor noise measurements may have more noise than the calculated value. This additional noise component is known as excess noise. Excess noise has a 1/f spectral response, and is proportional to the voltage drop across the resistor. It is convenient to define a noise index when referring to excess noise in resistors. The noise index is the RMS value in uV of noise in the resistor per volt of DC drop across the resistor in a decade of frequency. Noise index expressed in dB is:

$$NI = 20 \log ((E_{EX}/V_{DC}) \times 10^6) \text{ db}$$

where

- E_{EX} = resistor excess noise in uV per frequency decade
- V_{DC} = DC voltage drop across the resistor (2)

Excess noise in carbon composition resistors corresponds to a large noise index of +10 dB to -20 dB. Carbon film resistors have a noise index of -10 dB to -25 dB. Metal film and wire wound resistors show the least amount of excess noise, with a noise index figure of -15 dB to -40 dB.

Other noise sources:

As the op amp and resistor noise sources are decreased, other noise contributors will now be noticeable. Small air currents across thermocouples will result in low frequency variations. Any two dissimilar metals, such as the lead on the IC and the solder and copper foil of the pc board, will form a thermocouple. The source itself may also generate noise. An example would be a resistive bridge. All resistive sources generate thermal noise based on the same equation listed above under "resistor types". (2)

Putting it all together

To a first approximation, the total input referred noise of an op amp is:

$$E_t^2 = e_n^2 + e_{req}^2 + (i_n * Req)^2$$

where

- Req is the equivalent source resistance at the inputs (3)

At low impedances, voltage noise dominates. At high impedances, current noise dominates. With a typical noise current on most CMOS input op amps of 0.01 pA/$\sqrt{Hz}$, the current noise contribution will be smaller than the voltage noise for Req less than one megohm.

Other Considerations

Comparator operation

Occasionally operational amplifiers are used as comparators. This is not optimum for the LMV751 for several reasons. First, the LMV751 is compensated for unity gain stability, so the speed will be less than could be obtained on the same process with a circuit specifically designed for comparator operation. Second, op amp output stages are designed to be linear, and will not necessarily meet the logic levels required under all conditions. Lastly, the LMV751 has the newer PNP-NPN common emitter output stage, characteristic of many rail-to-rail output op amps. This means that when used in open loop applications, such as comparators, with very light loads, the output PNP will saturate, with the output current being diverted into the previous stage. As a result, the supply current will increase to the 20-30 mA. range. When used as a comparator, a resistive load between 2kΩ and 10kΩ should be used with a small amount of hysteresis to alleviate this problem. When used as an op amp, the closed loop gain will drive the inverting input to within a few millivolts of the non-inverting input. This will automatically reduce the output drive as the output settles to the correct value; thus it is only when used as a comparator that the current will increase to the tens of milliampere range.

Rail-to-Rail

Because of the output stage discussed above, the LMV751 will swing “rail-to-rail” on the output. This normally means within a few hundred millivolts of each rail with a reasonable load. Referring to the Electrical Characteristics table for 2.7V to 5.0V, it can be seen that this is true for resistive loads of 2kΩ and 10kΩ. The input stage consists of cascoded P-channel MOSFETS, so the input common mode range includes ground, but typically requires 1.2V to 1.3V headroom from the positive rail. This is better than the industry standard LM324 and LM358 that have PNP input stages, and the LMV751 has the advantage of much lower input bias currents.

Loading

The LMV751 is a low noise, high speed op amp with excellent phase margin and stability. Capacitive loads up to 1000 pF can be handled, but larger capacitive loads should be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

General Circuits

With the low noise and low input bias current, the LMV751 would be useful in active filters, integrators, current to voltage converters, low frequency sine wave generators, and instrumentation amplifiers. (3)

NOTE

1. Sherwin, Jim "Noise Specs Confusing?" AN-104 (SNVA515), Texas Instruments.
2. Christensen, John, "Noise-figure curve ease the selection of low-noise op amps", EDN, pp 81-84, Aug. 4, 1994.
3. "Op Amp Circuit Collection", AN-31 (SNLA140), Texas Instruments.

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV751M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A32A	
LMV751M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A32A	Samples
LMV751M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A32A	
LMV751M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A32A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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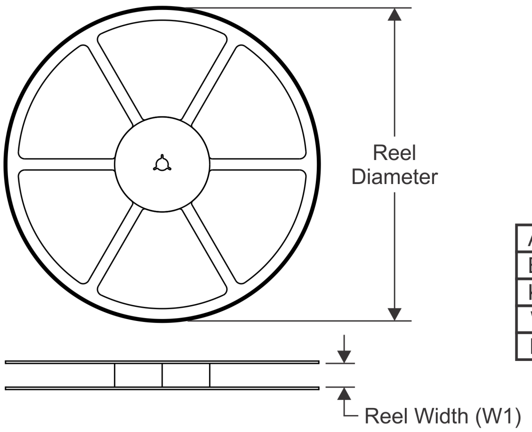
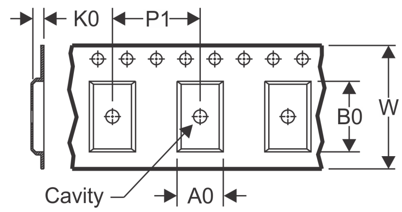
TAPE AND REEL INFORMATION

REEL DIMENSIONS

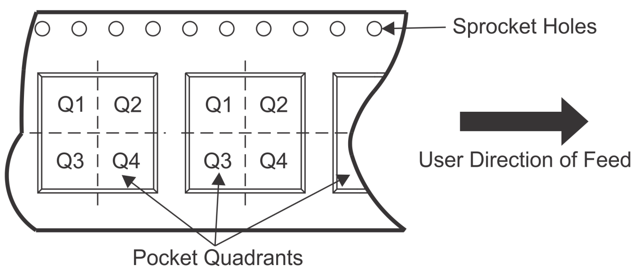


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

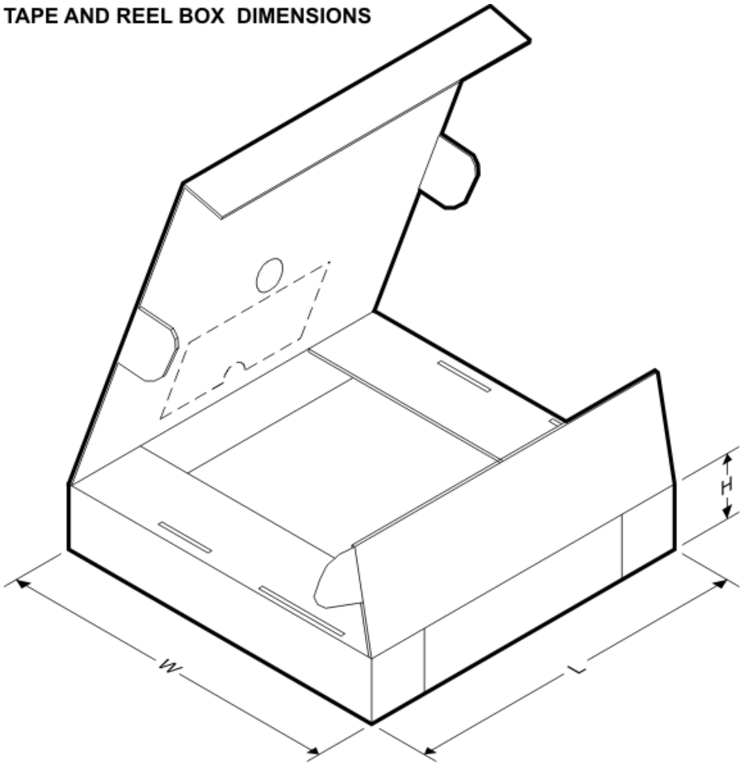
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV751M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV751M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV751M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV751M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

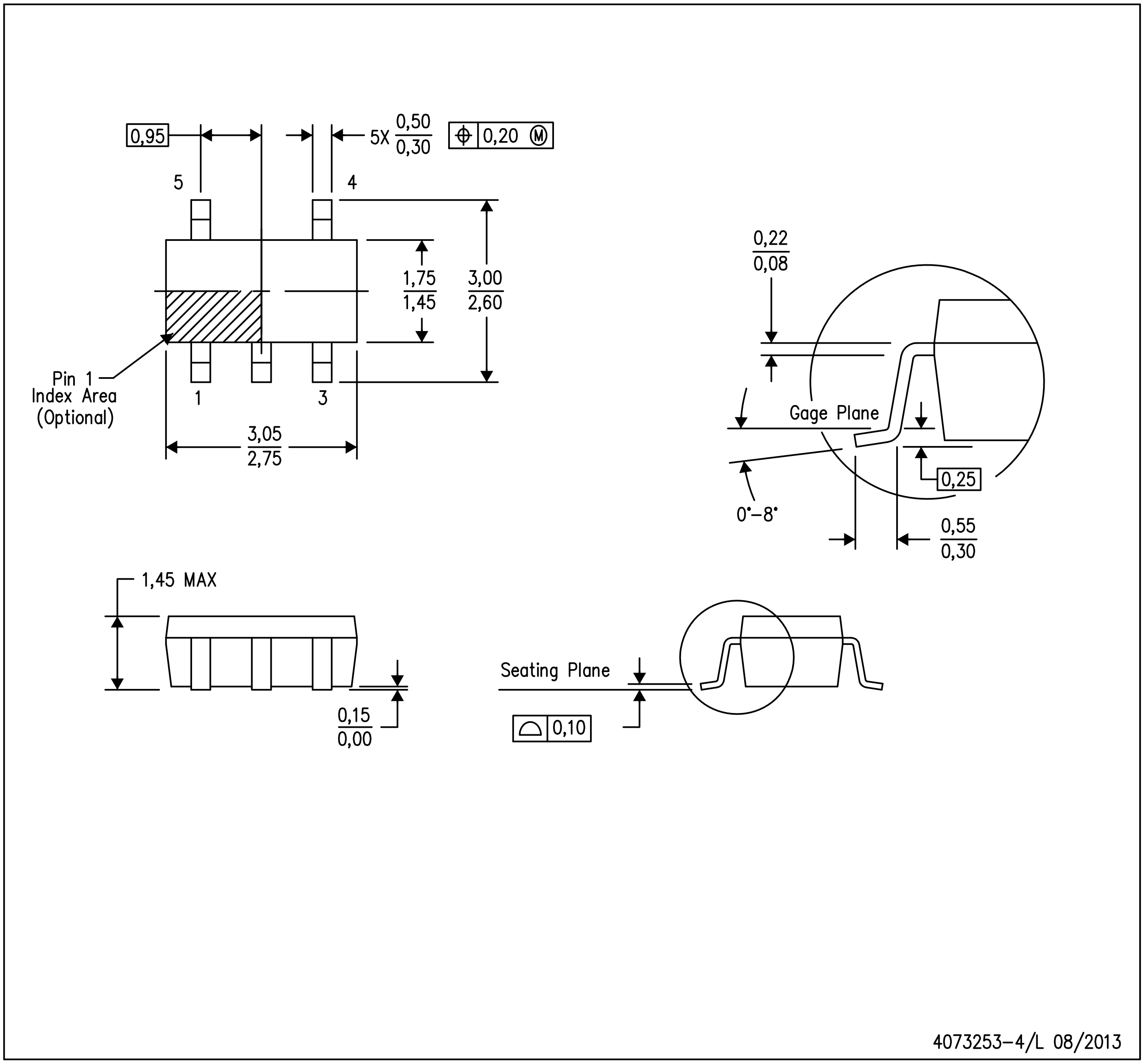
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

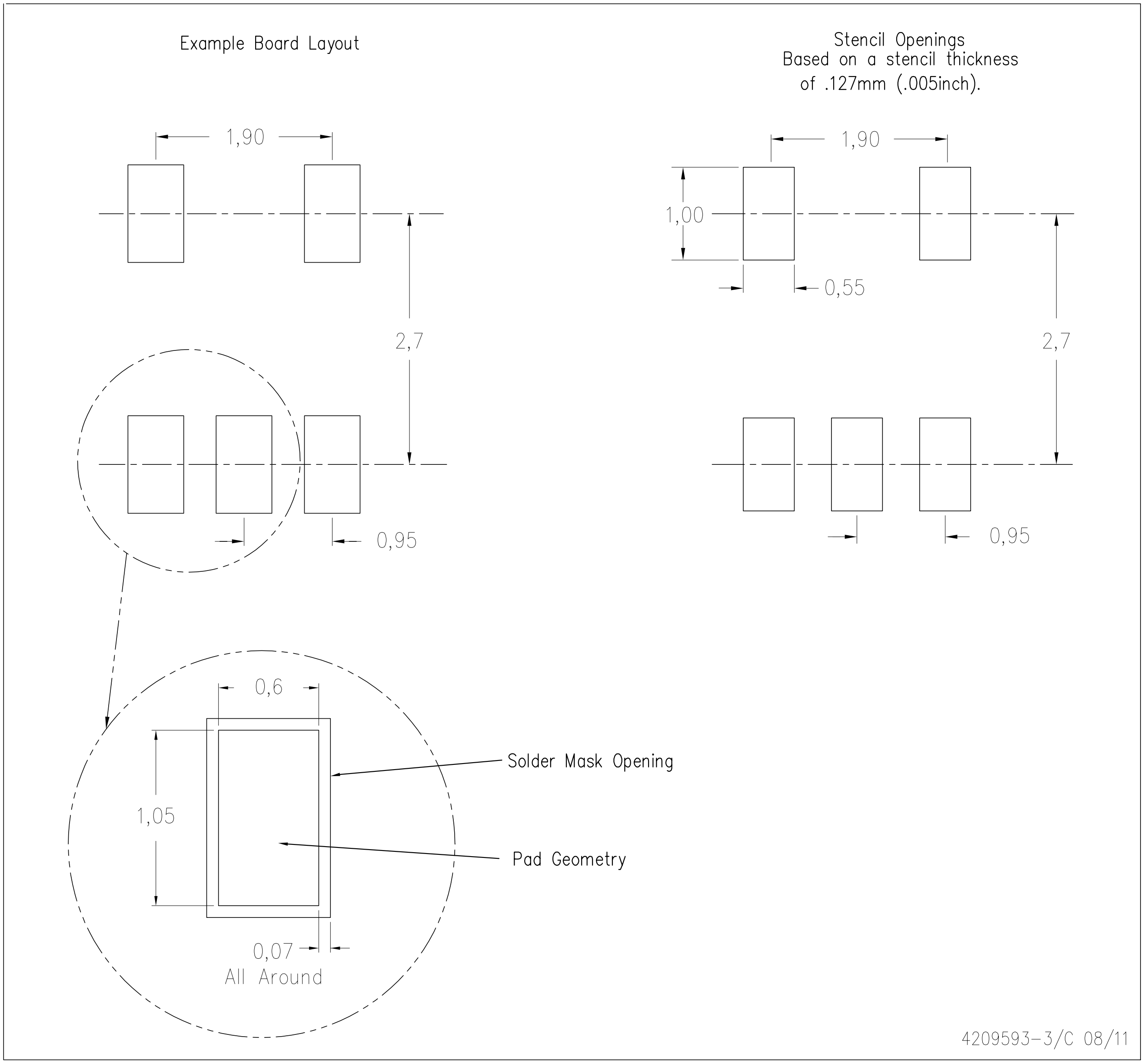
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV751M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV751M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV751M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV751M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.