July 2000



LMS8117 1A Low-Dropout Linear Regulator

General Description

The LMS8117 is a series of low dropout voltage regulators with a dropout of 1.2V at 1A of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LMS8117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in two fixed voltages, 1.8V and 3.3V.

The LMS8117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within $\pm 1\%$.

The LMS8117 series is available in SOT-223 and TO-252 D-PAK packages. A minimum of 10μ F tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 3.3V, and Adjustable Versions
- Space Saving SOT-223 and TO-252 Packages
- Current Limiting and Thermal Protection
- Output Current
- Temperature Range
- Line Regulation
- Load Regulation

Applications

- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

1A

0°C to 125°C

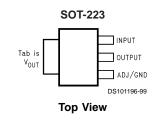
0.2% (Max)

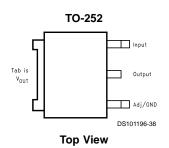
0.4% (Max)

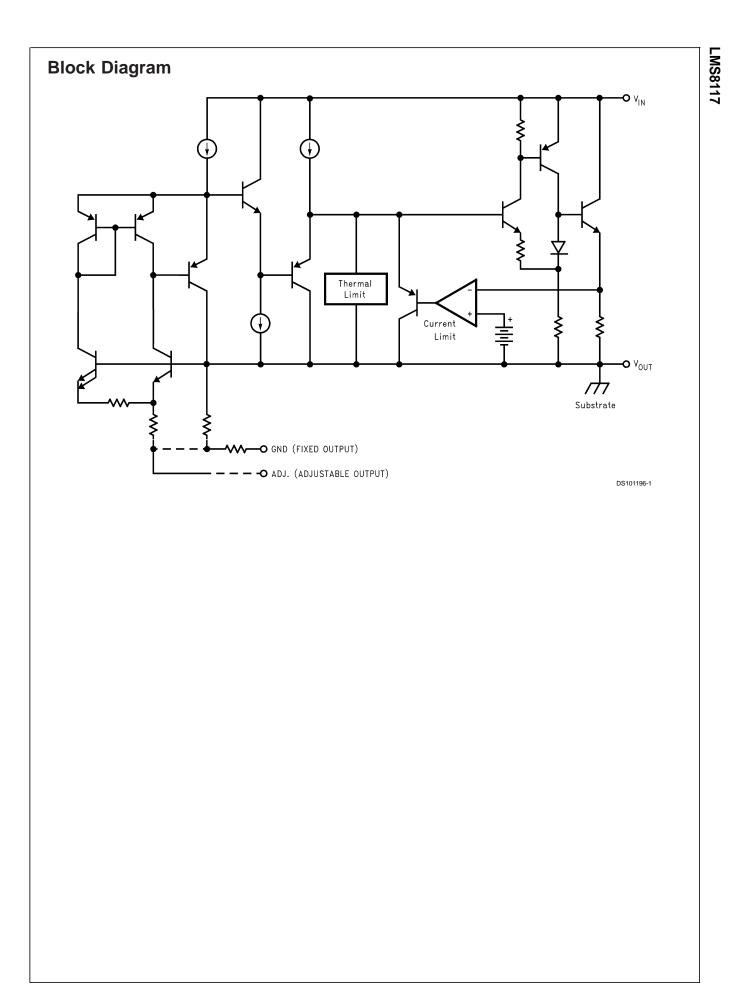
Ordering Information

Package	Temperature Range (T _J)	Packaging Marking	Transport Media	NSC Drawing	
	0°C to +125°C			Drawing	
3-lead	LMS8117AMP-ADJ	LS0A	1k Tape and Reel	MP04A	
SOT-223	LMS8117AMPX-ADJ	LS0A	2k Tape and Reel		
	LMS8117AMP-1.8	LS00	1k Tape and Reel		
	LMS8117AMPX-1.8	LS00	2k Tape and Reel		
	LMS8117AMP-3.3	LS01	1k Tape and Reel		
	LMS8117AMPX-3.3	LS01	2k Tape and Reel		
3-lead TO-252	LMS8117ADT-ADJ	LMS8117ADT-ADJ	Rails	TD03B	
	LMS8117ADTX-ADJ	LMS8117ADT-ADJ	2.5k Tape and Reel		
	LMS8117ADT-1.8	LMS8117ADT-1.8	Rails		
	LMS8117ADTX-1.8	LMS8117ADT-1.8	2.5k Tape and Reel		
	LMS8117ADT-3.3	LMS8117ADT-3.3	Rails		
	LMS8117ADTX-3.3	LMS8117ADT-3.3	2.5k Tape and Reel		

Connection Diagrams







Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Maximum Input Voltage (V _{IN} to GND)	
LMS8117-ADJ, LMS8117-1.8,	
LMS8117-3.3	20V
Power Dissipation (Note 2)	Internally Limited
Junction Temperature (T _J) (Note 2)	150°C
Storage Temperature Range	-65°C to 150°C

Soldering Information Infrared (20 sec) ESD Tolerance (Note 3)	235°C 2000V
Operating Ratings (Note 1)	
Input Voltage (V _{IN} to GND)	
LMS8117-ADJ, LMS8117-1.8,	
LMS8117-3.3	15V
Junction Temperature Range	0°C to 125°C

Electrical Characteristics

Typicals and limits appearing in normal type apply for $T_J = 25^{\circ}C$. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation, $0^{\circ}C$ to $125^{\circ}C$.

(T_J)(Note 2)

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Unit
V _{REF}	Reference Voltage	LMS8117-ADJ				
		$I_{OUT} = 10$ mA, V_{IN} - $V_{OUT} = 2V$, $T_J = 25$ °C	1.238	1.250	1.262	V
		$10mA \le I_{OUT} \le 1A, \ 1.4V \le V_{IN}-V_{OUT} \le$	1.225	1.250	1.270	V
		10V				
V _{OUT}	Output Voltage	LMS8117-1.8				
		$I_{OUT} = 10$ mA, $V_{IN} = 3.8$ V, $T_{J} = 25$ °C	1.782	1.800	1.818	V
		$0 \le I_{OUT} \le 1A, \ 3.2V \le V_{IN} \le 10V$	1.746	1.800	1.854	V
		LMS8117-3.3				
		$I_{OUT} = 10$ mA, $V_{IN} = 5$ V $T_{J} = 25$ °C	3.267	3.300	3.333	V
		$0 \le I_{OUT} \le 1A, 4.75V \le V_{IN} \le 10V$	3.235	3.300	3.365	V
ΔV_{OUT}	Line Regulation	LMS8117-ADJ				
	(Note 6)	I_{OUT} = 10mA, 1.5V \leq V _{IN} -V _{OUT} \leq 13.75V		0.035	0.2	%
		LMS8117-1.8		1	6	m∖
		I_{OUT} = 0mA, 3.2V $\leq V_{IN} \leq 10V$				
		LMS8117-3.3				
		$I_{OUT} = 0mA, \ 4.75V \le V_{IN} \le 15V$		1	6	m∖
ΔV _{OUT}	Load Regulation	LMS8117-ADJ				
	(Note 6)	V_{IN} - V_{OUT} = 3V, 10mA $\leq I_{OUT} \leq 1$ A		0.2	0.4	%
		LMS8117-1.8				
		V_{IN} = 3.2V, 0 $\leq I_{OUT} \leq 1A$		1	10	m∖
		LM1117-3.3				
		V_{IN} = 4.75V, $0 \le I_{OUT} \le 1A$		1	10	m∖
V _{IN} -V _{OUT}	Dropout Voltage (Note 7)	I _{OUT} = 100mA		1.1	1.15	V
		I _{OUT} = 500mA		1.15	1.2	V
		I _{OUT} = 1A		1.2	1.25	V
ILIMIT	Current Limit	$V_{IN}-V_{OUT} = 5V, T_J = 25^{\circ}C$	1.0	1.4	1.9	A
	Minimum Load	LMS8117-ADJ				
	Current (Note 8)	$V_{IN} = 15V$		1.7	5	mA
	Quiescent Current	LMS8117-1.8		5	10	mA
		$V_{IN} \le 15V$		Ŭ		110
		LMS8117-3.3				
		$V_{IN} \le 15V$		5	10	mA
	Thermal Regulation	$T_A = 25^{\circ}C$, 30ms Pulse		0.01	0.1	%/\
	Ripple Regulation	$f_{\text{RIPPLE}} = 120$ Hz, V_{IN} - $V_{\text{OUT}} = 3$ V	60	75		dB
		$V_{\text{RIPPLE}} = 12012$, $V_{\text{IN}} = 000$				uD
	Adjust Pin Current			60	120	μA
	Adjust Pin Current	$10\text{mA} \le I_{OUT} \le 1\text{A},$				
	Change	$1.4V \le V_{IN} - V_{OUT} \le 10V$		0.2	5	μA

Electrical Characteristics (Continued)

Typicals and limits appearing in normal type apply for $T_J = 25^{\circ}C$. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation, $0^{\circ}C$ to $125^{\circ}C$.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
	Temperature Stability			0.5		%
	Long Term Stability	T _A = 125°C, 1000Hrs		0.3		%
	RMS Output Noise	(% of V_{OUT}), 10Hz \leq f \leq 10kHz		0.003		%
	Thermal Resistance	3-Lead SOT-223		15.0		°C/W
	Junction-to-Case	3-Lead TO-252		10		°C/W
	Thermal Resistance	3-Lead SOT-223		136		°C/W
	Junction-to-Ambient	3-Lead TO-252 (Note 9)		92		°C/W
	(No heat sink;					
	No air flow)					

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 3: For testing purposes, ESD was applied using human body model, $1.5k\Omega$ in series with 100pF.

Note 4: Typical Values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: Load and line regulation are measured at constant junction room temperature.

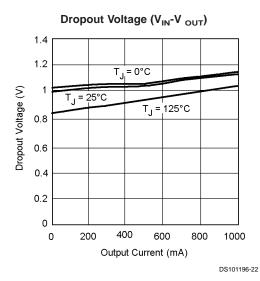
Note 7: The dropout voltage is the input/output differential at which the circuit ceases to regulate against further reduction in input voltage. It is measured when the output voltage has dropped 100mV from the nominal value obtained at $V_{IN} = V_{OUT} + 1.5V$.

Note 8: The minimum output current required to maintain regulation.

Note 9: Minimum pad size of $0.038in^2$

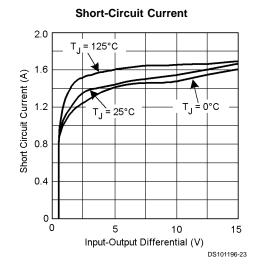


Typical Performance Characteristics

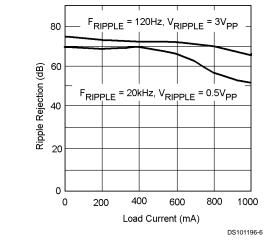


Load Regulation

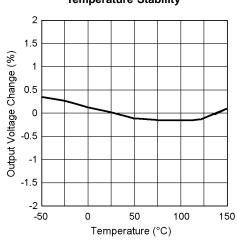
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LMS8117-ADJ Ripple Rejection vs. Current

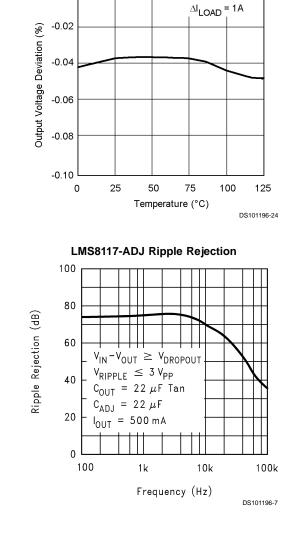




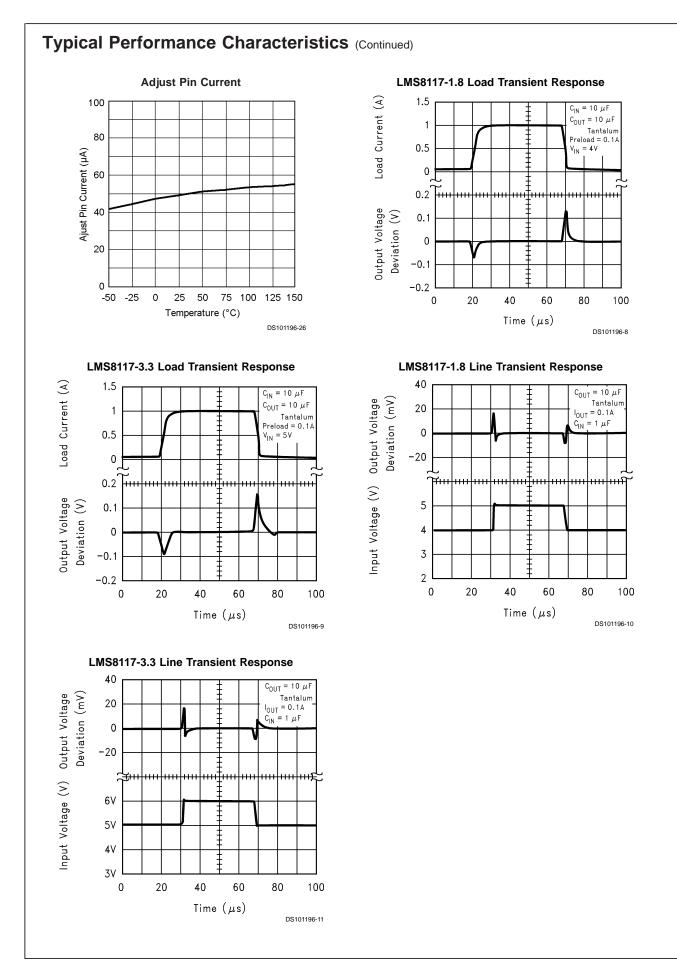












APPLICATION NOTE

1.0 External Capacitors/Stability

1.1 Input Bypass Capacitor

An input capacitor is recommended. A $10\mu F$ tantalum on the input is a suitable input bypassing for almost all applications.

1.2 Adjust Terminal Bypass Capacitor

The adjust terminal can be bypassed to ground with a bypass capacitor (C_{ADJ}) to improve ripple rejection. This bypass capacitor prevents ripple from being amplified as the output voltage is increased. At any ripple frequency, the impedance of the C_{ADJ} should be less than R1 to prevent the ripple from being amplified:

$(2\pi^* f_{RIPPLE}^* C_{ADJ}) < R1$

The R1 is the resistor between the output and the adjust pin. Its value is normally in the range of 100-200 Ω . For example, with R1=124 Ω and f_{RIPPLE}=120Hz, the C_{ADJ} should be > 11µF.

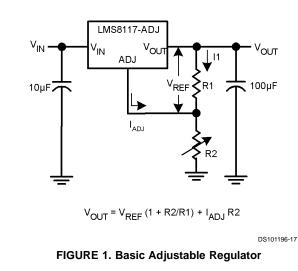
1.3 Output Capacitor

The output capacitor is critical in maintaining regulator stability, and must meet the required conditions for both minimum amount of capacitance and ESR (Equivalent Series Resistance). The minimum output capacitance required by the LMS8117 is 10µF, if a tantalum capacitor is used. Any increase of the output capacitance will merely improve the loop stability and transient response. The ESR of the output capacitor should be greater than 0.5 Ω and less than 5 Ω . In the case of the adjustable regulator, when the C_{ADJ} is used, a larger output capacitance (22µf tantalum) is required.

2.0 Output Voltage

The LMS8117 adjustable version develops a 1.25V reference voltage, V_{REF} , between the output and the adjust terminal. As shown in *Figure 1*, this voltage is applied across resistor R1 to generate a constant current I1. The current I_{ADJ} from the adjust terminal could introduce error to the output. But since it is very small (60µA) compared with the I1 and very constant with line and load changes, the error can be ignored. The constant current I1 then flows through the output set resistor R2 and sets the output voltage to the desired level.

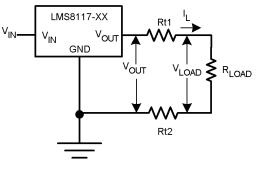
For fixed voltage devices, R1 and R2 are integrated inside the devices.



3.0 Load Regulation

The LMS8117 regulates the voltage that appears between its output and ground pins, or between its output and adjust pins. In some cases, line resistances can introduce errors to the voltage across the load. To obtain the best load regulation, a few precautions are needed.

Figure 2, shows a typical application using a fixed output regulator. The Rt1 and Rt2 are the line resistances. It is obvious that the V_{LOAD} is less than the V_{OUT} by the sum of the voltage drops along the line resistances. In this case, the load regulation seen at the R_{LOAD} would be degraded from the data sheet specification. To improve this, the load should be tied directly to the output terminal on the positive side and directly tied to the ground terminal on the negative side.



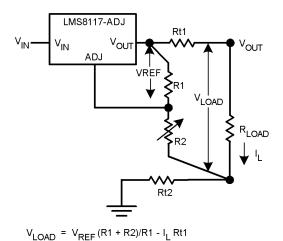
$$V_{LOAD} = V_{OUT} - I_{L} (Rt1 + Rt2)$$

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FIGURE 2. Typical Application using Fixed Output Regulator

When the adjustable regulator is used (*Figure 3*), the best performance is obtained with the positive side of the resistor R1 tied directly to the output terminal of the regulator rather than near the load. This eliminates line drops from appearing effectively in series with the reference and degrading regulation. For example, a 5V regulator with 0.05 Ω resistance between the regulator and load will have a load regulation due to line resistance of $0.05\Omega \times I_L$. If R1 (=125 Ω) is connected near the load, the effective line resistance will be $0.05\Omega (1+R2/R1)$ or in this case, it is 4 times worse. In addition, the ground side of the resistor R2 can be returned near the ground of the load to provide remote ground sensing and improve load regulation.

APPLICATION NOTE (Continued)



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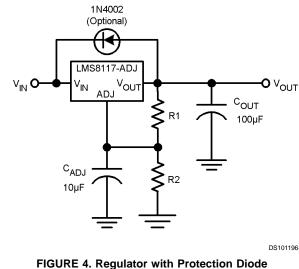
FIGURE 3. Best Load Regulation using Adjustable **Output Regulator**

4.0 Protection Diodes

Under normal operation, the LMS8117 regulators do not need any protection diode. With the adjustable device, the internal resistance between the adjust and output terminals limits the current. No diode is needed to divert the current around the regulator even with capacitor on the adjust terminal. The adjust pin can take a transient signal of ±25V with respect to the output voltage without damaging the device.

When a output capacitor is connected to a regulator and the input is shorted to ground, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage of the regulator, and rate of decrease of V_{IN}. In the LMS8117 regulators, the internal diode between the output and input pins can withstand microsecond surge currents of 10A to 20A. With an extremely large output capacitor ($\geq 1000 \ \mu F$), and with input instantaneously shorted to ground, the regulator could be damaged.

In this case, an external diode is recommended between the output and input pins to protect the regulator, as shown in Figure 4.



5.0 Heatsink Requirements

When an integrated circuit operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. A one-dimensional steady-state model of conduction heat transfer is demonstrated in Figure 5. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment. Below is a list of variables that may affect the thermal resistance and in turn the need for a heatsink.

R ^{θJC} (Component Vari- ables)	R ^{0CA} (Application Vari- ables)
Leadframe Size &	Mounting Pad Size,
Material	Material, & Location
No. of Conduction Pins	Placement of Mounting Pad
Die Size	PCB Size & Material
Die Attach Material	Traces Length & Width
Molding Compound Size and Material	Adjacent Heat Sources
	Volume of Air
	Ambient Temperatue
	Shape of Mounting Pad
Lead Fram Die Molded Package	$R^{0}LA = R^{0}JC + R^{0}CA$ $R^{0}JC$ $R^{0}JC$ $T_{A} = 25 \circ C$
Via	Board

Mounting Pad

FIGURE 5. Cross-sectional view of Integrated Circuit Mounted on a printed circuit board. Note that the case temperature is measured at the point where the leads contact with the mounting pad surface

The LMS8117 regulators have internal thermal shutdown to protect the device from over-heating. Under all possible operating conditions, the junction temperature of the LMS8117 must be within the range of 0°C to 125°C. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. To determine if a heatsink is needed, the power dissipated by the regulator, P_D , must be calculated:

$$I_{N} = I_{L} + I_{G}$$
$$P_{D} = (V_{IN} - V_{OUT})I_{L} + V_{IN}I_{G}$$

I

F

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LMS8117

APPLICATION NOTE (Continued)

Figure 6 shows the voltages and currents which are present in the circuit.

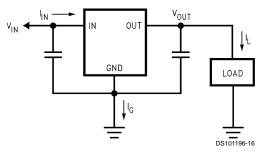


FIGURE 6. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(max)$:

 $T_{R}(max)=T_{J}(max)-T_{A}(max)$

where $T_J(max)$ is the maximum allowable junction temperature (125°C), and $T_A(max)$ is the maximum ambient temperature which will be encountered in the application.

Using the calculated values for $T_R(max)$ and P_D , the maximum allowable value for the junction-to-ambient thermal resistance (θ_{JA}) can be calculated:

 $\theta_{JA} = T_R(max)/P_D$

If the maximum allowable value for θ_{JA} is found to be $\geq 136^{\circ}C/W$ for SOT-223 package or $\geq 92^{\circ}C/W$ for TO-252 package, no heatsink is needed since the package alone will dissipate enough heat to satisfy these requirements. If the calculated value for θ_{JA} falls below these limits, a heatsink is required.

As a design aid, *Table 1* shows the value of the θ_{JA} of SOT-223 and TO-252 for different heatsink area. The copper patterns that we used to measure these θ_{JA} s are shown at the end of the Application Notes Section. *Figure 7* and *Figure 8* reflects the same test results as what are in the *Table 1*.

Figure 9 and *Figure 10* shows the maximum allowable power dissipation vs. ambient temperature for the SOT-223 and TO-252 device. *Figure 11* and *Figure 12* shows the maximum allowable power dissipation vs. copper area (in²) for the SOT-223 and TO-252 devices. Please see AN1028 for power enhancement techniques to be used with SOT-223 and TO-252 packages.

Layout	Copper Area		Thermal Resistance		
	Top Side (in ²)*	Bottom Side (in ²)	(θ _{JA} , °C/W) SOT-223	(θ _{JA} , °C/W) TO-252	
1	0.0123	0	136	103	
2	0.066	0	123	87	
3	0.3	0	84	60	
4	0.53	0	75	54	
5	0.76	0	69	52	
6	1	0	66	47	
7	0	0.2	115	84	
8	0	0.4	98	70	
9	0	0.6	89	63	
10	0	0.8	82	57	
11	0	1	79	57	
12	0.066	0.066	125	89	
13	0.175	0.175	93	72	
14	0.284	0.284	83	61	
15	0.392	0.392	75	55	
16	0.5	0.5	70	53	

TABLE 1. θ_{JA} Different Heatsink Area

*Tab of device attached to topside copper

APPLICATION NOTE (Continued)

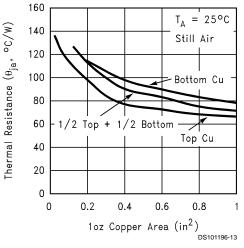


FIGURE 7. θ_{JA} vs. 1oz Copper Area for SOT-223

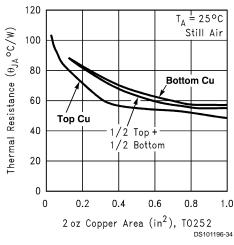
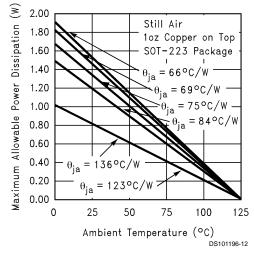
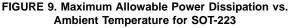


FIGURE 8. θ_{JA} vs. 2oz Copper Area for TO-252





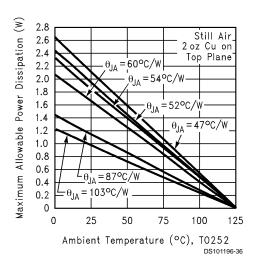
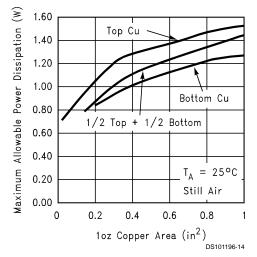
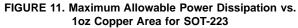


FIGURE 10. Maximum Allowable Power Dissipation vs. Ambient Temperature for TO-252





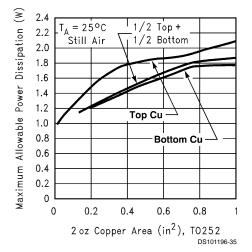
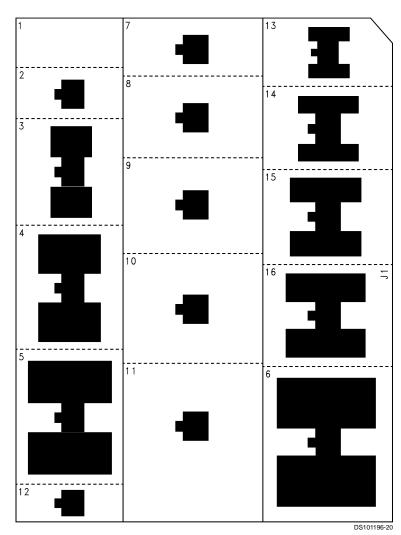


FIGURE 12. Maximum Allowable Power Dissipation vs. 2oz Copper Area for TO-252

LMS8117

APPLICATION NOTE (Continued)





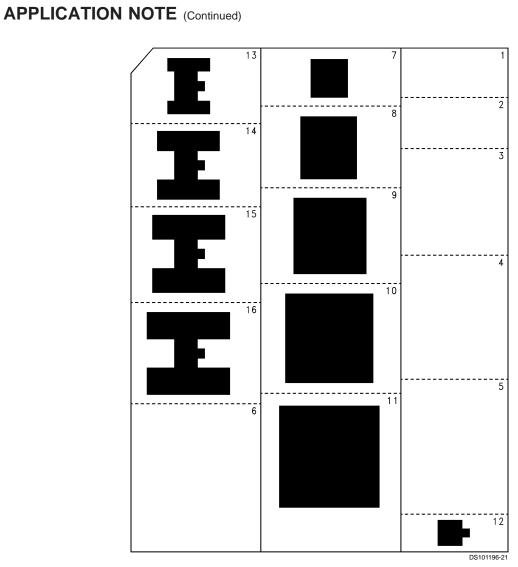
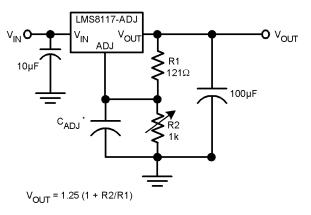


FIGURE 14. Bottom View of the Thermal Test Pattern in Actual Scale

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LMS8117

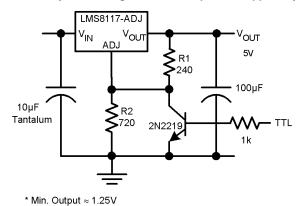
Typical Application Circuits



* ${\rm C}_{\rm ADJ}$ is optionall, however it will improve ripple rejection

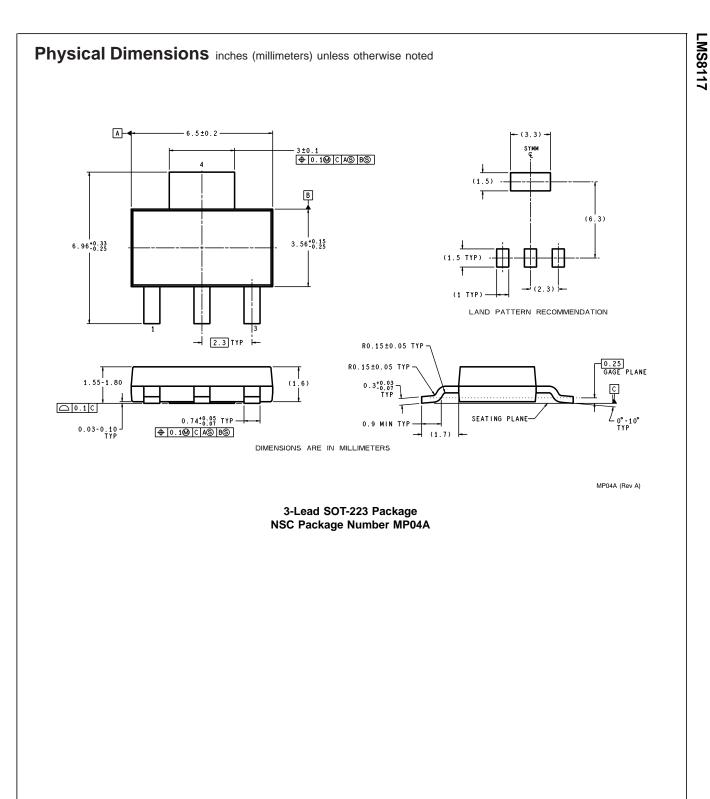
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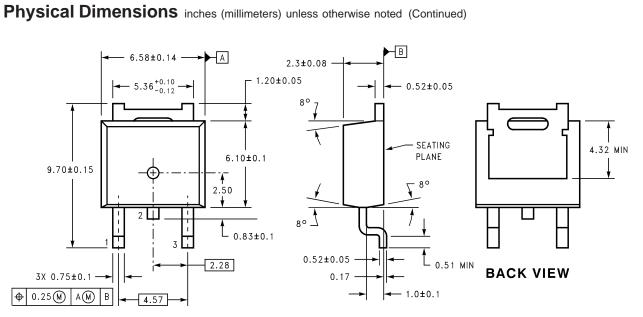




DS101196-27

5V Logic Regulator with Electronic Shutdown*





DIMENSIONS ARE IN MILLIMETERS 3-Lead TO-252 Package NSC Package Number TD03B

TD03B (REV A)

LIFE SUPPORT POLICY

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- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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