LMK00804B-Q1 1.5-V to 3.3-V, 1-to-4 High-Performance LVCMOS Fan-Out Buffer and Level Translator

1 Features

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C, T_A
- Four LVCMOS/LVTTL outputs supporting 1.5-V to 3.3-V levels
  - Additive jitter: 0.1-ps RMS (typical) at 40 MHz
  - Noise floor: –168 dBc/Hz (typical) at 40 MHz
  - Output frequency: 350 MHz (maximum)
  - Output skew: 35 ps (maximum)
  - Part-to-part skew: 700 ps (maximum)
- Two selectable inputs
  - CLK_P, CLK_N pair accepts LVPECL, LVDS, HCSL, SSTL, LVHSTL, or LVCMOS/LVTTL
  - LVCMOS_CLK accepts LVCMOS/LVTTL
- Synchronous clock enable
- Core/output power supplies:
  - 3.3 V/3.3 V
  - 3.3 V/2.5 V
  - 3.3 V/1.8 V
  - 3.3 V/1.5 V
- Package: 16-pin VQFN

2 Applications

- Advanced Driver Assistance Systems (ADAS)
  - Front long range radar
  - Medium/short range radar
  - Ultra short range radar

3 Description

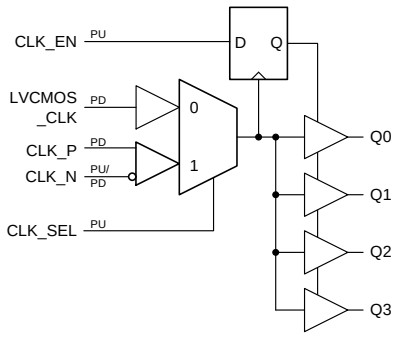
The LMK00804B-Q1 is a high-performance clock fan-out buffer and level translator that can distribute up to four LVCMOS/LVTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels) from one of two selectable inputs that can accept differential or single-ended inputs. The clock enable input is synchronized internally to eliminate runt or glitch pulses on the outputs when the clock enable terminal is asserted or deasserted. The outputs are held in logic low state when the clock is disabled. The LMK00804B-Q1 can also distrbute a low-jitter clock across four transceivers and can improve the overall target detection and resolution in a cascaded mmWave radar system.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMK00804B-Q1	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



(1) PU = 51-kΩ pullup, PD = 51-kΩ pulldown. See Figure 11.

Table of Contents

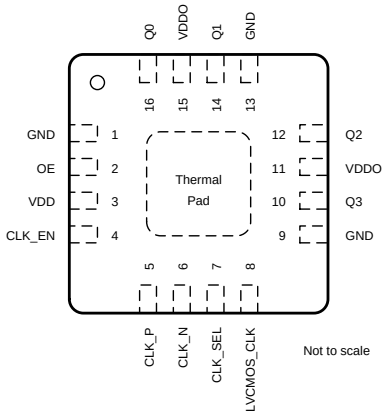
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2019) to Revision A	Page
• Changed data sheet status from Advanced Information to Production Data	1

5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions[1]

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
CLK_EN	4	I, PU	Synchronous clock enable input. Typically connected to VDD with a 1-kΩ pullup. When unused, leave floating. 0 = Outputs are forced to logic low state 1 = Outputs are enabled with LVCMOS/LVTTL levels
CLK_N	6	I, PD, PU	Inverting differential clock input 0. Typically connected to the inverting clock input. When unused, leave floating. Internally biased to V_{DD}/2 when left floating.
CLK_P	5	I, PD	Noninverting differential clock input 0. Typically connected to the noninverting clock input. A single-ended clock input can also be connected to CLK_P. When unused, leave floating.
CLK_SEL	7	I, PU	Clock select input. Typically connected to VDD with a 1-kΩ pullup. When unused, leave floating. 0 = Select LVCMOS_CLK (pin 8) 1 = Select CLK_P, CLK_N (pins 5, 6)
GND	1, 9, 13	G	Power supply ground.
LVCMOS_CLK	8	I, PD	Single-ended clock input. Typically connected to a single-ended clock input. When unused, leave floating. Accepts LVCMOS/LVTTL levels.
NC	2	NC	No connect pin. Typically left floating. Do not connect to ground.
Q0	16	O	Single-ended clock outputs with LVCMOS/LVTTL levels, 7-Ω output impedance. Typically connected to a receiver with a 43-Ω series termination. When unused, leave floating.
Q1	14		
Q2	12		
Q3	10		
VDD	3	P	Power supply terminal. Typically connected to a 3.3-V supply.
VDDO	11, 15	P	Output supply terminals. Typically connected to a 3.3-V, 2.5-V, 1.8-V, or 1.5-V supply.

(1) See *Recommendations for Unused Input and Output Pins*, if applicable.
(2) The definitions below define the functionality of the I/O cells for each pin.
TYPE:
(a) G = Ground,
(b) I = Input,
(c) O = Output,
(d) P = Power,
(e) PU = 51-kΩ pullup,
(f) PD = 51-kΩ pulldown.
(g) NC = No connect

6 Specifications

6.1 Absolute Maximum Ratings (1) (2)

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Supply input voltage	–0.5	3.6	V
V_{DDO}	Supply output voltage	–0.5	3.6	V
V_I	Input voltage (3)	–0.3	V_{DD} + 0.5	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) This value is limited to 4.6 V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C3	±250	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply input voltage	3.135	3.3	3.465	V
V_{DDO}	Supply output voltage	3.135	3.3	3.465	V
		2.375	2.5	2.625	
		1.71	1.8	1.89	
		1.425	1.5	1.575	
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		135	°C
f_{OUT}	Maximum output frequency (1)			350	MHz

(1) There is no minimum input / output frequency provided the input slew rate is sufficiently fast. Refer to *Input Slew Rate Considerations*.

6.4 Thermal Information

THERMAL METRIC[1][2]		LMK00804B-Q1 RGT (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-K board).

6.5 Power Supply Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current through VDD			21	mA
I_{DDO}	Power supply current through VDDO			5	mA

6.6 LVCMOS / LVTTL DC Electrical Characteristics

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage	CLK_EN, CLK_SEL		2		V_{DD} + 0.3	V
		LVCMOS_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input low voltage	CLK_EN, CLK_SEL		–0.3		0.8	V
		LVCMOS_CLK		–0.3		1.3	
I_{IH}	Input high current	CLK_EN, CLK_SEL	$V_{IH} = V_{DD}$			15	µA
		LVCMOS_CLK	V_{DD} = 3.465 V, V_{IN} = 3.465 V			150	
I_{IL}	Input low current	CLK_EN, CLK_SEL	V_{IL} = GND	–150			µA
		LVCMOS_CLK	V_{DD} = 3.465 V, V_{IN} = 0 V	–150			
V_{OH}	Output high voltage[1]	V_{DDO} = 3.3 V ± 5%		2.64			V
		V_{DDO} = 2.5 V ± 5%		2			
		V_{DDO} = 1.8 V ± 5%		1.44			
		V_{DDO} = 1.5 V ± 5%		1.2			
V_{OL}	Output low voltage[1]	V_{DDO} = 3.3 V ± 5%				0.66	V
		V_{DDO} = 2.5 V ± 5%				0.5	
		V_{DDO} = 1.8 V ± 5%				0.36	
		V_{DDO} = 1.5 V ± 5%				0.3	
I_{OZL}	Output Hi-Z current low			–5			µA
I_{OZH}	Output Hi-Z current high					5	

(1) Outputs terminated with 50 Ω to V_{DDO}/2.

6.7 Differential Input DC Electrical Characteristics

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ID}	Differential input voltage swing, (V_{IH} – V_{IL})(1)			0.15		1.4	V
V_{IC}	Input common-mode voltage(1)(2)			0.5		V_{DD} – 0.85	V
I_{IH}	Input high current(3)	CLK_N	V_{DD} = 3.465 V, V_{IN} = 3.465 V			150	µA
		CLK_P	V_{DD} = 3.465 V, V_{IN} = 3.465 V			150	
I_{IL}	Input low current(3)	CLK_N	V_{DD} = 3.465 V , V_{IN} = 0 V	–150			µA
		CLK_P	V_{DD} = 3.465 V, V_{IN} = 0 V	–150			

(1) V_{IL} should not be less than –0.3 V.
(2) Input common-mode voltage is defined as V_{IH}.
(3) For I_{IH} and I_{IL} measurements on CLK_Por CLK_N, one must comply with V_{ID} and V_{IC} specifications by using the appropriate bias on CLK_N or CLK.

6.8 Timing Characteristics (V_{DDO} = 3.3 V ± 5%)

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PDLH}	Propagation delay, Low-to-high	LVCMOS_CLK(1), CLK_P/CLK_N(2)	–40°C to 125°C	1		2.5	ns
			–40°C to 125°C	1		2.5	ns
$t_{SK(O)}$	Output skew(3)(4)	Measured on rising edge				35	ps
$t_{SK(PP)}$	Part-to-part skew(4)(5)					550	ps
t_R/t_F	Output rise/fall time	20% to 80%, C_L= 5 pF		100	310	600	ps
t_{JIT}	Additive jitter(6)	f = 40 MHz, Input slew rate = 1.25 V/ns, 12-kHz to 20-MHz integration band			115	200	fs RMS

(1) Measured from the V_{DD}/2 of the input to the V_{DDO}/2 of the output.
(2) Measured from the differential input crossing point to V_{DDO}/2 of the output.
(3) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at V_{DDO}/2 of the output.
(4) Parameter is defined in accordance with JEDEC Standard 65.
(5) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, various supply voltages, operating at the same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(6) Buffer additive jitter: t_{JIT} = SQRT($t_{JIT\_SYS}^2$ – $t_{JIT\_SOURCE}^2$), where t_{JIT_SYS} is the RMS jitter of the system output (source+buffer) and t_{JIT_SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality, ultra-low-noise oscillators. Refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.

Timing Characteristics (V_{DDO} = 3.3 V ± 5%) (continued)

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN_{FLOOR}	Phase noise floor(7)	f = 40 MHz, Input slew rate = 1.25 V/ns				dBc/Hz
		10-kHz offset		–151		
		100-kHz offset		–160		
		1-MHz offset		–162		
		10-MHz offset		–162		
		20-MHz offset		–162		
D_O	Output duty cycle	REF = CLK_P/CLK_N, 50% input duty cycle, f < 166 MHz	45%		55%	
		REF = LVCMOS_CLK, 50% input duty cycle, f > 166 MHz	42%		58%	
t_{DIS}	Output disable time			5		ns

(7) Buffer phase noise floor: PN_{FLOOR} (dBc/Hz) = 10 × log10[10^(PN_{SYSTEM}/10) – 10^(PN_{SOURCE}/10)], where PN_{SYSTEM} is the phase noise floor of the system output (source+buffer) and PN_{SOURCE} is the phase noise floor of the input source. Buffer Phase Noise Floor should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality, ultra-low-noise oscillators. Refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.

6.9 Timing Characteristics (V_{DDO} = 2.5 V ± 5%)

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PDLH}	Propagation delay, Low-to-high	LVCMOS_CLK(1), CLK_P/CLK_N	–40°C to 125°C	1		2.5	ns
			–40°C to 125°C	1		2.5	
$t_{SK(O)}$	Output skew(2)(3)	Measured on rising edge				35	ps
$t_{SK(PP)}$	Part-to-part skew(3)(4)					550	ps
t_R/t_F	Output rise/fall time	20% to 80%, C_L= 5 pF		100	310	600	ps
t_{JIT}	Additive jitter(5)	f = 40 MHz, Input slew rate = 1.25 V/ns, 12-kHz to 20-MHz integration band			115	200	ps RMS
D_O	Output duty cycle	REF = CLK_P/CLK_N, 50% input duty cycle, f < 166 MHz		45%		55%	
		REF = LVCMOS_CLK, 50% input duty cycle, f > 166 MHz		42%		58%	
t_{DIS}	Output disable time				5		ns

(1) Measured from the V_{DD}/2 of the input to the V_{DDO}/2 of the output.
(2) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at V_{DDO}/2 of the output.
(3) Parameter is defined in accordance with JEDEC Standard 65.
(4) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, various supply voltages, operating at the same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(5) Buffer additive jitter: t_{JIT} = SQRT($t_{JIT\_SYS}^2$ – $t_{JIT\_SOURCE}^2$), where J_{SYS} is the RMS jitter of the system output (source+buffer) and t_{JIT_SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality, ultra-low-noise oscillators. Refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.

6.10 Timing Characteristics (V_{DDO} = 1.8 V ± 5%)

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PDLH}	Propagation delay, Low-to-high	LVCMOS_CLK(1), CLK_P/CLK_N	–40°C to 125°C	1		2.5	ns
			–40°C to 125°C	1		2.5	ns

(1) Measured from the V_{DD}/2 of the input to the V_{DDO}/2 of the output.

Timing Characteristics (V_{DDO} = 1.8 V ± 5%) (continued)

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SK(O)}$	Output skew(2)(3)	Measured on rising edge			35	ps
$t_{SK(PP)}$	Part-to-part skew(3)(4)				550	ps
t_R/t_F	Output rise/fall time	20% to 80%, C_L= 5 pF	100	310	600	ps
t_{JIT}	Additive jitter(5)	f = 40 MHz, Input slew rate = 1.25 V/ns, 12-kHz to 20-MHz integration band		115	200	ps RMS
D_O	Output duty cycle	REF = CLK_P/CLK_N, 50% input duty cycle, f < 166 MHz	45%		55%	
		REF = LVCMOS_CLK, 50% input duty cycle, f > 166 MHz	42%		58%	
t_{DIS}	Output disable time			5		ns

(2) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at V_{DDO}/2 of the output.
(3) Parameter is defined in accordance with JEDEC Standard 65.
(4) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, various supply voltages, operating at the same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(5) Buffer additive jitter: $t_{JIT} = SQRT(t_{JIT\_SYS}^2 - t_{JIT\_SOURCE}^2)$, where J_{SYS} is the RMS jitter of the system output (source+buffer) and t_{JIT_SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality, ultra-low-noise oscillators. Refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.

6.11 Timing Characteristics (V_{DDO} = 1.5 V ± 5%)

V_{DD} = 3.135 V to 3.465 V, V_{DDO} = 1.425 V to 1.575 V, 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V and T_A = –40°C to 125°C

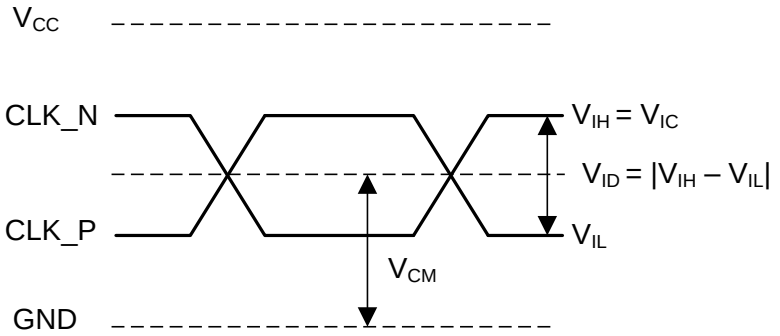
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PDLH}	Propagation delay, Low-to-high	LVCMOS_CLK(1), CLK_P/CLK_N	–40°C to 125°C	1		2.5	ns
			–40°C to 125°C	1		2.5	ns
$t_{SK(O)}$	Output skew(2)(3)	Measured on rising edge				35	ps
$t_{SK(PP)}$	Part-to-part skew(3)(4)					550	ns
t_R/t_F	Output rise/fall time	20% to 80%, C_L= 5 pF		100	310	600	ps
t_{JIT}	Additive Jitter(5)	f = 40 MHz, Input slew rate = 1.25 V/ns, 12-kHz to 20-MHz integration band			115	200	ps RMS
D_O	Output duty cycle	REF = CLK_P/CLK_N, 50% input duty cycle, f < 166 MHz		45%		55%	
t_{DIS}	Output disable time				5		ns

(1) Measured from the V_{DD}/2 of the input to the V_{DDO}/2 of the output.
(2) Defined as skew between outputs at the same supply voltage and with equal loading conditions. Measured at V_{DDO}/2 of the output.
(3) Parameter is defined in accordance with JEDEC Standard 65.
(4) Calculation for part-to-part skew is the difference between the fastest and slowest t_{PD} across multiple devices, various supply voltages, operating at the same frequency, same temperature, with equal load conditions, and using the same type of inputs on each device.
(5) Buffer additive jitter: $t_{JIT} = SQRT(t_{JIT\_SYS}^2 - t_{JIT\_SOURCE}^2)$, where t_{JIT_SYS} is the RMS jitter of the system output (source+buffer) and t_{JIT_SOURCE} is the RMS jitter of the input source, and system output noise is not correlated to the input source noise. Additive jitter should be considered only when the input source noise floor is 3 dB or better than the buffer noise floor (PN_{FLOOR}). This is usually the case for high-quality, ultra-low-noise oscillators. Refer to *System-Level Phase Noise and Additive Jitter Measurement* for input source and measurement details.

6.12 Pin Characteristics

		MIN	TYP	MAX	UNIT
C_I	Input capacitance		1		pF
R_{PU}	Input pullup resistance		51		kΩ
R_{PD}	Input pulldown resistance		51		kΩ
C_{PD}	Power dissipation capacitance (per output)		2		pF
R_{OUT}	Output impedance		7		Ω

7 Parameter Measurement Information



NOTE: $V_{CM} = V_{IC} – V_{ID}/2 = (V_{IH} + V_{IL})/2$

Figure 1. Differential Input Level

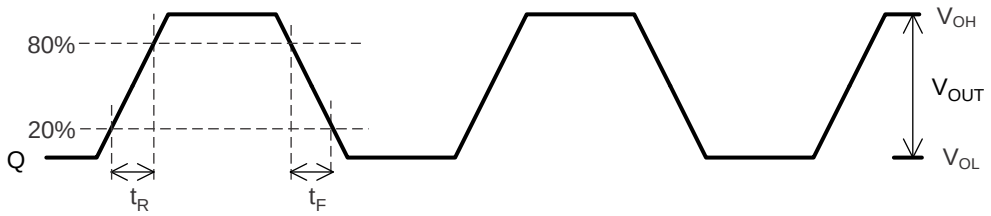


Figure 2. Output Voltage, and Rise and Fall Times

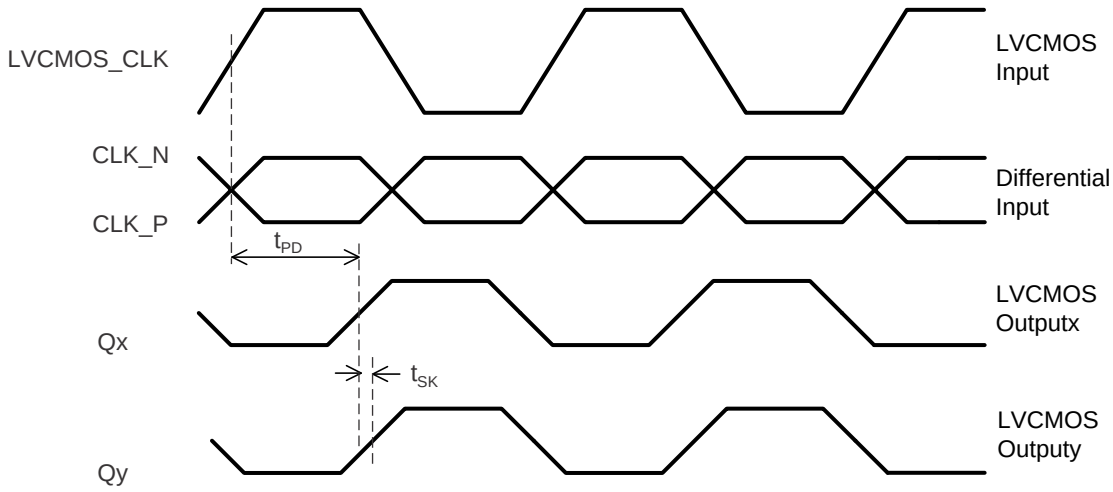


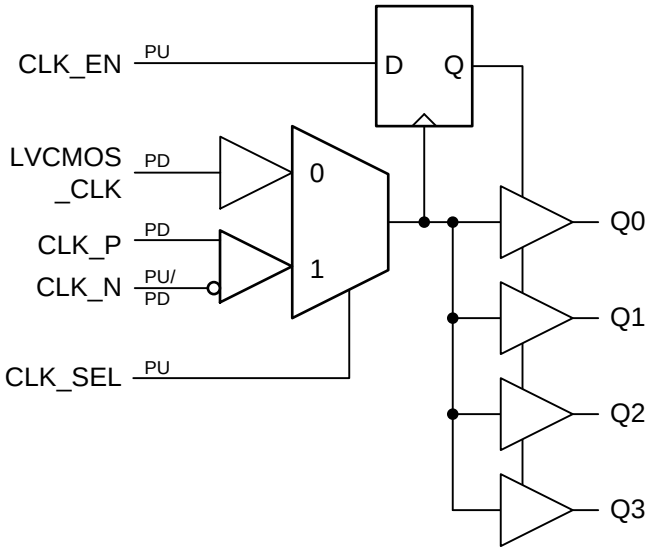
Figure 3. Output Skew and Propagation Delay

8 Detailed Description

8.1 Overview

The LMK00804B-Q1 is a clock fan-out buffer with two selectable clock inputs and four LVCMOS outputs. The LVCMOS_CLK input accepts a single-ended clock input, and the CLK_P/CLK_N input accepts a differential or single-ended clock input. The LMK00804B-Q1 has a synchronous clock enable feature allows the device to drive the outputs to a logic low using the CLK_EN pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Clock Enable Timing

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 4.

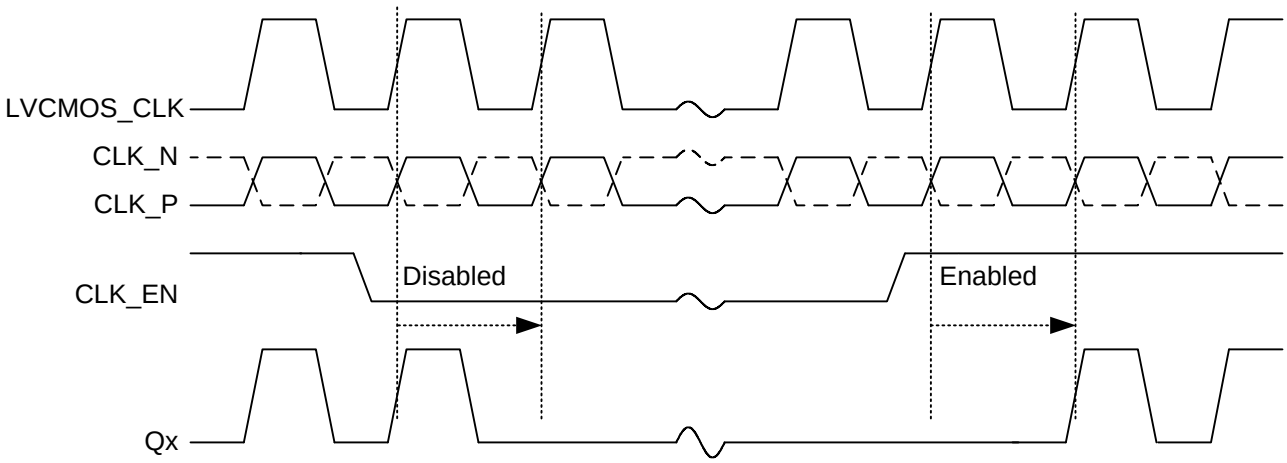


Figure 4. Clock Enable Timing Diagram

8.4 Device Functional Modes

The device can provide fan-out and level translation from a differential or single-ended input to a LVCMOS/LVTTL output where the output V_{OH} and V_{OL} levels are applied to the V_{DDO} pin and output load condition.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMK00804B-Q1 enables the distribution of up to four LVCMOS copies of a low-noise source designed for general-purpose and high-performance applications. For best jitter performance, TI recommends to use the appropriate matching networks for the clock driver and receiver format, as detailed in the *Typical Applications* section. Practice good high-speed layout design outlined in the *High-speed Layout Guidelines* application report (SCAA082).

The LMK00804B-Q1 is designed to drive 50-Ω controlled-impedance traces. TI recommends to design these clock traces as 50-Ω, single-ended controlled impedance traces. Use a series 43-Ω resistor at the clock outputs Q[3:0] to match the driver impedance and series resistance to the trace impedance.

9.2 Typical Applications

Refer to the following sections for output clock and input clock interface circuits.

9.2.1 Output Clock Interface Circuit

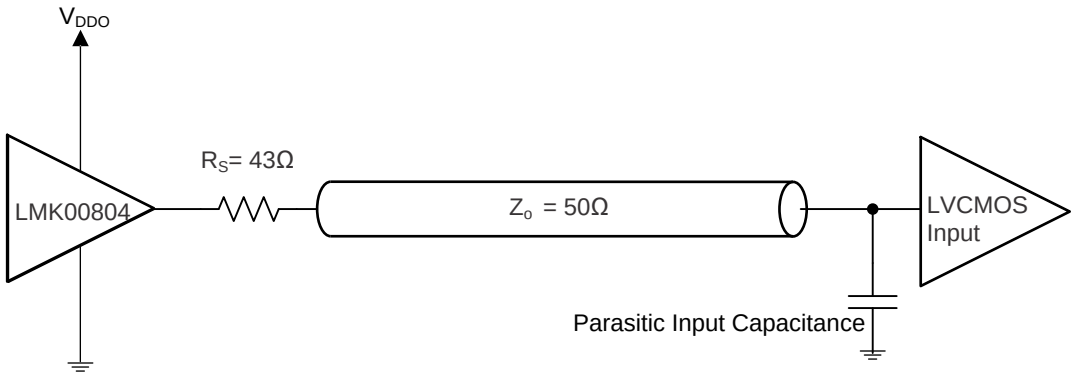


Figure 5. LVCMOS Output Configuration

9.2.1.1 Design Requirements

For high-performance devices, limitations of the equipment can affect phase-noise measurements. The noise floor of the equipment is often higher than the noise floor of the device. The real noise floor of the device is probably lower. It is important to understand that system-level phase noise measured at the DUT output is influenced by the input source and the measurement equipment.

For Figure 6 and system-level phase noise plots, a Rohde & Schwarz SMA100A low-noise signal generator was cascaded with an Agilent 70429A K95 single-ended-to-differential converter block with ultra-low phase noise and fast-edge slew rate (>3 V/ns) to provide a low-noise clock input source to the LMK00804B-Q1. An Agilent E5052 source signal analyzer with an ultra-low measurement noise floor was used to measure the phase noise of the input source (SMA100A + 70429A K95) and system output (input source + LMK00804B-Q1). The light blue trace shows the input source phase noise, and the dark blue trace in Figure 6 shows the system output phase noise.

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

Use Equation 1 to calculate the additive phase noise or noise floor of the buffer (PN_{FLOOR}):

$$PN_{FLOOR}\ (dBc/Hz) = 10 \times \log_{10}[10\text{^}(PN_{SYSTEM}/10) - 10\text{^}(PN_{SOURCE}/10)] \quad (1)$$

where

- PN_{SYSTEM} is the phase noise of the system output (source+buffer)
- PN_{SOURCE} is the phase noise of the input source

Use Equation 2 to calculate the additive jitter of the buffer (t_{JIT}):

$$t_{JIT} = SQRT(t_{JIT\_SYS}^2 - t_{JIT\_SOURCE}^2) \quad (2)$$

where:

- t_{JIT_SYS} is the RMS jitter of the system output (source+buffer), integrated from 10 kHz to 20 MHz
- t_{JIT_SOURCE} is the RMS jitter of the input source, integrated from 10 kHz to 20 MHz

Typical Applications (continued)

9.2.1.3 Application Curve

9.2.1.3.1 System-Level Phase Noise and Additive Jitter Measurement

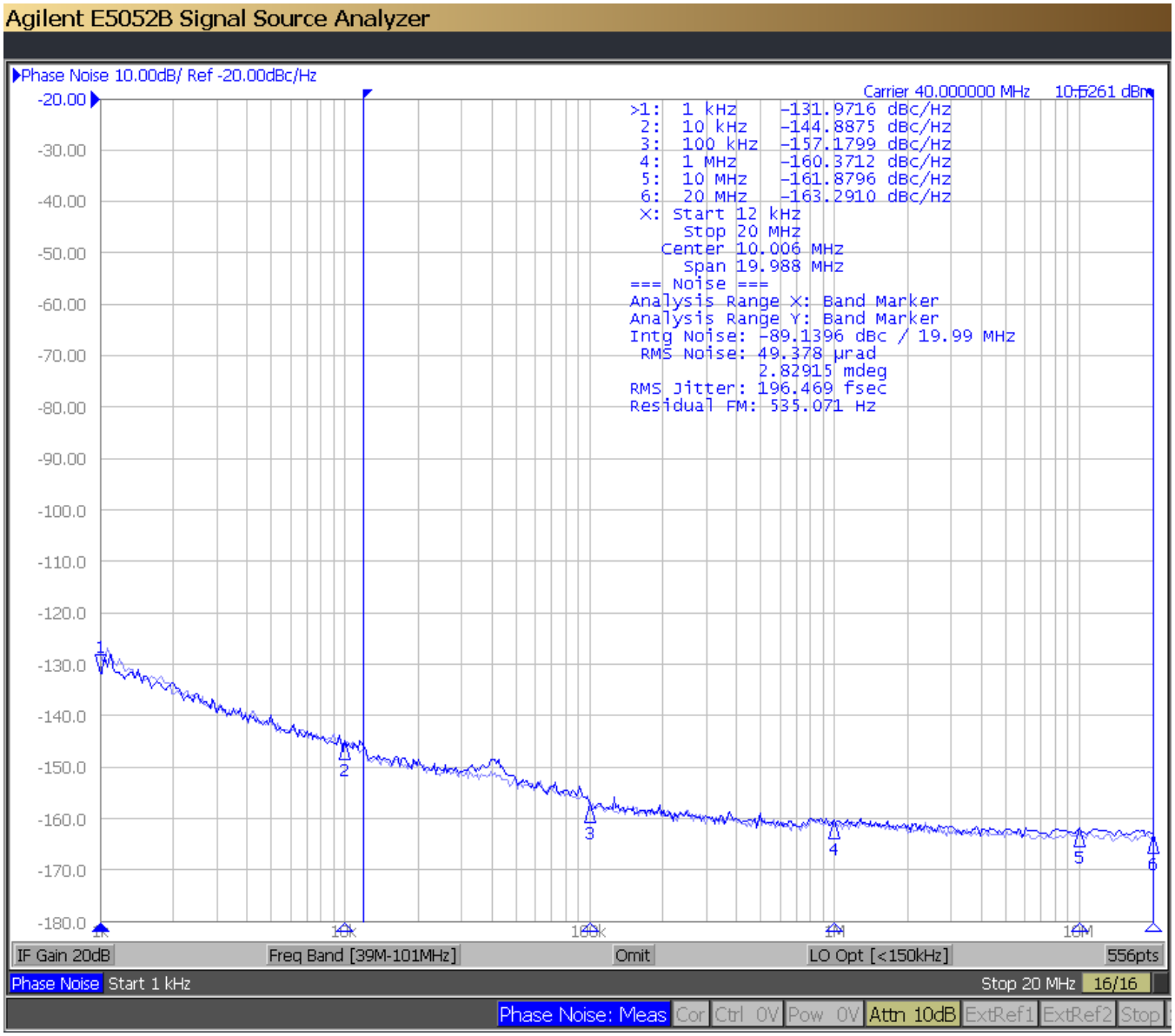


Figure 6. 40-MHz Input Phase Noise (181 fs rms, Light Blue), and Output Phase Noise (196 fs rms, Dark Blue), Additive Jitter = 77 fs rms

Typical Applications (continued)

9.2.2 Input Detail

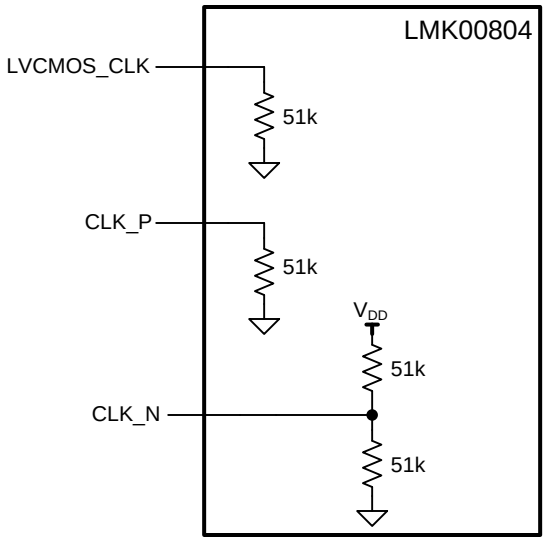


Figure 7. Clock Input Components

9.2.3 Input Clock Interface Circuits

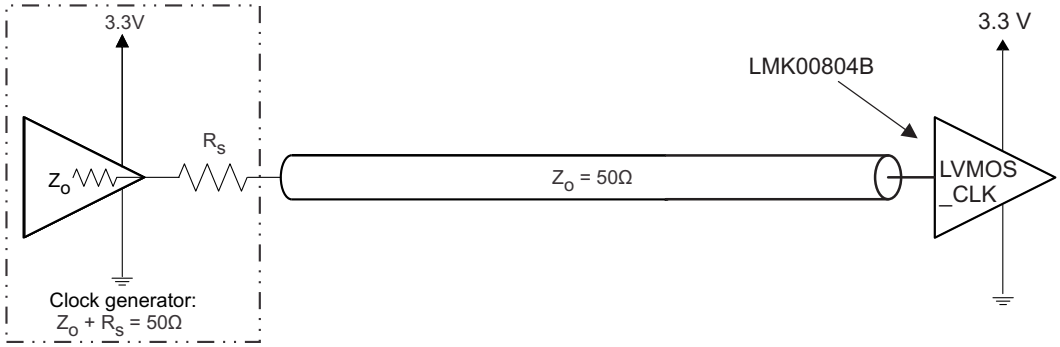
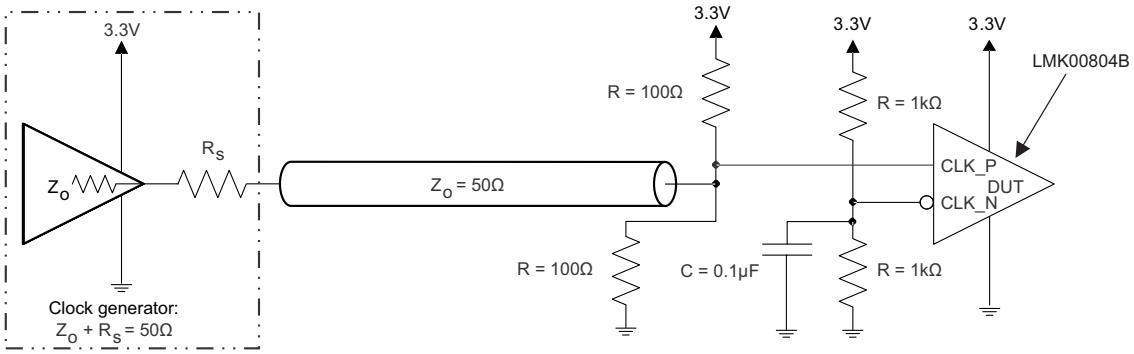


Figure 8. LVCMOS_CLK Input Configuration



(1) The Thevenin/split termination values (R = 100 Ω) at the CLK_P input may be adjusted to provide a small differential offset voltage (50 mV, for example) between the CLK_P and CLK_N inputs to prevent input chatter if the LVCMOS driver in a tri-state condition. For example, the engineer can use 105 Ω 1% to the 3.3-V rail and 97.6 Ω 1% to GND to receive a –60-mV offset voltage ($V_{CLK\_N} – V_{CLK\_P}$) . Ensure a logic low state if the LVCMOS driver enters a tri-state condition.

Figure 9. Single-Ended/LVCMOS Input DC Configuration

9.3 Do's and Don'ts

9.3.1 Power Considerations

The following power considerations refer to the device-consumed power consumption only. The device power consumption is the sum of static and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states
- Power required to charge any output load

The output load can be capacitive-only or capacitive and resistive. Use Equation 3 through Equation 5 to calculate the power consumption of the device:

$$P_{Dev} = P_{stat} + P_{dyn} + P_{Cload} \quad (3)$$

$$P_{stat} = (I_{DD} \times V_{DD}) + (I_{DDO} \times V_{DDO}) \quad (4)$$

$$P_{dyn} + P_{Cload} = (I_{DDO,dyn} + I_{DDO,Cload}) \times V_{DDO}$$

where:

- $I_{DDO,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA]
- $I_{DDO,Cload} = C_{load} \times V_{DDO} \times f \times n$ [mA] (5)

Example for power consumption of the LMK00804B-Q1: 4 outputs are switching, f = 100 MHz,

$V_{DD} = V_{DDO} = 3.465$ V and assuming $C_{load} = 5$ pF per output:

$$P_{Dev} = 90 \text{ mW} + 34 \text{ mW} = 124 \text{ mW} \quad (6)$$

$$P_{stat} = (21 \text{ mA} \times 3.465 \text{ V}) + (5 \text{ mA} \times 3.465 \text{ V}) = 90 \text{ mW} \quad (7)$$

$$P_{dyn} + P_{Cload} = (2.8 \text{ mA} + 6.9 \text{ mA}) \times 3.465 \text{ V} = 34 \text{ mW} \quad (8)$$

$$I_{DD,dyn} = 2 \text{ pF} \times 3.465 \text{ V} \times 100 \text{ MHz} \times 4 = 2.8 \text{ mA} \quad (9)$$

$$I_{DD,Cload} = 5 \text{ pF} \times 3.465 \text{ V} \times 100 \text{ MHz} \times 4 = 6.9 \text{ mA} \quad (10)$$

NOTE

For dimensioning the power supply, consider the total power consumption. The total power consumption is the sum of device power consumption and the power consumption of the load.

Do's and Don'ts (continued)

9.3.2 Recommendations for Unused Input and Output Pins

- **CLK_SEL and CLK_EN:** CLK_EN must be held low until a valid reference clock is provided before the engineer can use the pin to enable the outputs. These inputs both have an internal pullup (PU) according to Table 1. Table 1 shows the default floating state of these inputs:

Table 1. Input Floating Default States

INPUT	FLOATING STATE SELECTION
CLK_SEL	CLK_P/CLK_N selected
CLK_EN	Synchronous outputs enable

- **CLK_P/CLK_N Inputs:** See Figure 7 for the internal connections. When using a single-ended input, take note of the internal pullup and pulldown to make sure the unused input is properly biased. To interface a single-ended input to the CLK_P/CLK_N input, the configuration shown in Figure 9 is recommended.
- **LVCMOS_CLK Input:** See Figure 7 for the internal connection. The internal pulldown (PD) resistor ensures a low state when this input is left floating.
- **Outputs:** Connect the outputs to the receivers with a 43-Ω series resistor. Any unused output must be left floating.

9.3.3 Input Slew Rate Considerations

LMK00804B-Q1 employs high-speed and low-latency circuit topology to allow ultra-low additive jitter/phase noise and high-frequency operation. To take advantage of these benefits in the system application, it is optimal for the input signal to have a high slew rate of 3 V/ns or greater. Driving the input with a slower slew rate can degrade the additive jitter and noise floor performance. For this reason, a differential signal input is recommended over a single-ended signal, because a differential signal typically provides a higher slew rate and common-mode-rejection. Refer to and . Remember that using an input signal with a slow input slew rate less than 0.05 V/ns can cause output switching noise to feed back to the input stage and cause the output to chatter. This is especially true when driving either input single-ended fashion with a very slow slew rate, such as a sine-wave input signal.

10 Power Supply Recommendations

10.1 Power Supply Considerations

While there is no strict power supply sequencing requirement, it is generally best practice to sequence the supply input voltage (V_{DD}) before the supply output voltage (V_{DDO}).

10.1.1 Power-Supply Filtering

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

The use of bypass capacitors eliminates the low-frequency noise from power supply, because they can provide a very low-impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. The bypass capacitors also provide instantaneous current surges as required by the device, and should have low ESR. To use the bypass capacitors properly, place them close to the power supply terminals and lay out traces with short loops to minimize inductance. TI recommends that the engineer add as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply terminals in the package. TI recommends that the engineer insert a ferrite bead between the board power supply and the chip power supply to isolate the high-frequency switching noises generated by the clock driver. This would prevent leakage into the board supply. It is important to choose an appropriate ferrite bead with low DC resistance, because the bead must provide adequate isolation between the board supply and the chip supply. It is also important to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

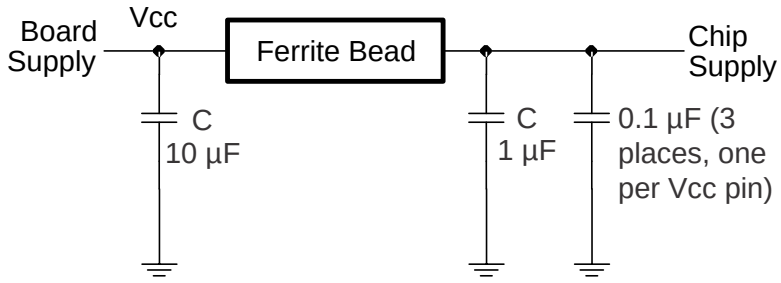


Figure 10. Power-Supply Decoupling

10.1.2 Thermal Management

For reliability and performance reasons, limit the die temperature to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times $R_{\theta JA}$ should not exceed 125°C.

Assuming the conditions in the *Power Considerations* section and operating at an ambient temperature of 70°C with all outputs loaded, Equation 11 shows the estimate of the LMK00804B-Q1 junction temperature:

$$T_J = T_A + P_{Total} \times R_{\theta JA} = 70°C + (124\ mW \times 48°C/W) = 70°C + 6.0°C = 76.0°C \quad (11)$$

Here are some recommendations to improve heat flow away from the die:

- Use multi-layer boards
- Specify a higher copper thickness for the board
- Increase the number of vias from the top level ground plane under and around the device to internal layers and to the bottom layer with as much copper area flow on each level as possible
- Apply air flow
- Leave unused outputs floating

11 Layout

11.1 Layout Guidelines

11.1.1 Ground Planes

Solid ground planes are recommended because these planes provide a low-impedance return paths between the device and bypass capacitors, along with the clock source and destination devices.

Avoid return paths of other system circuitry (for example, high-speed/digital logic, switching power supplies, and so forth) from passing through the local ground of the device to minimize noise coupling. Remember that noise coupling can lead to added jitter and spurious noise.

11.1.2 Power Supply Pins

Follow the power supply schematic and layout example described in *Power-Supply Filtering*.

11.1.3 Differential Input Termination

- Place input termination or biasing resistors as close to the CLK_P/CLK_N pins as possible.
- Avoid or minimize vias in the 50-Ω input traces to minimize impedance discontinuities. Intra-pair skew should also be minimized on the differential input traces.
- If not used, CLK_P/CLK_N inputs may be left as no connect.

11.1.4 LVCMOS Input Termination

- Input termination is not necessary when the LVCMOS_CLK input is driven from a LVCMOS driver that is series-terminated to match the characteristic impedance of the trace. Otherwise, place the input termination resistor as close to the LVCMOS_CLK input as possible.
- Avoid or minimize vias in the 50-Ω input trace to minimize impedance discontinuities.
- If not used, LVCMOS_CLK input may be left as no connect.

11.1.5 Output Termination

- Place 43-Ω series termination resistors close to the Qx outputs at the launch of the 50-Ω traces.
- Avoid or minimize vias in the 50-Ω input traces to minimize impedance discontinuities.
- If not used, any Qx output should be left as no connect.

11.2 Layout Example

Figure 11 shows the recommended PCB design for good electrical and thermal performance.

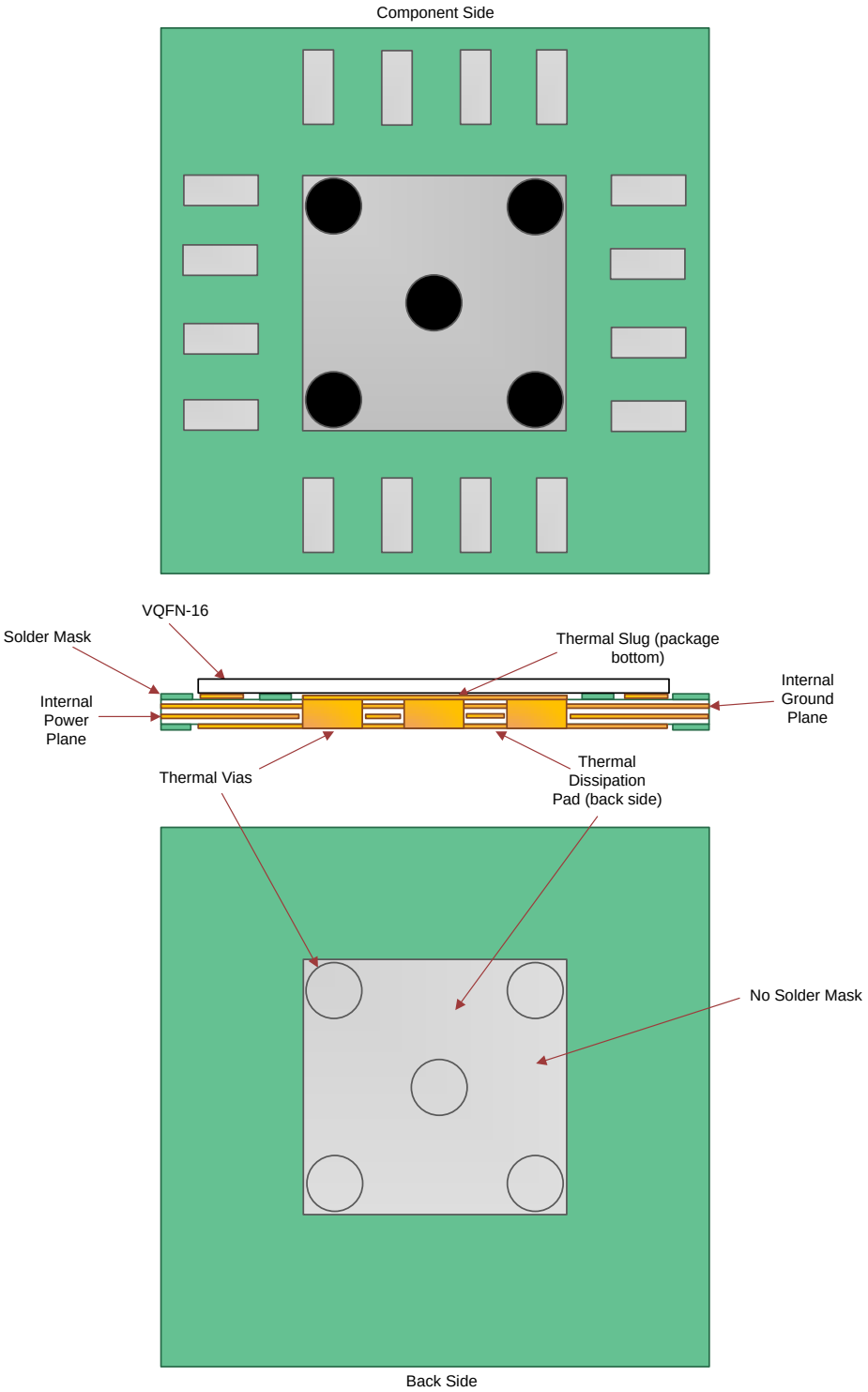


Figure 11. General PCB Ground Layout for Thermal Reliability

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *High-Speed Layout Guidelines,*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK00804BQWRGTRQ1	PREVIEW	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	804BQ	
LMK00804BQWRGTTQ1	PREVIEW	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	804BQ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMK00804B-Q1 :

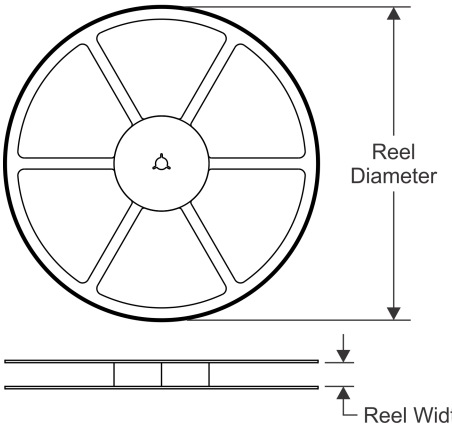
- Catalog: LMK00804B

NOTE: Qualified Version Definitions:

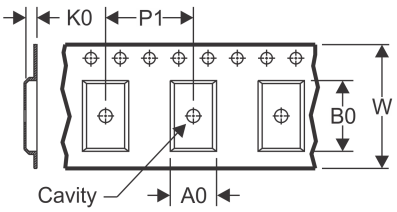
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

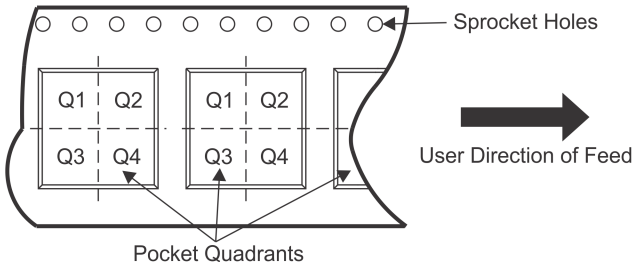


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

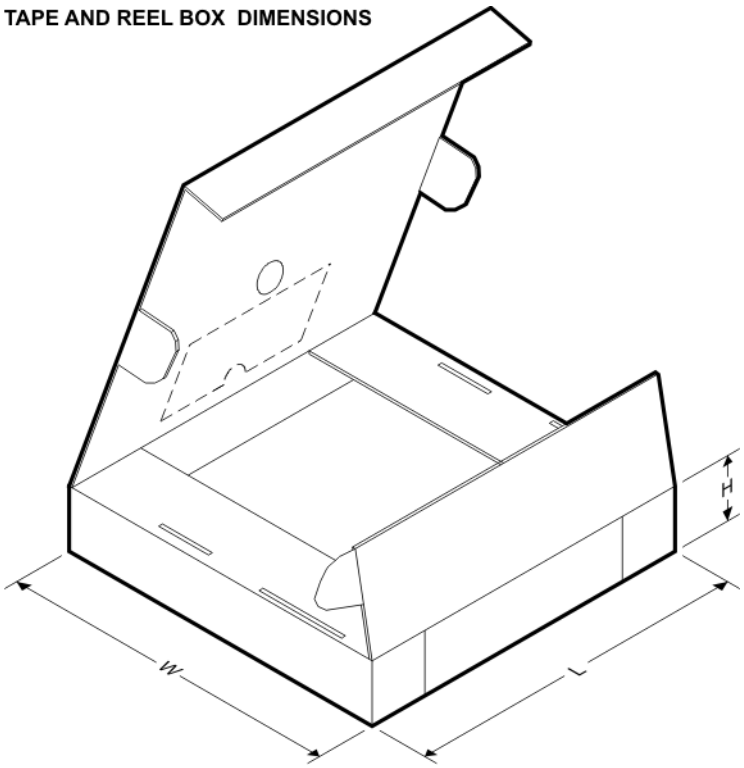
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK00804BQWRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMK00804BQWRGTTQ1	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

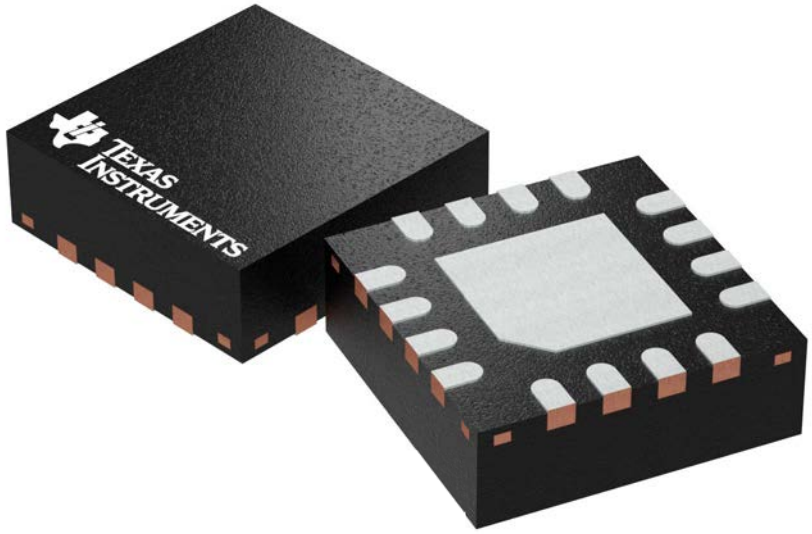


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK00804BQWRGTRQ1	VQFN	RGT	16	3000	367.0	367.0	35.0
LMK00804BQWRGTTQ1	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



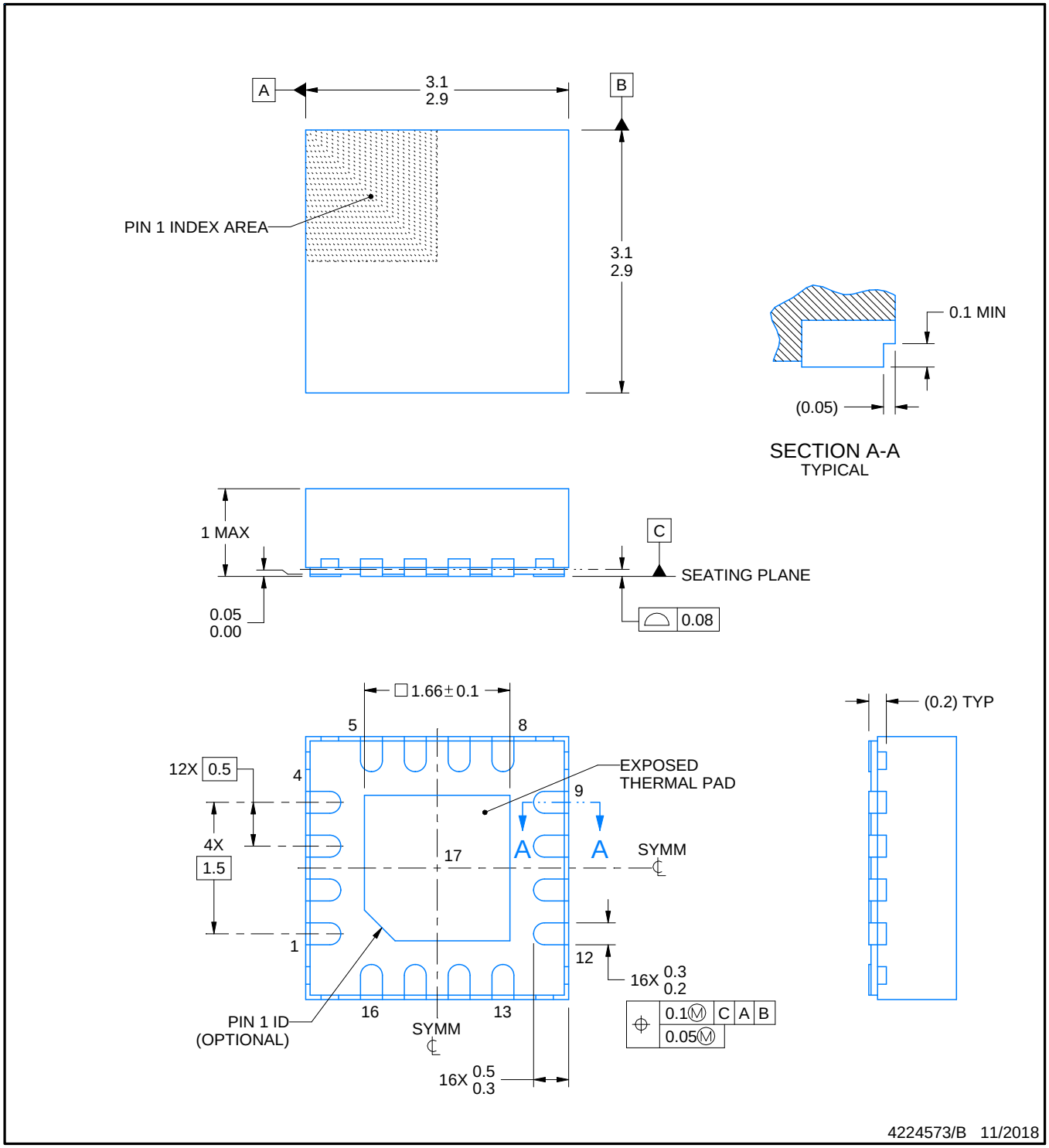
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RGT0016J

PACKAGE OUTLINE

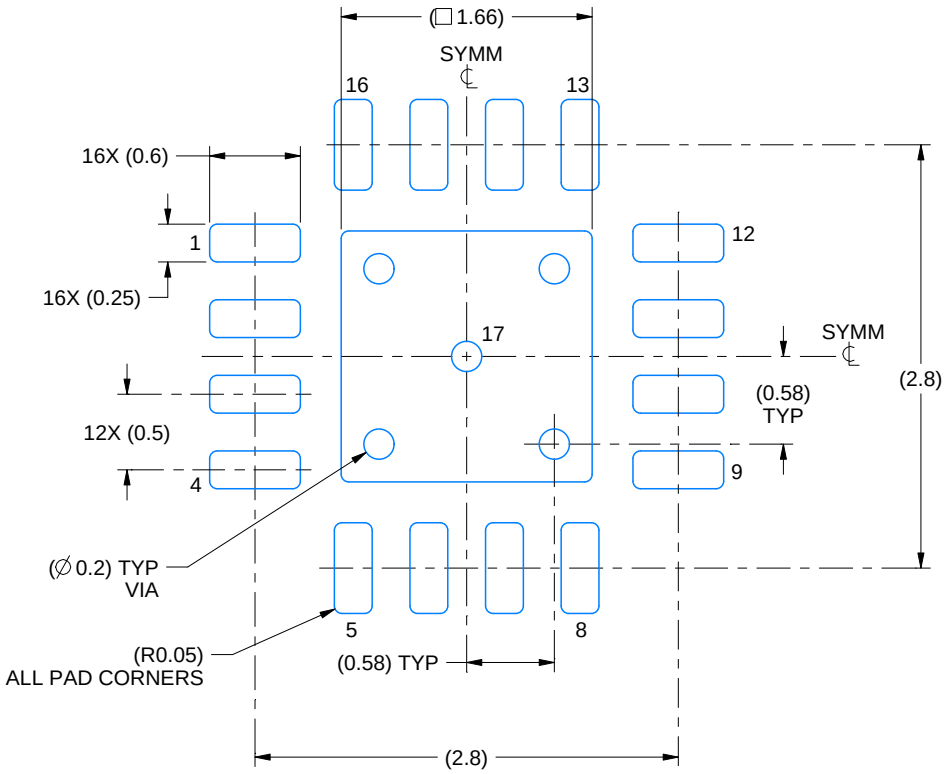
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

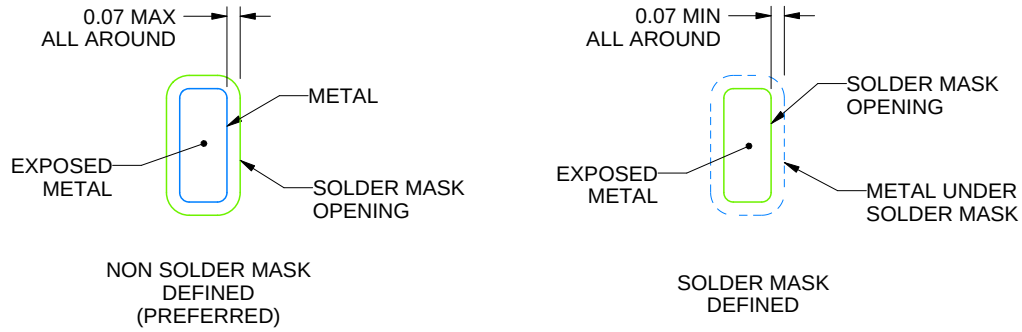


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

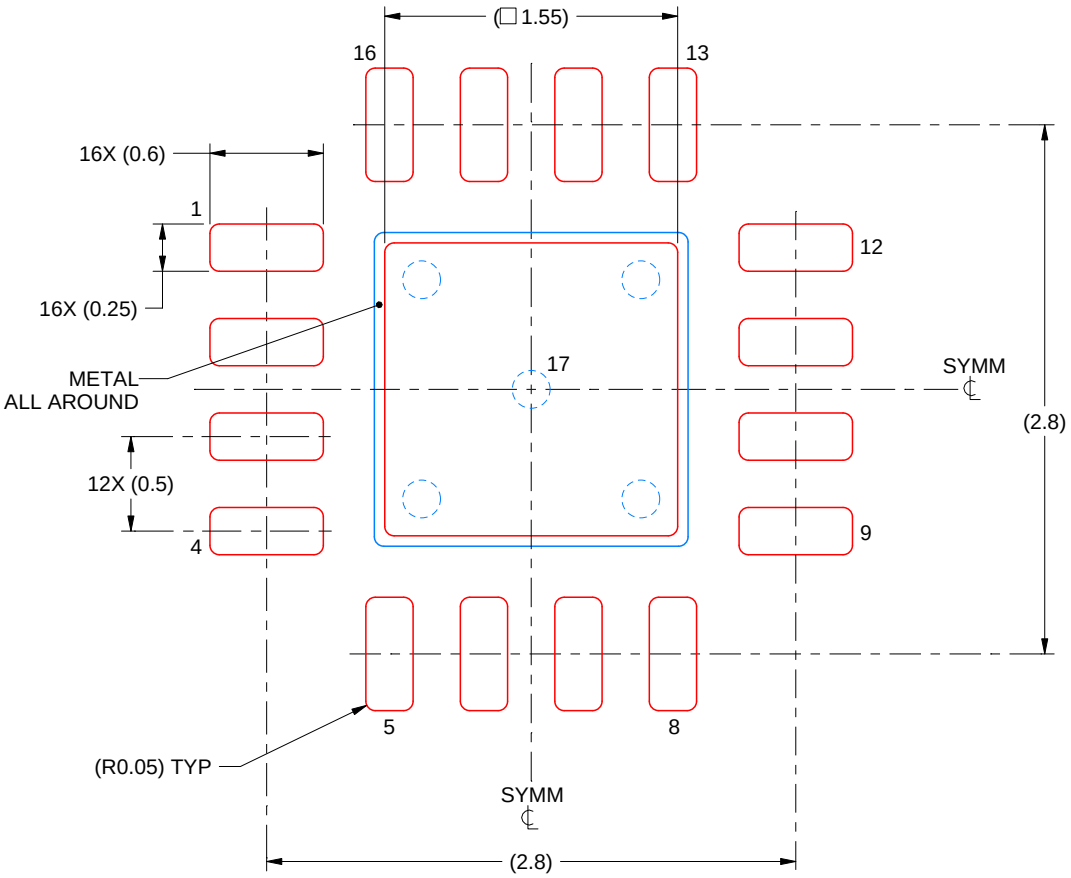


SOLDER MASK DETAILS

4224573/B 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

THERMAL PAD 17:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224573/B 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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