LMH6642/LMH6643/LMH6644 Low Power, 130MHz, 75mA Rail-to-Rail Output Amplifiers

Check for Samples: LMH6642, LMH6643, LMH6644

FEATURES

(V_S = ±5V, T_A = 25°C, R_L = 2kΩ, A_V = +1. Typical Values Unless Specified).

- **−3dB BW (A_V = +1) 130MHz**
- **Supply Voltage Range 2.7V to 12.8V**
- **Slew Rate (1), (A_V = −1) 130V/µs**
- **Supply Current (no load) 2.7mA/amp**
- **Output Short Circuit Current +115mA/−145mA**
- **Linear Output Current ±75mA**
- **Input Common Mode Volt. 0.5V Beyond V^-, 1V from V^+**
- **Output Voltage Swing 40mV from Rails**
- **Input Voltage Noise (100kHz) 17nV/$\sqrt{Hz}$**
- **Input Current Noise (100kHz) 0.9pA/$\sqrt{Hz}$**
- **THD (5MHz, R_L = 2kΩ, V_O = $2V_{PP}$, A_V = +2) −62dBc**
- **Settling Time 68ns**
- **Fully Characterized for 3V, 5V, and ±5V**
- **Overdrive Recovery 100ns**
- **Output Short Circuit Protected (2)**
- **No Output Phase Reversal with CMVR Exceeded**

APPLICATIONS

- **Active Filters**
- **CD/DVD ROM**
- **ADC Buffer Amp**
- **Portable Video**
- **Current Sense Buffer**

(1) Slew rate is the average of the rising and falling slew rates.
(2) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

DESCRIPTION

The LMH664X family true single supply voltage feedback amplifiers offer high speed (130MHz), low distortion (−62dBc), and exceptionally high output current (approximately 75mA) at low cost and with reduced power consumption when compared against existing devices with similar performance.

Input common mode voltage range extends to 0.5V below V^- and 1V from V^+. Output voltage range extends to within 40mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The output stage is capable of approximately 75mA in order to drive heavy loads. Fast output Slew Rate (130V/µs) ensures large peak-to-peak output swings can be maintained even at higher speeds, resulting in exceptional full power bandwidth of 40MHz with a 3V supply. These characteristics, along with low cost, are ideal features for a multitude of industrial and commercial applications.

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12MHz under 150Ω load and A_V = +2) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in ADC buffer, and high frequency filter applications as well as other applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01°) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150Ω) and throughout the output voltage range. The LMH664X family is offered in single (LMH6642), dual (LMH6643), and quad (LMH6644) options.

Closed Loop Gain vs. Frequency for Various Gain

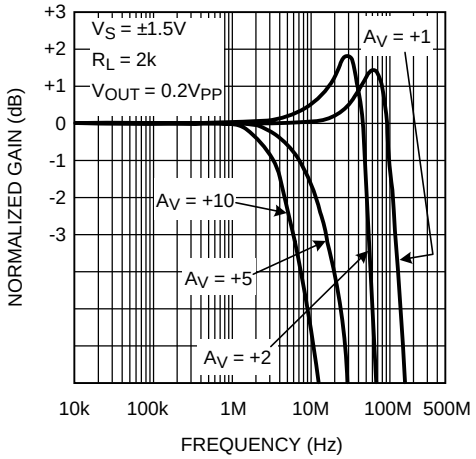


Figure 1.

Large Signal Frequency Response

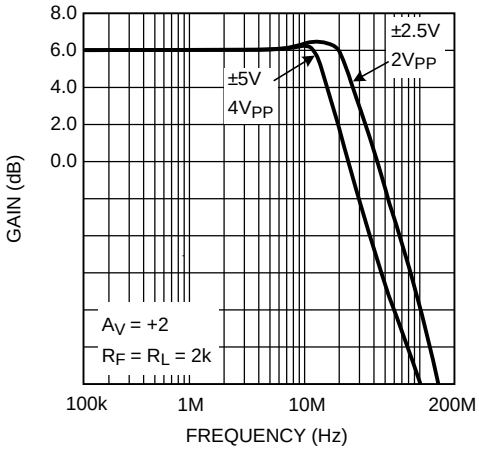


Figure 2.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance		2KV (3)
		200V (4)
		1000V (5)
V_{IN} Differential		±2.5V
Output Short Circuit Duration		See (6), (7)
Supply Voltage (V^+ - V^-)		13.5V
Voltage at Input/Output pins		V^+ +0.8V, V^- −0.8V
Input Current		±10mA
Storage Temperature Range		−65°C to +150°C
Junction Temperature (8)		+150°C
Soldering Information	Infrared or Convection Reflow (20 sec)	235°C
	Wave Soldering Lead Temp.(10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human body model, 1.5kΩ in series with 100pF.
(4) Machine Model, 0Ω in series with 200pF.
(5) CDM: Charge Device Model
(6) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.
(8) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Supply Voltage ($V^+ - V^-$)		2.7V to 12.8V
Junction Temperature Range (2)		−40°C to +85°C
Package Thermal Resistance (2) (θ_{JA})	5-Pin SOT-23	265°C/W
	8-Pin SOIC	190°C/W
	8-Pin VSSOP	235°C/W
	14-Pin SOIC	145°C/W
	14- Pin TSSOP	155°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$	80	115		MHz
		A_V = +2, −1, V_{OUT} = 200mV$_{PP}$		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_L = 402Ω, V_{OUT} = 200mV$_{PP}$		19		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 1V$_{PP}$		40		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		nV/√Hz
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		pA/√Hz
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = −1, R_L = 100Ω to $V^+/2$		−48		dBc
DG	Differential Gain	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to $V^+/2$		0.17		%
		R_L =1kΩ to $V^+/2$		0.03		
DP	Differential Phase	V_{CM} = 1V, NTSC, A_V = +2 R_L =150Ω to $V^+/2$		0.05		deg
		R_L =1kΩ to $V^+/2$		0.03		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: $R_f = R_g$ = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load, V_S = 5V		68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V$_{PP}$	90	120		V/µs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644		±1	±5 **±7**	mV
		For LMH6643		±1	±3.4 **±7**	
TC V_{OS}	Input Offset Average Drift	See (4)		±5		µV/°C
I_B	Input Bias Current	See (5)		−1.50	−2.60 **−3.25**	µA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

3V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.5	−0.2 **−0.1**	V
			1.8 **1.6**	2.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 1.5V	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 2.5V R_L = 2kΩ to $V^+/2$	80 **75**	96		dB
		V_O = 0.5V to 2.5V R_L = 150Ω to $V^+/2$	74 **70**	82		
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV	2.90	2.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV	2.80	2.93		
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV		25	75	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV		75	150	
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 200mV (6)	50 **35**	95		mA
		Sinking to $V^+/2$ V_{ID} = −200mV (6)	55 **40**	110		
I_{OUT}	Output Current	V_{OUT} = 0.5V from either supply		±65		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 3.0V to 3.5V, V_{CM} = 1.5V	75	85		dB
I_S	Supply Current (per channel)	No Load		2.70	4.00 **4.50**	mA

(6) Short circuit test is a momentary test. See Note 7 under 5V Electrical Characteristics.

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$	90	120		MHz
		A_V = +2, −1, V_{OUT} = 200mV$_{PP}$		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 402Ω, V_{OUT} = 200mV$_{PP}$		15		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 2V$_{PP}$		22		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		nV/√Hz
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		pA/√Hz
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = +2		−60		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L =150Ω to $V^+/2$		0.16		%
		R_L = 1kΩ to $V^+/2$		0.05		
DP	Differential Phase	NTSC, A_V = +2 R_L = 150Ω to $V^+/2$		0.05		deg
		R_L = 1kΩ to $V^+/2$		0.01		

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = $2V_{PP}$, ±0.1%, 8pF Load		68		ns
SR	Slew Rate (3)	A_V = −1, V_I = $2V_{PP}$	95	125		V/µs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644		±1	±5 **±7**	mV
		For LMH6643		±1	±3.4 **±7**	mV
TC V_{OS}	Input Offset Average Drift	See (4)		±5		µV/°C
I_B	Input Bias Current	See (5)		−1.70	−2.60 **−3.25**	µA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−0.5	−0.2 **−0.1**	V
			3.8 **3.6**	4.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	72	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.50V R_L = 2kΩ to $V^+/2$	86 **82**	98		dB
		V_O = 0.5V to 4.25V R_L = 150Ω to $V^+/2$	76 **72**	82		dB
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$, V_{ID} = 200mV	4.90	4.98		V
		R_L = 150Ω to $V^+/2$, V_{ID} = 200mV	4.65	4.90		V
	Output Swing Low	R_L = 2kΩ to $V^+/2$, V_{ID} = −200mV		25	100	mV
		R_L = 150Ω to $V^+/2$, V_{ID} = −200mV		100	150	mV
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 200mV (6)(7)	55 **40**	115		mA
		Sinking to $V^+/2$ V_{ID} = −200mV (6)(7)	70 **55**	140		mA
I_{OUT}	Output Current	V_O = 0.5V from either supply		±70		mA
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 4.0V to 6V	79	90		dB
I_S	Supply Current (per channel)	No Load		2.70	4.25 **5.00**	mA

(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) Short circuit test is a momentary test. See Note 7.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
BW	−3dB BW	A_V = +1, V_{OUT} = 200mV$_{PP}$	95	130		MHz
		A_V = +2, −1, V_{OUT} = 200mV$_{PP}$		46		
$BW_{0.1dB}$	0.1dB Gain Flatness	A_V = +2, R_L = 150Ω to V+/2, R_f = 806Ω, V_{OUT} = 200mV$_{PP}$		12		MHz
PBW	Full Power Bandwidth	A_V = +1, −1dB, V_{OUT} = 2V$_{PP}$		24		MHz
e_n	Input-Referred Voltage Noise	f = 100kHz		17		nV/√Hz
		f = 1kHz		48		
i_n	Input-Referred Current Noise	f = 100kHz		0.90		pA/√Hz
		f = 1kHz		3.3		
THD	Total Harmonic Distortion	f = 5MHz, V_O = 2V$_{PP}$, A_V = +2		−62		dBc
DG	Differential Gain	NTSC, A_V = +2 R_L = 150Ω to V^+/2		0.15		%
		R_L = 1kΩ to V^+/2		0.01		
DP	Differential Phase	NTSC, A_V = +2 R_L = 150Ω to V^+/2		0.04		deg
		R_L = 1kΩ to V^+/2		0.01		
CT Rej.	Cross-Talk Rejection	f = 5MHz, Receiver: R_f = R_g = 510Ω, A_V = +2		47		dB
T_S	Settling Time	V_O = 2V$_{PP}$, ±0.1%, 8pF Load, V_S = 5V		68		ns
SR	Slew Rate (3)	A_V = −1, V_I = 2V$_{PP}$	100	135		V/µs
V_{OS}	Input Offset Voltage	For LMH6642 and LMH6644		±1	±5 **±7**	mV
		For LMH6643		±1	±3.4 **±7**	
TC V_{OS}	Input Offset Average Drift	See (4)		±5		µV/°C
I_B	Input Bias Current	See (5)		−1.60	−2.60 **−3.25**	µA
I_{OS}	Input Offset Current			20	800 **1000**	nA
R_{IN}	Common Mode Input Resistance			3		MΩ
C_{IN}	Common Mode Input Capacitance			2		pF
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50dB		−5.5	−5.2 **−5.1**	V
			3.8 **3.6**	4.0		
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from −5V to 3.5V	74	95		dB
A_{VOL}	Large Signal Voltage Gain	V_O = −4.5V to 4.5V, R_L = 2kΩ	88 **84**	96		dB
		V_O = −4.0V to 4.0V, R_L = 150Ω	78 **74**	82		
V_O	Output Swing High	R_L = 2kΩ, V_{ID} = 200mV	4.90	4.96		V
		R_L = 150Ω, V_{ID} = 200mV	4.65	4.80		
	Output Swing Low	R_L = 2kΩ, V_{ID} = −200mV		−4.96	−4.90	V
		R_L = 150Ω, V_{ID} = −200mV		−4.80	−4.65	

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Slew rate is the average of the rising and falling slew rates.
(4) Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes by the total temperature change.
(5) Positive current corresponds to current flowing into the device.

±5V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V^+ = 5V, V^- = −5V, V_{CM} = V_O = 0V, V_{ID} (input differential voltage) as noted (where applicable) and R_L = 2kΩ to ground. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
I_{SC}	Output Short Circuit Current	Sourcing to Ground V_{ID} = 200mV (6)(7)	60 **35**	115		mA
		Sinking to Ground V_{ID} = −200mV (6)(7)	85 **65**	145		
I_{OUT}	Output Current	V_O = 0.5V from either supply	±75			mA
PSRR	Power Supply Rejection Ratio	(V^+, V^-) = (4.5V, −4.5V) to (5.5V, −5.5V)	78	90		dB
I_S	Supply Current (per channel)	No Load		2.70	4.50 **5.50**	mA

(6) Short circuit test is a momentary test. See Note 7.
(7) Output short circuit duration is infinite for V_S < 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

Connection Diagram

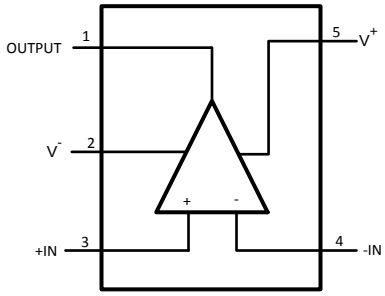


Figure 3. 5-Pin SOT-23 (LMH6642)
Top View
Package Number DBV0005A

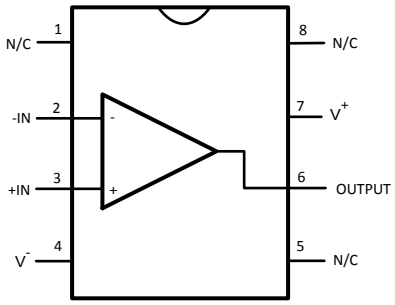


Figure 4. 8-Pin SOIC (LMH6642)
Top View
Package Number D0008A

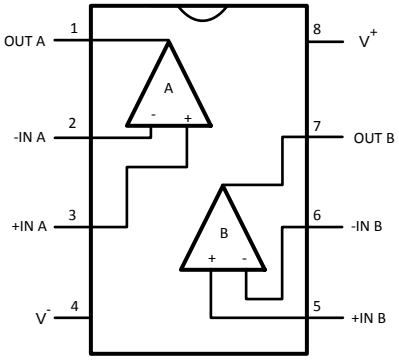


Figure 5. SOIC and VSSOP 8-Pin (LMH6643)
Top View
Package Number DGK0008A

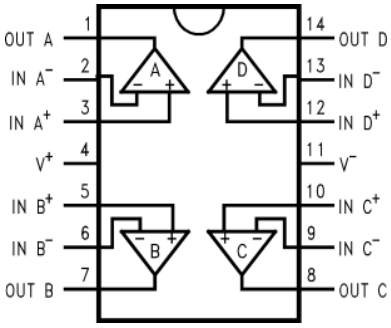


Figure 6. 14-Pin SOIC and 14-Pin TSSOP (LMH6644)
Top View
Package Numbers D0014A, PW0014A

Typical Performance Characteristics

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

Closed Loop Frequency Response for Various Supplies

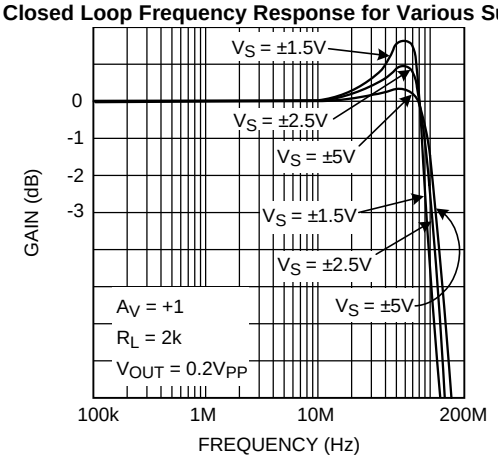


Figure 7.

Closed Loop Gain vs. Frequency for Various Gain

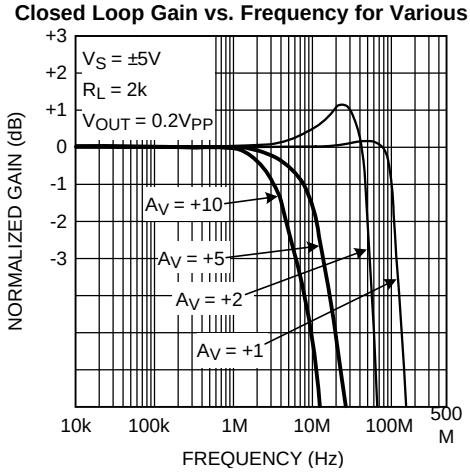


Figure 8.

Closed Loop Gain vs. Frequency for Various Gain

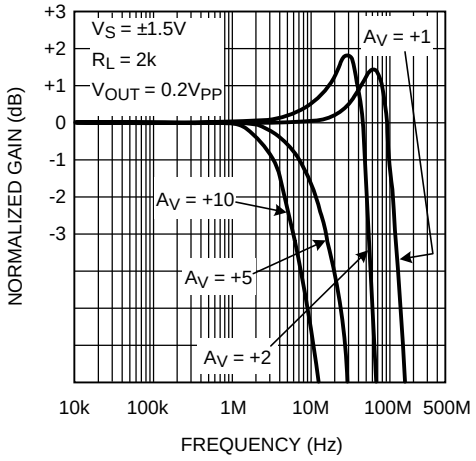


Figure 9.

Closed Loop Frequency Response for Various Temperature

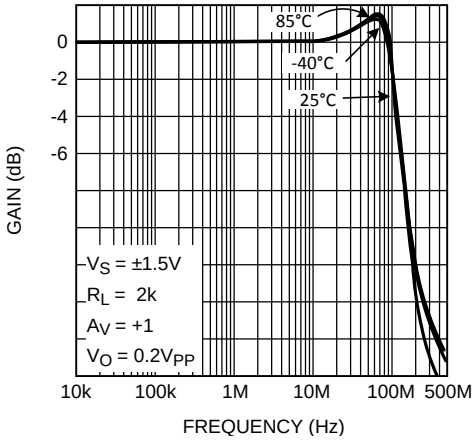


Figure 10.

Closed Loop Gain vs. Frequency for Various Supplies

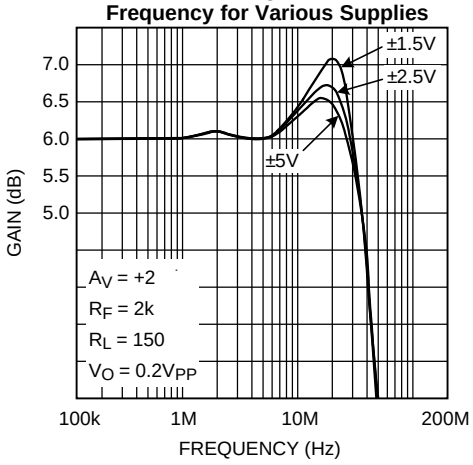


Figure 11.

Closed Loop Frequency Response for Various Temperature

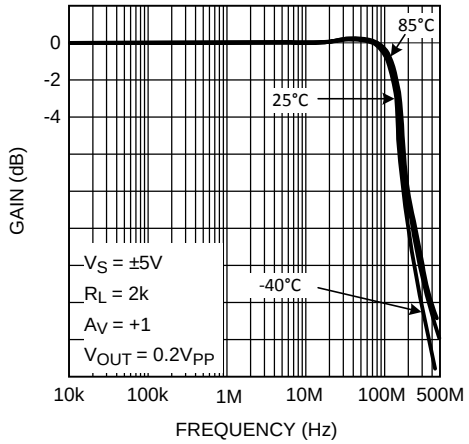


Figure 12.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

Large Signal Frequency Response

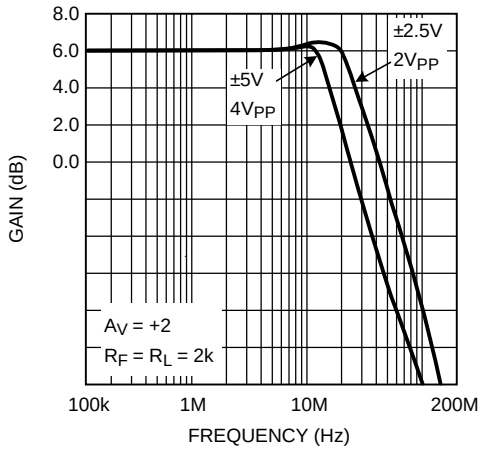


Figure 13.

Closed Loop Small Signal Frequency Response for Various Supplies

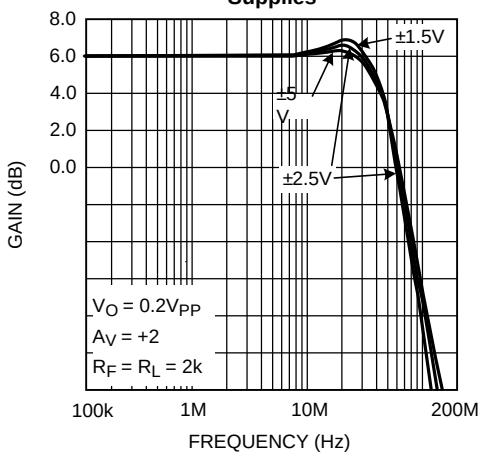


Figure 14.

Closed Loop Frequency Response for Various Supplies

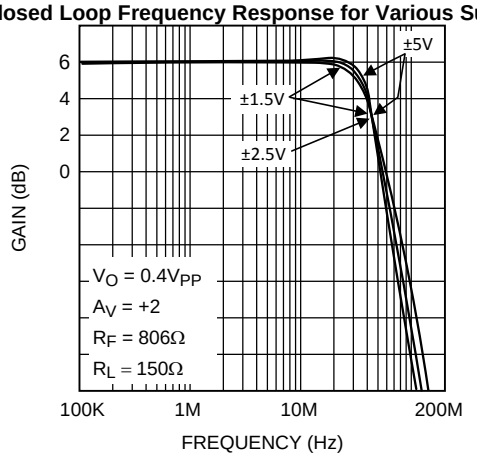


Figure 15.

±0.1dB Gain Flatness for Various Supplies

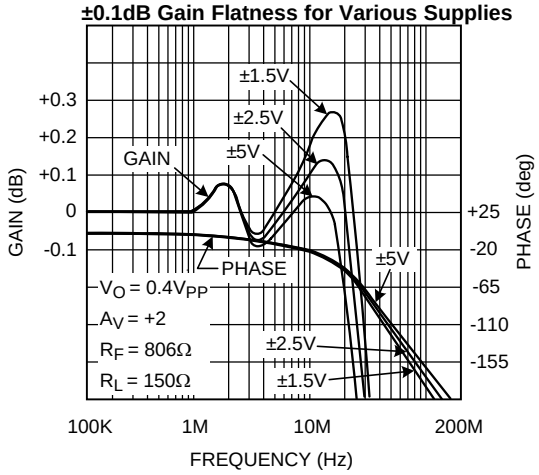


Figure 16.

V_{OUT} (V_{PP}) for THD < 0.5%

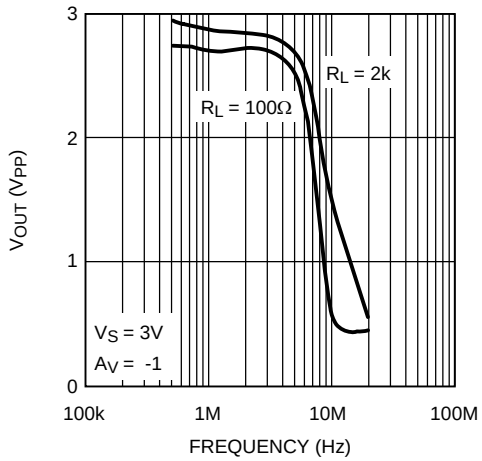


Figure 17.

V_{OUT} (V_{PP}) for THD < 0.5%

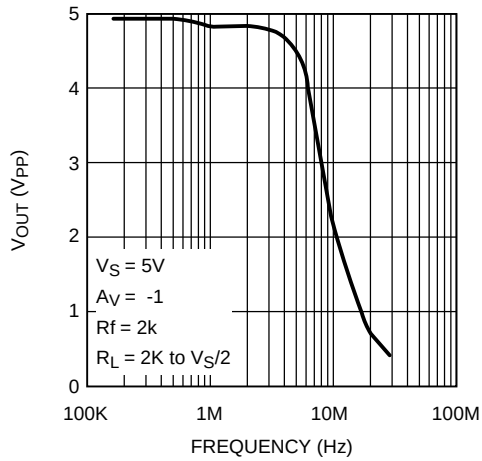


Figure 18.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

V_{OUT} (V_{PP}) for THD < 0.5%

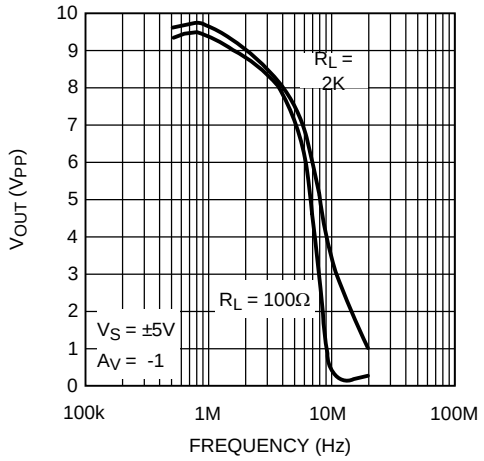


Figure 19.

Open Loop Gain/Phase for Various Temperature

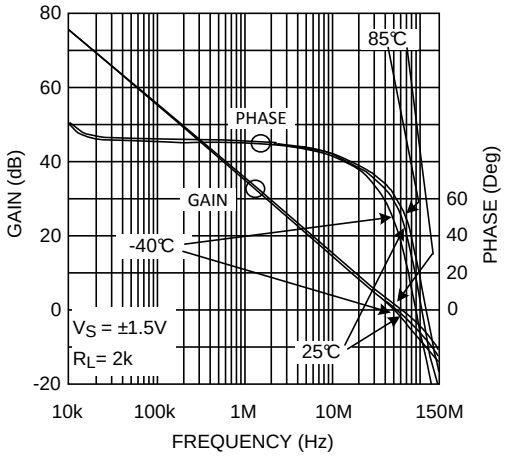


Figure 20.

Open Loop Gain/Phase for Various Temperature

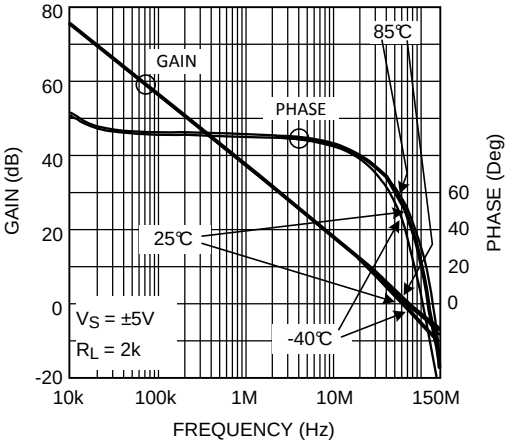


Figure 21.

HD2 (dBc) vs. Output Swing

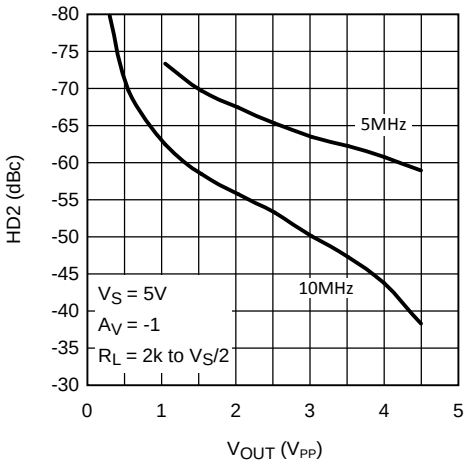


Figure 22.

HD3 (dBc) vs. Output Swing

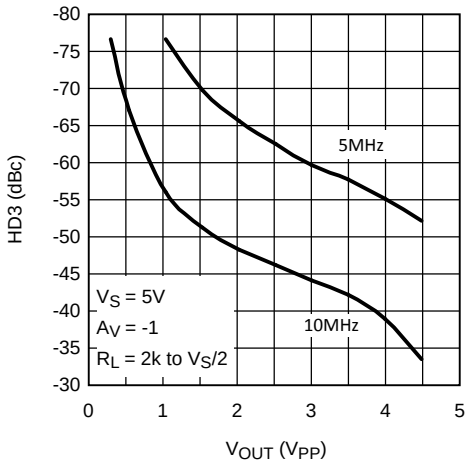


Figure 23.

HD2 vs. Output Swing

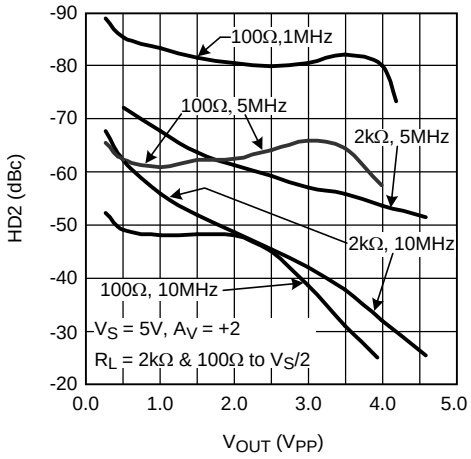


Figure 24.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

HD3 vs. Output Swing

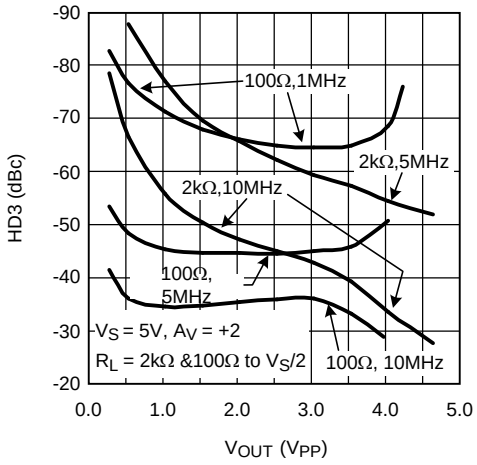


Figure 25.

THD (dBc) vs. Output Swing

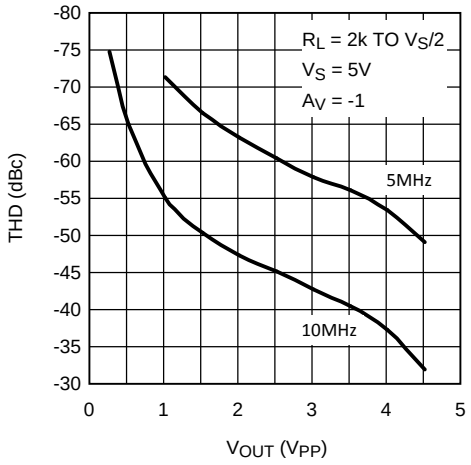


Figure 26.

Settling Time vs. Input Step Amplitude (Output Slew and Settle Time)

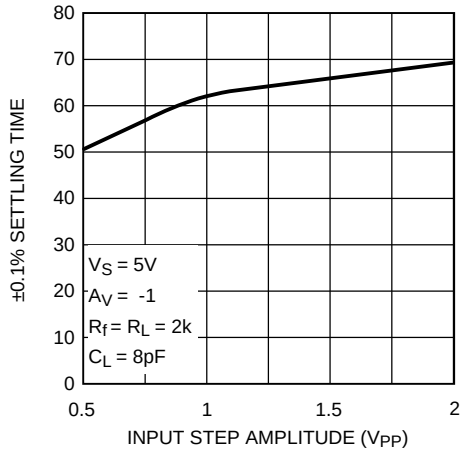


Figure 27.

Input Noise vs. Frequency

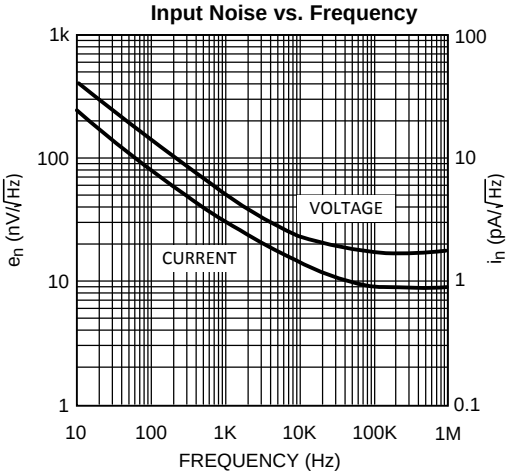


Figure 28.

V_{OUT} from V^+ vs. I_{SOURCE}

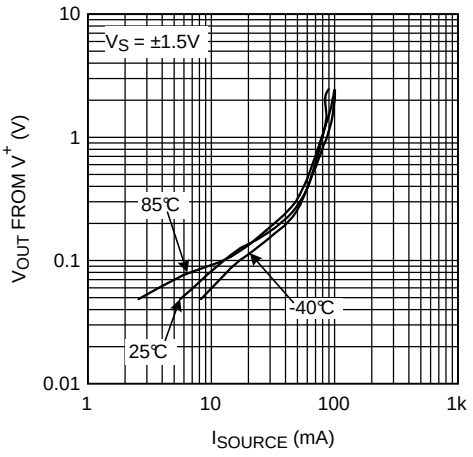


Figure 29.

V_{OUT} from V^- vs. I_{SINK}

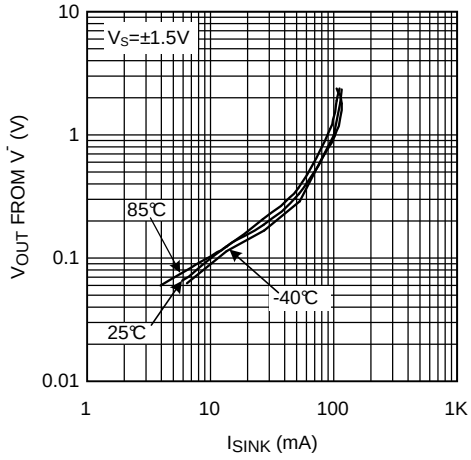


Figure 30.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

V_{OUT} from V^+ vs. I_{SOURCE}

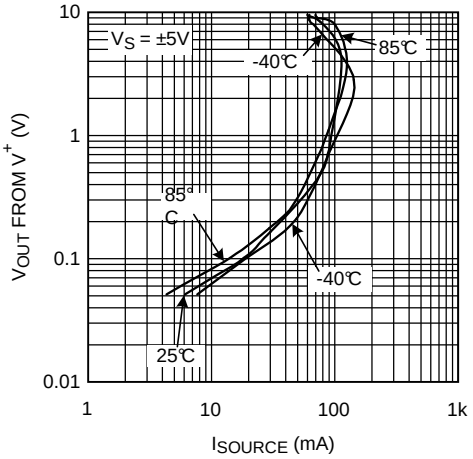


Figure 31.

V_{OUT} from V^- vs. I_{SINK}

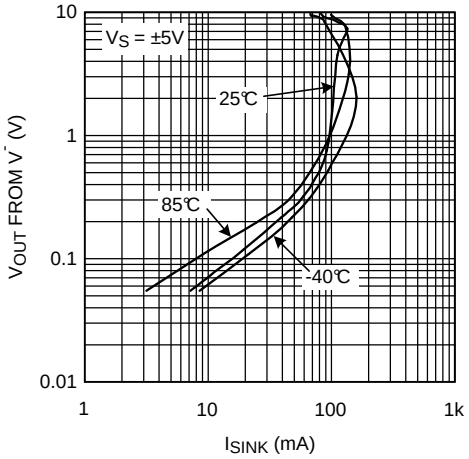


Figure 32.

Swing vs. V_S

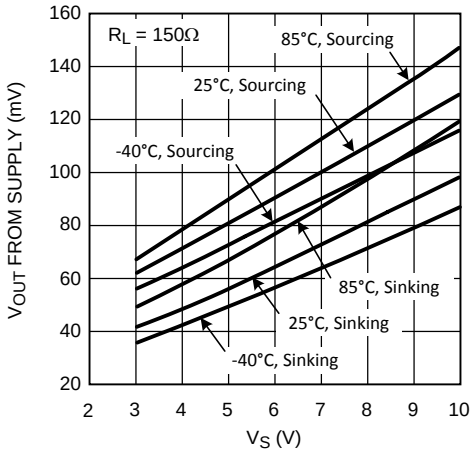


Figure 33.

Short Circuit Current (to V_S/2) vs. V_S

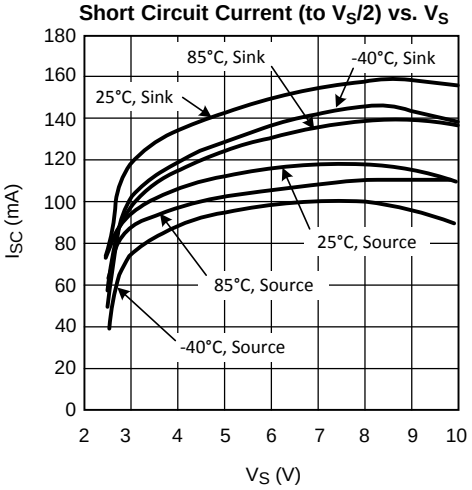


Figure 34.

Output Sinking Saturation Voltage vs. I_{OUT}

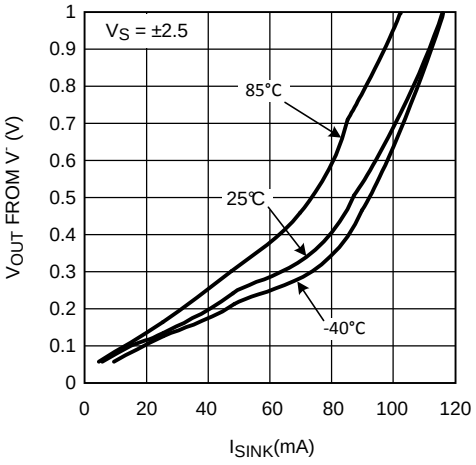


Figure 35.

Output Sourcing Saturation Voltage vs. I_{OUT}

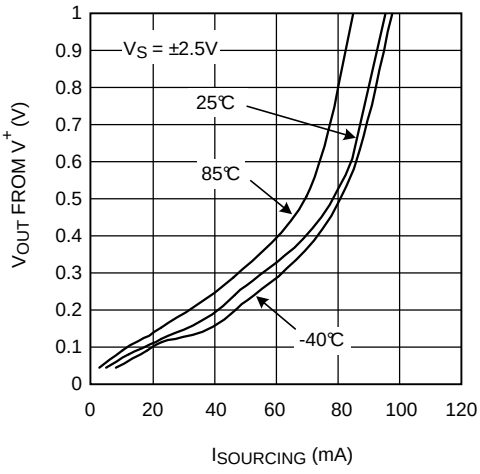


Figure 36.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

Closed Loop Output Impedance vs. Frequency A_V = +1

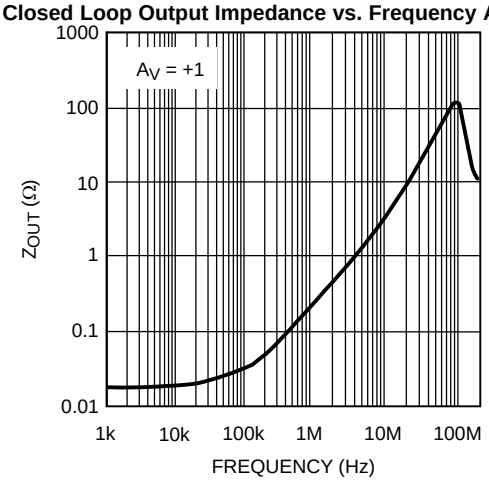


Figure 37.

PSRR vs. Frequency

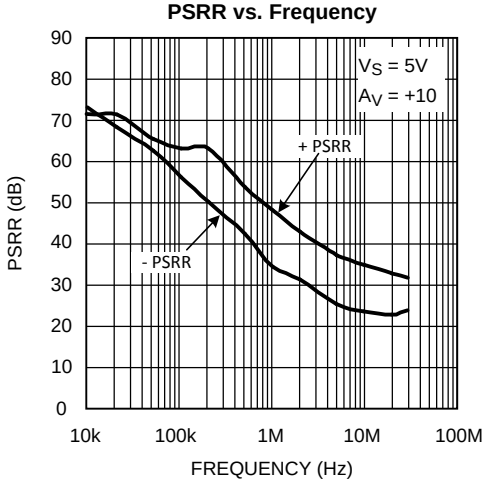


Figure 38.

CMRR vs. Frequency

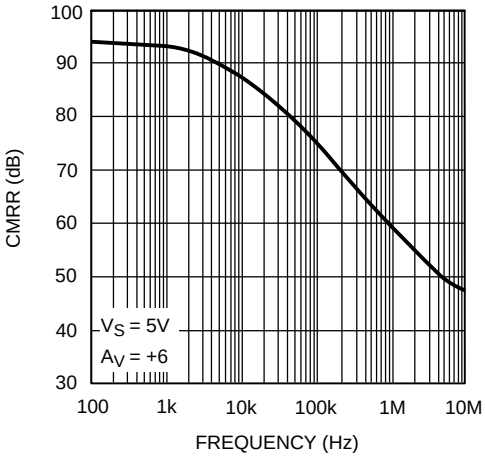


Figure 39.

Crosstalk Rejection vs. Frequency (Output to Output)

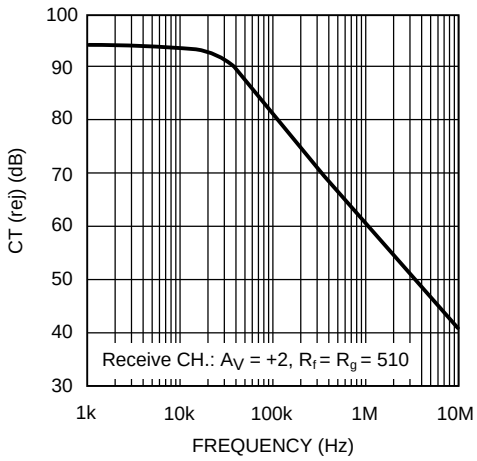


Figure 40.

V_{OS} vs. V_{OUT} (Typical Unit)

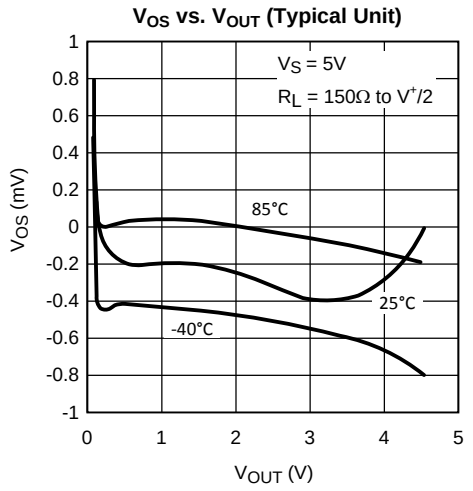


Figure 41.

V_{OS} vs. V_{CM} (Typical Unit)

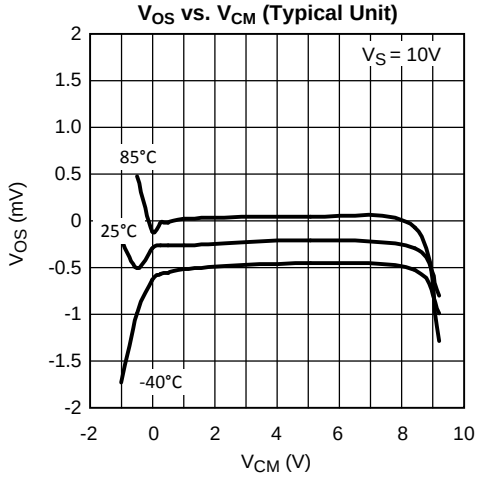


Figure 42.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

V_{OS} vs. V_S (for 3 Representative Units)

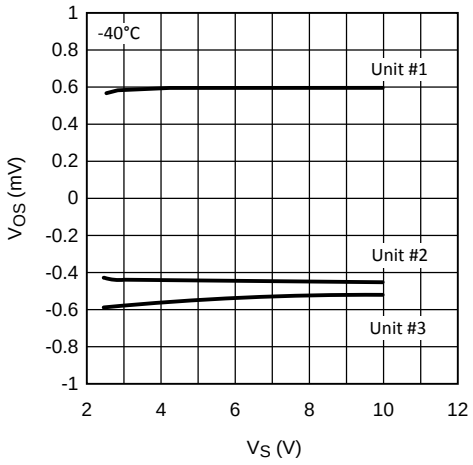


Figure 43.

V_{OS} vs. V_S (for 3 Representative Units)

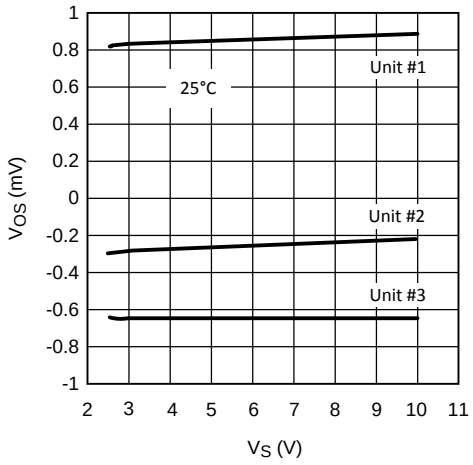


Figure 44.

V_{OS} vs. V_S (for 3 Representative Units)

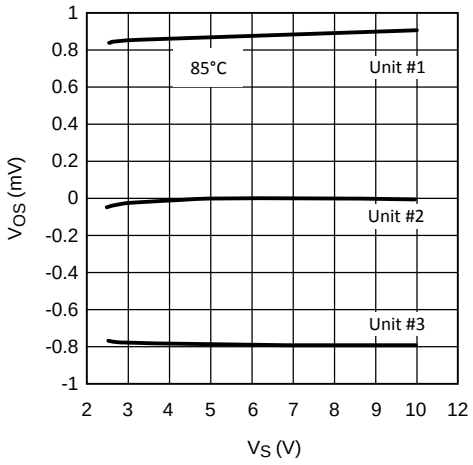


Figure 45.

I_B vs. V_S

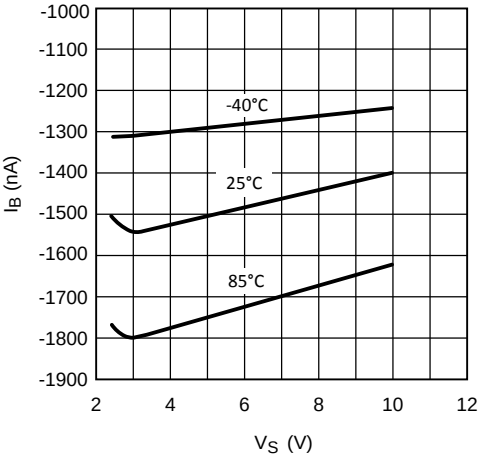


Figure 46.

I_{OS} vs. V_S

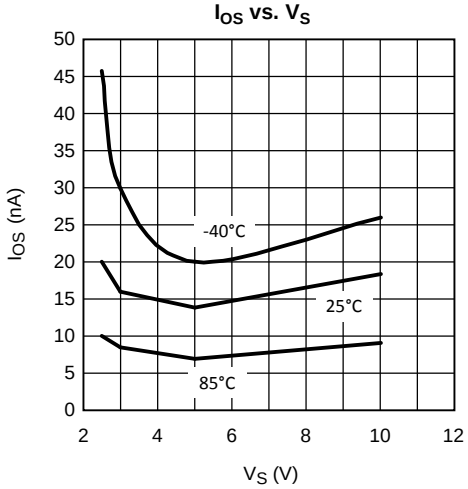


Figure 47.

I_S vs. V_{CM}

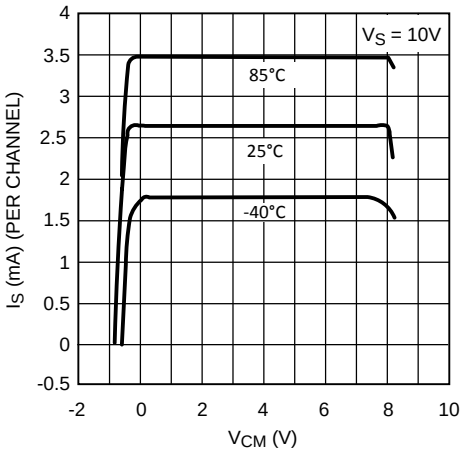


Figure 48.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

I_S vs. V_S

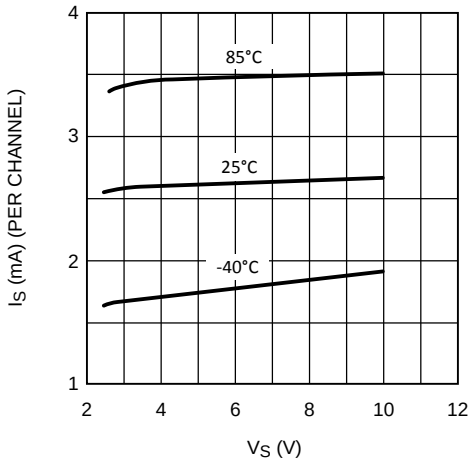


Figure 49.

Small Signal Step Response

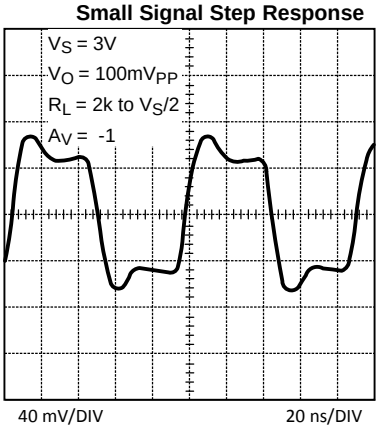


Figure 50.

Large Signal Step Response

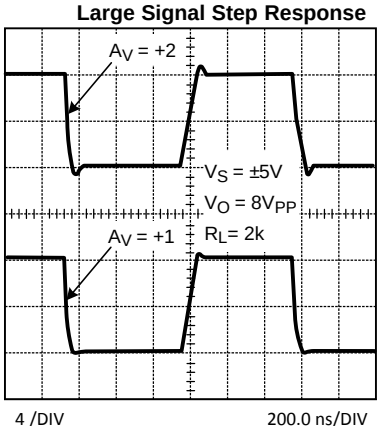


Figure 51.

Large Signal Step Response

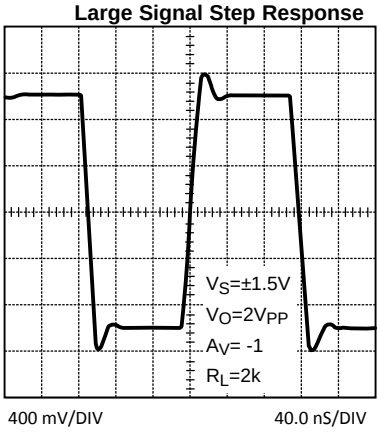


Figure 52.

Small Signal Step Response

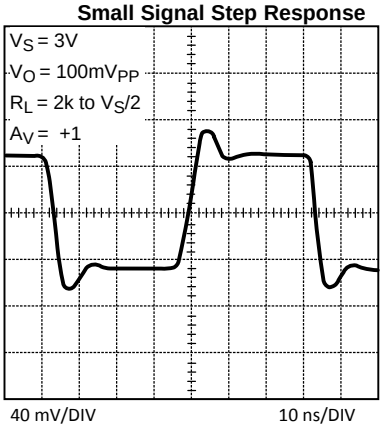


Figure 53.

Small Signal Step Response

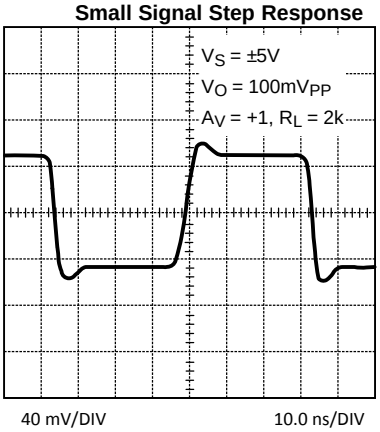


Figure 54.

Typical Performance Characteristics (continued)

At T_J = 25°C, V^+ = +5, V^- = −5V, R_F = R_L = 2kΩ. Unless otherwise specified.

Small Signal Step Response

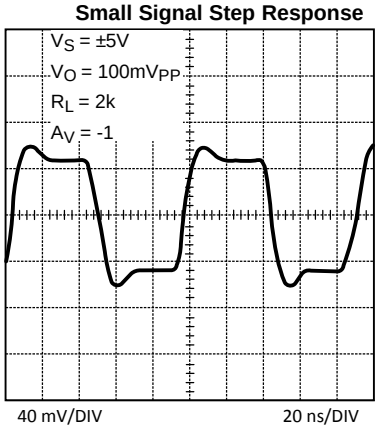


Figure 55.

Small Signal Step Response

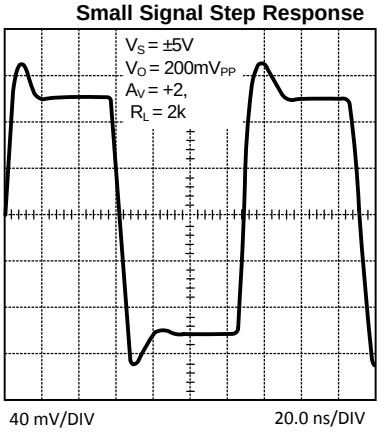


Figure 56.

Large Signal Step Response

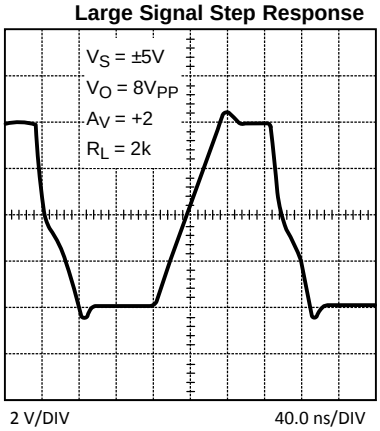


Figure 57.

Large Signal Step Response

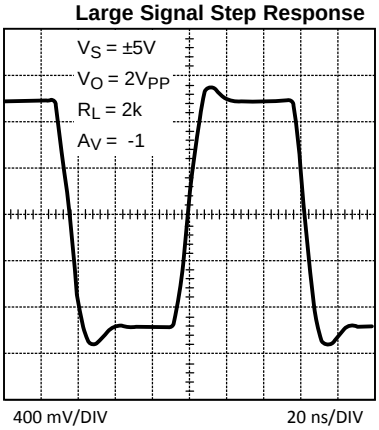


Figure 58.

Large Signal Step Response

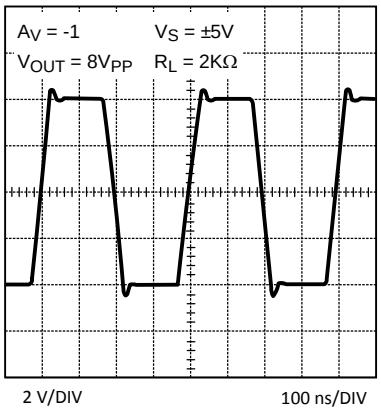


Figure 59.

APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The LMH664X family is based on proprietary VIP10 dielectrically isolated bipolar process.

This device family architecture features the following:

- Complimentary bipolar devices with exceptionally high f_t (~8GHz) even under low supply voltage (2.7V) and low bias current.
- A class A-B "turn-around" stage with improved noise, offset, and reduced power dissipation compared to similar speed devices (patent pending).
- Common Emitter push-push output stage capable of 75mA output current (at 0.5V from the supply rails) while consuming only 2.7mA of total supply current per channel. This architecture allows output to reach within milli-volts of either supply rail.
- Consistent performance over the entire operating supply voltage range with little variation for the most important specifications (e.g. BW, SR, I_{OUT}, etc.)
- Significant power saving (~40%) compared to competitive devices on the market with similar performance.

Application Hints

This Op Amp family is a drop-in replacement for the AD805X family of high speed Op Amps in most applications. In addition, the LMH664X will typically save about 40% on power dissipation, due to lower supply current, when compared to competition. All AD805X family's guaranteed parameters are included in the list of LMH664X guaranteed specifications in order to ensure equal or better level of performance. However, as in most high performance parts, due to subtleties of applications, it is strongly recommended that the performance of the part to be evaluated is tested under actual operating conditions to ensure full compliance to all specifications.

With 3V supplies and a common mode input voltage range that extends 0.5V below V^-, the LMH664X find applications in low voltage/low power applications. Even with 3V supplies, the −3dB BW (@ A_V = +1) is typically 115MHz with a tested limit of 80MHz. Production testing guarantees that process variations with not compromise speed. High frequency response is exceptionally stable confining the typical −3dB BW over the industrial temperature range to ±2.5%.

As can be seen from the typical performance plots, the LMH664X output current capability (~75mA) is enhanced compared to AD805X. This enhancement, increases the output load range, adding to the LMH664X's versatility.

Because of the LMH664X's high output current capability attention should be given to device junction temperature in order not to exceed the Absolute Maximum Rating.

This device family was designed to avoid output phase reversal. With input overdrive, the output is kept near supply rail (or as closed to it as mandated by the closed loop gain setting and the input voltage). See Figure 60:

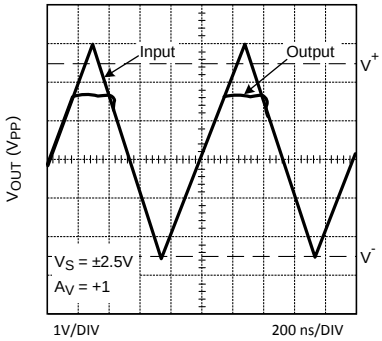


Figure 60. Input and Output Shown with CMVR Exceeded

However, if the input voltage range of −0.5V to 1V from V^+ is exceeded by more than a diode drop, the internal ESD protection diodes will start to conduct. The current in the diodes should be kept at or below 10mA.

Output overdrive recovery time is less than 100ns as can be seen from Figure 61 plot:

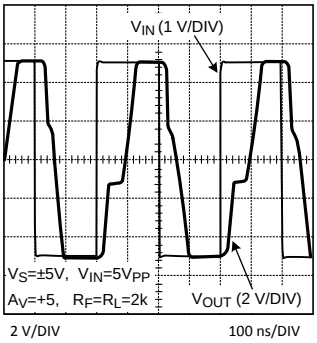


Figure 61. Overload Recovery Waveform

INPUT AND OUTPUT TOPOLOGY

All input / output pins are protected against excessive voltages by ESD diodes connected to V^+ and V^-rails (see Figure 62). These diodes start conducting when the input / output pin voltage approaches $1V_{be}$ beyond V^+ or V^- to protect against over voltage. These diodes are normally reverse biased. Further protection of the inputs is provided by the two resistors (R in Figure 62), in conjunction with the string of anti-parallel diodes connected between both bases of the input stage. The combination of these resistors and diodes reduces excessive differential input voltages approaching $2V_{be}$. The most common situation when this occurs is when the device is used as a comparator (or with little or no feedback) and the device inputs no longer follow each other. In such a case, the diodes may conduct. As a consequence, input current increases and the differential input voltage is clamped. It is important to make sure that the subsequent current flow through the device input pins does not violate the Absolute Maximum Ratings of the device. To limit the current through this protection circuit, extra series resistors can be placed. Together with the built-in series resistors of several hundred ohms, these external resistors can limit the input current to a safe number (i.e. < 10mA). Be aware that these input series resistors may impact the switching speed of the device and could slow down the device.

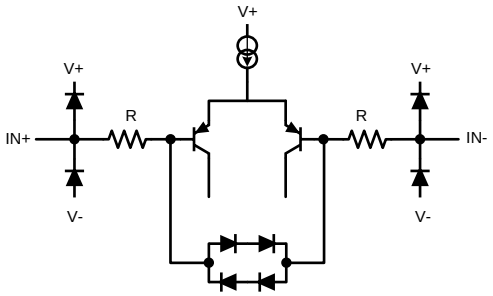


Figure 62. Input Equivalent Circuit

SINGLE SUPPLY, LOW POWER PHOTODIODE AMPLIFIER

The circuit shown in Figure 63 is used to amplify the current from a photodiode into a voltage output. In this circuit, the emphasis is on achieving high bandwidth and the transimpedance gain setting is kept relatively low. Because of its high slew rate limit and high speed, the LMH664X family lends itself well to such an application.

This circuit achieves approximately 1V/mA of transimpedance gain and capable of handling up to $1mA_{pp}$ from the photodiode. Q1, in a common base configuration, isolates the high capacitance of the photodiode (C_d) from the Op Amp input in order to maximize speed. Input is AC coupled through C1 to ease biasing and allow single supply operation. With 5V single supply, the device input/output is shifted to near half supply using a voltage divider from V_{CC}. Note that Q1 collector does not have any voltage swing and the Miller effect is minimized. D1, tied to Q1 base, is for temperature compensation of Q1's bias point. Q1 collector current was set to be large enough to handle the peak-to-peak photodiode excitation and not too large to shift the U1 output too far from mid-supply.

No matter how low an R_f is selected, there is a need for C_f in order to stabilize the circuit. The reason for this is that the Op Amp input capacitance and Q1 equivalent collector capacitance together (C_{IN}) will cause additional phase shift to the signal fed back to the inverting node. C_f will function as a zero in the feedback path counter-acting the effect of the C_{IN} and acting to stabilized the circuit. By proper selection of C_f such that the Op Amp open loop gain is equal to the inverse of the feedback factor at that frequency, the response is optimized with a theoretical 45° phase margin.

$$C_F = \sim \text{SQRT}\left[(C_{IN})/(2\pi \cdot GBWP \cdot R_F)\right] \quad (1)$$

where GBWP is the Gain Bandwidth Product of the Op Amp

Optimized as such, the I-V converter will have a theoretical pole, f_p, at:

$$f_P = \text{SQRT}\left[GBWP/(2\pi R_F \cdot C_{IN})\right] \quad (2)$$

With Op Amp input capacitance of 3pF and an estimate for Q1 output capacitance of about 3pF as well, C_{IN} = 6pF. From the typical performance plots, LMH6642/6643 family GBWP is approximately 57MHz. Therefore, with R_f = 1k, from Equation 1 and Equation 2 above.

C_f = ~4.1pF and f_p = 39MHz

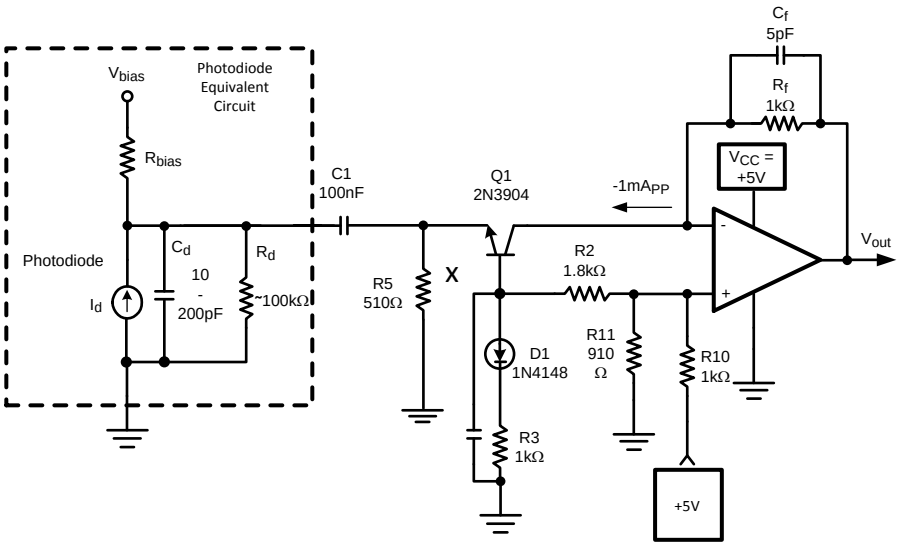


Figure 63. Single Supply Photodiode I-V Converter

For this example, optimum C_f was empirically determined to be around 5pF. This time domain response is shown in Figure 64 below showing about 9ns rise/fall times, corresponding to about 39MHz for f_p. The overall supply current from the +5V supply is around 5mA with no load.

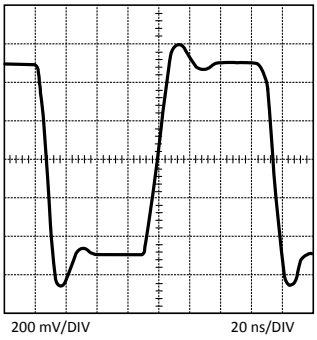


Figure 64. Converter Step Response ($1V_{PP}$, 20 ns/DIV)

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SECTION

Generally, a good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 for more information). Texas Instruments suggests the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization:

Device	Package	Evaluation Board PN
LMH6642MF	5-Pin SOT-23	LMH730216
LMH6642MA	8-Pin SOIC	LMH730227
LMH6643MA	8-Pin SOIC	LMH730036
LMH6643MM	8-Pin VSSOP	LMH730123
LMH6644MA	14-Pin SOIC	LMH730231
LMH6644MT	14-Pin TSSOP	LMH730131

Another important parameter in working with high speed/high performance amplifiers, is the component values selection. Choosing external resistors that are large in value will effect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These capacitors could be inherent to the device or a by-product of the board layout and component placement. Either way, keeping the resistor values lower, will diminish this interaction to a large extent. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation.

REVISION HISTORY

Changes from Revision O (March 2013) to Revision P	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6642MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA	Samples
LMH6642MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 42MA	Samples
LMH6642MF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A64A	
LMH6642MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A64A	Samples
LMH6642MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A64A	Samples
LMH6643MA	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMH66 43MA	
LMH6643MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA	Samples
LMH6643MAX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMH66 43MA	
LMH6643MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 43MA	Samples
LMH6643MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	A65A	
LMH6643MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A65A	Samples
LMH6643MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A65A	Samples
LMH6644MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA	Samples
LMH6644MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	SN | CU SN	Level-1-260C-UNLIM	-40 to 85	LMH6644MA	Samples
LMH6644MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT	Samples
LMH6644MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMH66 44MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

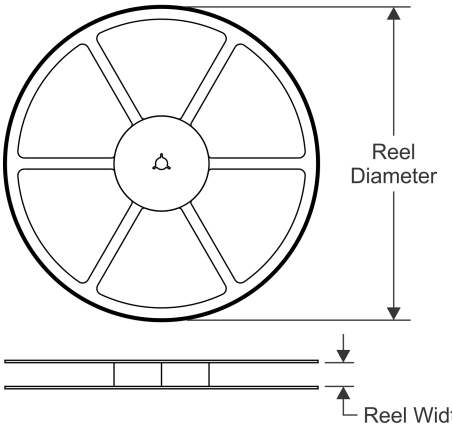
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

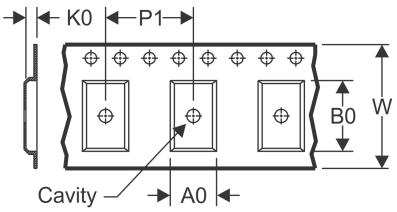
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

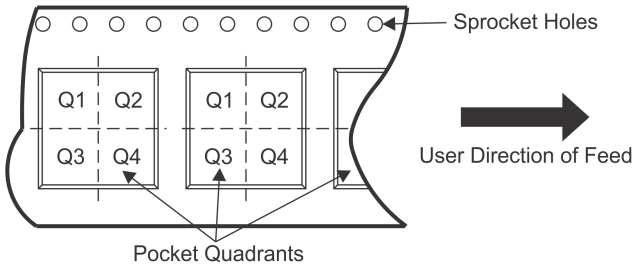


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

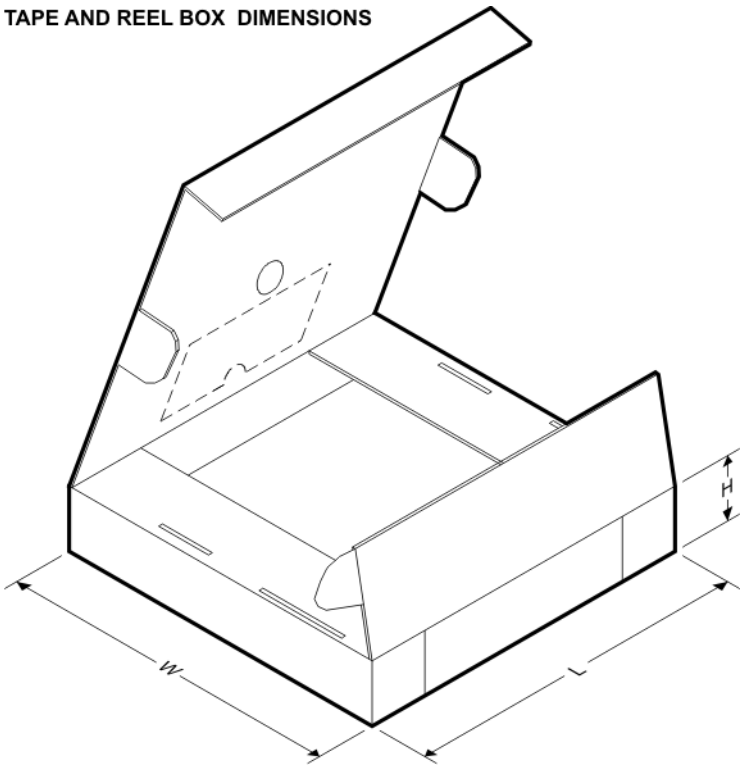
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6642MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6642MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6642MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6643MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6643MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6644MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMH6644MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1

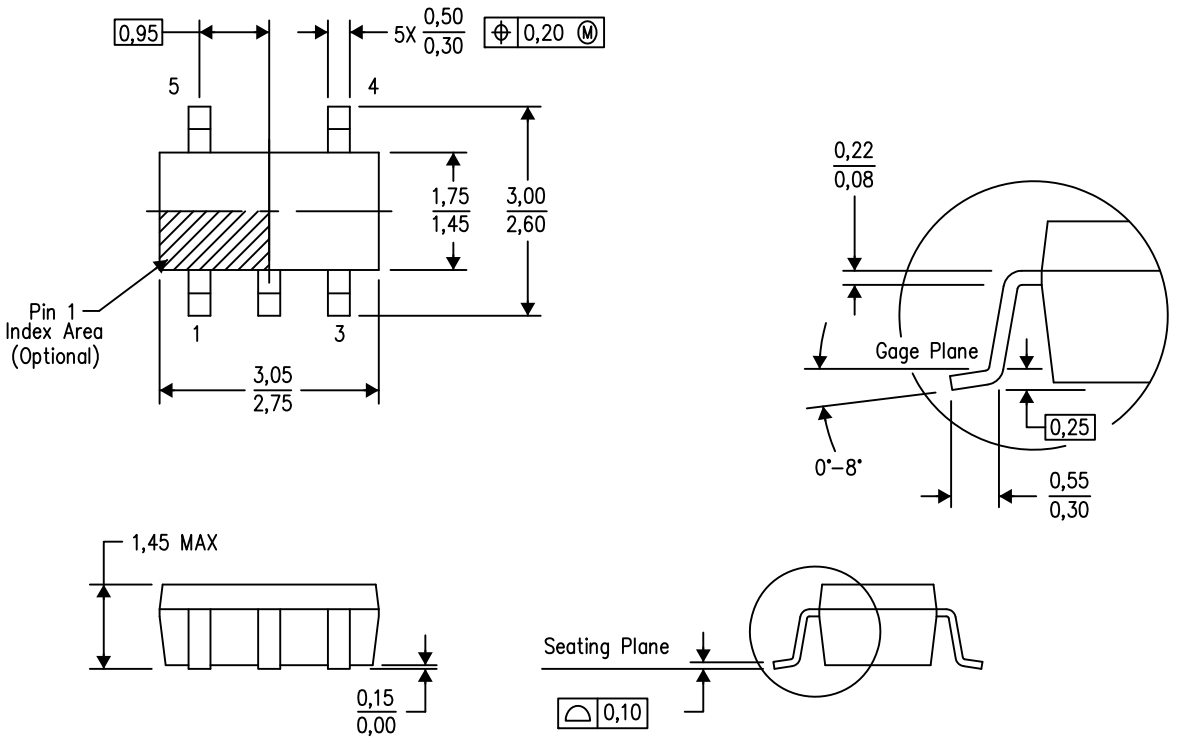
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6642MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6642MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6642MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6642MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6643MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMH6643MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6644MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMH6644MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

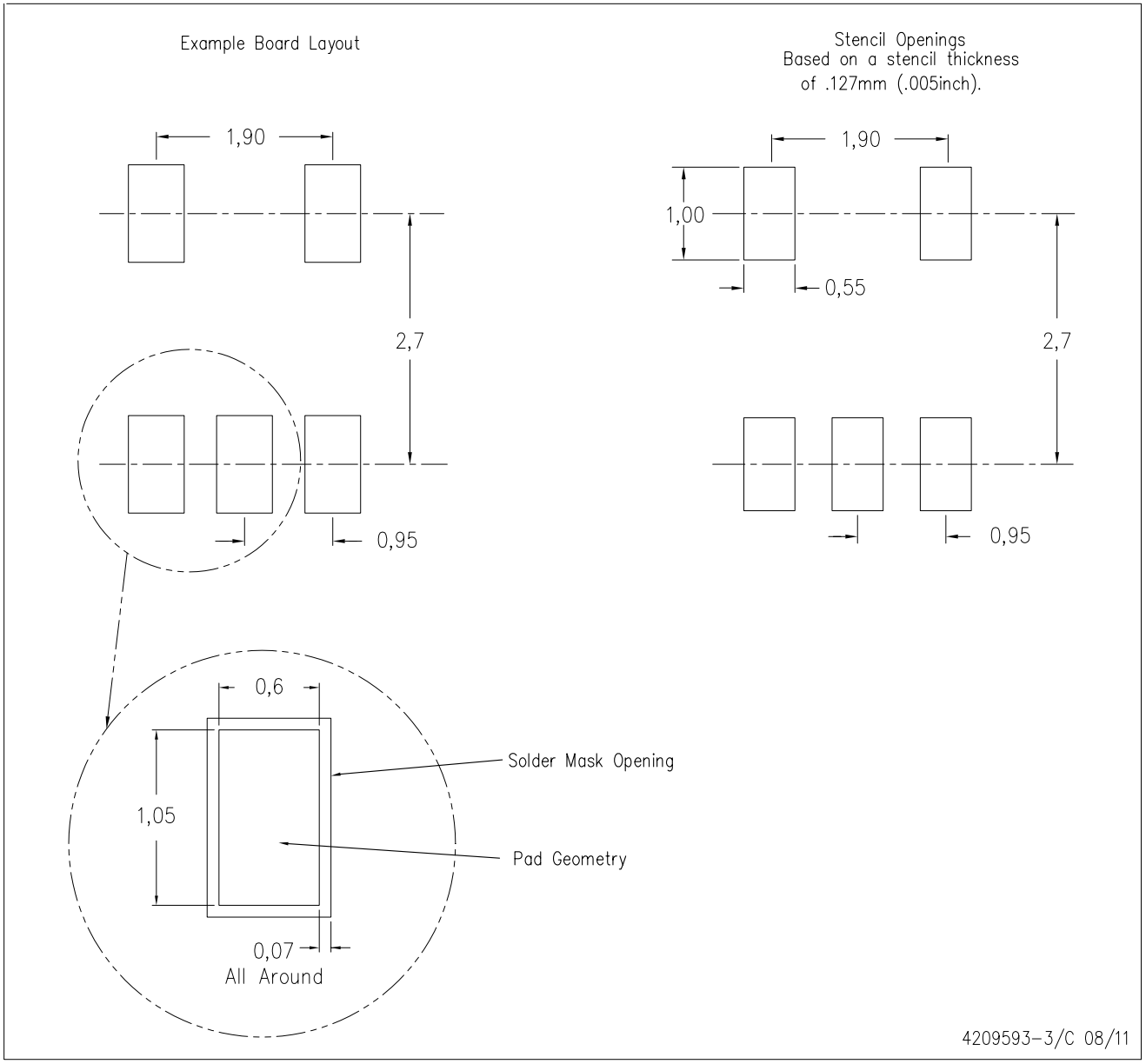
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

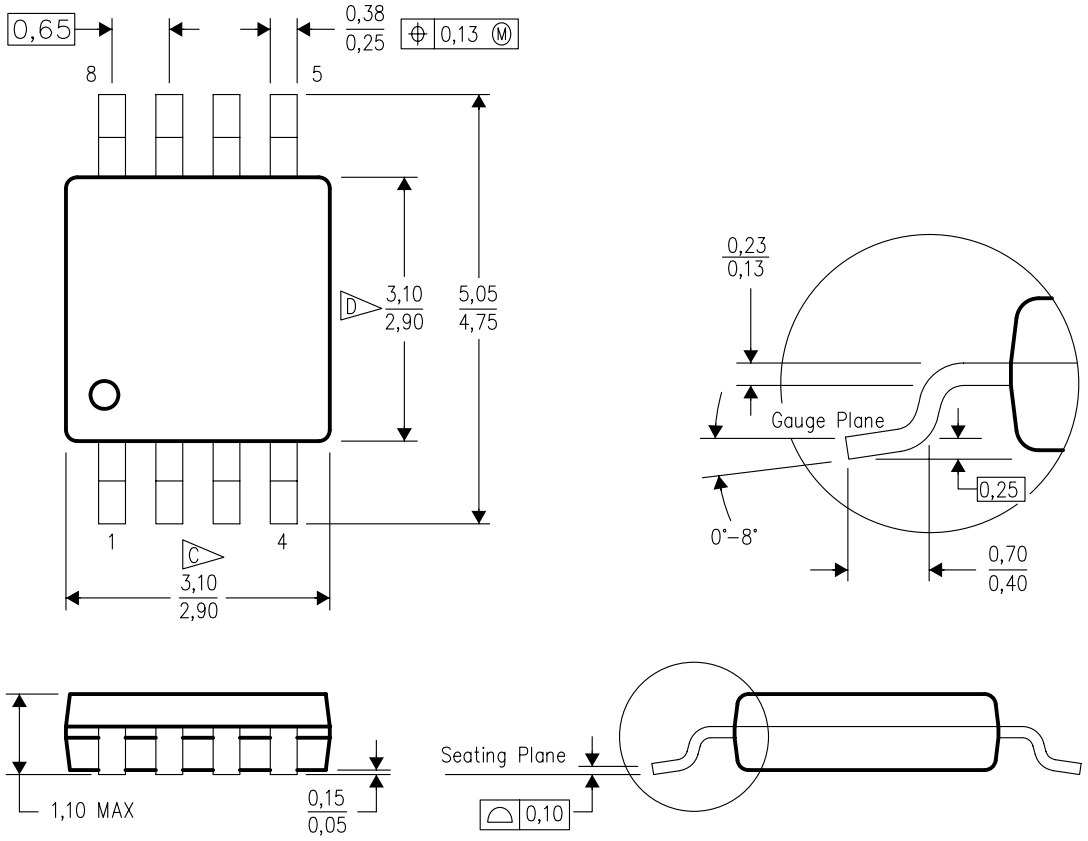
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

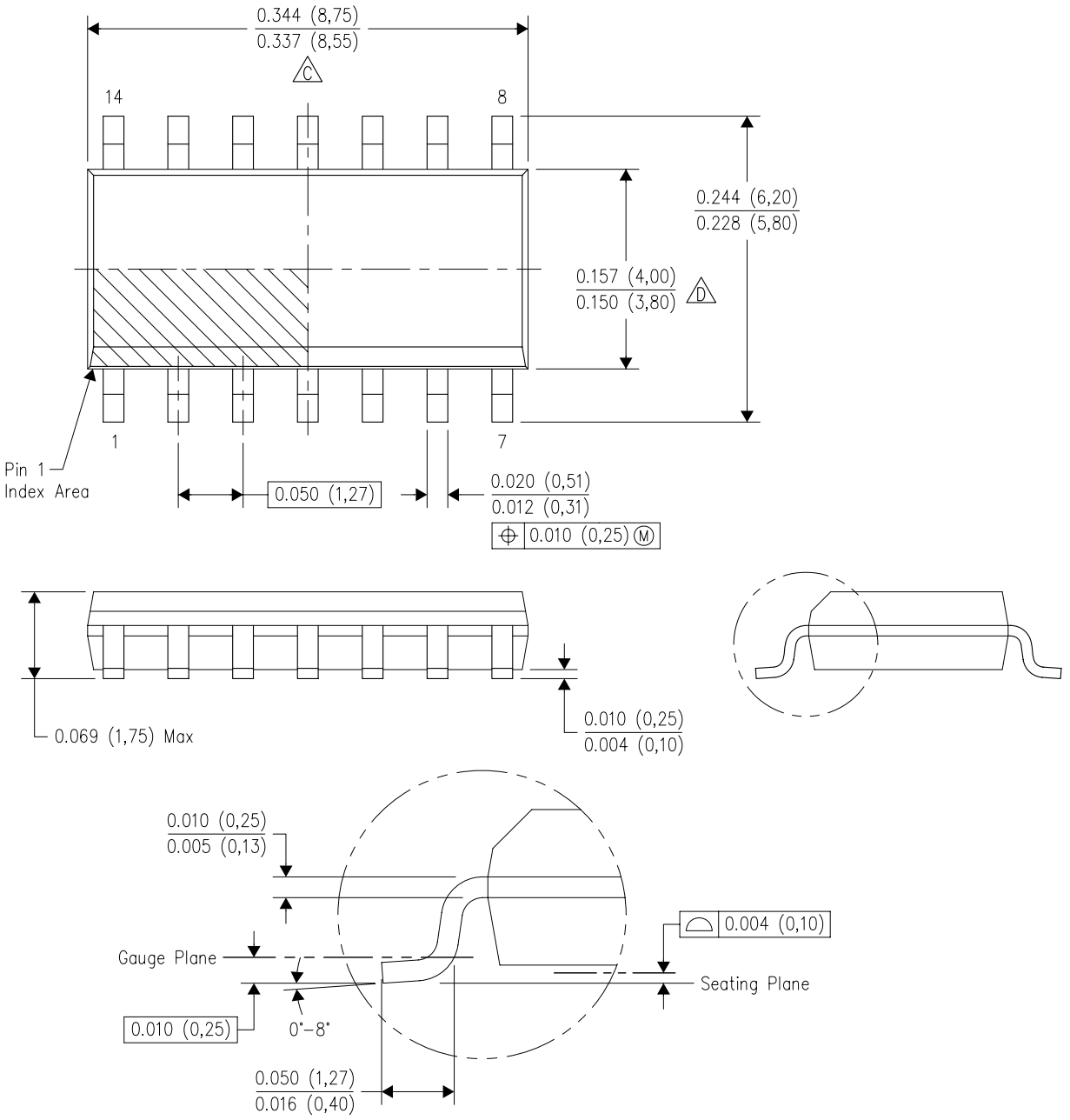
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

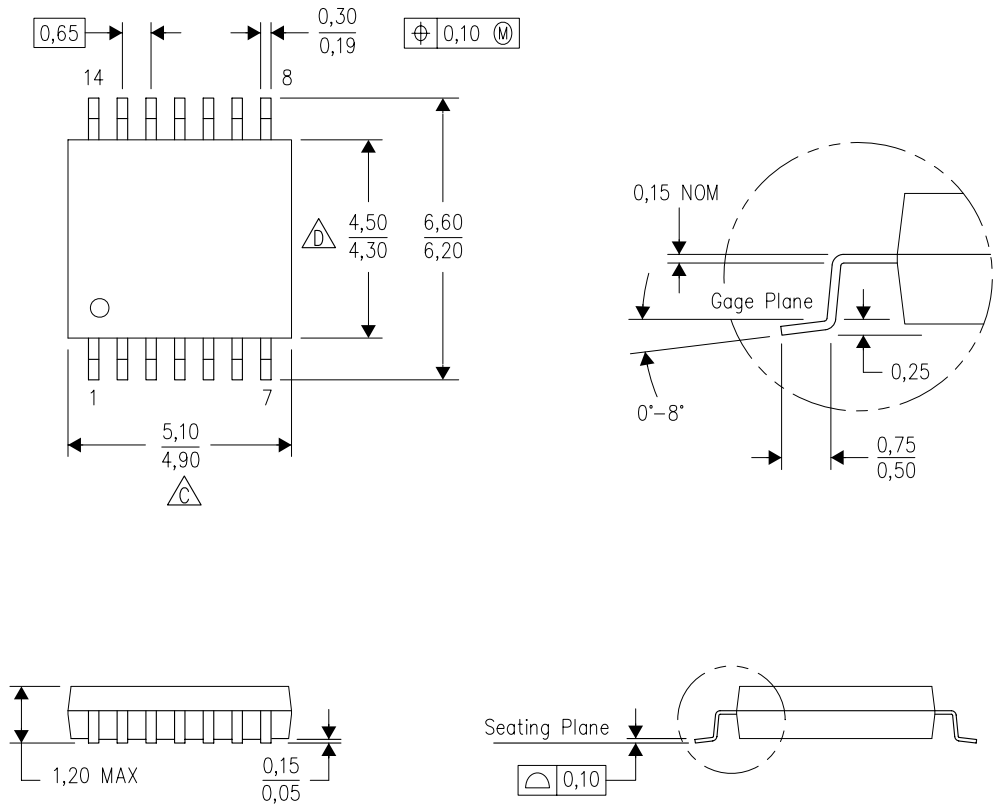
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

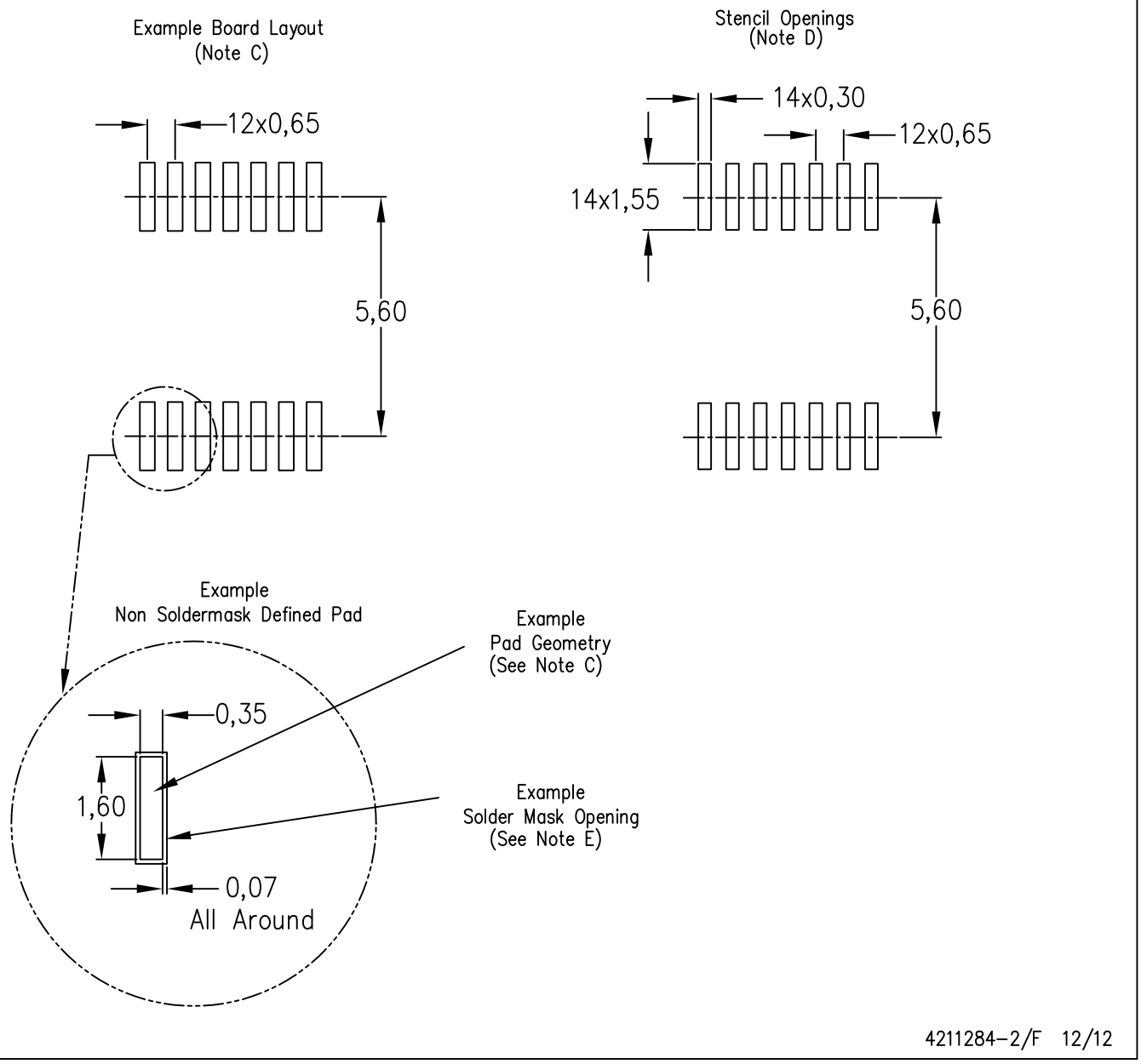
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

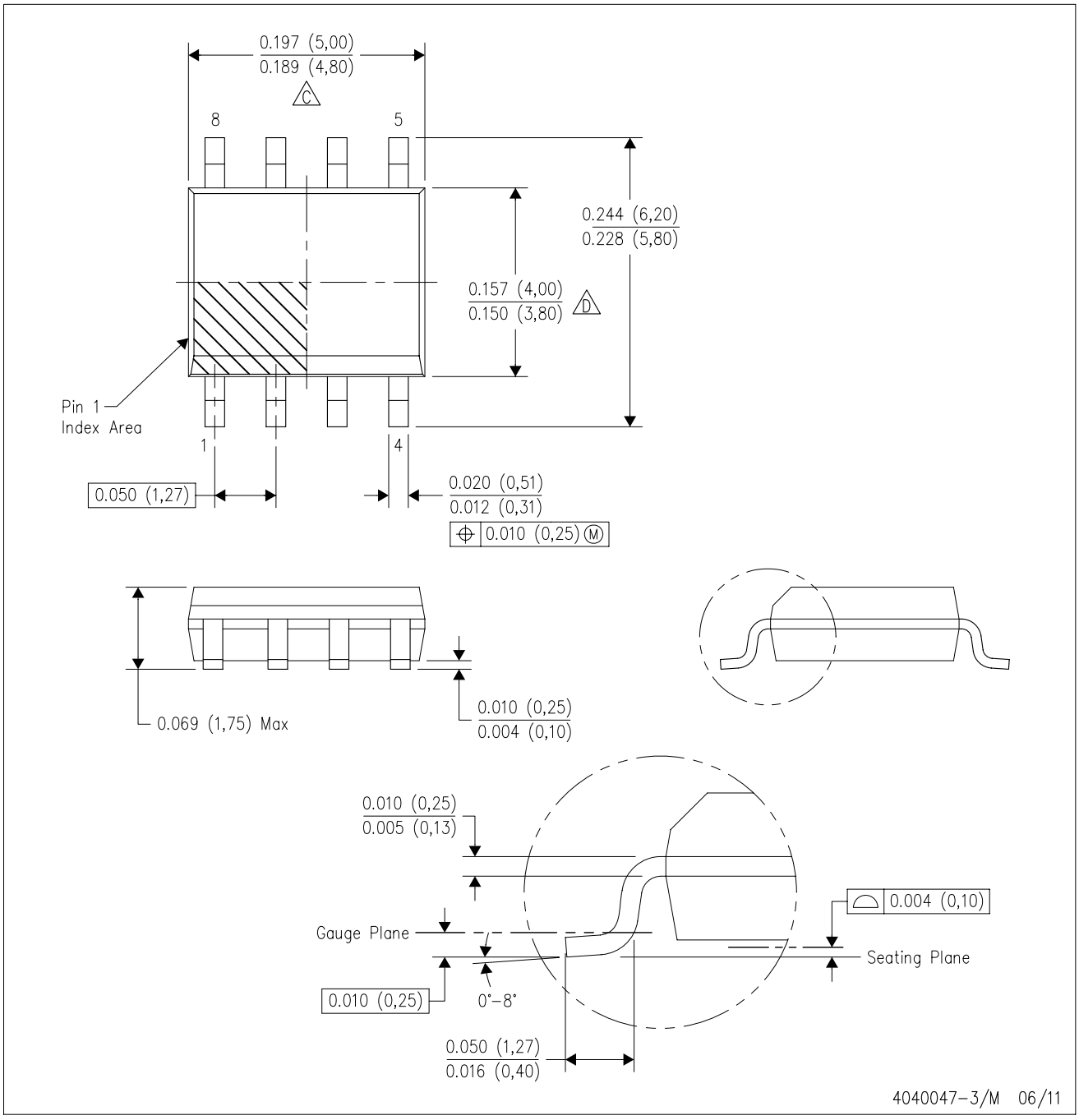
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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