LMH0303 3-Gbps HD/SD SDI Cable Driver With Cable Detect

1 Features

- Supports ST 424 (3G), 292 (HD), and 259 (SD)
- Data Rates up to 2.97 Gbps
- Supports DVB-ASI at 270 Mbps
- Cable Detect on Output
- Loss of Signal Detect at Input
- Output Driver Power-Down Control
- Typical Power Consumption: 130 mW in SD Mode and 155 mW in HD Mode
- Typical Power Consumption of the Power-Save Mode: 4 mW
- Single 3.3-V Supply Operation
- 75-Ω Single-Ended Outputs
- 100-Ω Differential Input
- Selectable Slew Rate
- Industrial Temperature Range: −40°C to 85°C
- 16-Pin WQFN Package
- Footprint Compatible With the LMH0302

2 Applications

- ST 424, ST 292, ST 344, and ST 259 Serial Digital Interfaces
- Digital Video Routers and Switches
- Distribution Amplifiers

3 Description

The LMH0303 device is designed for use in ST 424, ST 292, ST 344, and ST 259 serial digital video applications. The LMH0303 drives 75-Ω transmission lines (Belden 1694A, Belden 8281, or equivalent) at data rates up to 2.97 Gbps.

The LMH0303 includes intelligent sensing capabilities to improve system diagnostics. The cable detect feature senses near-end termination to determine if a cable is correctly attached to the output BNC. Input loss of signal (LOS) detects the presence of a valid signal at the input of the cable driver. These sensing features may be used to alert the user of a system fault and activate a deep power-save mode, reducing the power consumption of the cable driver to 4 mW. These features are accessible through an SMBus interface.

The LMH0303 provides two selectable slew rates for ST 259 and ST 424 or 292. The output amplitude is adjustable ±10% in 5-mV steps through the SMBus.

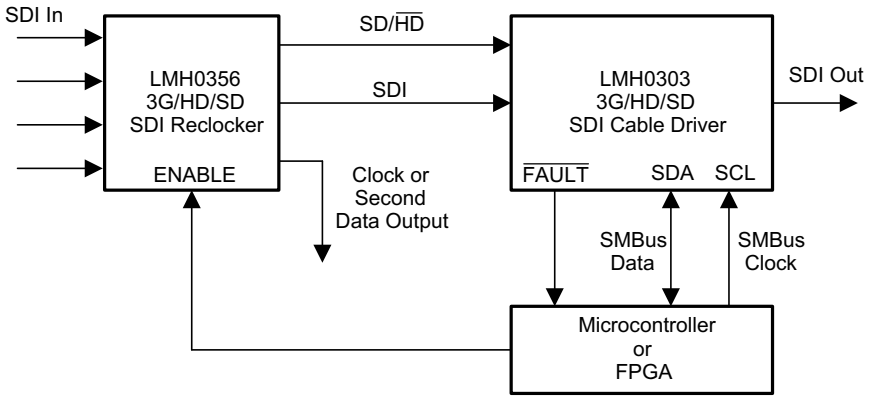
The LMH0303 is powered from a single 3.3-V supply. Power consumption is typically 130 mW in SD mode and 155 mW in HD mode. The LMH0303 is available in a 16-pin WQFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH0303	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2013) to Revision H **Page**

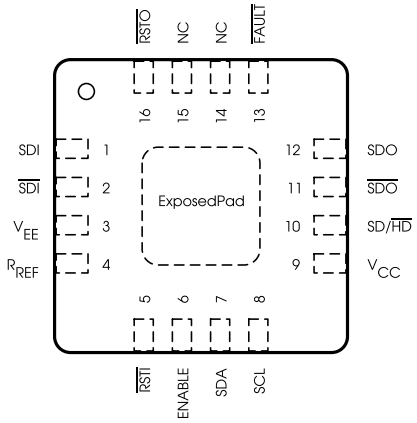
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision F (April 2013) to Revision G **Page**

- Changed layout of National Data Sheet to TI format ... 15

5 Pin Configuration and Functions

RUM Package
16-Pin WQFN
Top View



Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	SDI	I	Serial data true input.
2	$\overline{SDI}$	I	Serial data complement input.
3	V_{EE}	I	Negative power supply (ground)
4	R_{REF}	I	Bias resistor. Connect a 750-Ω resistor to V_{CC}.
5	$\overline{RSTI}$	I	Reset input. $\overline{RSTI}$ has an internal pullup, LVCMOS, 2-state logic. H = Normal operation. L = Device reset. The device operates with default register settings. Forcing $\overline{RSTI}$ low also forces $\overline{RSTO}$ low.
6	ENABLE	I	Output driver enable, LVCMOS, 2-state logic. ENABLE has an internal pullup. H = Normal operation. L = Output driver powered off.
7	SDA	I/O	SMBus bidirectional data pin, LVCMOS, 2-state logic, open drain. When functioning as an output, it is open drain. This pin requires an external pullup.
8	SCL	I	SMBus clock input, LVCMOS, 2-state logic, open drain. SCL is input only. This pin requires an external pullup.
9	V_{CC}	P	Positive power supply (3.3 V)
10	SD/$\overline{HD}$	I	Output slew rate control, LVCMOS, 2-state logic. SD/$\overline{HD}$ has an internal pulldown. H = Output rise or fall time complies with ST 259. L = Output rise or fall time complies with ST 424 or 292.
11	$\overline{SDO}$	O	Serial data complement output.

(1) G = Ground, I = Input, O = Output, and P = Power

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
12	SDO	O	Serial data true output.
13	$\overline{\text{FAULT}}$	O	Fault open drain output flag, LVCMOS, 2-state logic, open drain. Requires external pullup resistor and may be wire ORed with multiple cable drivers. H = Normal operation. L = Loss of signal or termination fault for any output.
14	NC	—	No connect. Not bonded internally.
15	NC	—	No connect. Not bonded internally.
16	$\overline{\text{RSTO}}$	O	Reset output, LVCMOS, 2-state logic. $\overline{\text{RSTO}}$ is automatically set to 1 when register 0 is written. It can be reset back to zero by forcing $\overline{\text{RSTI}}$ to zero to reset the device. Used to daisy chain multiple cable drivers on the same SMBus.
—	EP	G	EP is the exposed pad at the bottom of the WQFN package. The exposed pad must be connected to the ground plane through a via array.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage	–0.5	3.6	V
Input voltage (all inputs)	–0.3	V_{CC} + 0.3	V
Output current		28	mA
Lead temperature (soldering, 4 s)		260	°C
Junction temperature		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	
		Machine model (MM)	±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±8000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V_{CC} – V_{EE})	3.13	3.3	3.46	V
Operating junction temperature			100	°C
Operating free air temperature, T_A	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH0303 RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics – DC

Over supply voltage and operating temperature ranges (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CMIN}	Input common mode voltage	SDI, $\overline{SDI}$	1.6 + V_{SDI}/2		V_{CC} – V_{SDI}/2	V
V_{SDI}	Input voltage swing	Differential (SDI, $\overline{SDI}$)	100		2200	mV_{P-P}
V_{CMOUT}	Output common mode voltage	SDO, $\overline{SDO}$		V_{CC} – V_{SDO}		V
V_{SDO}	Output voltage swing (SDO, $\overline{SDO}$)	Single-ended, 75-Ω load, R_{REF} = 750 Ω 1%	720	800	880	mV_{P-P}
V_{IH}	Input voltage high level	SD/$\overline{HD}$, ENABLE	2			V
V_{IL}	Input voltage low level	SD/$\overline{HD}$, ENABLE			0.8	V
I_{CC}	Supply current	SD/$\overline{HD}$ = 0, SDO/$\overline{SDO}$ enabled		47	57	mA
		SD/$\overline{HD}$ = 1, SDO/$\overline{SDO}$ enabled		40	47	
		SDO/$\overline{SDO}$ disabled		1.3	2.5	
SMBUS DC SPECIFICATIONS						
V_{SIL}	Data, clock input low voltage				0.8	V
V_{SIH}	Data, clock input high voltage		2.1		V_{SDD}	V
$I_{SPULLUP}$	Current through pullup resistor or current source	V_{OL} = 0.4 V	4			mA
V_{SDD}	Nominal bus voltage		3		3.6	V
I_{SLEAKB}	Input leakage per bus segment(3)		–200		200	µA
I_{SLEAKP}	Input leakage per pin		–10		10	µA
C_{SI}	Capacitance for SDA and SCL(3)(4)				10	pF

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 V.
(2) Typical values are stated for V_{CC} = 3.3 V and T_A = 25°C.
(3) Recommended value — Parameter not tested.
(4) Recommended maximum capacitive load per bus segment is 400 pF.

6.6 Electrical Characteristics – AC

Over supply voltage and operating temperature ranges (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR_{SDI}	Input data rate				2970	Mbps
T_{jit}	Additive output jitter	2.97 Gbps		20		ps_{P-P}
		1.485 Gbps		18		
		270 Mbps		15		
t_r,t_f	Output rise time and fall time	SD/$\overline{HD}$ = 0, 20% to 80%		90	130	ps
		SD/$\overline{HD}$ = 1, 20% to 80%	400		800	
T_{MATCH}	Mismatch in rise or fall time	SD/$\overline{HD}$ = 0			30	ps
		SD/$\overline{HD}$ = 1			50	
T_{DCD}	Duty cycle distortion	SD/$\overline{HD}$ = 0, 2.97 Gbps(2)			27	ps
		SD/$\overline{HD}$ = 0, 1.485 Gbps(2)			30	
		SD/$\overline{HD}$ = 1(2)			100	
T_{OS}	Output overshoot	SD/$\overline{HD}$ = 0(2)			10%	
		SD/$\overline{HD}$ = 1(2)			8%	
RL_{SDO}	Output return loss	5 MHz to 1.5 GHz(3)	15			dB
		1.5 GHz to 3 GHz(3)	10			

(1) Typical values are stated for V_{CC} = 3.3 V and T_A = 25°C.
(2) Specification is ensured by characterization.
(3) Output return loss is dependent on board design. The LMH0303 meets this specification on the SD303EVK evaluation board.

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
f_{SMB}	Bus operating frequency	10		100	kHz
t_{BUF}	Bus free time between stop and start condition	4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated; at $I_{SPULLUP}$ = MAX	4			µs
$t_{SU:STA}$	Repeated start condition setup time	4.7			µs
$t_{SU:STO}$	Stop condition setup time	4			µs
$t_{HD:DAT}$	Data hold time	300			ns
$t_{SU:DAT}$	Data setup time	250			ns
t_{LOW}	Clock low period	4.7			µs
t_{HIGH}	Clock high period	4		50	µs
t_F	Clock or data fall time			300	ns
t_R	Clock or data rise time			1000	ns
t_{POR}	Time in which device must be operational after power on			500	ms

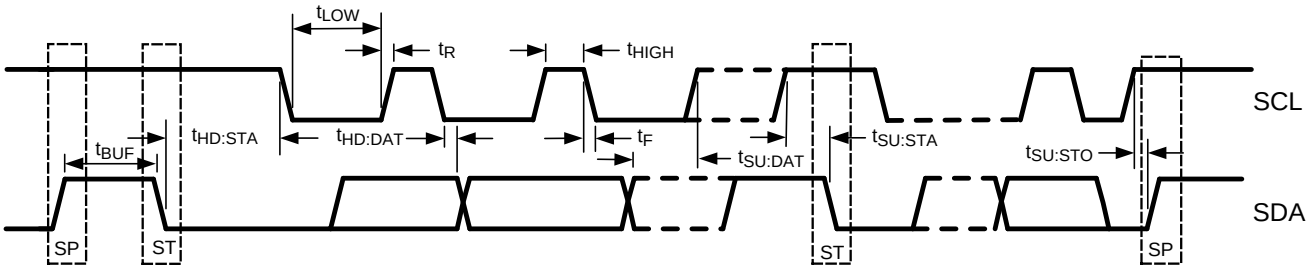


Figure 1. SMBus Timing Parameters

6.8 Typical Characteristics

Typical device characteristics at T_A = 25°C and V_{CC} = 3.3 V (unless otherwise noted)

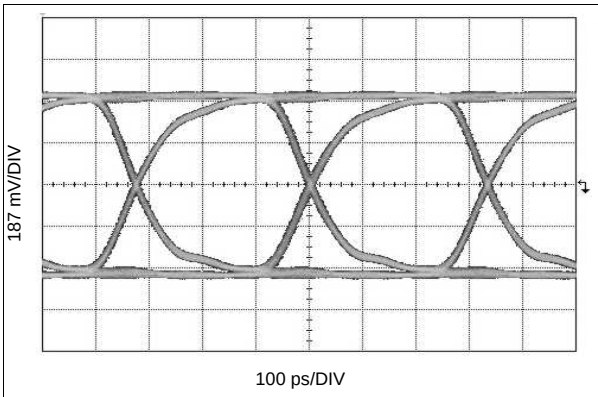


Figure 2. SDO PRBS10 at 2.97 Gbps

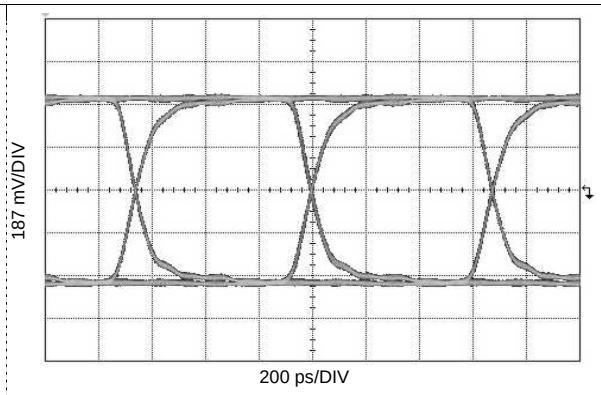


Figure 3. SDO PRBS10 at 1.485 Gbps

7 Detailed Description

7.1 Overview

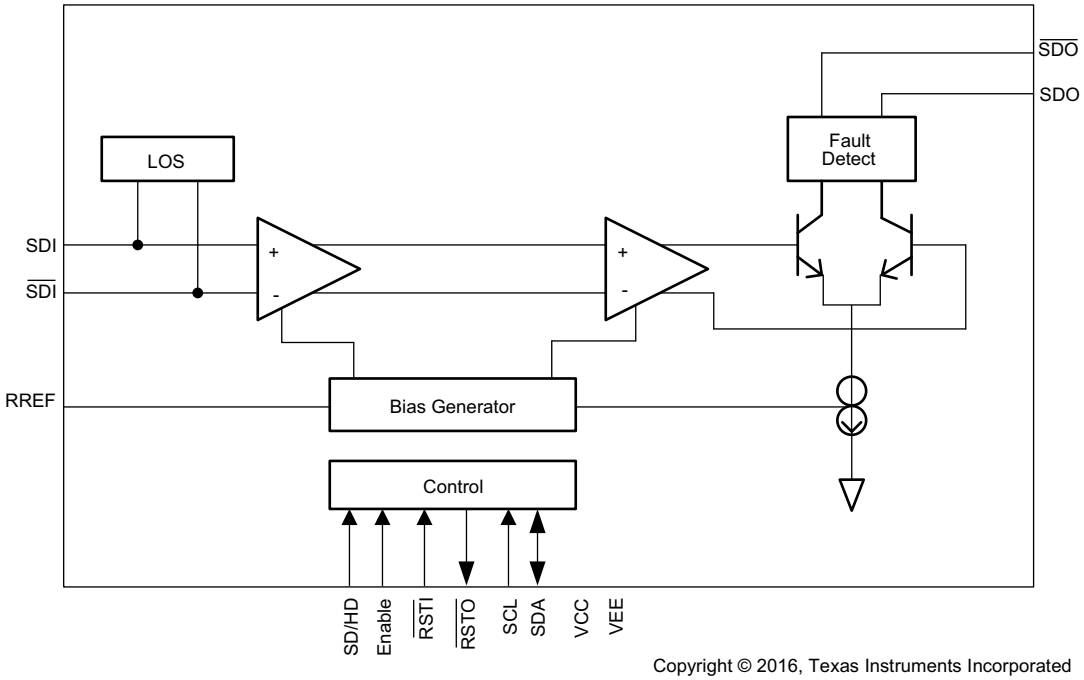
The LMH0303 ST 424, ST292, ST259 serial digital cable driver is a monolithic, high-speed cable driver designed for use in serial digital video data transmission applications. The LMH0303 drives 75-Ω transmission lines (Belden 8281, 1694A, Canare L-5CFB, or equivalent) at data rates up to 2.97 Gbps.

The LMH0303 provides two selectable slew rates for ST 259 and ST 292/424 compliance. The output voltage swing is adjustable through a single external resistor (R_{REF}) or SMBus interface in 5-mV steps.

The LMH0303 cable detect feature senses near-end termination to determine if a cable is attached to the output BNC. The LMH0303 input loss of signal (LOS) detects the presence of a valid signal at the 100-Ω differential input of the cable driver. These features can be used to activate power-save mode. These features are accessible through an SMBus interface.

The LMH0303 is powered from a single 3.3 V supply. Power consumption is typically 130 mW in SD mode and 155 mW in HD mode. The LMH0303 is available in a 16-pin WQFN package.

7.2 Functional Block Diagram



7.3 Feature Description

The LMH0303 data path consists of several key blocks as shown in the *Functional Block Diagram*. These key circuits are:

- Loss-of-signal detector
- Input interfacing
- Output interfacing
- Output slew rate control
- Cable fault detection
- SMBus configuration

Feature Description (continued)

7.3.1 Loss-of-Signal Detector

The LMH0303 detects when the input signal does not have a video-like pattern. Self-oscillation and low levels of noise are rejected. This loss-of-signal detector allows a very sensitive input stage that is robust against coupled noise without any degradation of jitter performance. Through the SMBus, the loss-of-signal detector can either add an input offset or mute the outputs. An offset is added by default. Additionally, the loss-of-signal detector can be linked to the ENABLE functionality so that when the LOS goes low, ENABLE also goes low.

7.3.2 Input Interfacing

The LMH0303 accepts either differential or single-ended input. For single-ended operation, the unused input must be properly terminated.

7.3.3 Output Interfacing

The LMH0303 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75-Ω AC-coupled coaxial cable with an R_{REF} resistor value of 750 Ω. The R_{REF} resistor is connected between the R_{REF} pin and V_{CC}.

The R_{REF} resistor should be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network should be removed to minimize parasitic capacitance.

7.3.4 Output Slew Rate Control

The LMH0303 output rise and fall times are selectable for either ST259 or ST 424 or 292 compliance through the SD/$\overline{HD}$ pin. For slower rise and fall times, or ST 259 compliance, SD/$\overline{HD}$ is set high. For faster rise and fall times, or ST 424 and ST 292 compliance, SD/$\overline{HD}$ is set low. SD/$\overline{HD}$ may also be controlled using the SMBus, provided the SD/$\overline{HD}$ pin is held low. SD/$\overline{HD}$ has an internal pulldown.

7.3.5 Cable Fault Detection

The LMH0303 termination fault detection purpose is to provide an indication when no cable is connected to the output (near end). The termination fault detection works by detecting reflections on the output. The device measures the peak-to-peak output voltage. The output amplitude is normally 800 mV_{p-p}. No termination results in 2x the output voltage (1600 mV_{p-p}) due to the 100% reflection.

When a video signal (or AC test signal) is present on SDI, the device senses the SDO and $\overline{SDO}$ amplitudes. If the output is not properly terminated (through a terminated cable or local termination), the amplitude will be higher than expected, and the termination fault signal is asserted. The termination fault signal is deasserted when the proper termination is applied. This feature allows the system designer the flexibility to react to cable attachment and removal. Note that a long length of cable will look like a proper termination at the device output. The cable driver must be enabled for the termination detection to operate. If the termination fault will be used to power down the LMH0303, then periodic polling (enabling) is recommended to monitor the output termination. For example, when a fault condition is triggered, ENABLE can be driven low to power down the device. The LMH0303 should be re-enabled periodically to check the status of the output termination. The LMH0303 must be powered on for at least 4 ms for termination fault detection to work.

7.3.6 SMBus Interface

The System Management Bus (SMBus) is a two-wire interface designed for the communication between various system component chips. By accessing the control functions of the circuit through the SMBus, pin count is kept to a minimum while allowing a maximum amount of versatility. The LMH0303 has several internal configuration registers which may be accessed through the SMBus.

The 7-bit default address for the LMH0303 is 0x17. The LSB is set to 0'b for a WRITE and 1'b for a READ, so the 8-bit default address for a WRITE is 0x2E and the 8-bit default address for a READ is 0x2F. The SMBus address may be dynamically changed.

In applications where there might be several LMH0303s, the SDA, SCL, and $\overline{FAULT}$ pins can be shared. The SCL, SDA, and $\overline{FAULT}$ pins are open drain and require external pullup resistors. Multiple LMH0303s may have the $\overline{FAULT}$ pin wire ORed. This signal becomes active when either loss of signal is detected or any termination faults are detected. The registers may be read in order to determine the cause. Additionally, each signal can be masked from the $\overline{FAULT}$ pin.

Feature Description (continued)

7.3.6.1 Transfer of Data through the SMBus

During normal operation the data on SDA must be stable during the time when SCL is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SCL is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SCL is High indicates a message STOP condition.

IDLE: If SCL and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH}, then the bus will transfer to the IDLE state.

7.3.6.2 SMBus Transactions

The device supports WRITE and READ transactions. See Table 1 for register address, type (Read/Write, Read Only), default value, and function information.

7.3.6.2.1 Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a *0* indicating a WRITE.
2. The Device (Slave) drives the ACK bit (*0*).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (*0*).
5. The Host drives the 8-bit data byte.
6. The Device drives an ACK bit (*0*).
7. The Host drives a STOP condition.

The WRITE transaction is completed, the bus goes IDLE, and communication with other SMBus devices may now occur.

7.3.6.2.2 Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host drives a START condition, the 7-bit SMBus address, and a *0* indicating a WRITE.
2. The Device (Slave) drives the ACK bit (*0*).
3. The Host drives the 8-bit Register Address.
4. The Device drives an ACK bit (*0*).
5. The Host drives a START condition.
6. The Host drives the 7-bit SMBus Address, and a *1* indicating a READ.
7. The Device drives an ACK bit *0*.
8. The Device drives the 8-bit data value (register contents).
9. The Host drives a NACK bit *1* indicating end of the READ transfer.
10. The Host drives a STOP condition.

7.3.6.3 Communicating With Multiple LMH0303 Cable Drivers through the SMBus

A common application for the LMH0303 uses multiple cable driver devices. Even though the LMH0303 devices all have the same default SMBus device ID (address), it is still possible for them share the SMBus signals as shown in Figure 4. A third signal is required from the host to the first device. This signal acts as a *Enable* or *Reset* signal. Additional LMH0303s are controlled from the upstream device. In this control scheme, multiple LMH0303s may be controlled through the two-wire SMBus and the use of one General Purpose Output (GPO) signal. Other SMBus devices may also be connected to the two wires, assuming they have their own unique SMBus addresses.

Feature Description (continued)

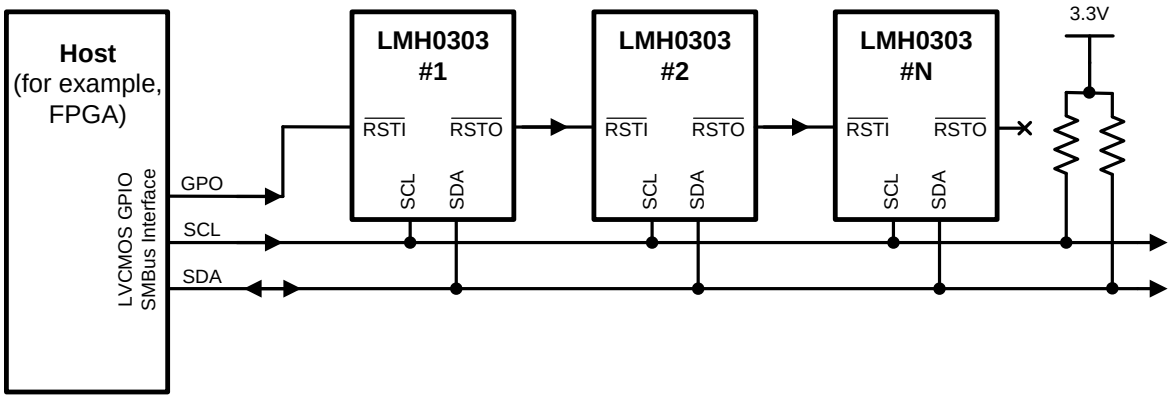


Figure 4. SMBus Configuration for Multiple LMH0303 Cable Drivers

The $\overline{\text{RSTI}}$ pin of the first device is controlled by the system with a GPO pin from the host. The first LMH0303 $\overline{\text{RSTO}}$ pin is then daisy chained to the next device's $\overline{\text{RSTI}}$ pin. That device's $\overline{\text{RSTO}}$ pin is connected to the next device and so on.

The procedure at initialization is to:

1. Hold the host GPO pin Low in RESET, to the first device. $\overline{\text{RSTO}}$ output default is also Low which holds the next device in RESET in the chain.
2. Raise the host GPO signal to LMH0303 #1 $\overline{\text{RSTI}}$ input pin.
3. Write to Address 0x2E Register 0 with the new address value (for example 0x2C).
4. Upon writing Register 0 in LMH0303 #1, its $\overline{\text{RSTO}}$ signal will switch High. Its new address is 0x2C, and the next LMH0303 in the chain will now respond to the default address of 0x2E.
5. The process is repeated until all LMH0303 devices have a unique address loaded.
6. Direct SMBus writes and reads may now take place between the host and any addressed device.

The 7-bit address field allows for 128 unique addresses. The above procedure allows for the reprogramming of the LMH0303 devices such that multiple devices may share the two-wire SMBus. Make sure all devices on the bus have unique device IDs.

If power is toggled to the system, the SMBus address routine needs to be repeated.

7.4 Device Functional Modes

The LMH0303 features can be controlled through the pin or SMBus interface. *SMBus Interface* describes detailed operation using SMBus interface.

7.5 Register Maps

Table 1 lists the SMBus registers of the LMH0303 device.

Table 1. SMBus Registers

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
0x00	R/W	ID	7:1	DEVID	0010111	Device ID. Writing this register will force the $\overline{\text{RSTO}}$ pin high. Further access to the device must use this 7-bit address.
			0	RSVD	0	Reserved as 0. Always write 0 to this bit.
0x01	R	STATUS	7:3	RSVD	00000	Reserved.
			2	TFN	0	Termination Fault for $\overline{\text{SDI}}$. 0: No Termination Fault Detected. 1: Termination Fault Detected.
			1	TFP	0	Termination Fault for SDI. 0: No Termination Fault Detected. 1: Termination Fault Detected.
			0	LOS	0	Loss Of Signal ($\overline{\text{LOS}}$) detect at input. 0: No Signal Detected. 1: Signal Detected.
0x02	R/W	MASK	7	SD	0	SD Rate select bit. If the SD/$\overline{\text{HD}}$ pin is set to V_{CC}, it overrides this bit. With the SD/$\overline{\text{HD}}$ pin set to ground, this bit selects the output edge rate as follows: 0: HD edge rate. 1: SD edge rate.
			6	RSVD	0	Reserved as 0. Always write 0 to this bit.
			5	PD	0	Power Down for SDO output stage. If the ENABLE pin is set to ground, it overrides this bit. With the ENABLE pin set to V_{CC}, PD functions as follows: 0: SDO active. 1: SDO powered down.
			4:3	RSVD	00	Reserved as 00. Always write 00 to these bits.
			2	MTFN	0	Mask TFN from affecting $\overline{\text{FAULT}}$ pin. 0: TFN=1 will cause $\overline{\text{FAULT}}$ to be 0. 1: TFN=1 will not affect $\overline{\text{FAULT}}$; the condition is masked off.
			1	MTFP	0	Mask TFP from affecting $\overline{\text{FAULT}}$ pin. 0: TFP=1 will cause $\overline{\text{FAULT}}$ to be 0. 1: TFP=1 will not affect $\overline{\text{FAULT}}$; the condition is masked off.
			0	MLOS	0	Mask $\overline{\text{LOS}}$ from affecting $\overline{\text{FAULT}}$ pin. 0: $\overline{\text{LOS}}$=0 will cause $\overline{\text{FAULT}}$ to be 0. 1: $\overline{\text{LOS}}$=0 will not affect $\overline{\text{FAULT}}$; the condition is masked off.

Register Maps (continued)

Table 1. SMBus Registers (continued)

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
0x03	R/W	DIRECTION	7	HDTFThreshLSB	1	Least Significant Bit for HDTFThresh detection threshold. Combines with HDTFThresh bits in register 0x04.
			6	SDTFThreshLSB	1	Least Significant Bit for SDTFThresh detection threshold. Combines with SDTFThresh bits in register 0x05.
			5:3	RSVD	000	Reserved as 000. Always write 000 to these bits.
			2	DTFN	0	Direction of TFN that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: TFN=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: TFN=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off).
			1	DTFP	0	Direction of TFP that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: TFP=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: TFP=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off).
			0	DLOS	0	Direction of $\overline{\text{LOS}}$ that affects $\overline{\text{FAULT}}$ pin (when not masked). 0: $\overline{\text{LOS}}$=0 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off). 1: $\overline{\text{LOS}}$=1 will cause $\overline{\text{FAULT}}$ to be 0 (when the condition is not masked off).
0x04	R/W	OUTPUT	7:5	HDTFThresh	100	Sets the Termination Fault threshold for SDO, when SD is set to HD rates (0). Combines with HDTFThreshLSB in register 0x03 (default for combined value is 1001).
			4:0	AMP	10000	SDO output amplitude in roughly 5 mV steps.

Register Maps (continued)

Table 1. SMBus Registers (continued)

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
0x05	R/W	OUTPUTCTRL	7	RSVD	0	Reserved as 0. Always write 0 to this bit.
			6	FLOSOF	0	Force $\overline{\text{LOS}}$ to always OFF in regards to its effect on the output signal. This forces the device into either the mute or “add offset” state. The $\overline{\text{LOS}}$ bit in register 0x01 still reflects the correct state of $\overline{\text{LOS}}$. 0: $\overline{\text{LOS}}$ operates normally, muting or adding offset as specified by the MUTE bit. 1: Muting or adding offset is always in place as specified by the MUTE bit.
			5	FLOSON	0	Force $\overline{\text{LOS}}$ to always ON in regards to its effect on the output signal. This prevents the device from muting or adding offset. The $\overline{\text{LOS}}$ bit in register 0x01 still reflects the correct state of $\overline{\text{LOS}}$. 0: $\overline{\text{LOS}}$ operates normally, muting or adding offset as specified in the MUTE bit. 1: Muting or adding offset never occurs.
			4	LOSEN	0	Configures $\overline{\text{LOS}}$ to be combined with the ENABLE functionality. 0: Only the PD bit and ENABLE pin affect the power down state of the output drivers. 1: If the ENABLE pin is set to ground, it powers down the output drivers regardless of the state of $\overline{\text{LOS}}$ or the PD bit. With the ENABLE pin set to V_{CC}, $\overline{\text{LOS}}$=0 will power down the output drivers, and $\overline{\text{LOS}}$=1 will leave the power down state dependent on the PD bit.
			3	MUTE	0	Selects whether the device will MUTE when loss of signal is detected or add an offset to prevent self oscillation. When an input signal is detected ($\overline{\text{LOS}}$=1), the device will operate normally. 0: Loss of signal will force a small offset to prevent self oscillation. 1: Loss of signal will force the channel to MUTE.
			2:0	SDTFThresh	010	Sets the Termination Fault threshold for SDO, when SD is set to SD rate. Combines with SDTFThreshLSB in register 0x03 (default for combined value is 0101).
0x06	R/W	RSVD	7:0	RSVD	00000000	Reserved as 00000000. Always write 00000000 to these bits.
0x07	R/W	RSVD	7:0	RSVD	00000000	Reserved as 00000000. Always write 00000000 to these bits.
0x08	R/W	TEST	7:5	CMPCMD	000	Compare command. Determines whether the peak value or the current value of the Termination Fault counters is read in registers 0x0A and 0x0B. 000: Resets compare value to 00; registers 0x0A and 0x0B show current counter values. Sets detection to look for MAX peak values. 001: Capture counter 0. Register 0x0A shows peak value. 010: Capture counter 1. Register 0x0B shows peak value. 011, 100: Reserved. 101: Resets compare value to 0x1F. Sets detection to look for MIN peak values. 110, 111: Reserved.
			4:0	RSVD	00000	Reserved as 00000. Always write 00000 to these bits.

Register Maps (continued)

Table 1. SMBus Registers (continued)

ADDRESS	R/W	NAME	BITS	FIELD	DEFAULT	DESCRIPTION
0x09	R	REV	7:5	RSVD	000	Reserved.
			4:3	DIREV	10	Die Revision.
			2:0	PARTID	011	Part Identifier. Note that single output devices (LMH0303) have the LSB=1. Dual output devices (LMH0307) have the LSB=0.
0x0A	R	TFPCOUNT	7:5	RSVD	000	Reserved.
			4:0	TFPCOUNT	00000	This is either the current value of TFP Counter, or the peak value of the counter, depending on CMPCMD in register 0x08.
0x0B	R	TFNCOUNT	7:5	RSVD	000	Reserved.
			4:0	TFNCOUNT	00000	This is either the current value of TFN Counter, or the peak value of the counter, depending on CMPCMD in register 0x08.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH0303 is a single-channel SDI cable driver that supports different application spaces. The following sections describe the typical use cases and common implementation practices.

8.1.1 General Guidance for All Applications

The LMH0303 supports two modes of configuration: Pin control or SMBus mode. Once one of these two control mechanism is chosen, pay attention to the PCB layout for the high-speed signals (see *Layout Guidelines*). The SMPTE specifications also define the use of AC-coupling capacitors for transporting uncompressed serial data streams with heavy low-frequency content. This specification requires the use of a 4.7-µF AC-coupling capacitor to avoid low frequency DC wander. The 75-Ω signal is also required to meet certain rise and fall timing to facilitate highest eye opening for the receiving device.

SMPTE specifies the requirements for the Serial Digital Interface to transport digital video at SD, HD, 3 Gb/s, and higher data rates over coaxial cables. One of the requirements is meeting the required return loss. This requirement specifies how closely the port resembles 75-Ω impedance across a specified frequency band. Output return loss is dependent on board design. The LMH0303 supports these requirements. To gain additional return loss margin, return loss network in Figure 5 can be optimized.

8.1.2 Cable Fault Detection Operation

The termination fault detection of the LMH0303 indicates when no cable is connected to the output (near end). The termination fault detection works by detecting reflections on the output. The device measures the peak-to-peak output voltage. The output amplitude is normally 800 mV_{p-p}. No termination results in 2x the output voltage (1600 mV_{p-p}) due to the 100% reflection. At the lowest threshold settings, the LMH0303 detects fault even with the amplitude down near 800 mV_{p-p} (perfect termination). At the highest threshold settings, the LMH0303 will detect no fault even as the amplitude approaches 1600 mV_{p-p} (completely unterminated). With the default register settings (HDTFThresh = 9) and with a 3G input, the cable driver will detect the *unloaded condition* if it sees an amplitude greater than about 450 mV_{p-p} below the maximum (that is, the output amplitude, including the reflection, is about 1.15 V_{p-p}). Each step of the HD threshold register changes this decision voltage by approximately 100 mV and this can range from 50 to 200 mV. These results are dependent on the board layout and passive components.

Since the termination fault detection threshold is dependent on the PCB layout, the threshold may need to be fine tuned for each design. To help in setting the termination fault threshold, the termination fault counters (registers 0x0A and 0x0B) gauges how the cable driver is interpreting the output termination. The termination fault counter counts the termination faults seen at the LMH0303 output. It counts up or down: up one tick when a termination fault is detected, and down one tick when a proper termination is detected. The counter ranges from 0 to 31 (decimal). When there is no termination fault, the value will be near 0. When the count hits 31, the termination fault indicator is asserted. These registers can be used to fine tune the termination fault threshold setting. If there are many termination fault counts when the output is properly terminated, then the termination fault threshold should be increased. If the register is not showing consistent counts of 31 when the output is unterminated, then the termination fault threshold should be decreased.

8.2 Typical Application

Figure 5 shows the application circuit for the LMH0303.

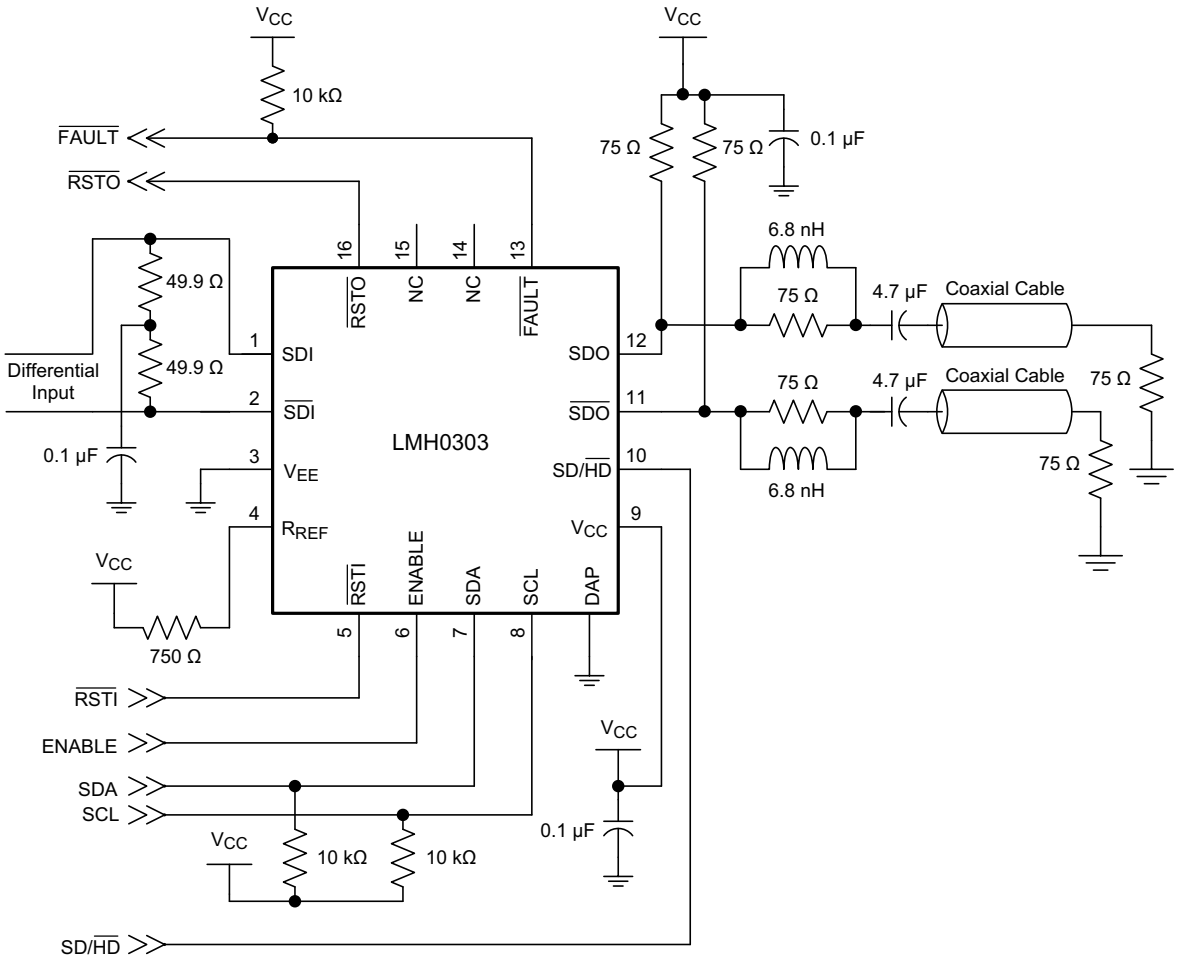


Figure 5. Application Circuit

8.2.1 Design Requirements

For the LMH0303 design example, Table 2 lists the design parameters.

Table 2. LMH0303 Design Parameters

PARAMETER	REQUIREMENT
Input termination	Required, 49.9 Ω are recommended (see Figure 5).
Output AC-coupling capacitors	Required. Both SDO and $\overline{\text{SDO}}$ require AC-coupling capacitors. SDO AC-coupling capacitors are expected to be 4.7 µF to comply with SMPTE wander requirement.
DC power supply coupling capacitors	To minimize power supply noise, place 0.1-µF capacitor as close to the device V_{CC} pin as possible.
Distance from device to BNC	Keep this distance as short as possible.
High speed SDI and $\overline{\text{SDI}}$ trace impedance	Design differential trace impedance of SDI and $\overline{\text{SDI}}$ with 100 Ω.
High speed SDO and $\overline{\text{SDO}}$ trace impedance	Single-ended trace impedance for SDO and $\overline{\text{SDO}}$ with 75 Ω.

8.2.2 Detailed Design Procedure

The following design procedure is recommended:

1. Select a suitable power supply voltage for the LMH0303. It can be powered from a single 3.3-V supply (see *Power Supply Recommendations*).
2. Check that the power supply meets the DC requirements in *Recommended Operating Conditions*.
3. Select the proper pull-high or pull-low for SD/$\overline{\text{HD}}$ to set the slew rate.
4. Select proper pull-high or pull-low for ENABLE to enable or disable the output driver.
5. Choose a high quality 75-Ω BNC that is capable to support 2.97-Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended BNC footprint for meeting SMPTE return loss requirements.
6. Choose small 0402 surface mount ceramic capacitors for the AC-coupling and bypass capacitors.
7. Use proper footprint for BNC and AC-coupling capacitors. Anti-pads are commonly used in power and ground planes under these landing pads to achieve optimum return loss.

8.2.3 Application Curves

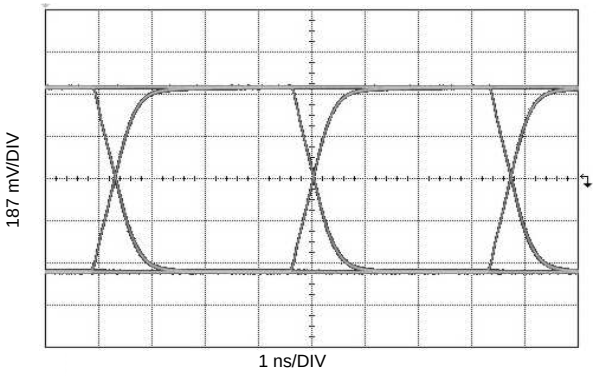


Figure 6. SDO PRBS10 at 270 Mbps

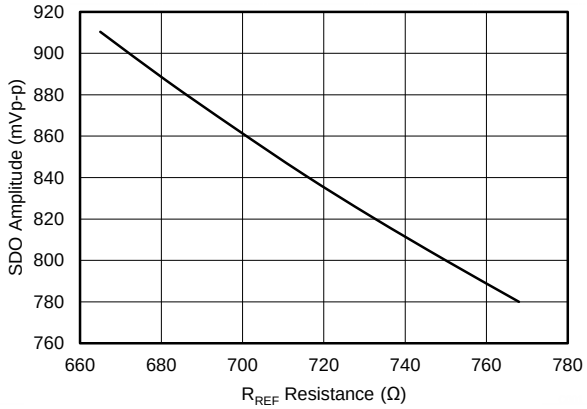


Figure 7. SDO Amplitude vs R_{REF} Resistance

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the recommended operating conditions (see *Recommended Operating Conditions*).
2. The maximum current draw for the LMH0303 is provided in *Electrical Characteristics – DC*. This figure can be used to calculate the maximum current the supply must provide.
3. The LMH0303 does not require any special power supply filtering, provided the recommended operating conditions are met. Only standard supply coupling is required.

10 Layout

10.1 Layout Guidelines

TI recommends the following layout guidelines for the LMH0303:

1. The R_{REF} 1% tolerance resistor should be placed as close as possible to the R_{REF} pin. In addition, the copper in the plane layers below the R_{REF} network should be removed to minimize parasitic capacitance.
2. Choose a suitable board stackup that supports 75-Ω single-ended trace and 100-Ω differential trace routing on the top layer of the board. This is typically done with a Layer 2 ground plane reference for the 100-Ω differential traces and a second ground plane at Layer 3 reference for the 75-Ω single-ended traces.
3. Use single-ended uncoupled trace designed with 75-Ω impedance for signal routing to SDO and $\overline{\text{SDO}}$. The trace width is typically 8-10 mil reference to a ground plane at Layer 3.
4. Use coupled differential traces with 100-Ω impedance for signal routing to SDI and $\overline{\text{SDI}}$. They are usually 5-mil to 8-mil trace width reference to a ground plane at Layer 2.
5. Place anti-pad (ground relief) on the power and ground planes directly under the 4.7-µF AC-coupling capacitor, return loss network, and IC landing pads to minimize parasitic capacitance. The size of the anti-pad depends on the board stackup and can be determined by a 3-dimension electromagnetic simulation tool.
6. Use a well-designed BNC footprint to ensure the BNC's signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
7. Keep trace length short between the BNC and SDO. The trace routing for SDO and $\overline{\text{SDO}}$ should be symmetrical, approximately equal lengths, and equal loading.
8. The exposed pad EP of the package should be connected to the ground plane through an array of vias. These vias are solder-masked to avoid solder flow into the plated-through holes during the board manufacturing process.
9. Connect each supply pin (V_{CC} and V_{EE}) to the power or ground planes with a short via. The via is usually placed tangent to the landing pads of the supply pins with the shortest trace possible.
10. Power-supply bypass capacitors should be placed close to the supply pins.

10.2 Layout Example

Figure 8 shows an example of proper layout requirements for the LMH0303.

Layout Example (continued)

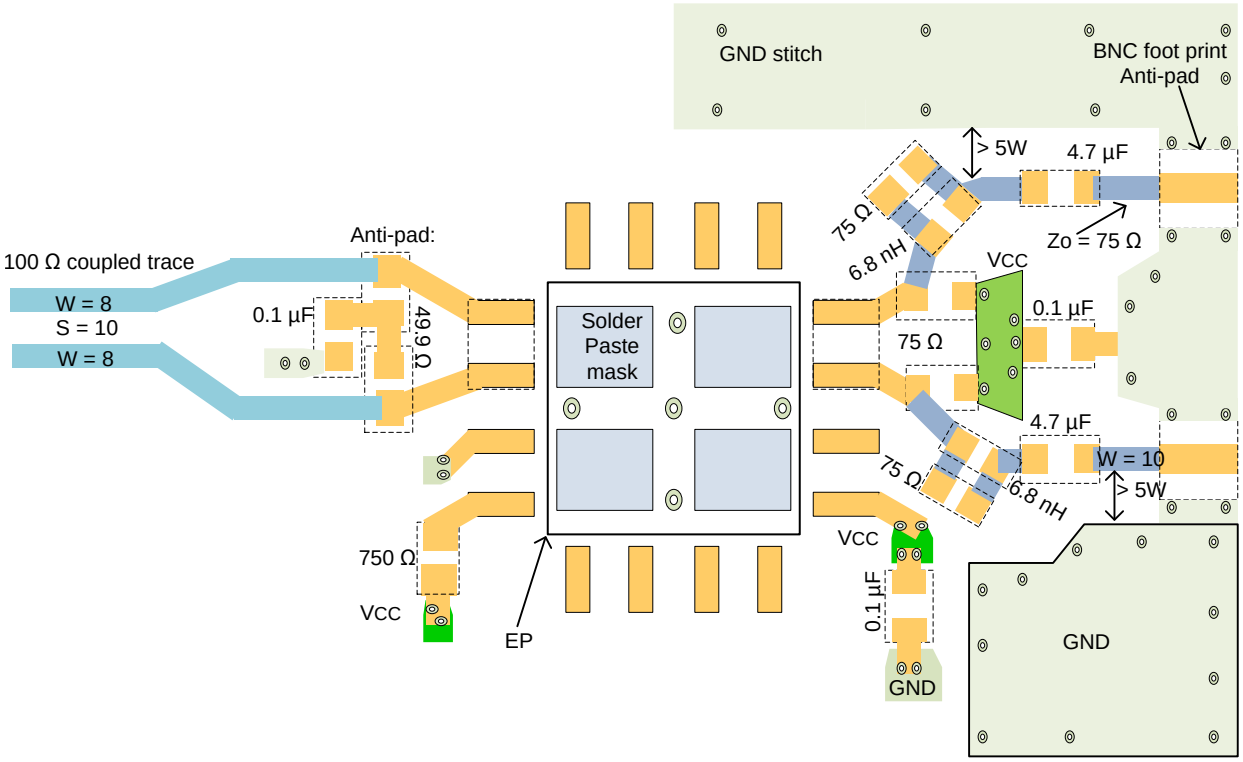


Figure 8. LMH0303 High-Speed Traces Layout Example

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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11.2 Trademarks

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11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0303SQ/NOPB	ACTIVE	WQFN	RUM	16	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L0303	Samples
LMH0303SQE/NOPB	ACTIVE	WQFN	RUM	16	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	L0303	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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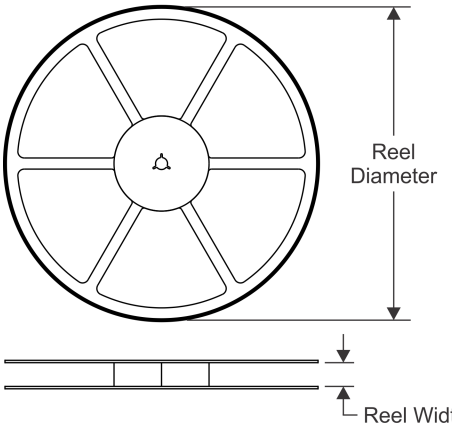
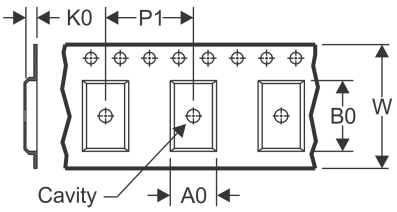
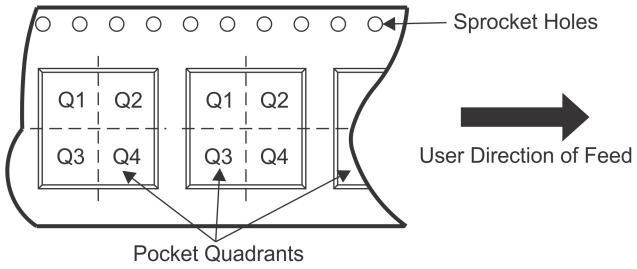


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

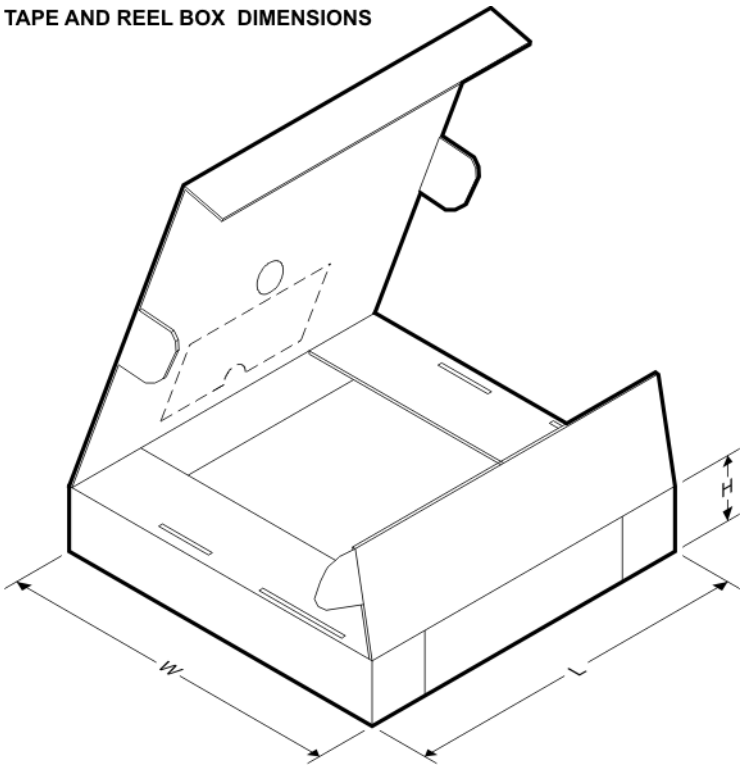
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0303SQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0303SQE/NOPB	WQFN	RUM	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

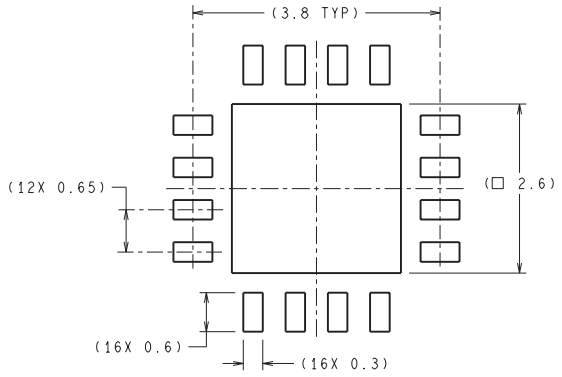
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0303SQ/NOPB	WQFN	RUM	16	1000	213.0	191.0	55.0
LMH0303SQE/NOPB	WQFN	RUM	16	250	213.0	191.0	55.0

RUM0016A



RECOMMENDED LAND PATTERN

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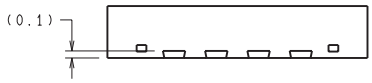
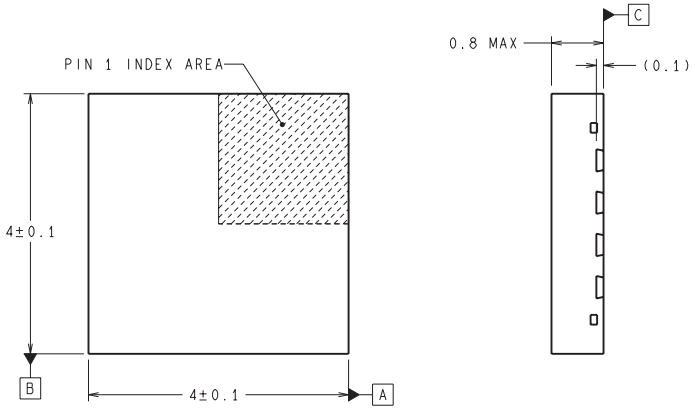
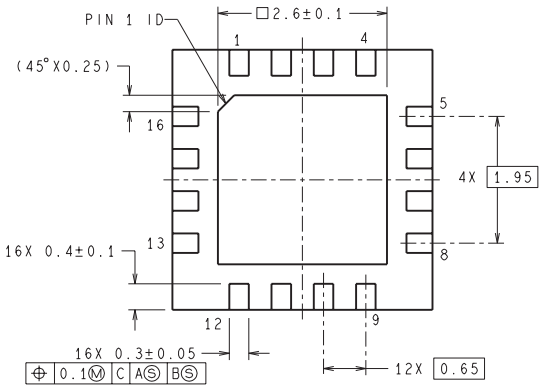
DIMENSIONS IN () FOR REFERENCE ONLY







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