GaN TECHNOLOGY PREVIEW
LMG5200 80-V, GaN Half-Bridge Power Stage

1 Features

- Input Voltage up to 80-V DC
- Integrated 80-V, 18-mΩ, GaN FETs
- Optimized Pinout for Easy PCB Layout
- Internal Bootstrap Supply Voltage Clamping to Prevent GaN FET Overdrive
- Supply Rail Undervoltage Lockout
- Independent High-Side and Low-Side TTL Logic Inputs
- Fast Propagation Times (29.5 ns Typical)
- Excellent Propagation Delay Matching (2 ns Typical)
- Low Power Consumption

2 Applications

- Multi MHz Synchronous Buck Converters
- Class D Amplifiers for Audio
- 48-V Point-of-Load (POL) Converters for Industrial, Computing and Telecom

3 Description

The LMG5200 device, a 80-V driver, GaN half-bridge power stage, provides an integrated power stage solution using enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two, 80-V GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration.

The TTL logic compatible inputs can withstand input voltages up to 14 V regardless of the VCC voltage. The proprietary bootstrap voltage clamping technique ensures the gate voltages of the enhancement mode GaN FETs are within a safe operating range. GaN FETs provide significant advantages for power conversion as they have near zero reverse recovery and very small input capacitance C_{ISS}. All the devices are mounted on a completely bond-wire-free package platform with minimized package parasitic elements. The LMG5200 device is available in a 6 mm x 8 mm x 2 mm lead free package and can be easily mounted on PCBs.

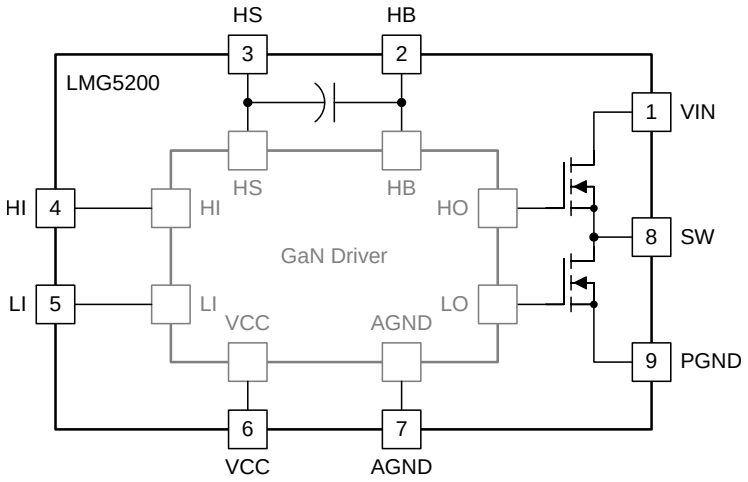
The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. It is an ideal solution for applications requiring high-frequency, high-efficiency operation in a small form factor. It reduces the board requirements for maintaining clearance and creepage requirements for medium voltage GaN applications while minimizing the loop inductances to ensure fast switching.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMG5200	QFN (9)	6.00 mm × 8.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application



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4 Revision History

Changes from Revision A (March 2015) to Revision B **Page**

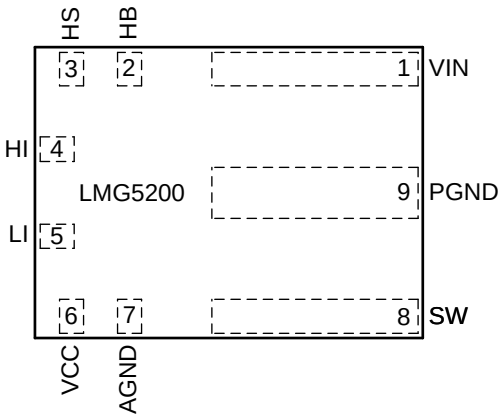
- Changed part number typo in Figure 12 ... 14

Changes from Original (March 2015) to Revision A **Page**

- Corrected typographical error in Simplified Application ... 1
- Corrected typographical error in Figure 5 ... 8
- Corrected typographical error in Figure 10 ... 10
- Corrected typographical error in Figure 11 ... 13

5 Pin Configuration and Functions

MOF (QFN) PACKAGE
9 PINS
(TOP VIEW)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	7	G	Analog ground. Ground of driver device.
HB	2	P	High-side gate driver bootstrap rail.
HI	4	I	High-side gate driver control input
HS	3	P	High-side GaN FET source connection
LI	5	I	Low-side driver control input
PGND	9	G	Power ground. Low-side GaN FET source. Electrically shorted to AGND pin.
SW	8	P	Switching node. Electrically shorted to HS pin.
VCC	6	P	5-V positive gate drive supply
VIN	1	P	Input voltage pin. Electrically connected to high-side GaN FET drain.

(1) I = Input, O = Output, G = Ground, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN (2)	0	90	V
	HB (3)	–0.3	96	
	HS (3)	–5	90	
	HI, LI (3)	–0.3	15	
	VCC (2), HB to HS	–0.3	6	
	HB to VCC	0	90	
	SW (2)	–5	90	
Output current	Pulsed current from SW pin (10-µs duration)	40		A
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) with respect to PGND
(3) with respect to AGND

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	VCC	4.75	5	5.25	V
	LI or HI Input	0		14	V
	HS, VIN, SW	-5		80	V
Output voltage range	HB	V_{HS}+ 4		V_{HS}+ 5.5	V
	HS, SW Slew rate			50	V/ns
IOUT from SW pin		10			A
Junction temperature, T_J		-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1) (2)		LMG5200 QFN 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12	
$R_{\theta JB}$	Junction-to-board thermal resistance	12	
ψ_{JT}	Junction-to-top characterization parameter	2.8	
ψ_{JB}	Junction-to-board characterization parameter	23	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC}	VCC quiescent current	LI = HI = 0 V, V_{VCC} = 5 V		0.07	0.1	mA
I_{CCO}	VCC operating current	f = 500 kHz		3.0	5.0	mA
I_{HB}	Total HB quiescent current	LI = HI = 0 V, V_{VCC} = 5 V		0.09	0.120	mA
I_{HBO}	Total HB operating current	f = 500 kHz, 50% Duty cycle, V_{DD} = 5 V		1.5	2	mA
INPUT PINS						
V_{IH}	High-level input voltage	Rising edge	1.89	2.06	2.18	V
V_{IL}	Low-level input voltage	Falling edge	1.48	1.66	1.76	V
V_{HYS}	Hysteresis between rising and falling threshold			400		mV
R_I	Input pull-down resistance		100	200	300	kΩ
UNDERVOLTAGE PROTECTION						
V_{VCC}	VCC rising edge threshold	Rising	3.2	3.8	4.5	V
$V_{VCC(hyst)}$	Hysteresis between falling and rising edge			185		mV
V_{HB}	HB rising edge threshold	Rising	2.7	3.2	3.7	V
	HB hysteresis between rising edge and falling edge			185		mV
BOOTSTRAP DIODE						
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 100 µA		0.45	0.65	V
V_{DH}	High-current forward voltage	I_{VDD-HB} = 100 mA		0.9	1.0	V
R_D	Dynamic resistance			1.6	2.8	Ω
	HB-HS clamp	Regulation voltage	4.7	5	5.3	V
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100 mA, I_R = 100 mA		40		ns
Q_{RR}	Bootstrap diode reverse recovery charge	V_{VIN} = 50 V		2		nC
POWER STAGE						
$R_{DS(on)HS}$	High-side GaN FET on-resistance	I_{OUT} = 5 A, V_{VCC} = 5 V, T_J = 25ºC		14	18	mΩ
$R_{DS(on)LS}$	Low-side GaN FET on-resistance	I_{OUT} = 5 A, V_{VCC} = 5 V, T_J = 25ºC		14	18	mΩ
V_{SD}	GaN 3rd quadrant conduction drop	I_{SD} = 500 mA, VIN floating, V_{VCC} = 5 V, HI, LI low		2		V
$I_{L-VIN-SW}$	Leakage between VIN to SW when the high-side GaN FET and low-side GaN FET are off	V_{IN} = 80 V, (HI = LI = 0 V) V_{VCC} = 5 V, T_J = 25ºC		25	150	µA
$I_{L-SW-GND}$	Leakage between SW and GND when the high-side GaN FET and low-side GaN FET are off	V_{SW} = 80 V, HI , LI = 0 V, V_{VCC} = 5 V, T_J = 25ºC		25	150	µA
C_{OSS}	Output capacitance of high-side GaN FET and low-side GaN FET	V_{DS} = 50 V, V_{GS} = 0 V (HI = LI = 0 V)		225	280	pF
Q_G	Total gate charge	V_{DS} = 50 V, I_D = 10 A, V_{GS} = 5 V		3.8		nC
Q_{OSS}	Output charge	V_{DS} = 50 V, I_D = 10 A		20		nC
Q_{RR}	Source to drain reverse recovery charge	Not including internal driver bootstrap diode		0		nC

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS						
t_{HIPLH}	Propagation delay(1)	HI turning from low to high and SW node being pulled to VIN (LO is low), V_{VIN} = 50 V, V_{VCC} = 5 V		29.5	47	ns
t_{HIPHL}		HI turning from high to low and SW node being tristated (LO is low), V_{VIN} = 50 V, V_{VCC} = 5 V		29.5	47	ns
t_{LPLH}		LI turning from low to high and switch node being pulled to PGND (HI is low), V_{VIN} = 50 V, V_{VCC} = 5 V		29.5	47	ns
t_{LPHL}		LI turning from high to low and switch node being tristated (HI is low), V_{VIN} = 50 V, V_{VCC} = 5 V		29.5	47	ns
t_{MON}	Delay matching: LI high and HI low (2)	V_{VIN} = 50 V, V_{VCC} = 5 V		2	8.0	ns
t_{MOFF}	Delay matching: LI low and HI high(2)	V_{VIN} = 50 V, V_{VCC} = 5 V		2	8.0	ns
t_{PW}	Minimum input pulse width that changes the output		10			ns

(1) See *Propagation Delay and Mismatch Measurement* section.
(2) See Figure 6 through Figure 9.

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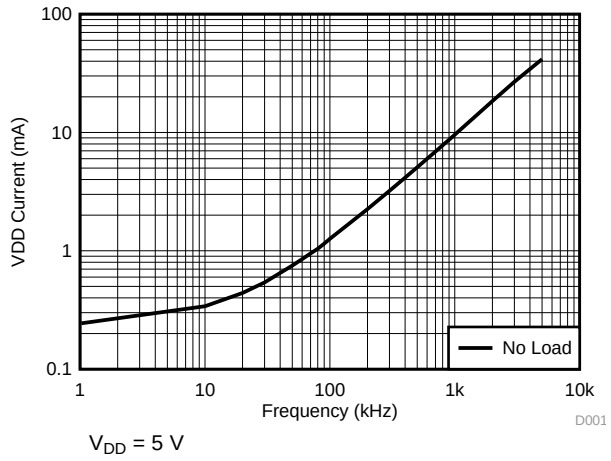
6.6 Typical Characteristics

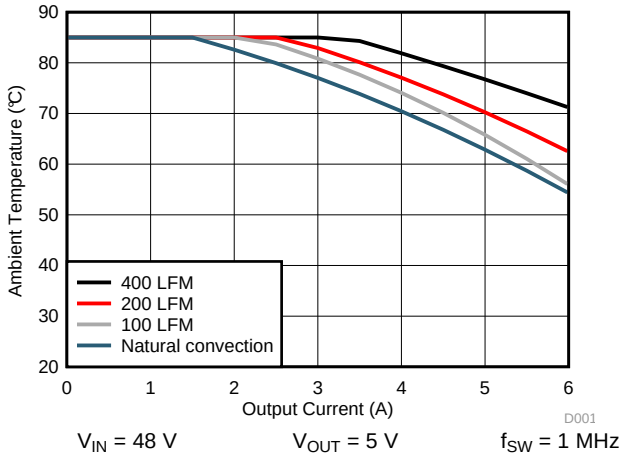
All the curves are based on measurements made on a PCB design with dimensions of 3.2 inches (W) × 2.7 inches (L) × 0.062 inch (T) and 4 copper layers of 2 oz.

The safe operating area (SOA) curves displays the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. A buck converter is used for measuring the SOA. Figure 2 outlines the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area for different airflow conditions.



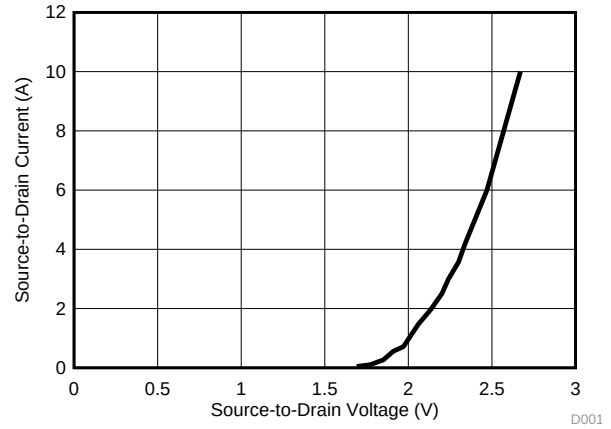
V_{DD} = 5 V

Figure 1. V_{DD} Supply Current vs Switching Frequency



V_{IN} = 48 V V_{OUT} = 5 V f_{SW} = 1 MHz

Figure 2. Safe Operating Area



GaN third quadrant conduction.

Figure 3. Source-to-Drain Current vs Source-to-Drain Voltage

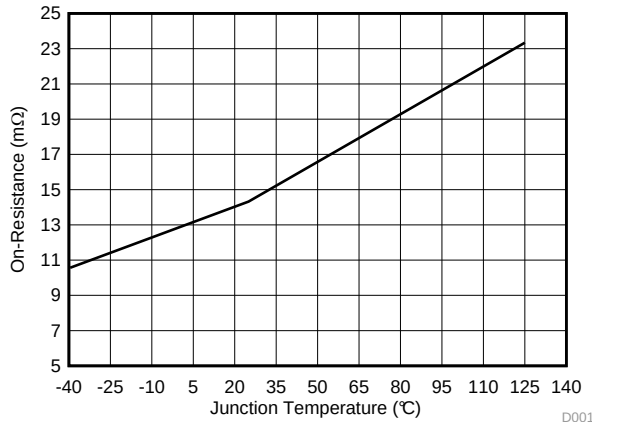


Figure 4. GaN FET On-Resistance vs Junction Temperature

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7 Parameter Measurement Information

7.1 Propagation Delay and Mismatch Measurement

Figure 5 shows the typical test setup used to measure the propagation mismatch. As the gate drives are not accessible, pull-up and pull-down resistors in this test circuit are used to indicate when the low-side GaN FET turns ON and the high-side GaN FET turns OFF and vice versa to measure the t_{MON} and t_{MOFF} parameters. Resistance values used in this circuit for the pull-up and pull-down resistors are in the order of 1 kΩ, the current sources used are 2 A.

Figure 6 through Figure 8 show propagation delay measurement waveforms. For turn-on propagation delay measurements, the current sources are not used. For turn-off time measurements, the current sources are set to 2 A and a voltage clamp limit is also set, referred to as $VIN_{(CLAMP)}$. When measuring the high-side component turn-off delay, the current source across the high-side FET is turned on, the current source across the low-side FET is off, HI transitions from high-to-low and output voltage transitions from V_{IN} to $V_{IN(CLAMP)}$. Similarly for low-side component turn-off propagation delay measurements, the high-side component current source is turned off and the low-side component current source is turned on, LI transitions from high to low and the output transitions from GND potential to $V_{IN(CLAMP)}$. The time between the transition of LI and the output change is the propagation delay time.

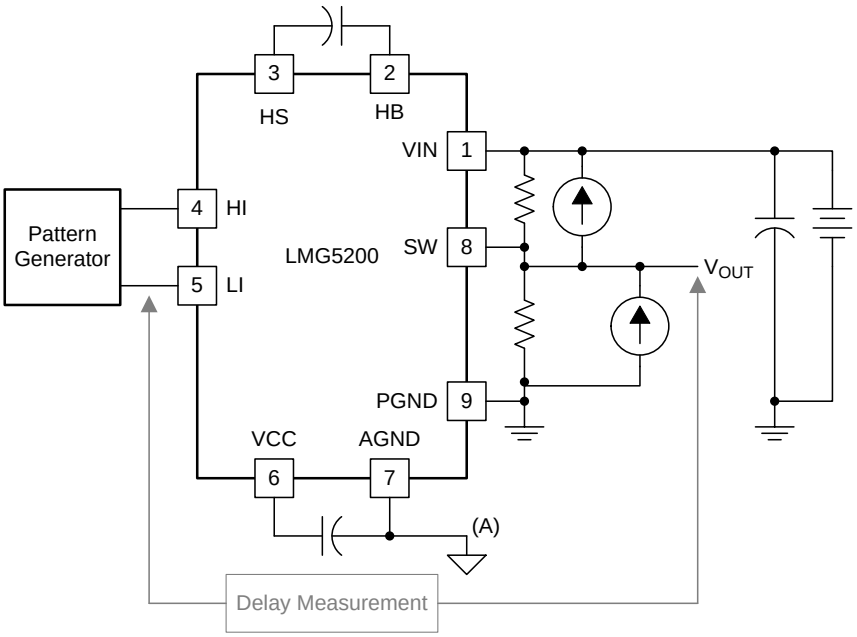

Figure 5. Propagation Delay and Propagation Mismatch Measurement

Propagation Delay and Mismatch Measurement (continued)

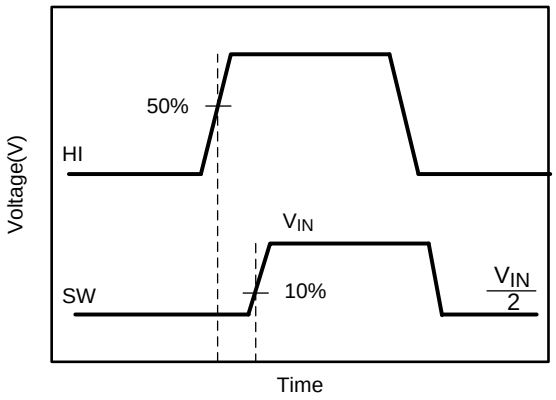

Figure 6. High-Side Gate Driver Turn-On

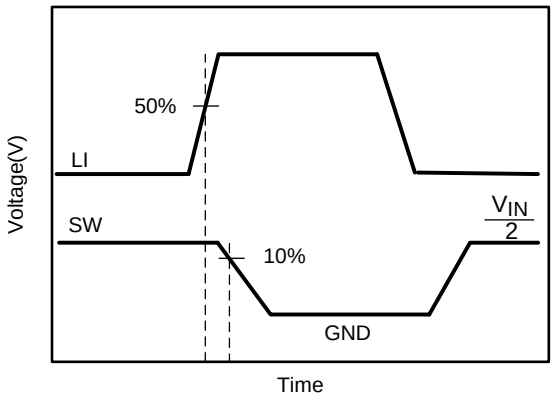

Figure 7. Low-Side Gate Driver Turn-On

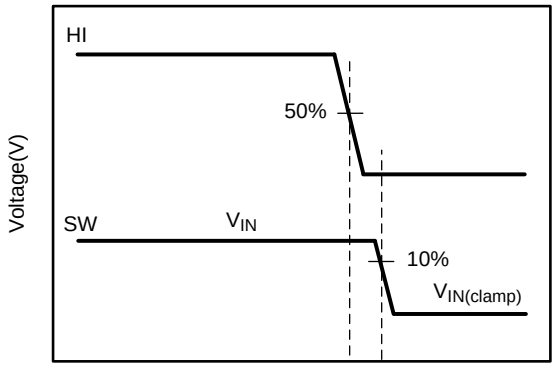

Figure 8. High-Side Gate Driver Turn-Off

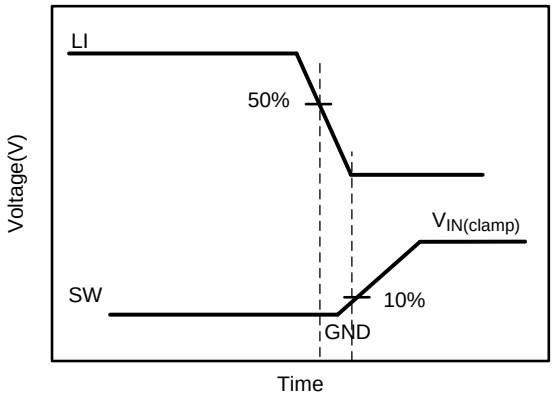

Figure 9. Low-Side Gate Driver Turn-Off

8 Detailed Description

8.1 Overview

Figure 10 shows the LMG5200, half-bridge, GaN power stage with a highly integrated high-side and low-side gate drivers which includes built in UVLO protection circuitry and a over voltage clamp circuitry. The clamp circuitry limits the bootstrap refresh operation to ensure that the high-side gate driver overdrive does not exceed 5.4 V. The device integrates two, 18-mΩ GaN FETs in a half-bridge configuration. The device can be used in many isolated and non-isolated topologies allowing very simple integration. The package is designed to minimize the loop inductance while keeping the PCB design simple. The drive strengths for turn-on and turn-off are optimized to ensure high voltage slew rates without causing any excessive ringing on the gate or power loop.

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8.2 Functional Block Diagram

Figure 10 shows the functional block diagram of the LMG5200 device with integrated high-side and low-side GaN FETs.

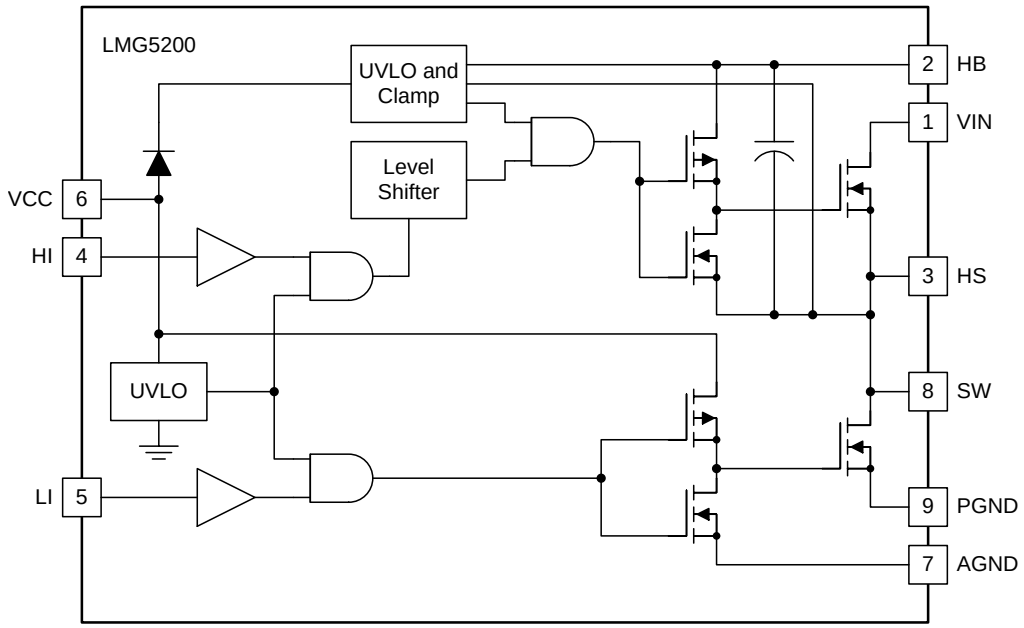

Figure 10. Functional Block Diagram

8.3 Feature Description

The LMG5200 device brings ease of designing high power density boards without the need for underfill while maintaining creepage and clearance requirements. The propagation delays between the high-side gate driver and low-side gate driver are matched to allow very tight control of dead time. Controlling the dead time is critical in GaN-based applications to maintain high efficiency. HI and LI can be independently controlled to minimize the third quadrant conduction of the low-side FET for hard switched buck converters. A very small propagation mismatch between the HI and LI to the drivers for both the falling and rising thresholds ensures dead times of <10 ns. Co-packaging the GaN FET half-bridge with the driver ensures minimized common source inductance. This minimized inductance has a significant performance impact on hard-switched topologies.

The built in bootstrap circuit with clamp prevents the high-side gate drive from exceeding the GaN FETs maximum gate-to-source voltage (Vgs) without any additional external circuitry. The built-in driver has an undervoltage lockout (UVLO) on the VDD and bootstrap (HB-HS) rails. When the voltage is below the UVLO threshold voltage, the device ignores both the HI and LI signals to prevent the GaN FETs from being partially turned on. Below UVLO, if there is sufficient voltage (V_{VCC} > 2.5 V), the driver actively pulls the high-side and low-side gate driver output low. The UVLO threshold hysteresis of 200 mV prevents chattering and unwanted turn-on due to voltage spikes. Use an external VCC bypass capacitor with a value of 0.1 µF or higher. A size of 0402 is recommended to minimize trace length to the pin. Place the bypass and bootstrap capacitors as close to the device as possible to minimize parasitic inductance.

Feature Description (continued)

8.3.1 Bootstrap Capacitor

The bootstrap capacitor provides the gate charge for the high-side gate drive, dc bias power for HB undervoltage lockout circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated using Equation 1.

$$C_{BST} > \left(\frac{Q_{gH} + I_{HB} + t_{ON(max)} + Q_{rr}}{\Delta V} \right)$$

where

- I_{HB} is the quiescent current of the high-side gate driver (100 µA, max)
- $t_{ON(max)}$ is the maximum on-time period of the high-side gate driver
- Q_{rr} is the reverse recovery charge of the bootstrap diode
- QgH is the gate charge of the high-side GaN FET
- ΔV is the permissible ripple in the bootstrap capacitor (< 100 mV, typ) (1)

A 100-nF, 16-V, 0402 ceramic capacitor is suitable for most applications. Place the bootstrap capacitor as close to the HB and HS pins as possible.

8.3.2 Power Dissipation

Ensure that the power loss in the driver and the GaN FETs is maintained below the maximum power dissipation limit of the package at the operating temperature. The smaller the power loss in the driver and the GaN FETs, the higher the maximum operating frequency that can be achieved in the application.. The total power dissipation of the LMG5200 device is the sum of the gate driver losses, the bootstrap diode power loss and the switching and conduction losses in the FETs.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated using Equation 2.

$$P = \left(2 \times Q_g\right) \times V_{DD} \times f_{SW}$$

where

- Q_g is the gate charge
- V_{DD} is the bias supply
- f_{SW} is the switching frequency (2)

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the outputs. Figure 1 shows the measured gate driver power dissipation versus frequency and load capacitance. Use this graph to approximate the power losses due to the gate drivers.

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Because each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

The power losses due to the GaN FETs can be divided into conduction losses and switching losses. Conduction losses are resistive losses and can be calculated using Equation 3.

$$P_{COND} = \left(\left(I_{RMS(HS)}\right)^2 \times R_{DS(on)HS} \right) + \left(\left(I_{RMS(LS)}\right)^2 \times R_{DS(on)LS} \right)$$

where

- $R_{DS(on)HS}$ is the high-side GaN FET on-resistance
- $R_{DS(on)LS}$ is the low-side GaN FET on-resistance
- $I_{RMS(HS)}$ is the high-side GaN FET RMS current
- $I_{RMS(LS)}$ and low-side GaN FET RMS current (3)

The switching losses can be computed to a first order using Equation 4.

$$P_{SW} = V_{IN} \times I_{OUT} \times f_{SW} \times t_{TR}$$

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Feature Description (continued)

where

- t_{TR} is the switch transition time from ON to OFF and from OFF to ON (4)

Note that the low-side FET does not suffer from this loss. The third quadrant loss in the low-side device is ignored in this first order loss calculation.

The sum of the driver loss, the bootstrap diode loss and the switching and conduction losses in the GaN FETs is the total power loss of the device. Careful board layout with an adequate amount of thermal vias close to the power pads (VIN, SW and GND) allows optimum power dissipation from the package. A top-side mounted heat sink with airflow can also improve the package power dissipation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 11 shows a buck converter application with VCC connected to a 5-V supply. It is critical to optimize the power loop (loop impedance from VIN capacitor to PGND). Having a high power loop inductance causes significant ringing in the SW node and also causes the associated power loss. Refer to the layout guidelines to minimize this power loop.

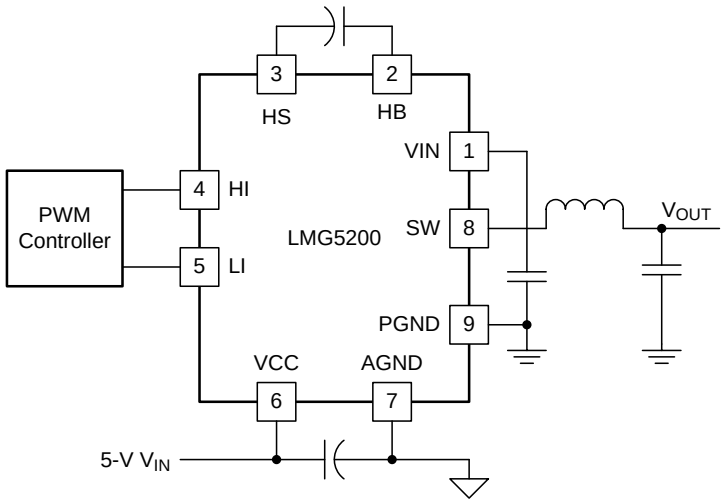

Figure 11. Typical Connection Diagram For a Buck Converter

10 Power Supply Recommendations

For proper operation, power-up the VCC rail before the VIN rail. Similarly, power-down the VIN rail before the VCC rail.

CAUTION

Failure to follow correct power-up and power-down procedures can cause catastrophic failure of the device.

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11 Layout

11.1 Layout Guidelines

To maximize the efficiency benefits of fast switching, its extremely important to optimize the board layout such that the power loop impedance is minimum. When using a multilayer board (more than 2 layers), power loop parasitic impedance is minimized by having the return path to the input capacitor (between VIN and PGND) small and directly underneath the first layer as shown in Figure 12 and Figure 13. Loop inductance is reduced due to inductance cancellation as the return current is directly underneath and flowing in the opposite direction. It is also critical that the VCC capacitors and the bootstrap capacitors are as close to the device as possible and in the first layer. Carefully consider the AGND connection of LMG5200 device. It should NOT be directly connected to PGND so that PGND noise does not directly shift AGND and cause spurious switching events due to noise injected in HI and LI signals. Placements shown in Figure 12 and in the cross section of Figure 13 show the suggested placement of the device with respect to sensitive passive components, such as VIN, bootstrap capacitors (HS and HB) and VSS capacitors. Use appropriate spacing in the layout to reduce creepage and maintain clearance requirements in accordance with the application pollution level. Inner layers if present can be more closely spaced due to negligible pollution.

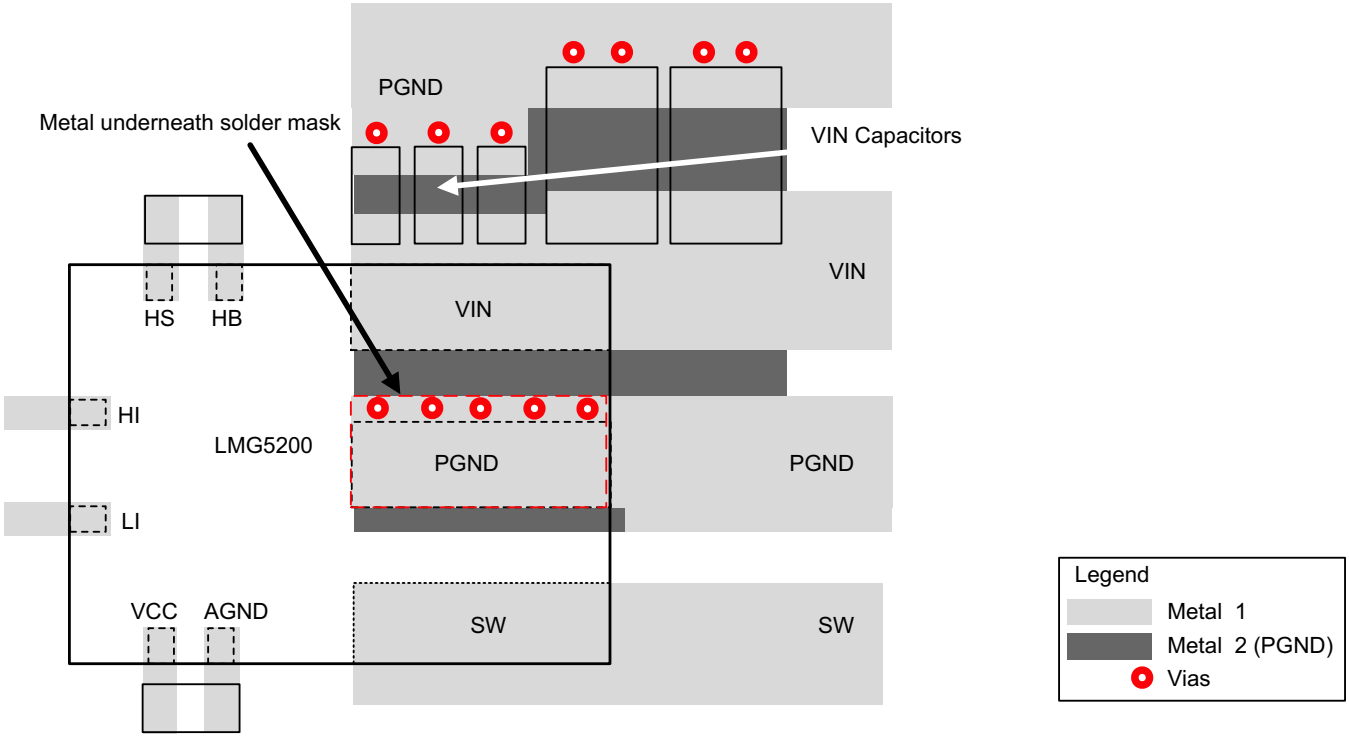

Figure 12. External Component Placement (Single Layer)

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Layout Guidelines (continued)

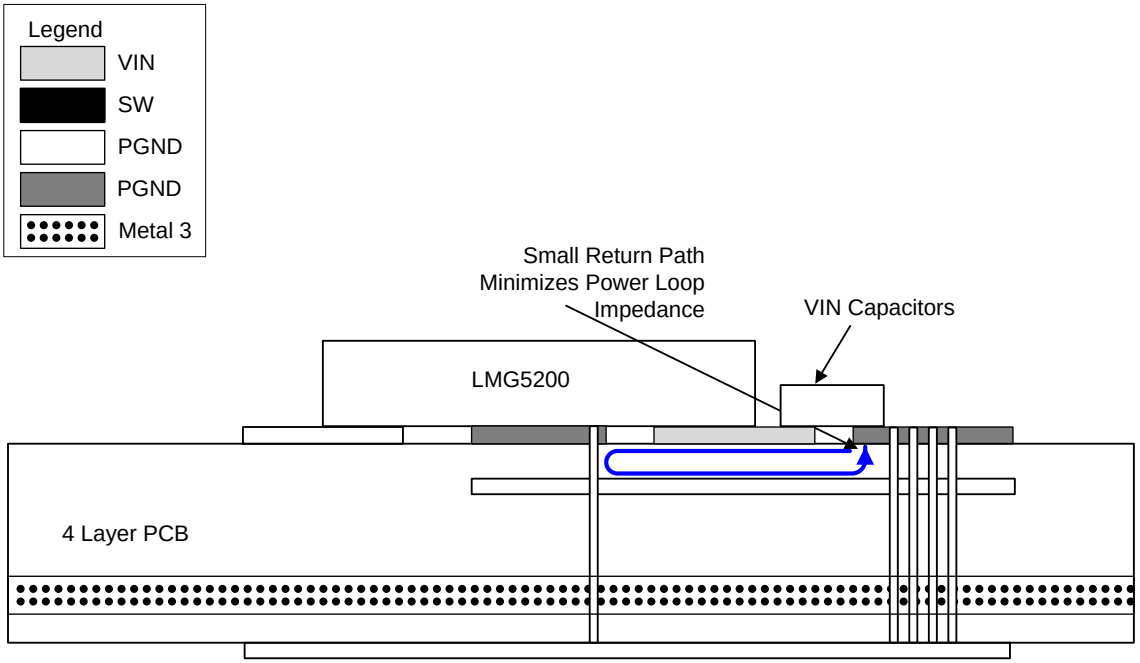

Figure 13. Four Layer Board Cross Section With Return Path Directly Underneath for Power Loop

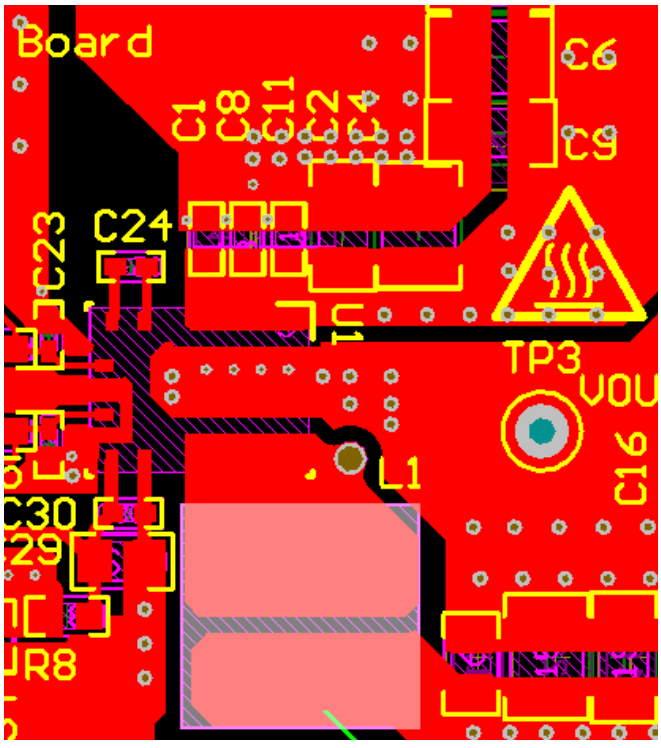

Figure 14. Top Layer

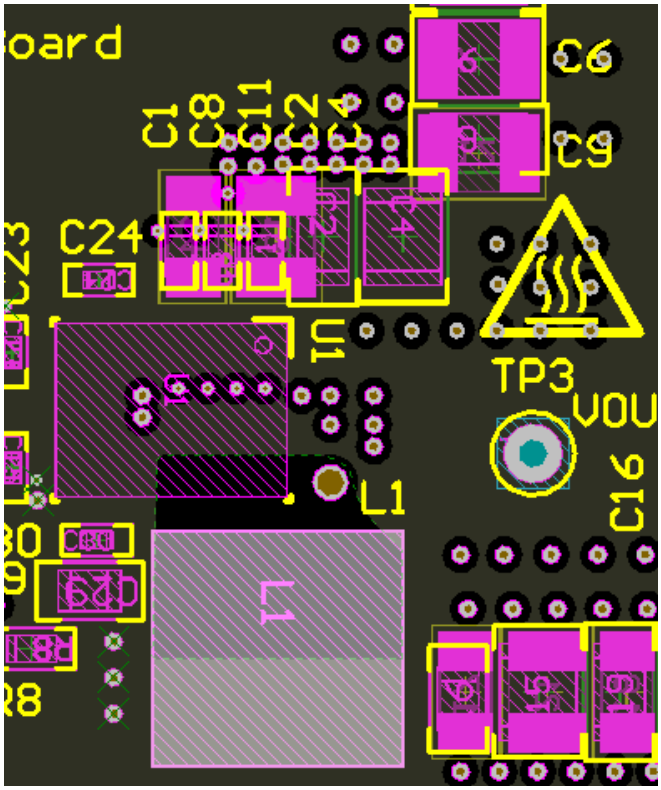

Figure 15. Ground Plane

GaN TECHNOLOGY PREVIEW

Layout Guidelines (continued)

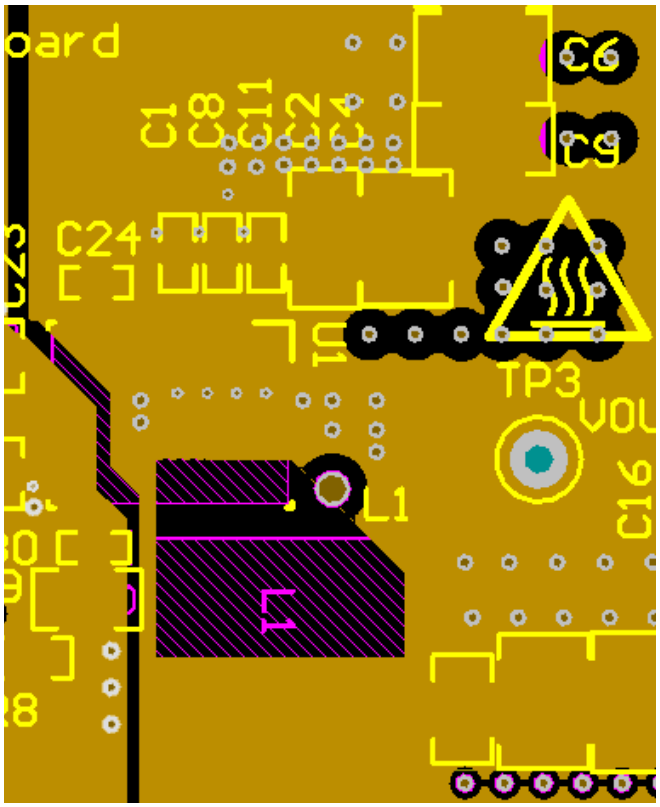

Figure 16. Middle Layer

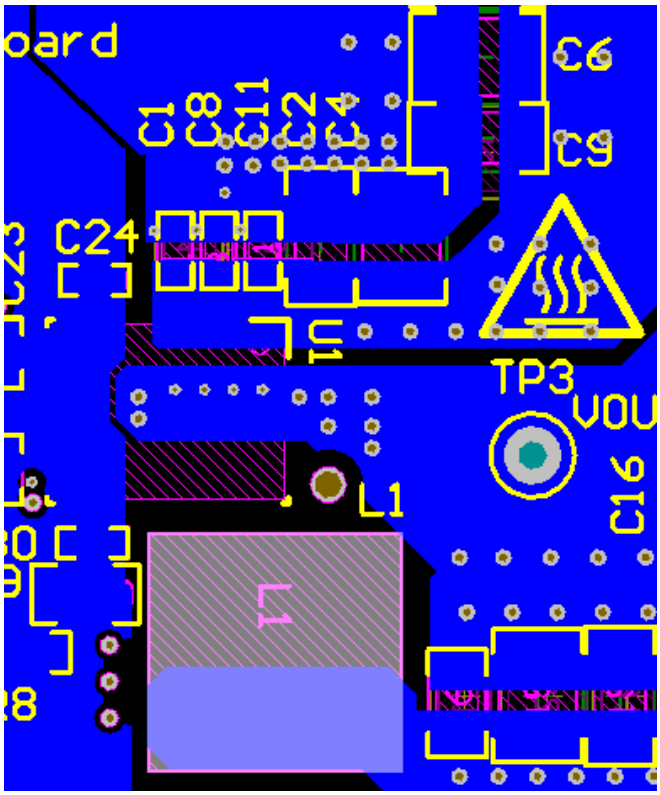

Figure 17. Bottom Layer

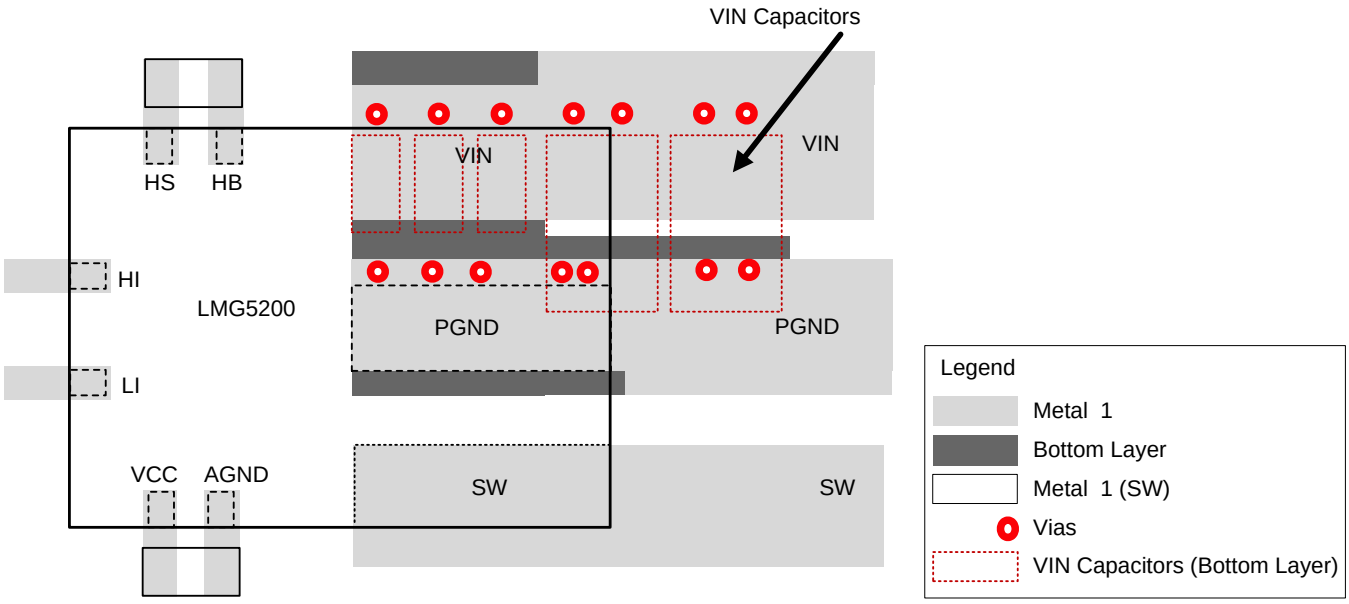

Figure 18. External Component Placement (Double Layer PCB)

GaN TECHNOLOGY PREVIEW

Layout Guidelines (continued)

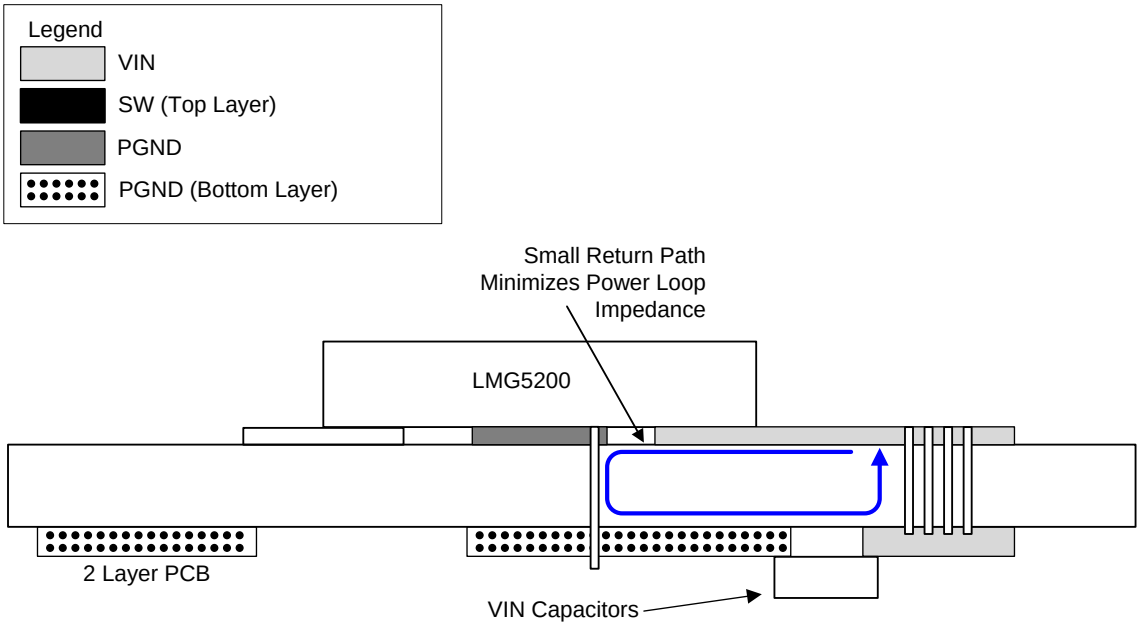

Figure 19. Two Layer Board Cross Section With Return Path

Two-layer boards are not recommended for use with LMG5200 device due to the larger power loop inductance. However, if design considerations allow only two board layers, place the input decoupling capacitors immediately behind the device on the back-side of the board to minimize loop inductance.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

LMG5200 PSpice Transient Model

LMG5200 TINA-TI Transient Reference Design

12.2 Documentation Support

12.2.1 Related Documentation

Layout Guidelines for LMG5200 GaN Power Stage Module (SNVA729)

Using the LMG5200: GaN Half-Bridge Power Module Evaluation Module (SNVU461)

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Information

The LMG5200 device package is rated as a MSL3 package (Moisture Sensitivity Level 3). Please refer to application report SNOA550 for specific handling and process recommendations of a MSL3 package.

Figure 20 and Figure 21 show preliminary packaging information for the device.

Package Information (continued)

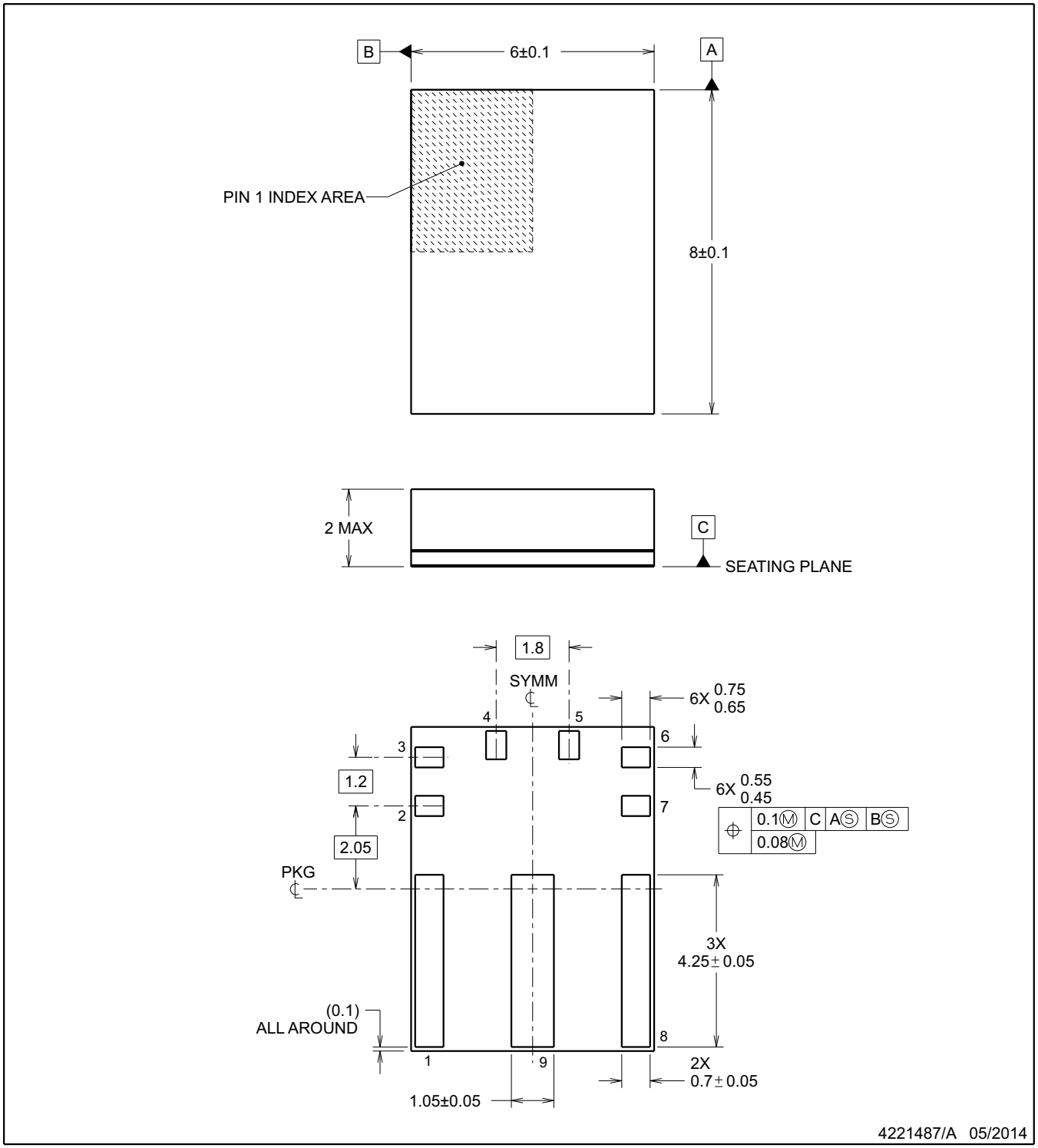

Figure 20. Package Top, Side and Bottom View

GaN TECHNOLOGY PREVIEW

Package Information (continued)

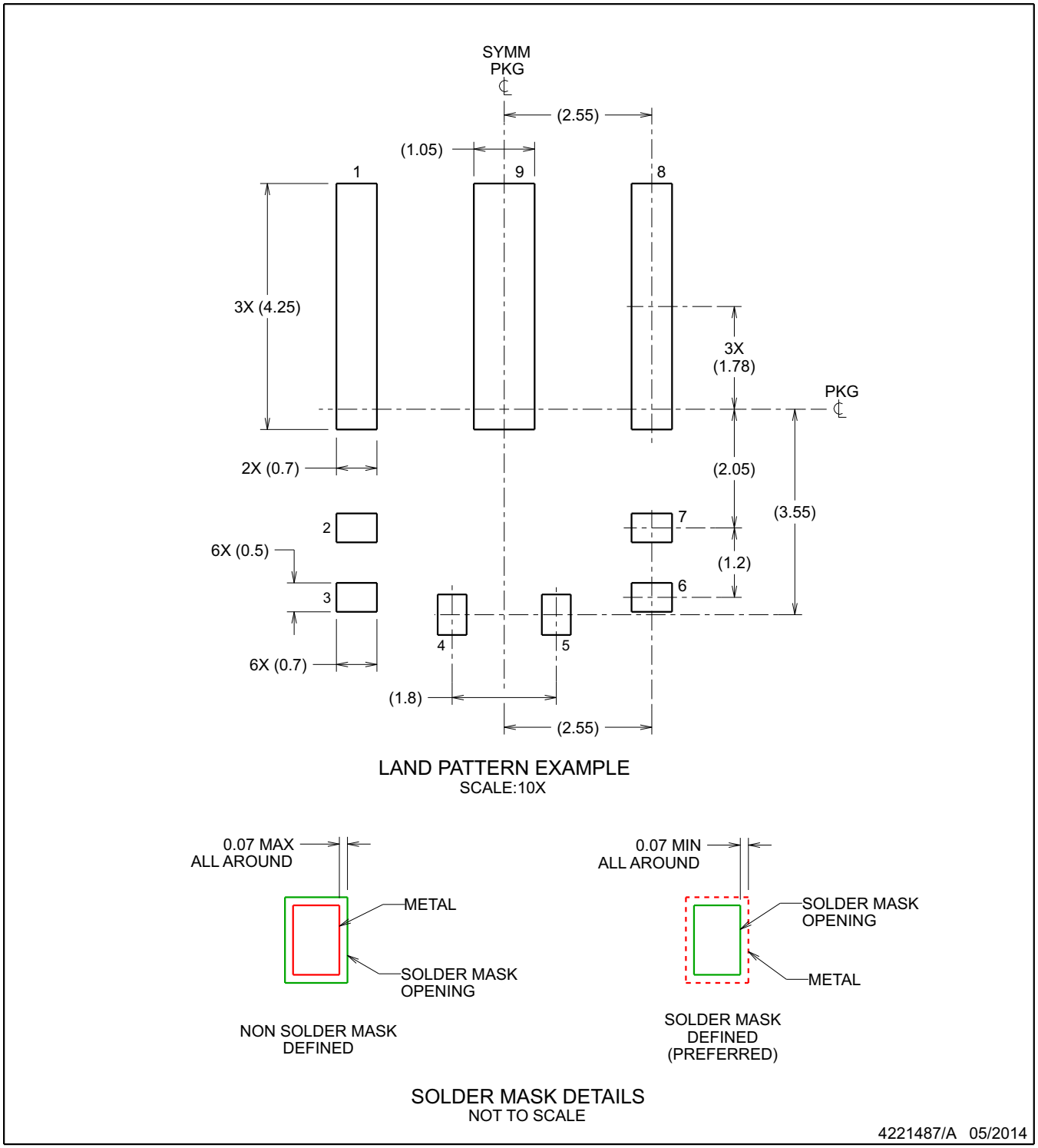

Figure 21. Package Bottom View Showing Pinout

GaN TECHNOLOGY PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLMG5200MOFT	ACTIVE	QFM	MOF	9	250	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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