LMG1020 5-V, 7-A, 5-A Low-Side GaN Driver With 60-MHz, 1-ns Speed

1 Features

- Low-Side, Ultra-Fast Gate Driver for GaN and Silicon FETs
- 1 ns Minimum Pulse
- Up to 60 MHz Operation
- 2.5 ns Typical, 4.5 ns Maximum Propagation Delay
- 400 ps Typical Rise and Fall Time
- 7-A Peak Source and 5-A Peak Sink Currents
- UVLO and Overtemperature Protection
- 0.8 mm × 1.2 mm WCSP Package

2 Applications

- LiDAR
- Time-of-Flight Laser Drivers
- Class-E Wireless Chargers
- VHF Resonant Power Converters
- GaN-Based Synchronous Rectifier
- Augmented Reality

3 Description

The LMG1020 device is a single, low-side GaN driver designed for driving GaN FETs and logic-level MOSFETs in high-speed applications. The design simplicity of the LMG1020 enables extremely fast propagation delays of 2.5 nanoseconds. The drive strength is independently adjustable for the pull-up and pull-down edges by connecting external resistors between the gate and OUTH and OUTL, respectively.

The GaN driver features undervoltage lockout (UVLO) and overtemperature protection (OTP) in the event of overload or fault conditions.

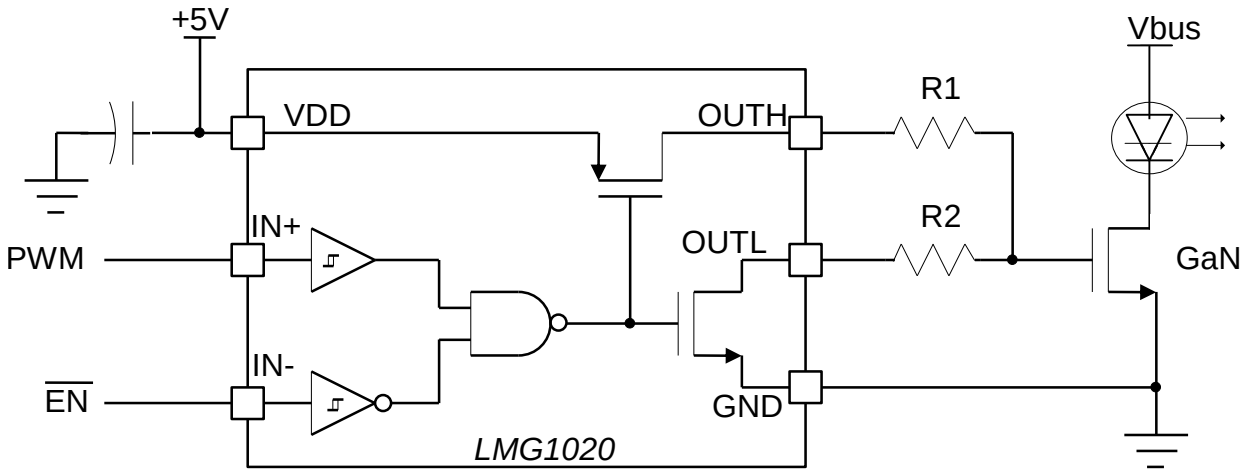
0.8-mm × 1.2-mm WCSP package of LMG1020 minimizes gate loop inductance and maximizes power density in high-frequency applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMG1020	WCSP (6)	0.80 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified LiDAR Driver Stage Diagram



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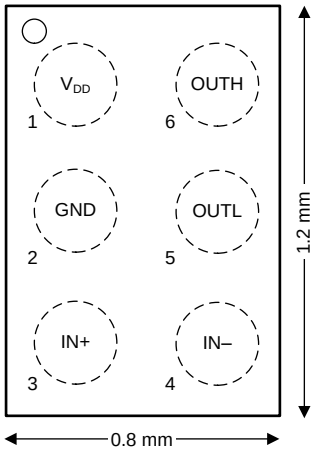
4 Revision History

DATE	REVISION	NOTES
February 2018	*	Initial release.

5 Pin Configuration and Functions

YFF Package
6-Ball WCSP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
IN+	3	I	Positive logic-level input
IN–	4	I	Negative logic-level input
OUTL	5	O	Pulldown gate drive output. Connect through an optional resistor to the target transistor's gate
OUTH	6	O	Pullup gate drive output. Connect through a resistor to the target transistor's gate
VDD	1	I	Input voltage supply. Decouple through a compact capacitor to GND

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage		5.75	V
V_{IN}	IN+, IN- pin voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	OUTH, OUTL pin voltage	-0.3	5.75	V
T_{STG}	Storage Temperature	-55	150	°C
T_J	Operating Temperature	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.75	5	5.25	V
V_{INx}	IN+ or IN- input voltage	0		V_{DD}	V
T_J	Operating Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMG1020 YFF (WCSP) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Y_{JB}	Junction-to-board characterization parameter	38.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Characteristics						
$I_{VDD, Q}$	VDD Quiescent Current	IN_+ = IN_- = 0 V			75	µA
$I_{VDD, op}$	VDD Operating Current	fsw = 30 MHz, no load		40		mA
		fsw = 30 MHz, 100pF load		51		mA
$V_{DD, UVLO}$	Under-voltage Lockout	V_{DD} rising	4.1		4.2	V
$\Delta V_{DD, UVLO}$	UVLO Hysteresis			85		mV
T_{OTP}	Over temperature shutdown, turn-off threshold			170		°C
ΔT_{OTP}	Over temperature hysteresis			20		°C
Input DC Characteristics						
V_{IH}	IN+, IN- high threshold		1.7		2.6	V
V_{IL}	IN+, IN- low threshold		1.1		1.8	V
V_{HYST}	IN+, IN- hysteresis		0.5		1	V
R_{IN+}	Positive input pull-down resistance	To GND	100	150	250	kΩ
R_{IN-}	Negative input pull-up resistance	to V_{DD}	100	150	250	kΩ
C_{IN+}	Positive input pin capacitance (1)	To GND		1.25		pF
C_{IN-}	Negative input pin capacitance (1)	To GND		1.45		pF
Output DC Characteristics						
V_{OL}	OUTL voltage	I_{OUTL} = 100 mA, IN+= IN- = 0 V			36	mV
V_{DD}-V_{OH}	OUTH voltage	I_{OUTH} = 100 mA, IN+= 5 V, IN- = 0 V, V_{DD} = 5 V			50	mV
I_{OH}	Peak source current (1)	V_{OUTH} = 0 V, IN+= 5 V, IN- = 0 V, V_{DD} = 5 V		7		A
I_{OL}	Peak sink current (1)	V_{OUTL} = 5 V, IN+= IN- = 0 V, V_{DD} = 5 V		5		A

(1) Ensured by design.

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6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{start}	Startup Time, V_{DD} rising above UVLO	IN- = GND, IN+ = V_{DD} , V_{DD} rising to 4.2V to OUTH rising		45		µs
$t_{shut-off}$	ULVO falling	IN- = GND, IN+ = VDD , VDD falling below 4.1V to OUTH falling		1.9		µs
$t_{pd, r}$	Propagation delay, turn on	IN- = 0 V, IN+ to OUTH, 100 pF load		2.5		ns
$t_{pd, f}$	Propagation delay, turn off	IN- = 0 V, IN+ to OUTL, 100 pF load		2.6		ns
t_{rise}	Output rise time	0Ω series 100 pF load(1)		375		ps
		0Ω series 1 nF load(1)		1		ns
t_{fall}	Output fall time	0Ω series 100 pF load(1)		360		ps
		0Ω series 1 nF load(1)		1		ns
t_{min}	Minimum pulse width	0Ω series 100 pF load(1)		1		ns
$t_{mismatch}$	Part-to-part propagation time mismatch			0.5		ns

(1) rise and fall calulated as a 20% to 80%

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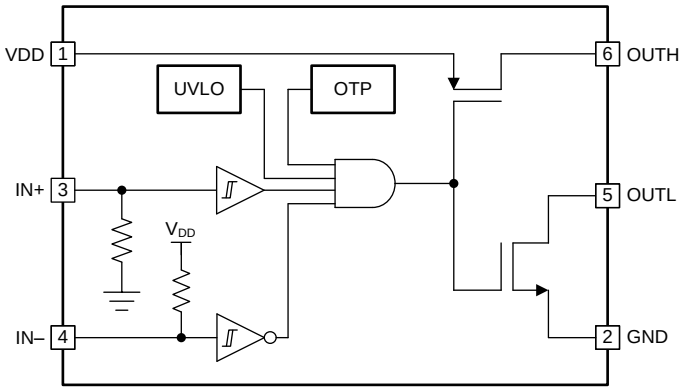
7 Detailed Description

7.1 Overview

LMG1020 is a high-performance low-side 5-V gate driver for GaN and logic-level silicon power transistors. While the LMG1020 is designed for high-speed applications, such as wireless power transmission and LiDAR applications, it is a high-performance solution for any other low-side driving application.

The LMG1020 is optimized to provide the lowest propagation delay through the driver to the power transistor.

7.2 Functional Block Diagram



7.3 Feature Description

The driver features internal undervoltage lockout (UVLO) and overtemperature protection (OTP) to protect the driver and circuit in case of fault conditions. The driver input stage features Schmitt-trigger inputs to reduce sensitivity to noise on the input. It also features input pulldown and pullup resistors to prevent unintended device turnon.

The OUTH and OUTL outputs of the LMG1020 allow the user to use independent resistors connecting to the gate. The two resistors allow the user to independently control the turnon and turnoff drive strengths to control slew rate and EMI, and to control ringing on the gate signal. For GaN FETs, controlling ringing is important to reduce stress on the GaN FET and driver.

7.4 Device Functional Modes

Table 1. Truth Table

IN-	IN+	OUTH	OUTL
L	L	OPEN	L
L	H	H	OPEN
H	L	OPEN	L
H	H	OPEN	L

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

To operate GaN transistors at very high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the GaN transistor. Also, gate drivers are indispensable when the outputs of the PWM controller do not meet the voltage or current levels needed to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3 V logic signal, which cannot effectively turn on a power switch. A level-shift circuit is needed to boost the 3.3 V signal to the gate-drive voltage (such as 5 V) in order to fully turn on the power device and minimize conduction losses.

Gate drivers effectively provide the buffer-drive functions. Gate drivers also address other needs such as minimizing the effect of high-frequency switching noise (by placing the high-current driver IC physically close to the power switch), reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

The LMG1020 is a 60-MHz low-side gate driver for enhancement mode GaN FETs in single-ended configuration. The split-gate outputs with strong source and sink capability, provides flexibility to adjust the turnon and turnoff strength independently.

8.2 Typical Application

The LMG1020 is designed to be used with a single low-side, ground-referenced GaN or logic-level FET, as shown in Figure 1. Independent gate drive resistors, R1 and R2, are used to independently control the turnon and turnoff drive strengths, respectively. For fast and strong turnoff, R2 can be shorted and OUTL directly connected to the transistor's gate. For symmetric drive strengths, it is acceptable to short OUTH and OUTL and use a single gate-drive resistor.

TI strongly recommends using at least a 2 Ω resistor at each OUTH and OUTL to avoid voltage overstress due to inductive ringing. Ringing overshoot must not exceed V_{DD} + 0.3 V.

For applications requiring smaller resistance values, contact TI E2E for guidance.

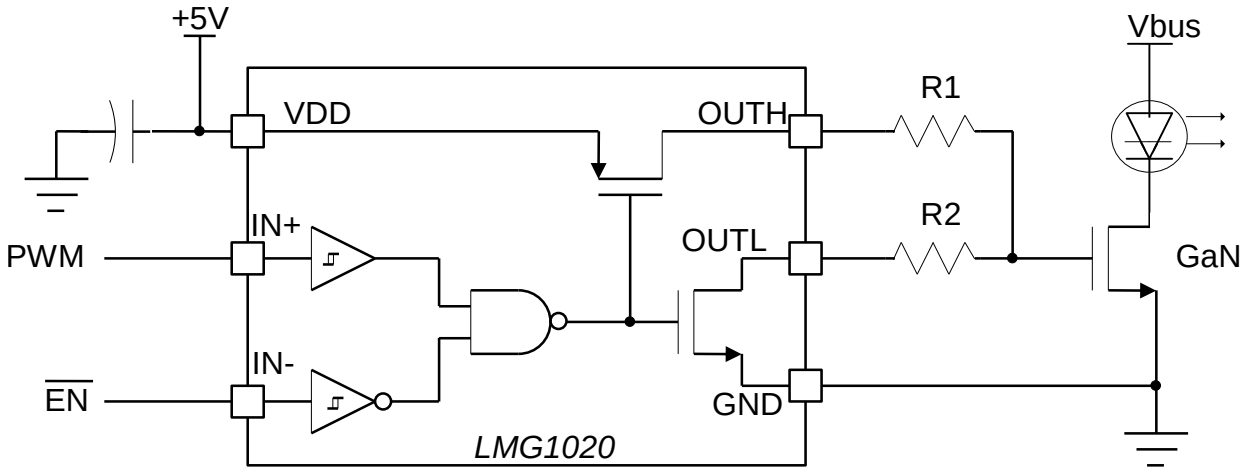

Figure 1. Typical Implementation of a Circuit

Typical Application (continued)

8.2.1 Design Requirements

When designing a multi-MHz (or nano-second pulse) application that incorporates the LMG1020 gate driver and GaN power FETs, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are layout optimization, circuit voltages, passive components, operating frequency, and controller selection.

8.2.2 Detailed Design Procedure

8.2.2.1 Using Source-Based Current Sense

As the input signals (IN+ and IN–) are referenced to the GND pin, it is important to consider the path between the power controller and the LMG1020. Excessive voltage drop in the ground path between the GND pin (typically connected to the transistor's source) and the controller ground may interfere with the operation of the circuit.

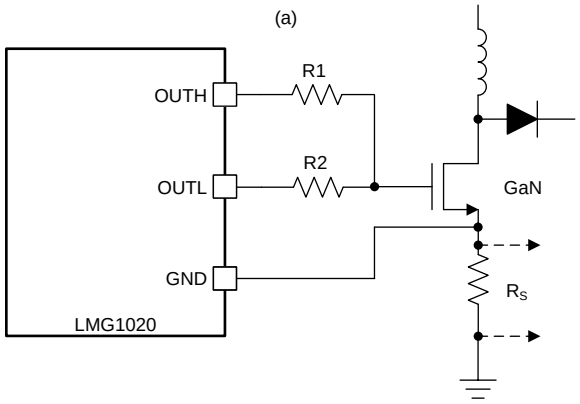

Figure 2. Source Resistor Current Sense A Configuration

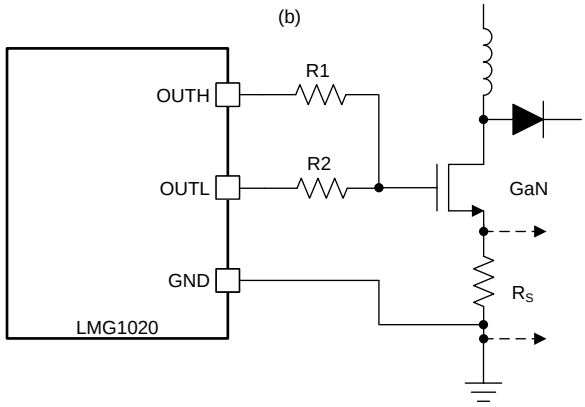

Figure 3. Source Resistor Current Sense B Configuration

Current sense through a source resistor as shown in Figure 2 is a common and inexpensive method of current sense. The DC voltage across this resistor can be made minimal and will not disrupt DC operations in either configuration. However, due to the fast switching of GaN and potentially very fast current slew rates, the inductance of the sense resistor can disrupt the operation of the circuit.

In configuration (a), the GND pin is connected to the transistor's source. In this case, a large di/dt may trigger the gate driver to produce a false pulse or oscillation. The maximum di/dt allowed to prevent the input voltage transient from exceeding the input hysteresis is given by Equation 1.

$$\frac{di_s}{dt} = \frac{V_{HYST}}{L_{RS}} \quad (1)$$

where

- L_{RS} is the inductance of the sense resistor,
- V_{HYST} is the hysteresis of the input pin,
- and $di_s/\Delta t$ is the maximum allowed current slew rate.

For a parasitic inductance of 0.5 nH and a minimum hysteresis of 0.5 V, the maximum slew rate is 1 A/ns. Many applications would exhibit higher current slew rates, up to the 10 A/ns range, which would make this approach impractical. For soft-switched applications, this approach can be used as long as the parasitic inductance is minimized through layout.

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Typical Application (continued)

The stability of this approach can be improved by using the IN– input for the PWM signal and locally tying IN+ to VDD. By using the inverting input, the transient voltage applied to the input pin reinforces the PWM signal in a positive feedback loop. While this approach would reduce the probability of false pulses or oscillation, the transient spikes due to high di/dt may overly stress the inputs to the LMG1020. A current-limiting, 100 Ω resistor can be placed right before the IN– input to limit excessive current spikes in the device.

Approach (b) places the current sense resistor within the gate drive loop path. In this case, the LMG1020 GND pin is connected to the signal ground, and with good ground plane connection, the input signals will not cause trouble to the operation of the LMG1020. However, the inductance of the current sense resistor adds common-source inductance to the gate drive loop. The voltage generated across the parasitic inductance will subtract from the gate-drive voltage of the FET, slowing down the turnon and turnoff di/dt of the FET. Additional gate resistance will have to be added to ensure the loop is stable and ring-free. The slower rise may negate the advantage of the fast switching of the GaN FET and may cause additional losses in the circuit.

9 Power Supply Recommendations

A low-ESR/ESL ceramic capacitor must be connected close to the IC, between V_{DD} and GND pins to support the high peak current being drawn from V_{DD} during turnon of the FETs. It is most desirable to place the V_{DD} decoupling capacitor on the same side of the PC board as the driver. The inductance of via holes can impose excessive ringing on the IC pins.

10 Layout

10.1 Layout Guidelines

The layout of the LMG1020 is critical to its performance and functionality. The LMG1020 is available in a WCSP ball-grid array package, which enables low-inductance connection to a BGA-type GaN FET. Figure 4 shows the recommended layout of the LMG1020 with a ball-grid array GaN FET.

A four-layer or higher layer count board is required to reduce the parasitic inductances of the layout to achieve suitable performance. To minimize inductance and board space, resistors and capacitors in the 0201 package are used here. The gate drive power loss must be calculated to ensure an 0201 resistor will be able to handle the power level.

10.1.1 Gate Drive Loop Inductance and Ground Connection

A compact, low-inductance gate-drive loop is essential to achieving fast switching frequencies with the LMG1020. The LMG1020 should be placed as close to the GaN FET as possible, with gate drive resistors R1 and R2 immediately connecting OUTH and OUTL to the FET gate. Large traces must be used to minimize resistance and parasitic inductance.

To minimize gate drive loop inductance, the source return should be on layer 2 of the PCB, immediately under the component (top) layer. Vias immediately adjacent to both the FET source and the LMG1020 GND pin connect to this plane with minimal impedance. Finally, take care to connect the GND plane to the source power plane only at the FET to minimize common-source inductance and to reduce coupling to the ground plane.

10.1.2 Bypass Capacitor

The VDD power terminal of the LMG1020 must by bypassed to ground immediately adjacent to the IC. Because of the fast gate drive of the IC, the placement and value of the bypass capacitor is critical. The bypass capacitor must be place on the top layer, as close as possible to the IC, and connected to both VDD and GND using large power planes. This bypass capacitor has to be at least a 0.1 µF, up to 1 µF, with temperature coefficient X7R or better. Recommended body types are LICC, IDC, Feed-though, and LGA. Finally, an additional 1 µF capacitor (not shown in) must be placed as close to the IC as practical.

10.2 Layout Example

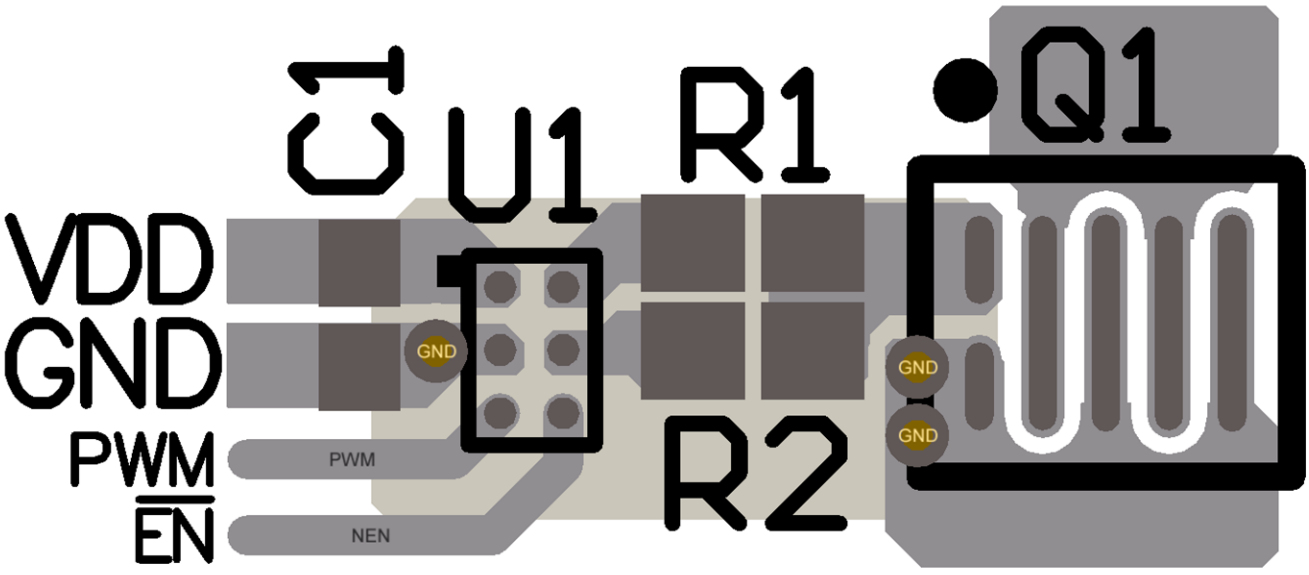

Figure 4. Typical LMG1020 Layout With Ball-Grid GaN FET

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Using the LMG1020-EVM Nano-second LiDAR EVM* (SNOU150)
- *LMG1020 PSpice Transient Model* (SNOM618)
- *LMG1020 TINA-TI Reference Design* (SNOM619)
- *LMG1020 TINA-TI Transient Spice Model* (SNOM620)
- *LMG1020EVM Altium Design Files* (SNOR025)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMG1020YFFR	PREVIEW	DSBGA	YFF	6	3000	TBD	Call TI	Call TI	-40 to 125		
LMG1020YFFT	PREVIEW	DSBGA	YFF	6	250	TBD	Call TI	Call TI	-40 to 125		
XLMG1020YFFT	ACTIVE	DSBGA	YFF	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

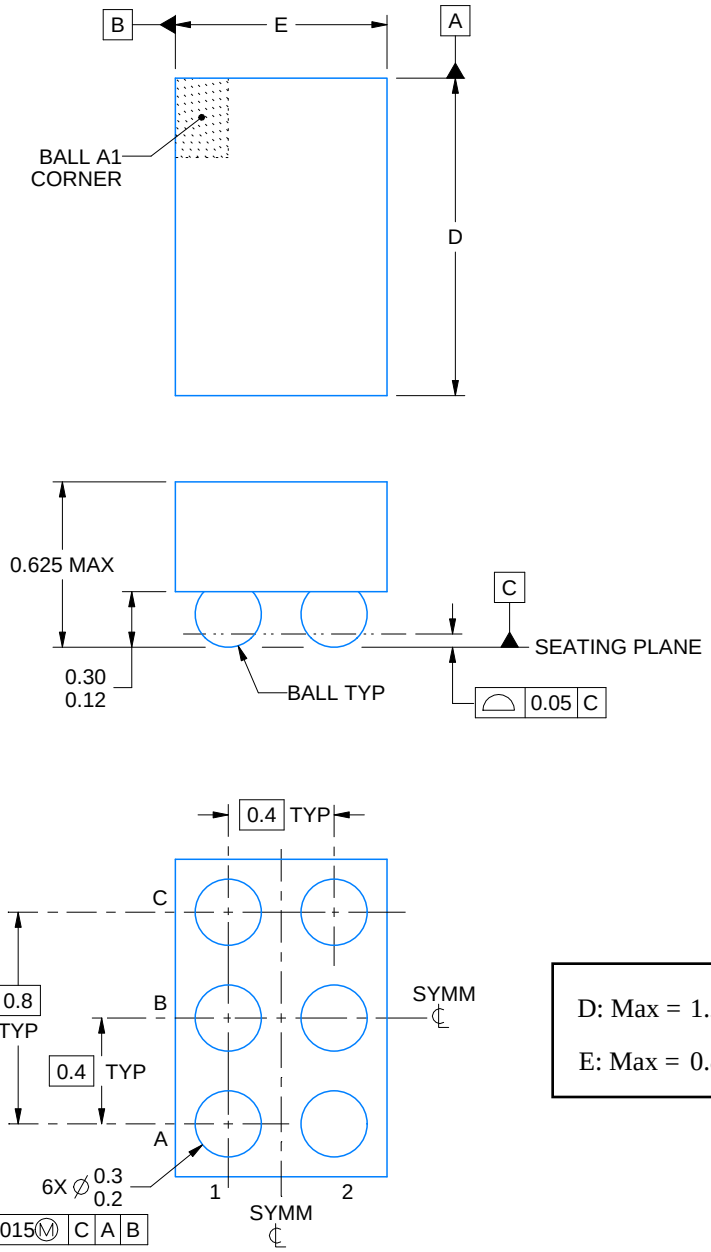
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



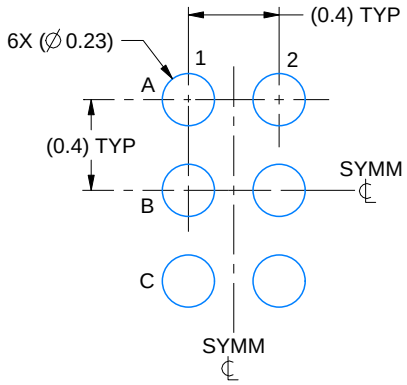
D: Max = 1.285 mm, Min =1.225 mm

E: Max = 0.885 mm, Min =0.825 mm

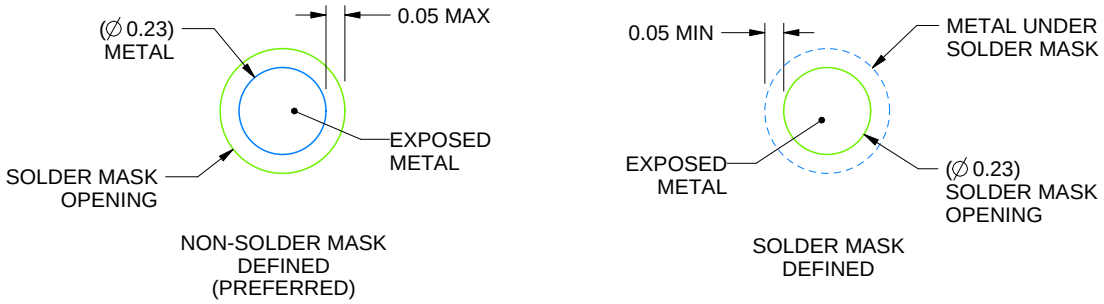
4223785/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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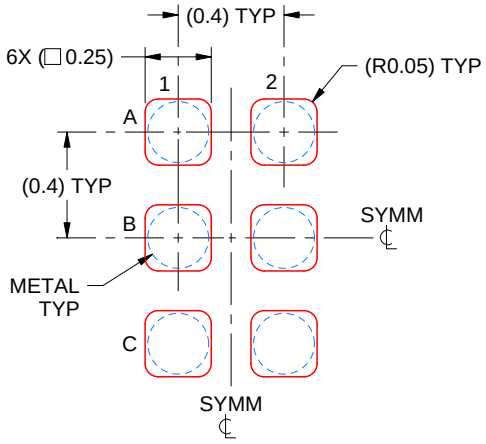
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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