LM5160-Q1 Wide Input 65-V, 1.5-A Synchronous Buck / Fly-Buck™ Converter

1 Features

- AEC-Q100 Grade 1 Qualified with the following results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide 4.5-V to 65-V Input Voltage Range
- Integrated High and Low Side Switches
  - No Schottky Diode Required
- 1.5-A Maximum Load Current
- Constant On-Time Control
  - No External Loop Compensation
  - Fast Transient Response
- Selectable Forced CCM or DCM Operation
- CCM Option Supports Multi-Output Fly-Buck
- Nearly Constant Switching Frequency
- Frequency Adjustable up to 1 MHz
- Programmable Soft-Start Time
- Pre-Biased Startup
- Peak Current Limiting Protection
- Adjustable Input UVLO and Hysteresis
- ±1% Feedback Voltage Reference
- Thermal Shutdown Protection

2 Applications

- Industrial Programmable Logic Controller
- IGBT Gate Drive Bias Supply
- Telecom Primary/Secondary Side Bias
- E-meter Power Line Communication
- Low Power Isolated DC-DC (Fly-Buck)
- Automotive Electronics

3 Description

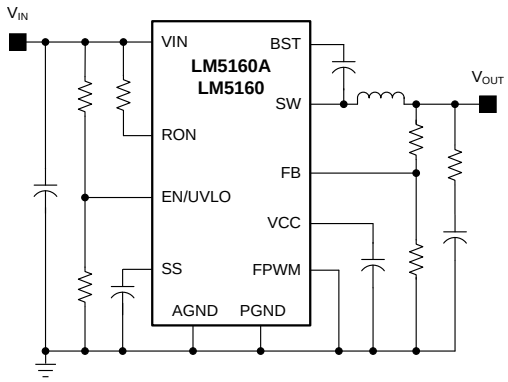
The LM5160 family is a 65-V, 1.5-A synchronous step-down converter with integrated high-side and low-side MOSFETs. The constant-on-time control scheme requires no loop compensation and supports high step-down ratios with fast transient response. An internal feedback amplifier maintains ±1% output voltage regulation over the entire operating temperature range. The on-time varies inversely with input voltage resulting in nearly constant switching frequency. Peak and valley current limit circuits protect against overload conditions. The under-voltage lockout (EN/UVLO) circuit provides independently adjustable input under-voltage threshold and hysteresis. The LM5160 is programmed through the FPWM pin to operate in continuous conduction mode (CCM) from no load to full load or to automatically switch to discontinuous conduction mode (DCM) at light load for higher efficiency. Forced CCM operation supports multiple output and isolated Fly-Buck applications using a coupled inductor.

Device Information[1]

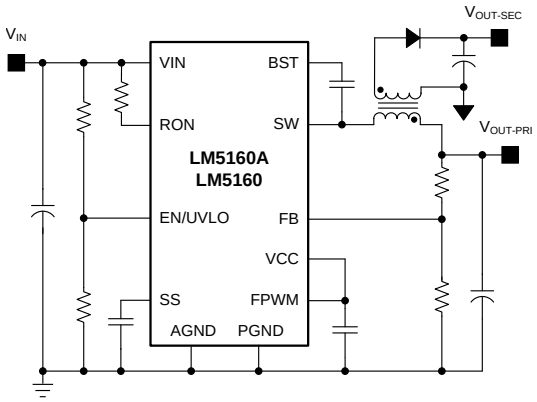
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5160-Q1	HTSSOP (14) PWP	4.4 mm x 5.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Sync-Buck Application Circuit



Typical Fly-Buck Application Circuit



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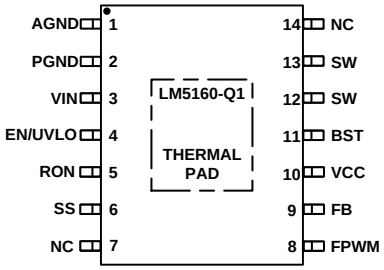
4 Revision History

Changes from Original (July 2015) to Revision A **Page**

- Changed current limit off-timer in the Electrical Characteristics to 16 ... 6

5 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NUMBER		
	HTSSOP	WSON	
AGND	1	1	Analog Ground. Ground connection of internal control circuits.
PGND	2	2	Power Ground. Ground connection of the internal synchronous rectifier FET.
VIN	3	3	Input supply connection. Operating input range is 4.5 V to 65 V.
EN/UVLO	4	4	Precision enable. Input pin of under-voltage lockout (UVLO) comparator.
RON	5	5	On-time programming pin. A resistor between this pin and VIN sets the switch on-time as a function of input voltage.
SS	6	6	Soft-start. Connect a capacitor from SS to AGND to control output rise time and limit overshoot.
FPWM	8	7	Forced PWM logic input pin. Connect to AGND for discontinuous conduction mode (DCM) with light loads. Connect to VCC for continuous conduction mode (CCM) at all loads and Fly-Buck configuration.
FB	9	8	Feedback input of voltage regulation comparator.
VCC	10	9	Internal high voltage startup regulator bypass capacitor pin.
BST	11	10	Bootstrap capacitor pin. Connect a capacitor between BST and SW to bias gate driver of high side buck FET.
SW	12,13	11,12	Switch node. Source connection of high side buck FET and drain connection of low side synchronous rectifier FET.
NC	7,14	-	No Connection.
EP			Exposed Pad. Connect to AGND and printed circuit board ground plane to improve power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Input Voltage	VIN to AGND	–0.3	70	V
	EN/UVLO to AGND	–0.3	70	
	RON to AGND	-0.3	70	
	BST to AGND	-0.3	84	
	VCC to AGND	-0.3	14	
	FPWM to AGND	-0.3	14	
	SS to AGND	-0.3	7	
	FB to AGND	-0.3	7	
Output Voltage	BST to SW	-0.3	14	V
	BST to VCC		70	
	SW to AGND	–1.5	70	
	SW to AGND (20 ns transient)	–3		
Lead Temperature(4)			200	°C
Maximum Junction Temperature(3)		–40	150	
Storage temperature range T_{STG}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

(4) For detailed information on soldering plastic SO PowerPAD package, refer to the SNOA549 available from Texas Instruments. Maximum solder time not to exceed 4 seconds.

6.2 ESD Ratings: LM5160-Q1

		VALUE	UNIT
$V_{(ESD)}$	Human body model (HBM), per AEC Q100-002(1)	±2000	V
	Charged device model (CDM), per AEC Q100-011	±750	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN} Input Voltage	4.5		65	V
I_O Output Current			1.5	A
Operating Junction Temperature(2) (LM5160-Q1 only)	-40		150	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information(1)

THERMAL METRIC		LM5160, LM5160-Q1		UNIT
		PWP (HTSSOP)	DNT (WSON)	
		14 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	39.3	33.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance(1)	2.0	1.9	
ψ_{JB}	Junction-to-board thermal characteristic parameter	19.3	11.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	19.6	11.1	
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	22.8	24.7	
ψ_{JT}	Junction-to-top thermal characteristic parameter	0.5	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C[1][2] for the LM5160-Q1. Unless otherwise stated, V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{SD}	Input Shutdown Current	V_{IN} = 24 V, EN/UVLO = 0 V		50	90.7	µA
I_{OP}	Input Operating Current	V_{IN} = 24 V, FB = 3 V, Non-switching		2.3	2.84	mA
VCC SUPPLY						
V_{CC}	Bias Regulator Output	V_{IN} = 24 V, I_{CC} = 20 mA	6.47	7.5	8.52	V
V_{CC}	Bias Regulator Current Limit	V_{IN} = 24 V	30			mA
$V_{CC(UV)}$	VCC Undervoltage Threshold	V_{CC} rising		3.98	4.1	V
$V_{CC(HYS)}$	VCC Undervoltage Hysteresis	V_{CC} falling		185		mV
$V_{CC(LDO)}$	VIN - VCC Dropout Voltage	V_{IN} = 4.5 V, I_{CC} = 20 mA		165	260	mV
HIGH-SIDE FET						
$R_{DS(ON)}$	High Side On Resistance	$V_{(BST - SW)}$ = 7 V, I_{SW} = 1 A		0.29		Ω
$BST_{(UV)}$	Bootstrap Gate Drive UV	$V_{(BST - SW)}$ rising		2.93	3.6	V
$BST_{(HYS)}$	Gate Drive UV hysteresis	$V_{(BST - SW)}$ falling		200		mV
LOW-SIDE FET						
$R_{DS(ON)}$	Low Side On Resistance	I_{SW} = 1 A		0.13		Ω
HIGH SIDE CURRENT LIMIT						
$I_{LIM\ (HS)}$	High Side Current Limit Threshold		2.125	2.5	2.875	A
T_{RES}	Current Limit Response Time	$I_{LIM\ (HS)}$Threshold detect to FET Turn-off		100		ns
T_{OFF1}	Current Limit Forced Off-Time	FB = 0 V, VIN = 65 V	16	29	39.8	µs
T_{OFF2}	Current Limit Forced Off-Time	FB = 1 V, VIN = 24 V	2.18	3.5	5.12	µs
LOW SIDE CURRENT LIMIT						
$I_{SOURCE(LS)}$	Sourcing Current Limit		1.9	2.5	3.0	A
$I_{SINK(LS)}$	Sinking Current Limit			5.4		
DIODE EMULATION						
$V_{FPWM(LOW)}$	FPWM Input Logic Low	V_{IN} = 24 V			1	V
$V_{FPWM(HIGH)}$	FPWM Input Logic High	V_{IN} = 24 V	3			
I_{ZX}	Zero Cross Detect Current	FPWM = 0 (Diode Emulation)		0		mA
REGULATION COMPARATOR						
V_{REF}	FB Regulation Level	V_{IN} = 24 V (WSON-12)	1.977	2	2.017	V
		V_{IN} = 24 V (HTSSOP-14)	1.975	1.995	2.015	
$I_{(Bias)}$	FB Input Bias Current	V_{IN} = 24 V			100	nA
ERROR CORRECTION AMPLIFIER & SOFT-START						
G_M	Error Amp Transconductance	FB = V_{REF} (+/–) 10 mV		105		µA/V
$I_{EA(Source)}$	Error Amp Source Current	FB = 1 V, SS = 1 V	7.62	10.2	12.51	µA
$I_{EA(Sink)}$	Error Amp Sink Current	FB = 5 V, SS = 2.25 V	7.46	10	12.2	
$V_{(SS-FB)}$	V_{SS} - V_{FB} Clamp Voltage	FB = 1.75 V, C_{SS}= 1 nF		135		mV
I_{SS}	Soft-Start Charging current	SS = 0.5 V	7.63	10.2	12.5	µA
ENABLE/UVLO						
$V_{UVLO\ (TH)}$	UVLO Threshold	EN/UVLO rising	1.213	1.24	1.277	V
$I_{UVLO(HYS)}$	UVLO Hysteresis Current	EN/UVLO = 1.4 V	15	20	25	µA
$V_{SD(TH)}$	Shutdown Mode Threshold	EN/UVLO falling	0.28	0.35		V
$V_{SD(HYS)}$	Shutdown Threshold Hysteresis	EN/UVLO rising		47		mV
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			175		°C
$T_{SD(HYS)}$	Thermal Shutdown Hysteresis			20		

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \bullet R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in the Thermal Information section.

6.6 Switching Characteristics(1)

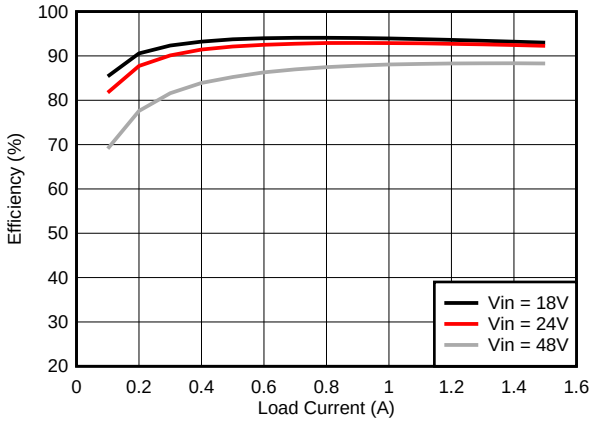
Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over T_J = –40°C to 125°C for the LM5160-Q1. Unless otherwise stated, V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MINIMUM OFF-TIME						
$T_{OFF-MIN}$	Minimum Off-Time, FB = 0 V			170		ns
ON-TIME GENERATOR						
T_{ON} Test 1	VIN = 24 V, RON = 100 kΩ		312	428	520	ns
T_{ON} Test 2	VIN = 24 V, RON = 200 kΩ		625	818	1040	
T_{ON} Test 3	VIN = 8 V, RON = 100 kΩ		937	1247	1563	
T_{ON} Test 4	VIN = 65 V, RON = 100 kΩ		132	176	220	

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

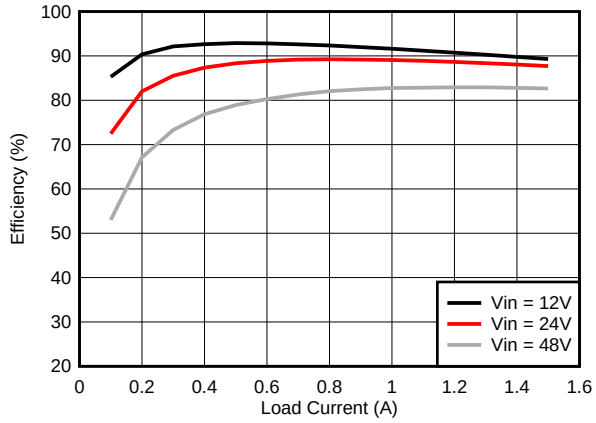
6.7 Typical Characteristics

At T_A = 25°C and applicable to LM5160-Q1, unless otherwise noted.



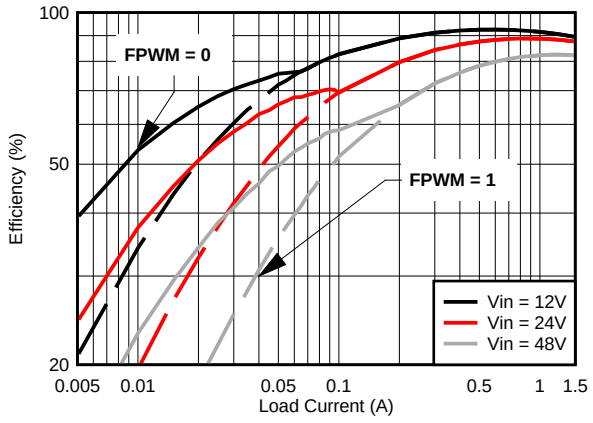
V_{Out}= 10V R_{On}=200kΩ
L=47µH

Figure 1. Efficiency at 500 kHz



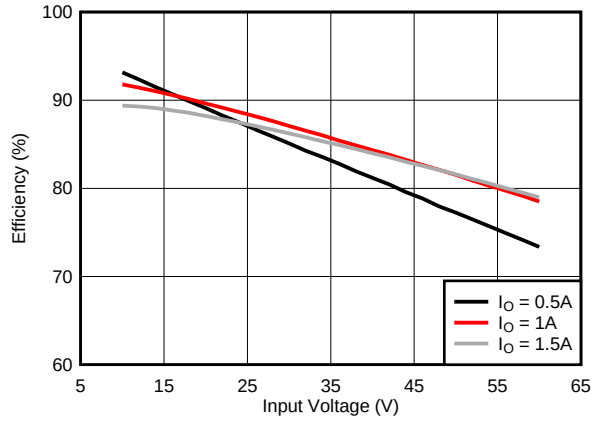
V_{Out}= 5V R_{On}=215kΩ
L=100µH

Figure 2. Efficiency at 250 kHz



V_{Out}= 5V R_{On}=169kΩ
L=47µH F_{SW}=300 kHz

Figure 3. Efficiency CCM vs. DCM at 300kHz



V_{Out}= 5V R_{On}=169kΩ
L=47µH

Figure 4. Efficiency vs. Input Voltage at 300kHz

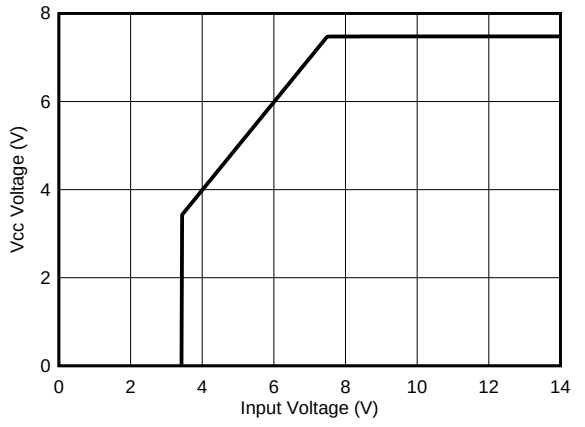
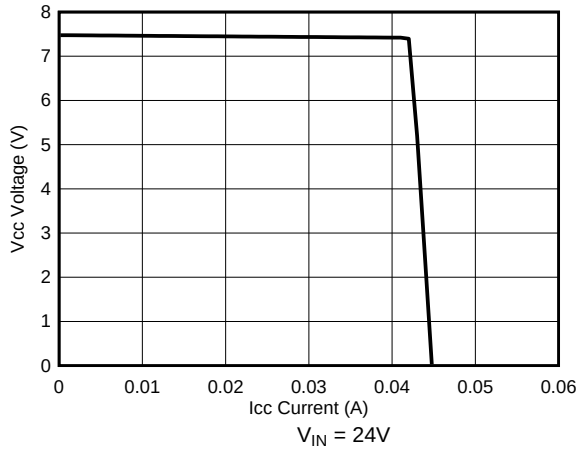


Figure 5. V_{CC} vs. V_{IN}



V_{IN} = 24V

Figure 6. V_{CC} vs. I_{CC}

Typical Characteristics (continued)

At T_A = 25°C and applicable to LM5160-Q1, unless otherwise noted.

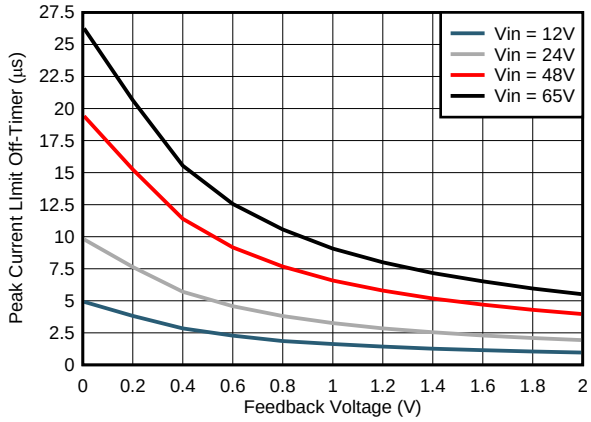


Figure 7. T_{OFF} (I_{LIM}) vs. V_{FB}

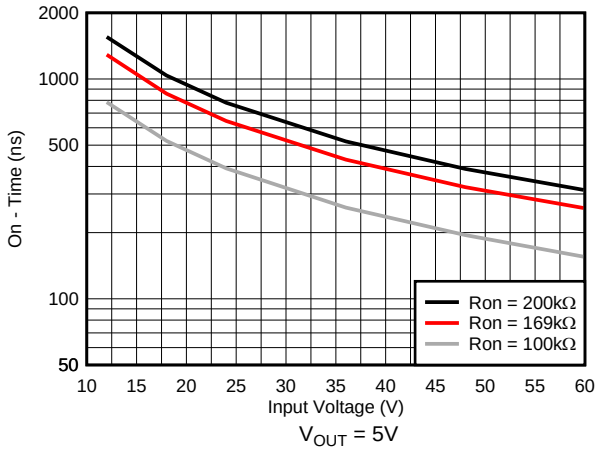


Figure 8. T_{ON} vs. V_{IN}

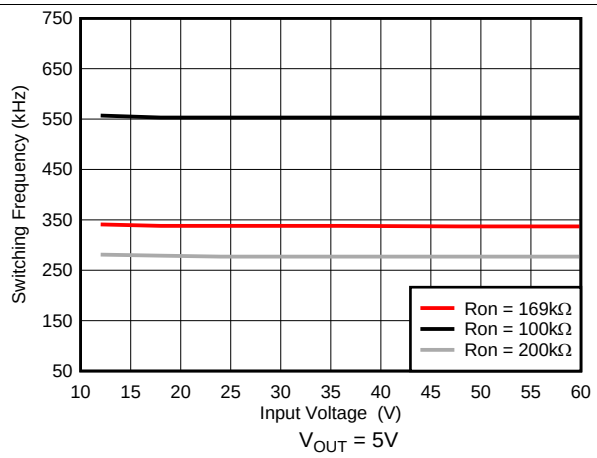


Figure 9. Switching Frequency vs. V_{IN}

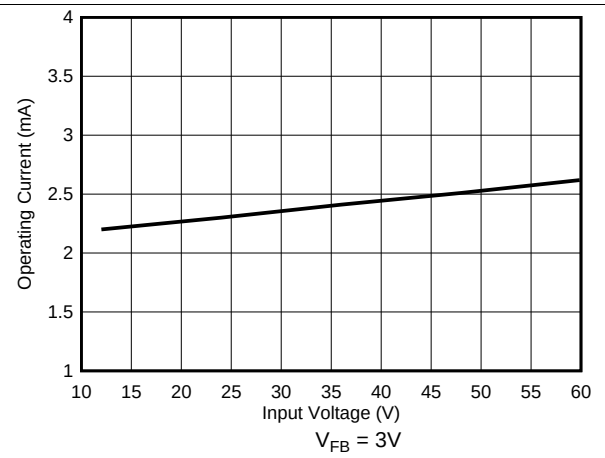


Figure 10. I_{IN} vs. V_{IN} (Operating, Non Switching)

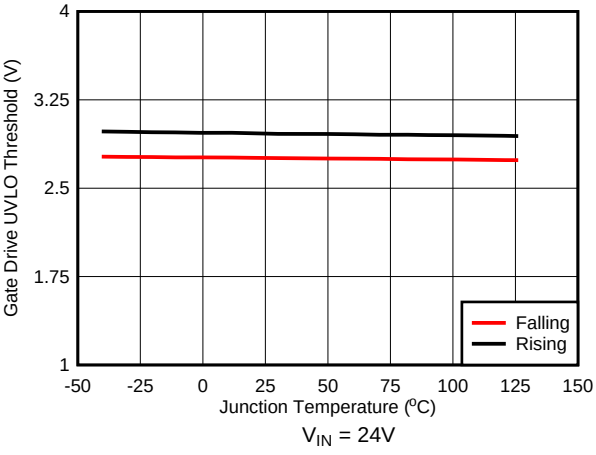


Figure 11. Gate Drive UVLO vs. Temperature

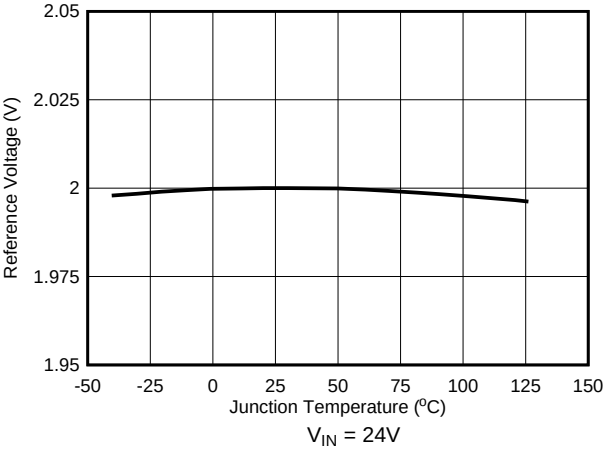


Figure 12. Reference Voltage vs. Temperature

Typical Characteristics (continued)

At T_A = 25°C and applicable to LM5160-Q1, unless otherwise noted.

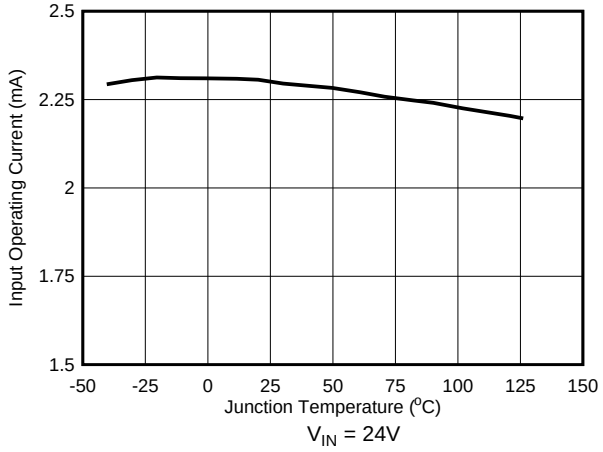


Figure 13. Input Operating Current vs. Temperature

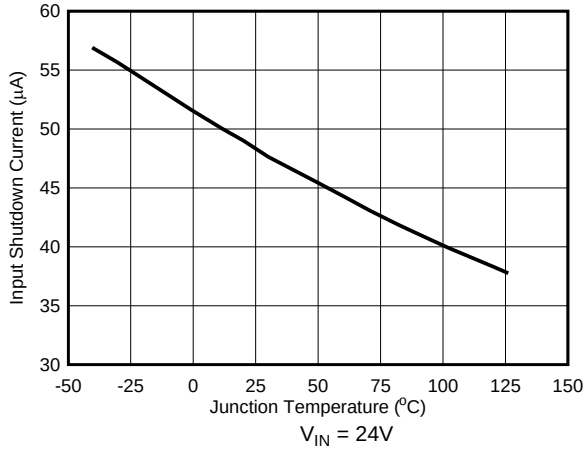


Figure 14. Input Shutdown Current vs. Temperature

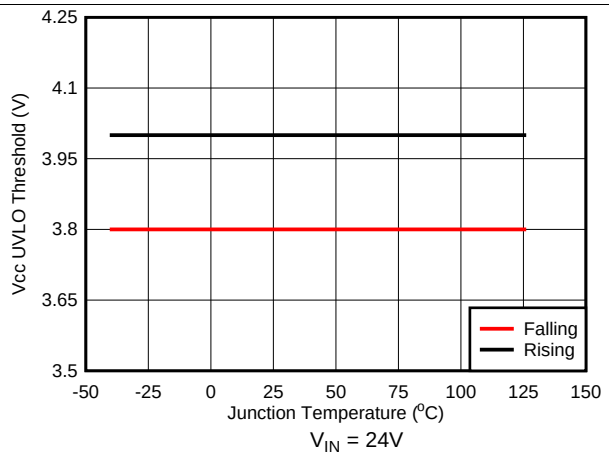


Figure 15. V_{CC} UVLO vs. Temperature

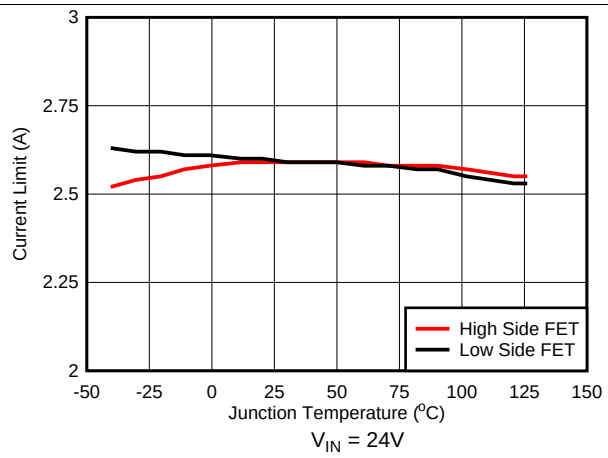


Figure 16. Current Limit vs. Temperature

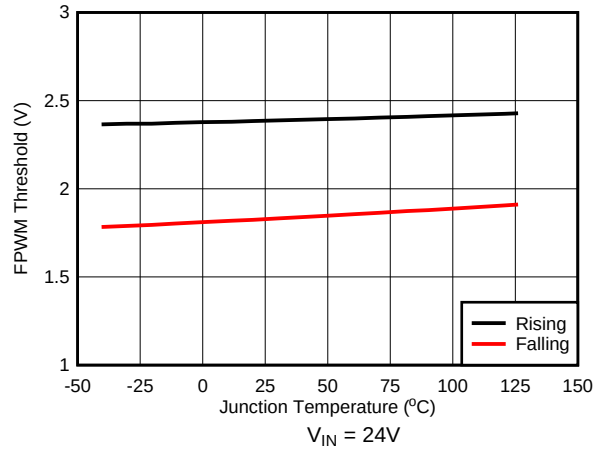


Figure 17. FPWM Threshold vs. Temperature

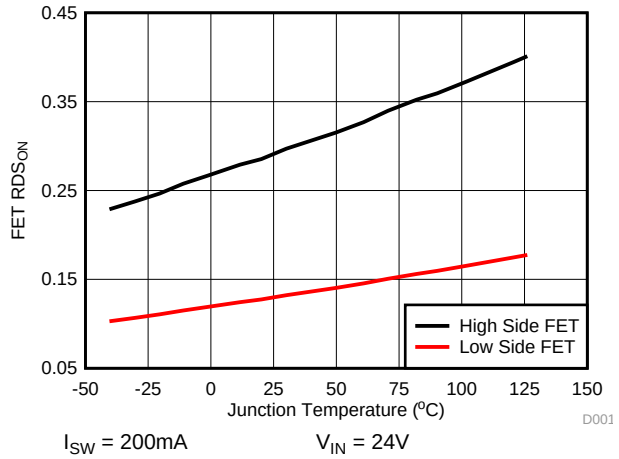


Figure 18. Switch Resistance vs. Temperature

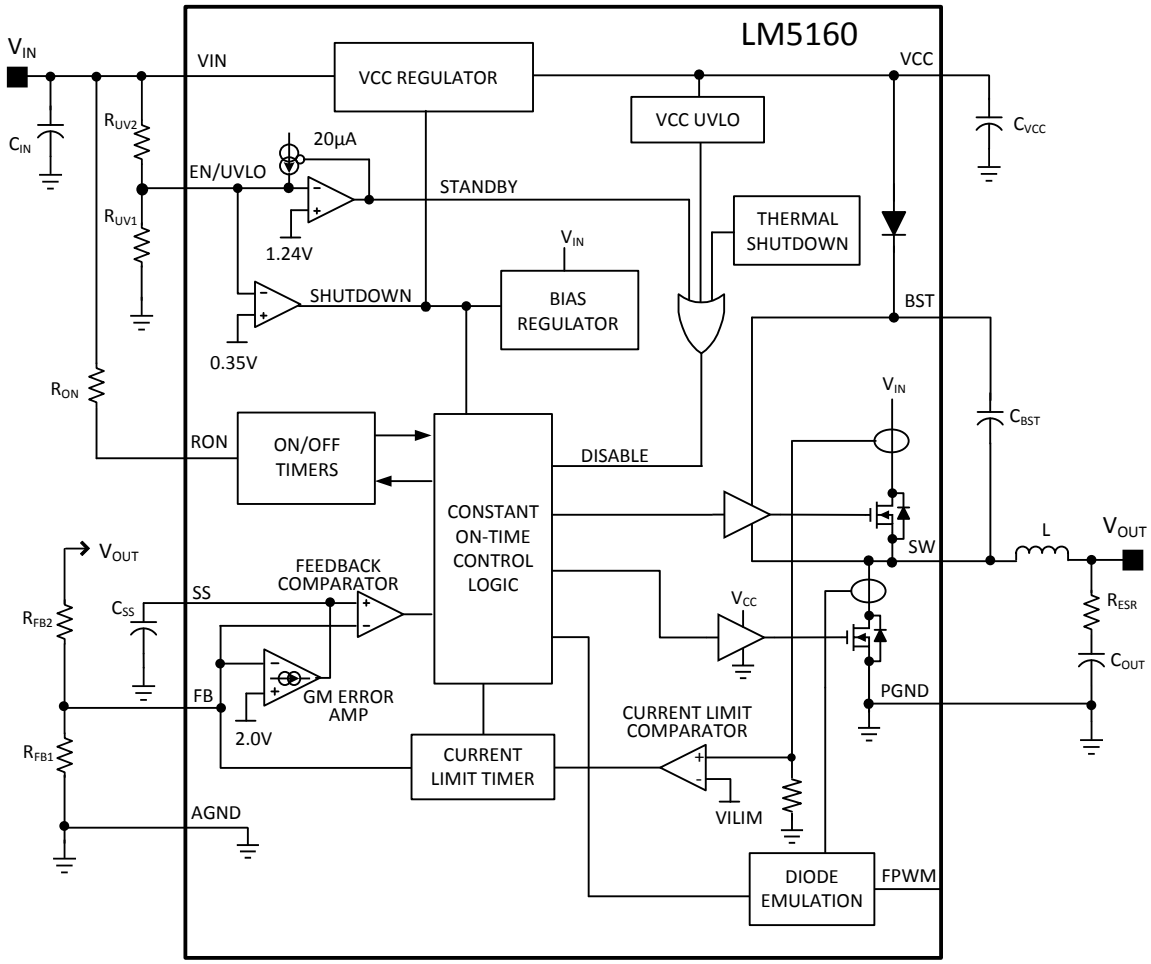
7 Detailed Description

7.1 Overview

The LM5160 family of step-down switching regulators features all the functions needed to implement a low cost, efficient buck converter capable of supplying 1.5 A to the load. This high voltage regulator contains 65-V N-Channel buck and synchronous rectifier switches and is available in the WSON-12 package. The LM5160-Q1 is available in the HTSSOP-14 package. The regulator operation is based on constant on-time control where the on-time is inversely proportional to input voltage V_{IN}. This feature maintains a relatively constant operating frequency with load and input voltage variations. A constant on-time switching regulator requires no loop compensation resulting in fast load transient response. Peak current limit detection circuit is implemented with a forced off-time during current limiting which is inversely proportional to voltage at the feedback pin, V_{FB} and directly proportional to V_{IN}. Varying the current limit off-time with V_{FB} and V_{IN} ensures short circuit protection with minimal current limit foldback. The LM5160 can be applied in numerous end equipment systems requiring efficient step-down regulation from higher input voltages. This regulator is well suited for 24 V industrial systems as well as 48 V telecom and PoE voltage ranges. The LM5160 integrates an under-voltage lockout (EN/UVLO) circuit to prevent faulty operation of the device at low input voltages and features intelligent current limit and thermal shutdown to protect the device during overload or short circuit.

The LM5160 device name is used generically throughout this document and represents both the LM5160-Q1 and LM5160A unless stated otherwise. The only difference between the two is the ability to connect an external voltage source to the VCC pin of the LM5160A.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Circuit

The LM5160 step-down switching regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to the voltage at the Soft-Start (SS) pin (V_{SS}). If the FB voltage is below V_{SS}, the internal buck switch is turned on for a time period determined by the input voltage and one-shot programming resistor (R_{ON}). Following the on-time, the buck switch must remain off for the minimum off-time forced by the minimum off-time one-shot. The buck switch remains off until the FB voltage falls below the Soft-Start again, when it turns back on for another on-time one-shot period.

During a rapid start-up or when the load current increases suddenly, the regulator will operate with minimum off-time per cycle. When regulating the output in steady state operation, the off-time will automatically adjust to produce the SW pin duty cycle required for output voltage regulation.

When in regulation, the LM5160 operates in continuous conduction mode at heavy load currents. If the FPWM pin is connected to ground or left floating, the regulator will operate in discontinuous conduction mode at light load with the synchronous rectifier FET in diode emulation. With sufficient load, the LM5160 operates in continuous conduction mode with the inductor current never reaching zero during the off-time of the high side FET. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The operating frequency is programmed by the R_{ON} pin resistor and can be calculated from Equation 1 with R_{ON} expressed in ohms.

$$F_{sw} = \frac{V_{OUT}}{R_{ON} \times 1 \times 10^{-10}} \text{ Hz} \tag{1}$$

In discontinuous conduction mode, current through the inductor ramps up from zero to a peak value during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below V_{SS}. When the inductor current is zero during the high side FET off-time, the load current is supplied by the output capacitor. In this mode, the operating switching frequency is lower than the continuous conduction mode switching frequency and the frequency varies with load. The discontinuous conduction mode maintains conversion efficiency at light loads since the switching losses decrease with the decrease in load and frequency.

The output voltage is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated from Equation 2, where V_{REF} = 2 V (typ) is the feedback reference voltage.

$$V_{OUT} = \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} \text{ V} \tag{2}$$

7.3.2 VCC Regulator

The LM5160 contains an internal high voltage linear regulator with a nominal output voltage of 7.5 V (typ). The VCC regulator is internally current limited to 30 mA (minimum). This regulator supplies power to internal circuit blocks including the synchronous FET gate driver and the logic circuits. When the voltage on the VCC pin reaches the under-voltage lockout ($V_{CC(UV)}$) threshold of 3.98 V (typ), the IC is enabled. An external capacitor at the VCC pin stabilizes the regulator and supplies transient VCC current to the gate drivers. An internal diode connected from VCC to the BST pin replenishes the charge in the high side gate drive bootstrap capacitor when the SW pin is low.

In high input voltage applications, the power dissipated in the regulator is significant and can limit the efficiency and maximum achievable output power. The LM5160A allows the internal VCC regulator power loss to be reduced by supplying the VCC voltage via a diode from an external voltage source regulated between 9V and 13 V. The external VCC bias can be supplied from the LM5160A converter output rail if the regulation voltage is within this range. When the VCC pin of the LM5160A is raised above the regulation voltage (7.5 V typical), the internal regulator is disabled and the power dissipation in the IC is reduced. The only difference between the LM5160 and LM5160A is wide operating V_{CC} voltage range of the LM5160A.

Feature Description (continued)

7.3.3 Regulation Comparator

The feedback voltage at the FB pin is compared to the SS pin voltage V_{SS}. In normal operation when the output voltage is in regulation, an on-time period is initiated when the voltage at FB pin falls below V_{SS}. The high side buck switch will stay on for the on-time one-shot period causing the FB voltage to rise. After the on-time period expires, the high side switch will remain off until the FB voltage falls below V_{SS}. During the startup, the FB voltage will be below V_{SS} at the end of each on-time period and the high side switch turns on again after the minimum forced off-time of 170 ns (typ). When the output is shorted to ground (FB = 0 V), the high side peak current limit is triggered, the high side FET is turned off, and remains off for a period determined by the current limit off-timer. See the *Current Limit* section for additional information.

7.3.4 Soft-Start

The soft-start feature of the LM5160 allows the converter to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. When the EN/UVLO pin is above the EN/UVLO standby threshold $V_{UVLO(TH)}$ = 1.24 V (typ) and the VCC exceeds the VCC under-voltage $V_{CC(UV)}$ = 3.98 V (typ) threshold, an internal 10 µA current source charges the external capacitor at the SS pin (C_{SS}) from 0 V to 2 V. The voltage at the SS pin is the non-inverting input of the internal FB comparator. The soft-start interval ends when the SS capacitor is charged to the 2V reference level. The ramping voltage at the SS pin produces a controlled, monotonic output voltage start-up. A minimum 1 nF soft-start capacitor should be used in all applications.

7.3.5 Error Transconductance (G_M) Amplifier

The LM5160 provides a trans-conductance (G_M) error amplifier that minimizes the difference between the reference voltage (V_{REF}) and the average feedback (FB) voltage. This amplifier reduces the load and line regulation errors that are common in constant-on-time regulators. The soft-start capacitor (C_{SS}) provides compensation for this error correction loop. The soft-start capacitor should be greater than 1 nF to ensure stability.

7.3.6 On-Time Generator

The on-time of the LM5160 high side FET is determined by the R_{ON} resistor and is inversely proportional to the input voltage (V_{IN}). The inverse relationship with V_{IN} results in a nearly constant frequency as V_{IN} is varied. The on-time can be calculated from Equation 3 with R_{ON} expressed in ohms.

$$T_{ON} = \frac{R_{ON} \times 1 \times 10^{-10}}{V_{IN}} \text{ s} \tag{3}$$

To set a specific continuous conduction mode switching frequency (F_{SW} expressed in Hz), the R_{ON} resistor is determined from the following:

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 1 \times 10^{-10}} \ \Omega \tag{4}$$

R_{ON} should be selected for a minimum on-time (at maximum V_{IN}) greater than 150 ns for proper operation. This minimum on-time requirement will limit the maximum switching frequency of applications with relatively high V_{IN} and low V_{OUT}.

7.3.7 Current Limit

The LM5160 provides an intelligent current limit off-timer that adjusts the off-time to reduce the foldback in the current limit. If the peak value of the current in the buck switch exceeds 2.5 A (typ) the present on-time period is immediately terminated, and a non-resettable off-timer is initiated. The length of the off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when V_{FB} = 0 V and V_{IN} = 24 V, the off-time is set to 10 µs. This condition would occur if the output is shorted or during the initial phase of start-up. In cases of output overload where the FB voltage is greater than zero volts (a soft short), the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the current limit foldback, overload recovery time, and start-up time. The current limit off-time, $T_{OFF(CL)}$ is calculated from Equation 5:

$$T_{OFF(CL)} = \frac{5V_{IN}}{24V_{FB} + 12} \ \mu\text{s} \tag{5}$$

Feature Description (continued)

7.3.8 N-Channel Buck Switch and Driver

The LM5160 integrates an N-Channel buck switch and associated floating high side gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage bootstrap diode. A 10 nF or larger ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the high-side driver during the buck switch on-time. During the off-time, the SW node is pulled down to approximately 0 V and the bootstrap capacitor charges from VCC through the internal bootstrap diode. The minimum off-time of 170 ns (typ) provides a minimum time each cycle to recharge the bootstrap capacitor.

7.3.9 Synchronous Rectifier

The LM5160 provides an internal low side synchronous rectifier N-Channel FET. This low side FET provides a low resistance path for the inductor current when the high-side FET is turned off.

With the FPWM pin connected to ground or left floating, the LM5160 synchronous rectifier operates in diode emulation mode. Diode emulation enables the pulse-skipping during light load conditions. This leads to a reduction in the average switching frequency at light loads. Switching losses and FET gate driver losses, both of which are proportional to switching frequency, are significantly reduced and efficiency is improved. This pulse-skipping mode also reduces the circulating inductor currents and losses associated with a continuous conduction mode (CCM).

When the FPWM pin is pulled high, diode emulation is disabled. The inductor current can flow in either direction through the low side FET resulting in CCM operation with nearly constant switching frequency. A negative sink current limit circuit limits the current that can flow into the SW pin and through the low side FET to ground. In a buck regulator application, large negative current will only flow from V_{OUT} to the SW pin if V_{OUT} is lifted above the output regulation set-point.

7.3.10 Enable / Under-Voltage Lockout (EN/UVLO)

The LM5160 contains a dual level under-voltage lockout (EN/UVLO) circuit. When the EN/UVLO pin voltage is below 0.35 V, the regulator is in a low current shutdown mode. When the EN/UVLO pin voltage is greater than 0.35 V (typ.) but less than 1.24 V (typ.), the regulator is in standby mode. In standby mode, the VCC bias regulator is active but converter switching remains disabled. When the voltage at the VCC pin exceeds the VCC rising threshold $V_{CC(UV)}$ = 3.98 V (typ) and the EN/UVLO pin voltage is greater than 1.24 V, normal switching operation begins. An external resistor voltage divider from VIN to GND can be used to set the minimum operating voltage of the regulator.

EN/UVLO hysteresis is accomplished with an internal 20 µA (typ) current source ($I_{UVLO(HYS)}$) that is switched on or off into the impedance of the EN/UVLO pin resistor divider. When the EN/UVLO threshold is exceeded, the current source is activated to effectively raise the voltage at the EN/UVLO pin. The hysteresis is equal to the value of this current times the upper resistance of the resistor divider, (R_{UV2}) (See *Functional Block Diagram*).

7.3.11 Thermal Protection

The LM5160 should be operated such that the junction temperature does not exceed 150 °C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM5160 in the event of a higher than normal junction temperature. When activated, typically at 175 °C, the controller is forced into a low power reset state, disabling the high side buck switch and the VCC regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature falls below 155 °C (typical hysteresis = 20 °C), the VCC regulator is enabled, and operation resumes.

7.4 Device Functional Modes

7.4.1 Forced Pulse Width Modulation (FPWM) Mode

The *Synchronous Rectifier* section gives a brief introduction to the LM5160 diode emulation feature. The FPWM pin allows the power supply designer to select either CCM or DCM mode of operation at light loads. When the FPWM pin is connected to ground or left floating (FPWM = 0), a pulse-skipping mode is enabled and a zero-cross current detector circuit is enabled. The zero-cross detector will turn off the low side FET when the inductor current falls to zero (I_{ZX}, see *Electrical Characteristics*). This feature allows the LM5160 regulator to operate in DCM mode at light loads. In the DCM state, the switching frequency will decrease with lighter loads.

Device Functional Modes (continued)

If the FPWM pin is pulled high (FPWM connected to VCC), the LM5160 will operate in CCM mode even at light loads. This option allows the synchronous rectifier FET to conduct continuously until the start of the next high side switch cycle. The inductor current will drop to zero and then reverse direction (negative direction through inductor), passing from drain to source of low side FET. The current will flow continuously until the FB comparator initiates another high side switch on-time. CCM operation reduces efficiency at light load but improves the output transient response to step load changes and provides nearly constant switching frequency.

Table 1. FPWM Pin Mode Summary

FPWM PIN CONNECTION	LOGIC STAGE	DESCRIPTION
GND or Floating (High Z)	0	The FPWM pin is grounded or left floating. DCM enabled at light loads.
V_{CC}	1	The FPWM pin is connected to VCC. The LM5160 then operates in CCM mode at light loads.

7.4.2 Under-Voltage Detector

The following table summarizes the dual threshold levels of the under-voltage lockout (EN/UVLO) circuit explained in *Enable / Under-Voltage Lockout (EN/UVLO)* .

Table 2. UVLO Pin Mode Summary

EN/UVLO PIN VOLTAGE	VCC REGULATOR	MODE	DESCRIPTION
< 0.35 V	Off	Shutdown	V_{CC} regulator disabled. High and low side FETs disabled.
0.35 V to 1.24 V	On	Standby	V_{CC} regulator enabled. High and low side FETs disabled.
> 1.24 V	$V_{CC} < V_{CC(UV)}$	Standby	V_{CC} regulator enabled. High and low side FETs disabled.
	$V_{CC} > V_{CC(UV)}$	Operating	V_{CC} regulator enabled. Switching enabled.

If an EN/UVLO set-point is not required, the EN/UVLO pin can be driven by a logic signal as an enable input or connected directly to the VIN pin. If the EN/UVLO is directly connected to the VIN pin, the regulator will begin switching when the $V_{CC(UV)}$ = 3.98 V (typ) is satisfied.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5160 family is a synchronous-buck regulator converter designed to operate over a wide input voltage and output current range. Spreadsheet based Quick-Start Calculator tools, available on the www.ti.com product website, can be used to design a single output synchronous buck converter or an isolated dual output Fly-Buck converter using both the LM5160 and LM5160A. See application note AN-2292 for a detailed design guide for the Fly-Buck converter. Alternatively, online WEBENCH® software can be used to create a complete buck or Fly-Buck designs and generate the bill of materials, estimated efficiency, solution size, and cost of the complete solution.

Typical Application describes a few application circuits using the LM5160 or LM5160A with detailed, step by step design procedures.

8.2 Typical Application

8.2.1 LM5160 Synchronous Buck (10-V to 60-V Input, 5-V Output, 1.5-A Load)

A typical application example is a synchronous buck converter operating from a wide input voltage range of 10 V to 65 V and providing a stable 5 V output voltage with maximum output current capability of 1.5 A. The complete schematic for a typical synchronous buck application circuit is shown in *Figure 19* . In the application schematic below, the components are labeled by numbers instead of the descriptive name used in the previous sections. For example, R3 represents R_{ON} and so on.

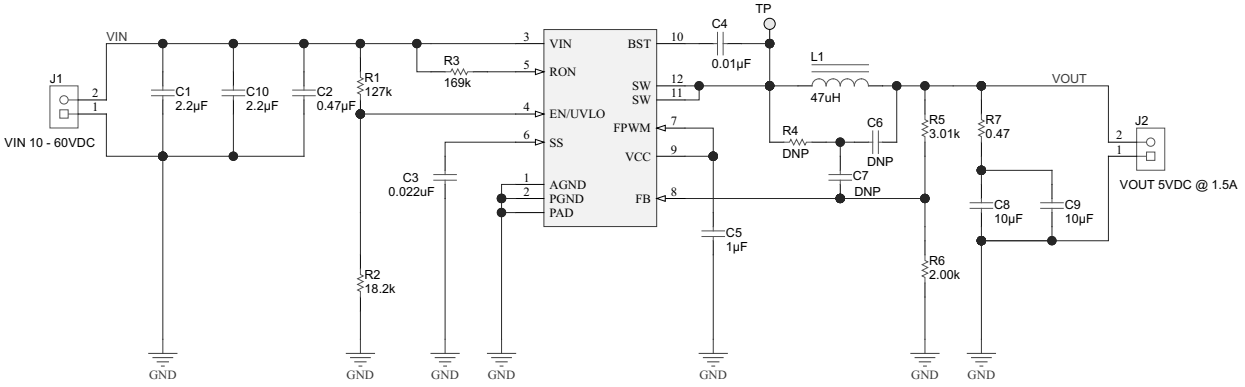


Figure 19. Synchronous Buck Application Circuit

8.2.1.1 Design Requirements

A typical synchronous-buck application introduced in *LM5160 Synchronous Buck (10-V to 60-V Input, 5-V Output, 1.5-A Load)* , Table 3 summarizes the operating parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 65 V
Output	5 V
Maximum Load Current	1.5 A
Nominal Switching Frequency	300 kHz
Light Load Operating Mode	CCM, FPWM=1

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Resistor Divider Selection

With the required output voltage set point at 5 V and V_{FB} = 2 V (typ.), the ratio of R6 (R_{FB1}) to R5 (R_{FB2}) can be calculated using the formula:

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT}}{V_{REF}} - 1 \tag{6}$$

The resistor ratio calculates to be 3:2. Standard values of R6 (R_{FB1}) = 2 kΩ and R5 (R_{FB2}) =3.01 kΩ are chosen. Higher or lower values could be used as long as the ratio of the 3:2 is maintained.

8.2.1.2.2 Frequency Selection

The duty cycle required to maintain output regulation at the minimum input voltage restricts the maximum switching frequency of LM5160. The maximum value of the minimum forced off-time $T_{OFF,min}$ (max), limits the duty cycle and therefore the switching frequency. The maximum frequency that will avoid output dropout at minimum input voltage can be calculated from Equation 7.

$$F_{SW,\,max\,(@\,V_{IN,\,min})} = \frac{V_{IN,\,min} - V_{OUT}}{V_{IN,\,min} \times T_{OFF,\,min}(ns)} \tag{7}$$

For this design example, the maximum frequency based on the minimum off-time limitation for $T_{OFF,min}$(typ) = 170 ns is calculated to be $F_{SW,max(@VIN,min)}$ = 2.9 MHz. This value is well above 1 MHz, the maximum possible operating frequency of the LM5160. Therefore, the minimum off-time parameter cannot be used further for the maximum achievable switching frequency calculation in this application.

At the maximum input voltage, the maximum switching frequency of LM5160 is restricted by the minimum on-time, $T_{ON,min}$ which limits the minimum duty cycle of the converter. The maximum frequency at maximum input voltage can be calculated using Equation 8.

$$F_{SW,\,max\,(@\,V_{IN,\,max})} = \frac{V_{OUT}}{V_{IN,\,max} \times T_{ON,\,min}(ns)} \tag{8}$$

Using Equation 8 and $T_{ON,min}$ (typ) = 150 ns, the maximum achievable switching frequency is $F_{SW,max(@VIN,min)}$=514 kHz. Taking this value as the maximum possible operational switching frequency over the input voltage range in this application, a nominal switching frequency of F_{SW} = 300 kHz is chosen for this design.

The value of the resistor, R_{ON} sets the nominal switching frequency based on Equation 9.

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 1 \times 10^{-10}}\ \Omega \tag{9}$$

For this particular application with F_{SW} = 300 kHz, R_{ON} calculates to be 167 kΩ . Selecting a standard value for R3 (R_{ON}) = 169 kΩ (±1%) will result in an ideal nominal frequency of 296 kHz. The resistor value may need to adjusted further in order to achieve the required switching frequency as the switching frequency in COTs varies slightly(±10%) with input voltage and/or output current. Operation at a lower nominal switching frequency will result in higher efficiency but increase in the inductor and capacitor values leading to a larger total solution size.

8.2.1.2.3 Inductor Selection

The inductor is selected to limit the inductor ripple current between 20 and 40 percent of the maximum load current. The minimum value of the inductor required in this application can be calculated from:

$$L_{min} = \frac{V_O \times (V_{IN,\,max} - V_O)}{V_{IN,\,max} \times F_{SW} \times I_{O,\,max} \times 0.4} \tag{10}$$

Based on Equation 10 , the minimum value of the inductor is calculated to be 26 µH for V_{IN} = 65 V (max) and inductor current ripple equal to 40 percent of the maximum load current. Allowing some margin for inductance variation and inductor saturation, a higher standard value of L1 (L) = 47 µH is selected for this design.

The peak inductor current at maximum load must be smaller than the minimum current limit threshold of the high side FET as given in *Electrical Characteristics* table. The inductor current ripple at any input voltage is given by:

$$\Delta I_L = \frac{V_O \times (V_{IN} - V_O)}{V_{IN} \times F_{SW} \times L} \quad (11)$$

The peak-to-peak inductor current ripple is calculated to be 180 mA and 332 mA at the minimum and maximum input voltages respectively. The maximum peak inductor current in the buck FET is given by:

$$I_{L(peak)} = I_{O,max} + \frac{\Delta I_{L,max}}{2} \quad (12)$$

In this design with maximum output current of 1.5 A, the maximum peak inductor current is calculated to be approximately 1.67 A which is less than the minimum high-side FET current limit threshold.

The saturation current of the inductor must also be carefully considered. The peak value of the inductor current will be bound by the high side FET current limit during overload or short circuit conditions. Based on the high side FET current limit specification in the *Electrical Characteristics* , an inductor with saturation current rating above 2.875 A (max) should be selected.

8.2.1.2.4 Output Capacitor Selection

The output capacitor is selected to limit the capacitive ripple at the output of the regulator. Maximum capacitive ripple is observed at maximum input voltage. The output capacitance required for a ripple voltage ΔV_O across the capacitor is given by Equation 13.

$$C_{OUT} = \frac{\Delta I_{L,max}}{8 \times F_{SW} \times \Delta V_{O,ripple}} \quad (13)$$

Substituting $\Delta V_{O,\ ripple}$ = 10 mV gives C_{OUT} = 14 µF. Two standard 10 µF ceramic capacitors in parallel (C8, C9) are selected. An X7R type capacitor with a voltage rating 16 V or higher should be used for C_{OUT} (C8, C9) to limit the reduction of capacitance due to dc bias voltage.

8.2.1.2.5 Series Ripple Resistor - R_{ESR}

The series resistor is selected such that sufficient ripple injection is ensured at the feedback node FB. The ripple produced by R_{ESR} is proportional to the inductor current ripple, and therefore, R_{ESR} should be chosen for minimum inductor current ripple which occurs at minimum input voltage. The R_{ESR} is calculated by Equation 14.

$$R_{ESR} \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L,min}} \quad (14)$$

With V_O = 5 V, V_{REF} = 2 V and $\Delta I_{L,\ min}$ = 180 mA (at $V_{IN,\ min}$= 10 V) as calculated in Equation 11, Equation 14 requires an R_{ESR} greater than or equal to 0.35 Ω. Selecting R7 (R_{ESR}) = 0.47 Ω will result in ~150 mV of maximum output voltage ripple at $V_{IN,max}$. For applications requiring lower output voltage ripple, Type II or Type III ripple injection circuits should be used as described in *Ripple Configuration*.

8.2.1.2.6 VCC and Bootstrap Capacitor

The VCC capacitor charges the bootstrap capacitor during the off-time of the high side switch and powers internal logic circuits and the low side sync FET gate driver. The bootstrap capacitor biases the high side gate driver during the high side FET on-time. A good value for C5 (C_{VCC}) is 1 µF. A good choice for C4 (C_{BST}) is 10 nF. Both should be high quality X7R ceramic capacitors.

8.2.1.2.7 Input Capacitor Selection

The input capacitor must be large enough to limit the input voltage ripple to an acceptable level. Equation 15 provides the input capacitance C_{IN} required for a worst case input ripple of $\Delta V_{IN,\ ripple}$.

$$C_{IN} = \frac{I_{O,max} \times D \times (1-D)}{\Delta V_{IN,ripple} \times F_{SW}} \quad (15)$$

C_{IN} (C1, C10) supplies most of the switch current during the on-time to limit the voltage ripple at the VIN pin. At maximum load current, when the buck switch turns on, the current into the VIN pin quickly increases to the valley current of the inductor ripple and then ramps up to the peak of the inductor ripple during the on-time of the high side FET. The average current during the on-time is the output load current. For a worst case calculation, C_{IN} must supply this average load current during the maximum on-time, without letting the voltage at VIN drop more than the desired input ripple. For this design, the input voltage drop is limited to 0.5 V and the value of C_{IN} is calculated using Equation 15.

Based on Equation 15, the value of the input capacitor is calculated to be approximately 2.5 µF at D = 0.5. Taking into account the decrease in capacitance over an applied voltage, two standard value ceramic capacitors of 2.2 µF are selected for C1 and C10. The input capacitors should be rated for the maximum input voltage under all operating and transient conditions. A 100 V, X7R dielectric was selected for this design.

A third input capacitor C2 may be needed in this design as a bypass path for the high frequency component of the input switching current. The value of C2 is 0.47 µF and this bypass capacitor (when used with the LM5160-Q1 HTSSOP-14 package, a bypass capacitor C2 = 0.1 µF is used) should be placed directly across VIN and PGND (pin 3 and 2) near the IC. The C_{IN} values and location are critical to reducing switching noise and transients.

8.2.1.2.8 Soft-Start Capacitor Selection

The capacitor at the SS pin determines the soft-start time, i.e. the time for the output voltage to reach its final steady state value. The capacitor value is determined from Equation 16:

$$C_{SS} = \frac{I_{SS} \times T_{Startup}}{V_{SS}} \tag{16}$$

With C3 (C_{SS}) set at 22 nF and the Vss = 2 V, I_{SS} = 10 µA, the $T_{Startup}$ should measure approximately 4 ms.

8.2.1.2.9 EN/UVLO Resistor Selection

The UVLO resistors R1 (R_{UV2}) and R2 (R_{UV1}) set the input under-voltage lockout threshold and hysteresis according to the following equations:

$$V_{IN(HYS)} = I_{UVLO(HYS)} \times R_{UV2} \tag{17}$$

and,

$$V_{IN,\,UVLO(rising)} = V_{UVLO(TH)} \left(1 + \frac{R_{UV2}}{R_{UV1}} \right) \tag{18}$$

From the Electrical Characteristics table, $I_{UVLO(HYS)}$ = 20 µA (typ). To design for V_{IN} rising threshold ($V_{IN,\,UVLO(rising)}$) at 10 V and EN/UVLO hysteresis of 2.5 V, Equation 17 and Equation 18 yield R_{UV1} = 17.98 kΩ and R_{UV2} = 125 kΩ . Selecting 1% standard value of R2 (R_{UV1}) = 18.2 kΩ and R1 (R_{UV2}) = 127 kΩ results in UVLO thresholds and hysteresis of 9.89 V and 2.54 V respectively.

8.2.1.3 Application Performance Plots

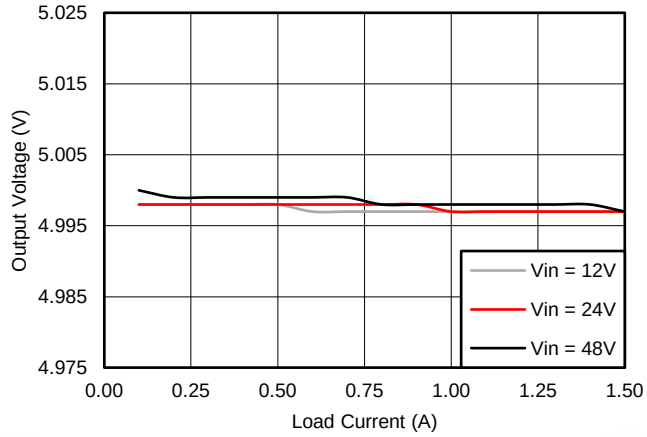


Figure 20. Load Regulation

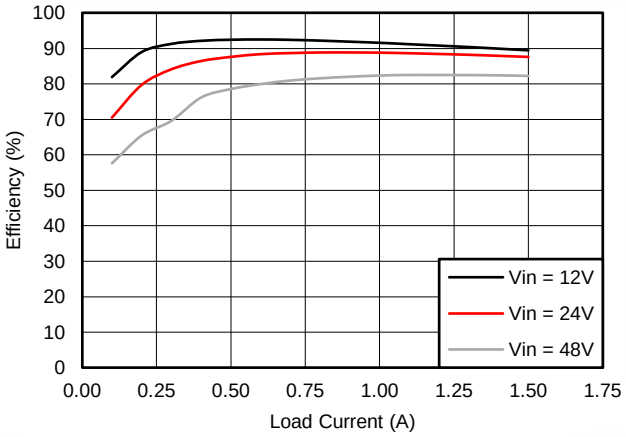


Figure 21. Efficiency vs I_{OUT}

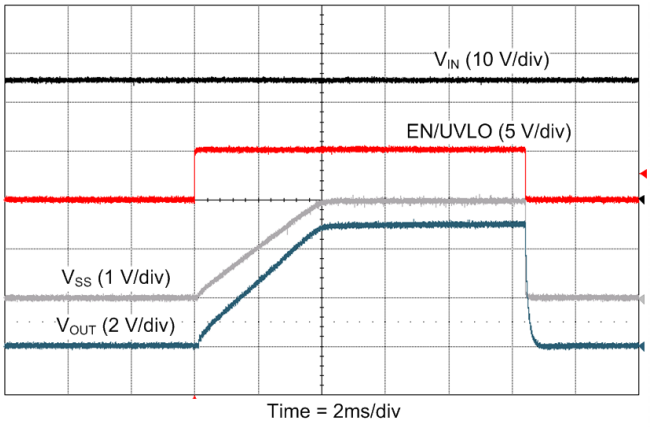


Figure 22. EN/UVLO Startup at V_{IN}= 24 V and I_{OUT} = 1 A

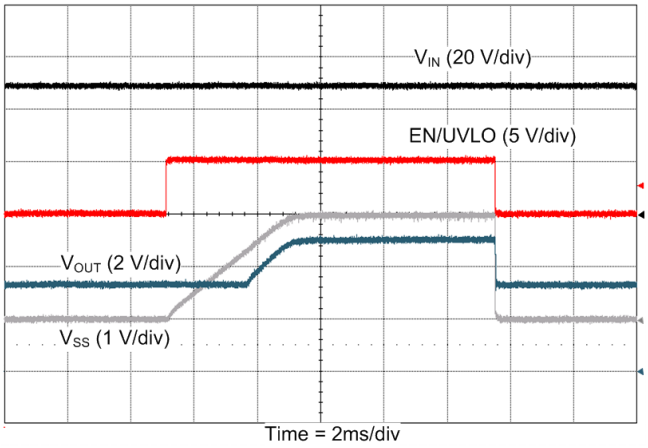


Figure 23. Pre-Bias Startup at V_{IN}= 48 V and R_{LOAD} = 3Ω

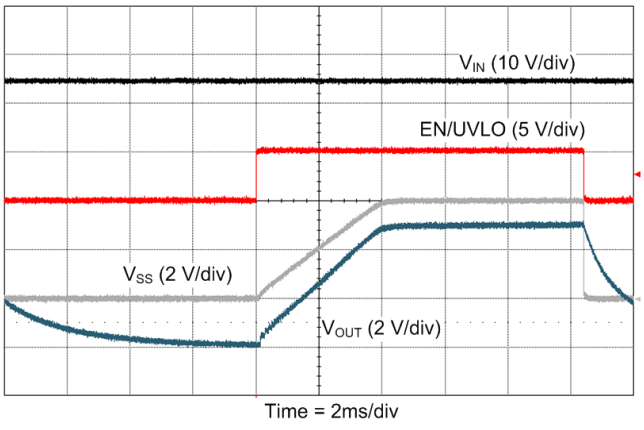


Figure 24. EN/UVLO Startup at V_{IN}= 24 V and R_{LOAD} = 100Ω

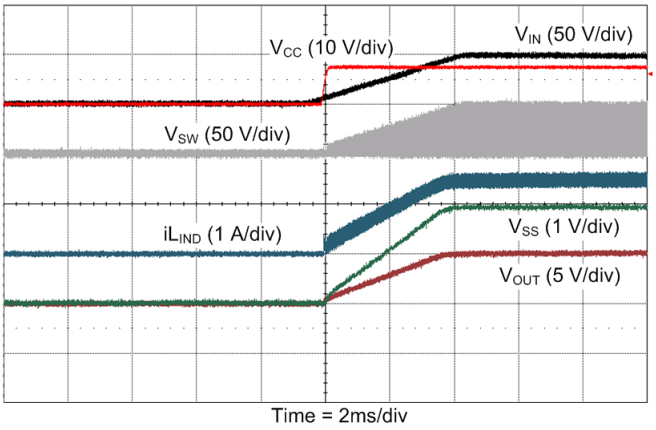


Figure 25. Startup at V_{IN}= 48 V and R_{LOAD} = 10Ω

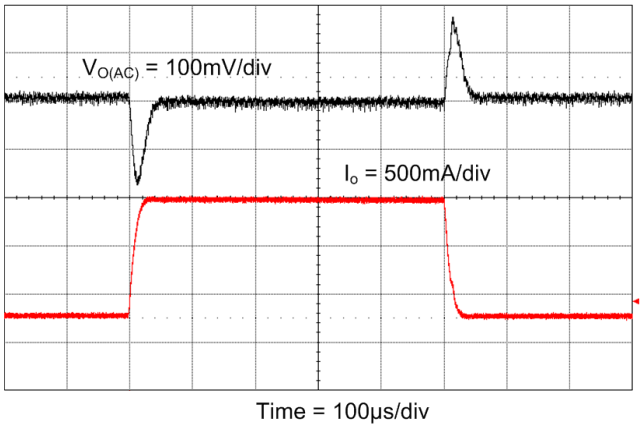


Figure 26. Load Transient (300 mA - 1.5 A) at V_{IN} = 24 V with Type 3 Ripple Configuration

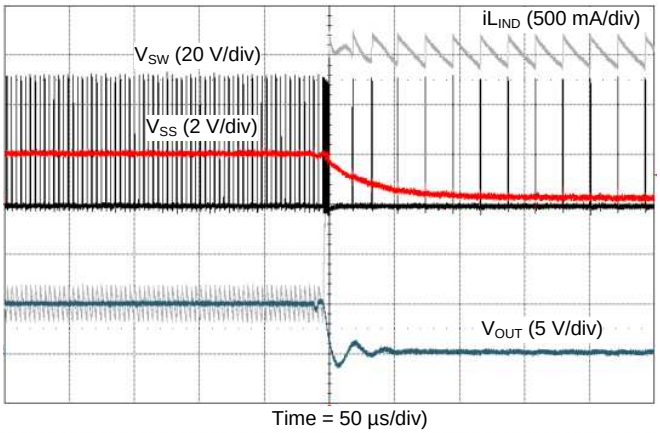


Figure 27. Output Short-Circuit at V_{IN} = 48 V

8.2.2 LM5160 Isolated Fly-Buck (18-V to 32-V Input, 12-V/4.5W Isolated Output)

A typical application example for an isolated Fly-Buck converter operates over an input voltage range of 18 V to 32 V. It provides a stable 12 V isolated output voltage with output power capability of 4.5 W. The complete schematic of the Fly-Buck application circuit is shown in *Figure 28* .

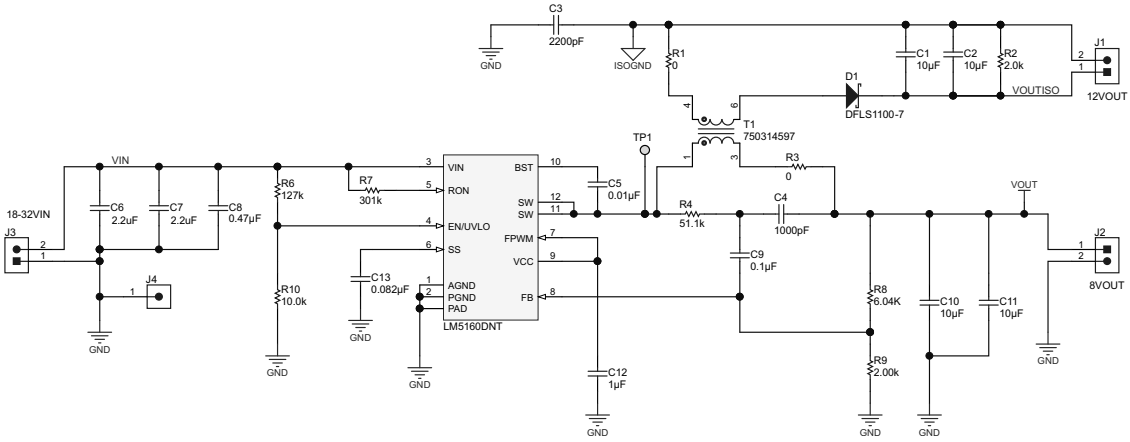


Figure 28. 12 V/ 4.5 W Fly-Buck Schematic

8.2.2.1 LM5160 Fly-Buck Design Requirements

The LM5160 Fly-Buck application example is designed to operate from a 24 V DC supply with line variations from 18 V to 32 V. This example provides a space-optimized and efficient 12 V isolated output solution with secondary load current capability from 0 mA to 400 mA. The primary side remains unloaded in this application. The switching frequency is set at 300 kHz (nominal). This design achieves greater than 88% peak efficiency.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	18 V - 32 V
Isolated output	12 V
Isolated load current range	0 mA to 400 mA
Nominal switching frequency	300 KHz
Peak Efficiency	88%

8.2.2.2 Detailed Design Procedure

The Fly-Buck converter design procedure closely follows the buck converter design outlined in *LM5160 Synchronous Buck (10-V to 60-V Input, 5-V Output, 1.5-A Load)* . The selection of primary output voltage, transformer turns ratio, rectifier diode, and output capacitors are covered here.

8.2.2.2.1 Selection of V_{OUT1} and Turns Ratio

The primary output voltage in a Fly-Buck converter should be no more than one half of the minimum input voltage. For a minimum V_{IN} of 18 V, the primary output voltage (V_{OUT}) should be no higher than 9 V. To generate an isolated output voltage of $V_{OUT\ (ISO)}$ = 12 V, a transformer turns ratio (N1:N2) of 1:1.5 is selected. Using this turns ration, the required primary output voltage V_{OUT} is calculated to be:

$$V_{OUT} = \frac{V_{OUT(ISO)} - 0.7\ V}{1.5} = 8.47\ V \tag{19}$$

The 0.7 V subtracted from $V_{OUT(ISO)}$ represents the forward voltage drop of the secondary rectifier diode. Fine tuning the primary side V_{OUT1} may be required to account for voltage errors due to the leakage inductance of the transformer and the resistance of the transformer windings and the low side FET of LM5160.

8.2.2.2.2 Secondary Rectifier Diode

The secondary rectifier diode must block the maximum input voltage multiplied by the transformer turns ratio. The minimum diode reverse voltage $V_{R(diode)}$ rating is given by:

$$V_{R(diode)} = V_{IN(max)} \times \frac{N2}{N1} = 32\ V \times 1.5 = 48\ V \tag{20}$$

A diode of 60 V or higher reverse voltage rating should be selected in this application. If the input voltage (V_{IN}) has transients above the normal operating maximum input voltage of 32 V, then the worst case transient input voltage should be used in the diode voltage calculation of Equation 20.

8.2.2.2.3 External Ripple Circuit

Type 3 ripple circuit is required for Fly-Buck applications. The design procedure for ripple components is identical to that in a buck converter. See *Ripple Configuration* for ripple design information.

8.2.2.2.4 Output Capacitor (C_{OUT2})

The Fly-Buck output capacitor conducts higher ripple current than a buck converter output capacitor. The capacitive ripple for the isolated output capacitor is calculated based on the time the rectifier diode is off. During this time the entire output current is supplied by the output capacitor. The required capacitance for a worst case V_{OUT2} ($V_{OUT\ (ISO)}$) ripple voltage can be calculated using Equation 21 where, ΔV_{OUT2} is the target ripple at the secondary output.

$$C_{OUT2} = \frac{I_{OUT2}}{\Delta V_{OUT2}} \left(\frac{V_{OUT1}}{V_{IN(MIN)}} \right) \times \frac{1}{f_{sw}} \tag{21}$$

Equation 21 is an approximation and ignores the ripple components associated with ESR and ESL of the output capacitor. For a ΔV_{OUT2} = 100 mV, Equation 21 requires C_{OUT2} = 6.5 µF. When selecting a capacitor, its DC bias should be considered to ensure sufficient capacitance over the output voltage.

8.2.2.3 Application Performance Plots

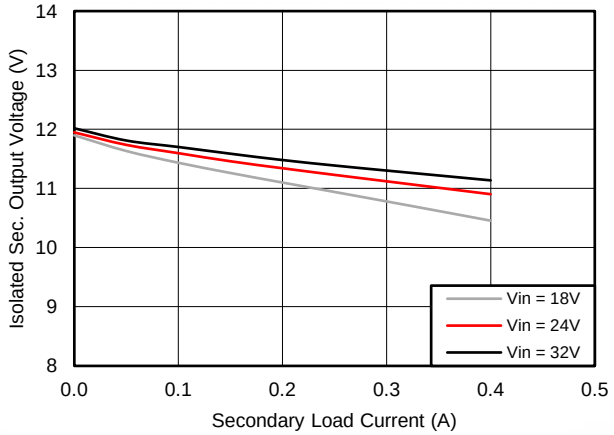


Figure 29. Load Regulation

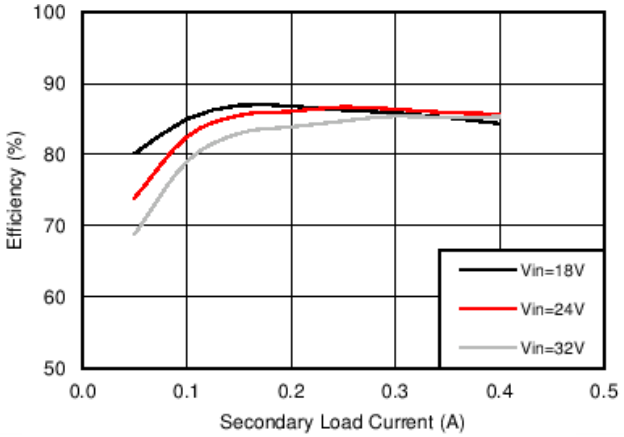


Figure 30. Efficiency vs. I_{OUT2}

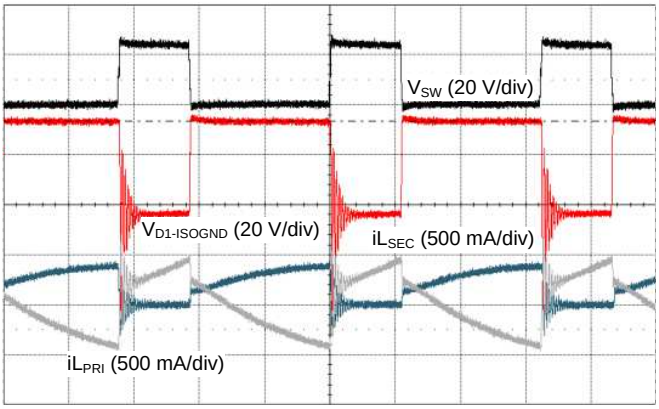


Figure 31. Primary Switch Node at V_{IN} = 24 V and I_{OUT2} = 200 mA

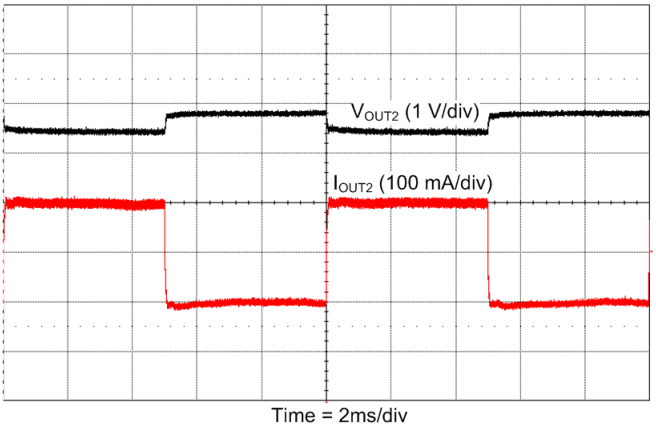


Figure 32. Load Transient at I_{OUT2} = 100 mA - 300mA

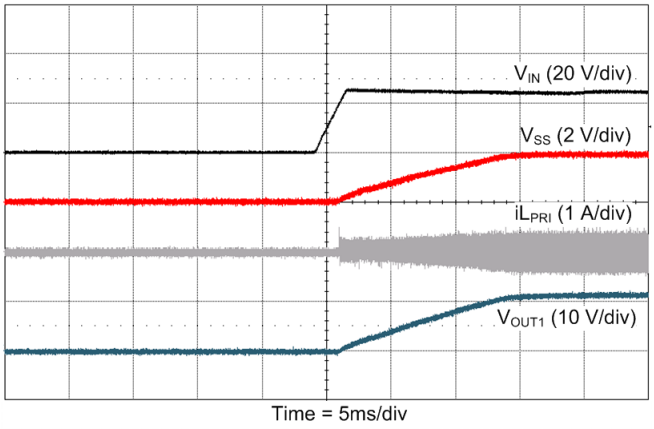


Figure 33. VIN Startup at I_{OUT2} = 200 mA

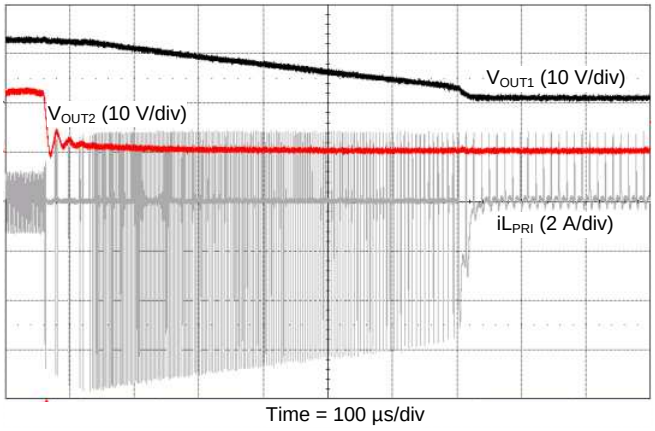


Figure 34. Secondary Short at I_{OUT2} = 600mA and I_{OUT1} = 200mA

8.2.3 LM5160A Isolated Fly-Buck (18-V to 32-V Input, 12-V/4.5W Isolated Output)

The LM5160A when used in either the buck or the Fly-Buck application, can also be biased by an external voltage source for improved efficiency requirements. The LM5160A, can be externally biased to VOUT by connecting VCC to VOUT through a diode as shown in the Fly-Buck application circuit in *Figure 35* . In this dual output rail Fly-Buck application circuit, the VCC pin is externally diode connected (D2) to VOUT (primary). The design procedure with LM5160A, for both Buck and the Fly-Buck™, remain same as with LM5160. The voltage applied to the VCC pin, either from VOUT or an external supply should be between 9V and 13V.

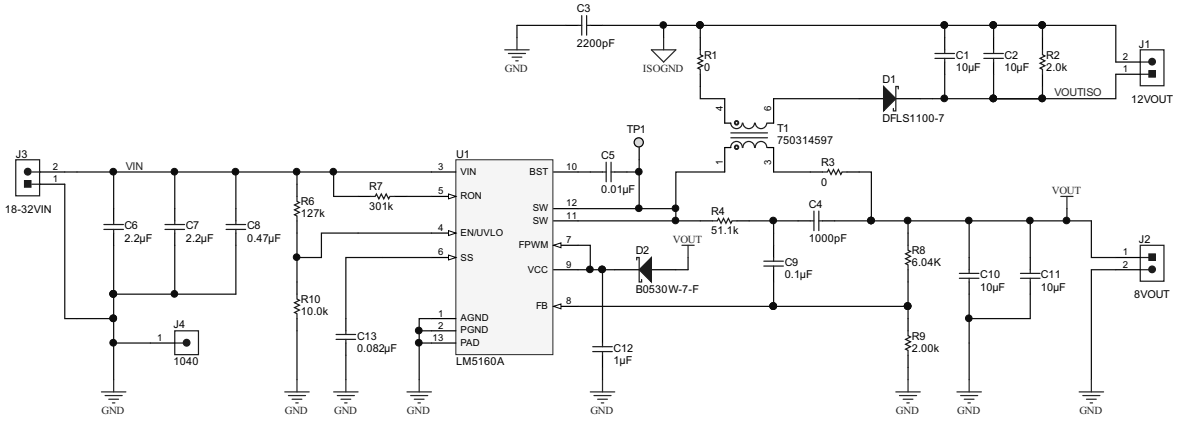


Figure 35. 12 V/ 4.5 W Fly-Buck Schematic with LM5160A

8.2.4 Ripple Configuration

LM5160 and LM5160A uses a Constant-On-Time (COT) control scheme, in which the on-time is terminated by a one-shot, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage. Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be large enough to dominate any noise present at the feedback node.

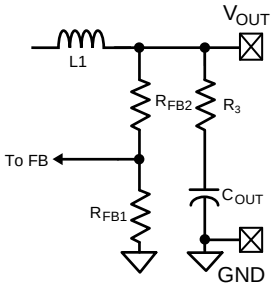
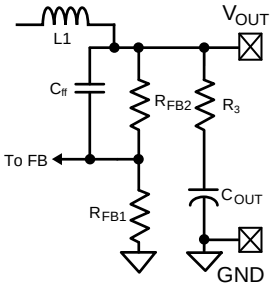
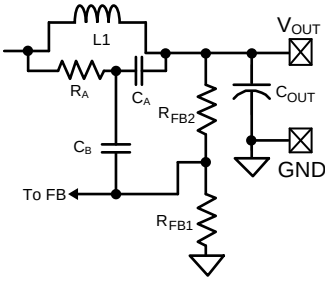
Table 5 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple from the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor and R3.

The capacitive ripple is out of phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at output (V_{OUT}) for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses a ripple injection circuit with R_A, C_A and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then ac coupled into the feedback node (FB) using the capacitor C_B. Since this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is imperative. See application note AN-1481 for more details for each ripple generation method.

Table 5. Ripple Configuration

TYPE 1	TYPE 2	TYPE 3
Lowest Cost	Reduced Ripple	Minimum Ripple
		
$R_3 \geq \frac{25\ mV \times V_O}{V_{REF} \times \Delta I_{L1,min}}$ (22)	$C_{ff} \geq \frac{5}{F_{SW} \times (R_{FB2} \text{ IIR}_{FB1})}$ $R_3 \geq \frac{25\ mV}{\Delta I_{L1,min}}$ (23)	$R_A C_A \geq \frac{(V_{IN,min} - V_O) \times T_{ON(@\ V_{IN,min})}}{25mV}$ (24)

8.3 Do's and Don'ts

As mentioned earlier in *Soft-Start* , the SS capacitor C_{SS}, should always be more than 1 nF in both buck and Fly-Buck applications. Apart from determining the startup time, this capacitor serves as the external compensation of the internal G_M error amplifier. A minimum value of 1 nF is necessary to maintain stability. The SS pin should not be left floating.

The VCC pin in the LM5160-Q1 should not be biased with an external voltage source. When improved efficiency requirement warrants an external Vcc bias, the LM5160A should be used.

9 Power Supply Recommendations

The LM5160 is designed to operate with an input power supply capable of supplying a voltage range between 4.5 V and 65 V. The power supply should be well regulated and capable of supplying sufficient current to the regulator during the sync buck mode or the isolated Fly-Buck mode of operation. As in all DC/DC applications, the power supply source impedance must be small compared to the converter input impedance in order to maintain the stability of the converter.

If the LM5160 is used in a buck topology with low input supply voltage (4.5 V) and large load current (1.5 A), it is prudent to add a large electrolytic capacitor, in parallel the C_{IN} capacitors. The electrolytic capacitor will stabilize the input voltage to the IC and prevent droop or oscillation, over the entire load range.

10 Layout

10.1 Layout Guidelines

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

- C_{IN}: The loop consisting of input capacitor (C_{IN}), VIN pin, and PGND pin carries the switching current. Therefore, in both the LM5160 and the LM5160A, the input capacitor should be placed close to the IC, directly across VIN and PGND pins, and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to place all of input capacitances near the IC. A good layout practice includes placing the bulk capacitor as close as possible to the VIN pin (see Figure 36).When using the LM5160-Q1 HTSSOP-14 package, a bypass capacitor measuring ~0.1 µF should be placed directly across VIN and PGND (pin 3 and 2), as close as possible to the IC while complying with all layout design rules.
- C_{VCC} and C_{BST}: The VCC and bootstrap (BST) bypass capacitors supply switching currents to the high and low side gate drivers. These two capacitors should also be placed as close to the IC as possible, and the connecting trace length and loop area should be minimized (see Figure 36).
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of both the LM5160 and the LM5160A. Therefore, care should be taken while routing the feedback trace to avoid coupling any noise into this pin. In particular, the feedback trace should be short and not run close to magnetic components, or parallel to any other switching trace.
- SW trace: The SW node switches rapidly between VIN and GND every cycle and is therefore a source of noise. The SW node area should be minimized. In particular, the SW node should not be inadvertently connected to a copper plane or pour.

10.2 Layout Example

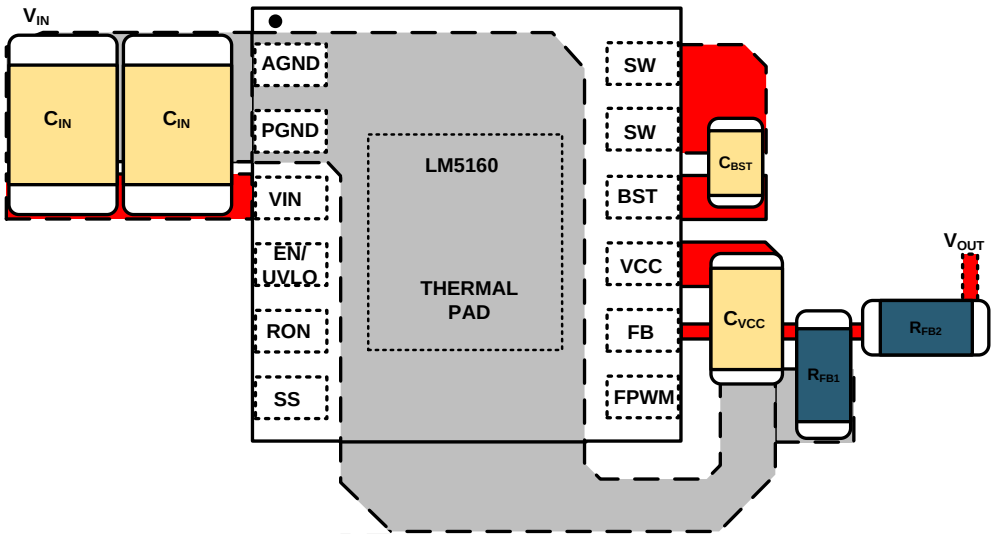


Figure 36. Placement of Bypass Capacitors

11 Device and Documentation Support

11.1 Related Documentation

AN-2292 *Designing an Isolated Buck (Fly-Buck) Converter*

AN-1481 *Controlling Output Ripple & Achieving ESR Independence in Constant On-Time Regulator Designs*

SPRA953 *IC Package Thermal Metrics* application report,

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

Fly-Buck, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5160QPWPQ1	ACTIVE	HTSSOP	PWP	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1	Samples
LM5160QPWPRQ1	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1	Samples
LM5160QPWPTQ1	ACTIVE	HTSSOP	PWP	14	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	5160 QPWPQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LM5160-Q1 :

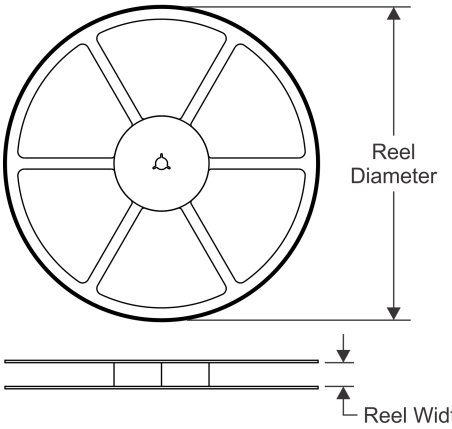
- Catalog: LM5160

NOTE: Qualified Version Definitions:

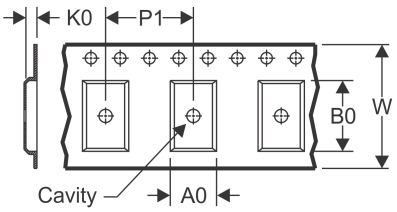
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

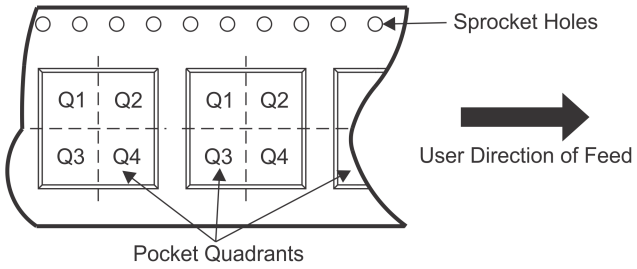


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

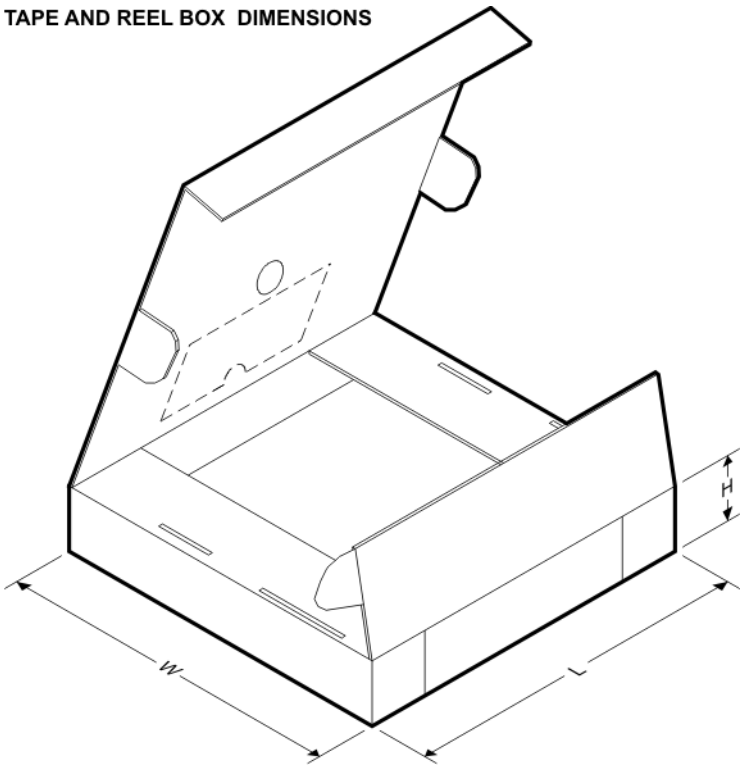
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5160QPWPRQ1	HTSSOP	PWP	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LM5160QPWPTQ1	HTSSOP	PWP	14	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

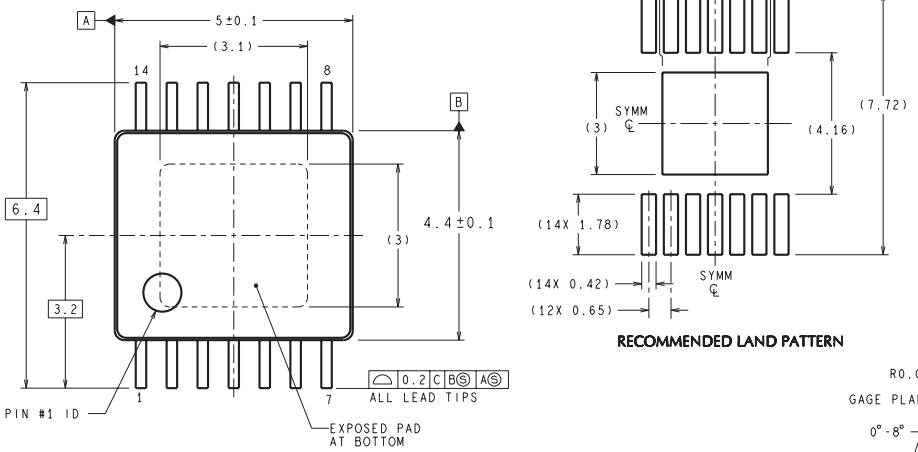
TAPE AND REEL BOX DIMENSIONS



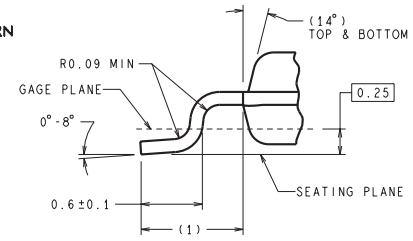
*All dimensions are nominal

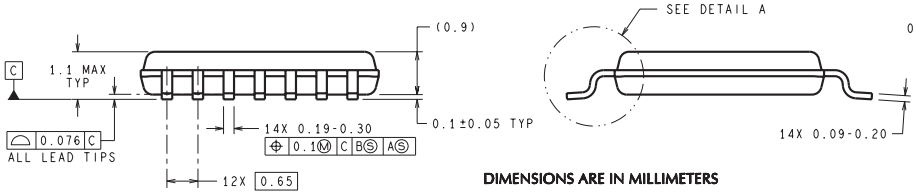
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5160QPWPRQ1	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM5160QPWPTQ1	HTSSOP	PWP	14	250	213.0	191.0	55.0

PWP0014A



RECOMMENDED LAND PATTERN





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