100-V 150-mA Constant On-Time Buck Switching Regulator

Check for Samples: LM5009A

FEATURES

- **Operating input voltage range: 6V to 95V**
- **Integrated 100V, N-Channel buck switch**
- **Internal start-up regulator**
- **No loop compensation required**
- **Ultra-Fast transient response**
- **On time varies inversely with input voltage**
- **Operating frequency remains constant with varying line voltage and load current**
- **Adjustable output voltage from 2.5V**
- **Highly efficient operation**
- **Precision internal reference**
- **Low bias current**
- **Intelligent current limit**
- **Thermal shutdown**
- **VSSOP-8 and WSON-8 (4mm x 4mm) packages**

APPLICATIONS

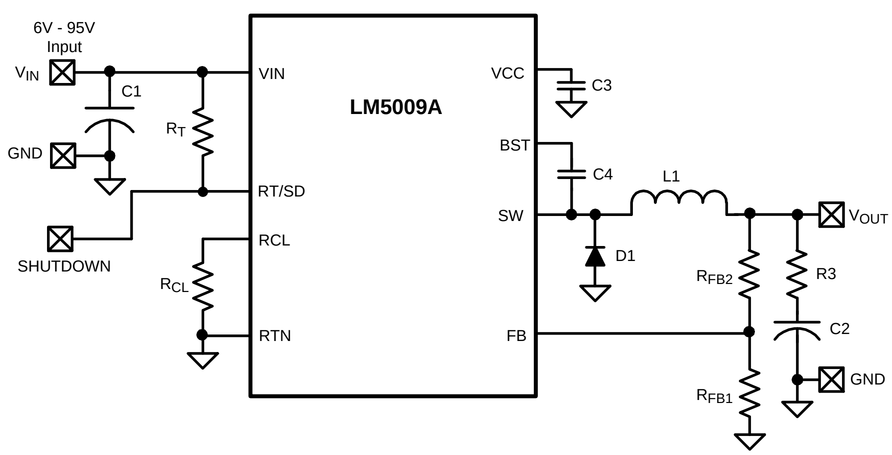
- **Non-Isolated Telecommunication Buck Regulator**
- **Secondary High Voltage Post Regulator**
- **+42V Automotive Systems**

DESCRIPTION

The LM5009A is a functional variant of the LM5009 COT Buck Switching Regulator. The functional differences of the LM5009A are: The minimum input operating voltage is 6 volts, the on-time equation is slightly different, and the requirement for a minimum load current is removed.

The LM5009A Step Down Switching Regulator features all of the functions needed to implement a low cost, efficient, Buck bias regulator. This high voltage regulator contains an 100 V N-Channel Buck Switch. The device is easy to implement and is provided in the VSSOP-8 and the thermally enhanced WSON-8 packages. The regulator is based on a control scheme using an ON time inversely proportional to V_{IN}. This feature allows the operating frequency to remain relatively constant. The control scheme requires no loop compensation. An intelligent current limit is implemented with forced OFF time, which is inversely proportional to Vout. This scheme ensures short circuit control while providing minimum foldback. Other features include: Thermal Shutdown, V_{CC} under-voltage lockout, Gate drive under-voltage lockout, Max Duty Cycle limiter, and a pre-charge switch.

Typical Application, Basic Step-Down Regulator



Connection Diagram

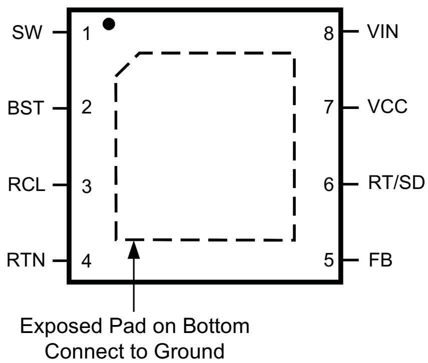


Figure 1. Top View
8-Lead WSON

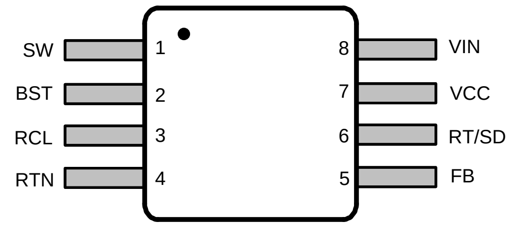


Figure 2. Top View
8-Lead VSSOP

Pin Functions

Table 1. Pin Descriptions

Pin	Name	Description	Application Information
1	SW	Switching node	Power switching node. Connect to the output inductor, re-circulating diode, and bootstrap capacitor.
2	BST	Boost pin (bootstrap capacitor input)	An external capacitor is required between the BST and the SW pins. A 0.01 µF ceramic capacitor is recommended. An internal diode charges the capacitor from V_{CC} during each off-time.
3	RCL	Current limit OFF time set pin	A resistor between this pin and RTN sets the off-time when current limit is detected. The off-time is preset to 35 µs if FB = 0V.
4	RTN	Ground pin	Ground for the entire circuit.
5	FB	Feedback input from regulated output	This pin is connected to the inverting input of the internal regulation comparator. The regulation threshold is 2.5V.
6	RT/SD	On time set pin	A resistor between this pin and VIN sets the switch on time as a function of V_{IN}. The minimum recommended on time is 400 ns at the maximum input voltage. This pin can be used for remote shutdown.
7	VCC	Output from the internal high voltage series pass regulator.	This regulated voltage provides gate drive power for the internal Buck switch. An internal diode is provided between this pin and the BST pin. A local 0.47 µF decoupling capacitor is required. The series pass regulator is current limited to 9 mA.
8	VIN	Input voltage	Input operating range: 6V to 95V.
	EP	Exposed pad	The exposed pad has no electrical contact. Connect to system ground plane for reduced thermal resistance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings [1]

V_{IN} to GND	-0.3V to 100V
BST to GND	-0.3V to 114V
SW to GND (Steady State)	-1V
ESD Rating, Human Body Model [2]	2kV
BST to V_{CC}	100V
BST to SW	14V
V_{CC} to GND	14V
All Other Inputs to GND	-0.3 to 7V
Lead Temperature (Soldering 4 sec) [3]	260°C
Storage Temperature Range	-55°C to +150°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The ESD rating for pin 2, pin 7, and pin 8 is 1 kV for HBM and 150V for MM.
(3) For detailed information on soldering plastic VSSOP and WSON packages, refer to the Packaging Data Book.

Operating Ratings [1]

V_{IN}	6V to 95V
Operating Junction Temperature	−40°C to + 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, unless otherwise stated [1].

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VCC Supply						
Vcc Reg	Vcc Regulator Output [2]	Vin = 48V	**6.6**	7	**7.4**	V
	Vin – Vcc	6V < Vin < 8.5V		100		mV
	Vcc Bypass Threshold	Vin Increasing		8.5		V
	Vcc Bypass Hysteresis			300		mV
	Vcc Output Impedance	Vin =6V		100		Ω
		Vin = 10V		8.8		Ω
		Vin = 48V		0.8		Ω
	Vcc Current Limit	Vin = 48V		9.2		mA
	Vcc UVLO	Vcc Increasing		5.3		V
	Vcc UVLO hysteresis			190		mV
	Vcc UVLO filter delay			3		µs
	Iin Operating current	FB = 3V, Vin = 48V		550	**750**	µA
	Iin Shutdown Current	RT/SD = 0V		110	**176**	µA
Switch Characteristics						
	Buck switch Rds(on) [3]	Itest = 200 mA		2.2	**4.6**	Ω
	Gate Drive UVLO	Vbst – Vsw Rising	**2.8**	3.8	**4.8**	V
	Gate Drive UVLO hysteresis			490		mV
	Pre-charge switch voltage	At 1 mA		0.8		V
	Pre-charge switch on-time			150		ns

(1) All electrical characteristics having room temperature limits are tested during production with T_A = T_J = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The V_{CC} output is intended as a self bias for the internal gate drive power and control circuits. Device thermal limitations limit external loading.
(3) For devices procured in the WSON-8 package, the Rds(on) limits are specified by design characterization data only.

Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, unless otherwise stated [(1)].

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Current Limit						
	Current Limit Threshold		**0.24**	0.3	**0.36**	A
	Current Limit Response Time	I_{switch} Overdrive = 0.1A, Time to Switch Off		350		ns
T_{OFF-1}	OFF time generator	FB=0V, R_{CL} = 100K		35		µs
T_{OFF-2}	OFF time generator	FB=2.3V, R_{CL} = 100K		2.56		µs
On Time Generator						
	T_{ON} - 1	Vin = 10V, Ron = 200K	**2.15**	2.77	**3.5**	µs
	T_{ON} - 2	Vin = 95V, Ron = 200K	**200**	300	**420**	ns
	Remote Shutdown Threshold	Rising	**0.40**	0.70	**1.05**	V
	Remote Shutdown Hysteresis			35		mV
Minimum Off Time						
	Minimum Off Timer	FB = 0V		300		ns
Regulation and OV Comparators						
	FB Reference Threshold	Internal reference, Trip point for switch ON	**2.445**	2.5	**2.550**	V
	FB Over-Voltage Threshold	Trip point for switch OFF		2.875		V
	FB Bias Current			100		nA
Thermal Shutdown						
Tsd	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			25		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	VSSOP Package		200		°C/W
		WSON Package		40		°C/W

Typical Performance Characteristics

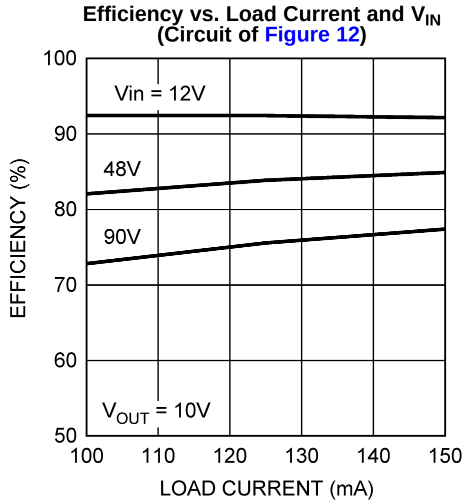


Figure 3.

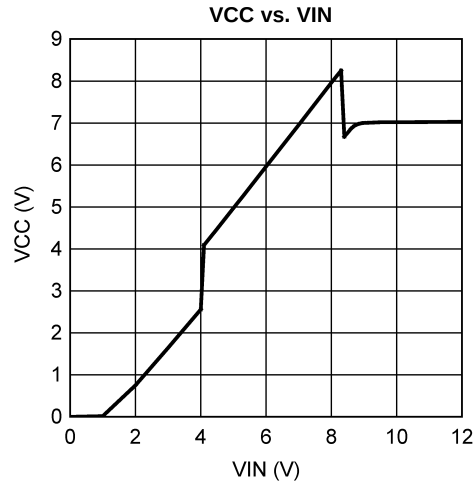


Figure 4.

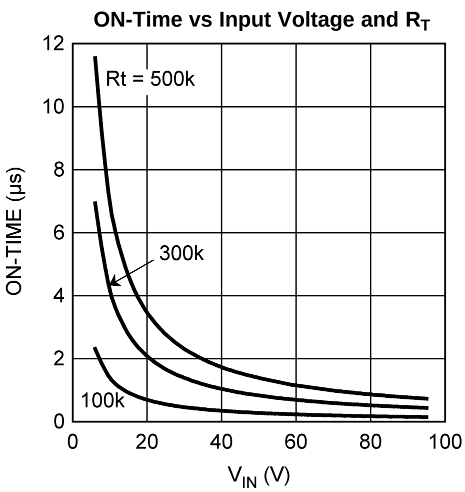


Figure 5.

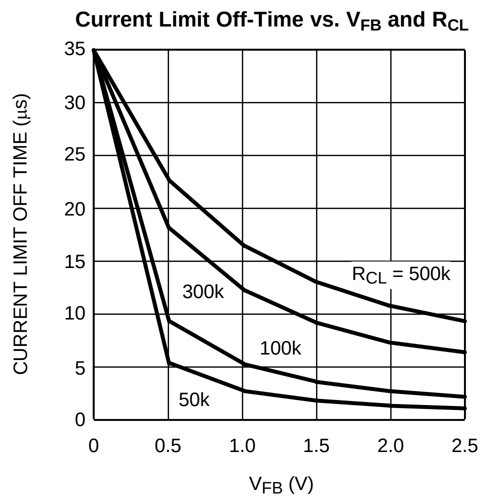


Figure 6.

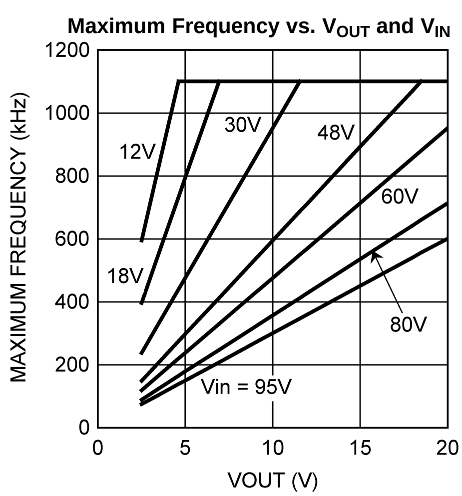


Figure 7.

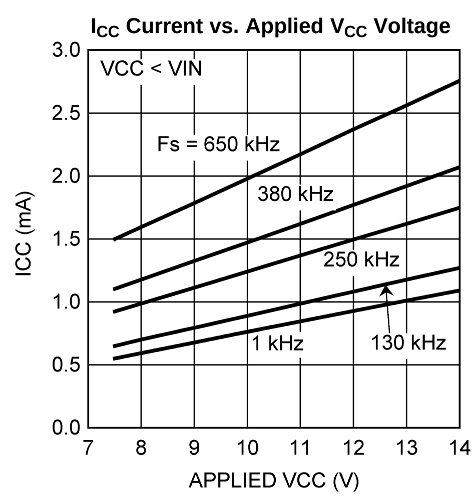
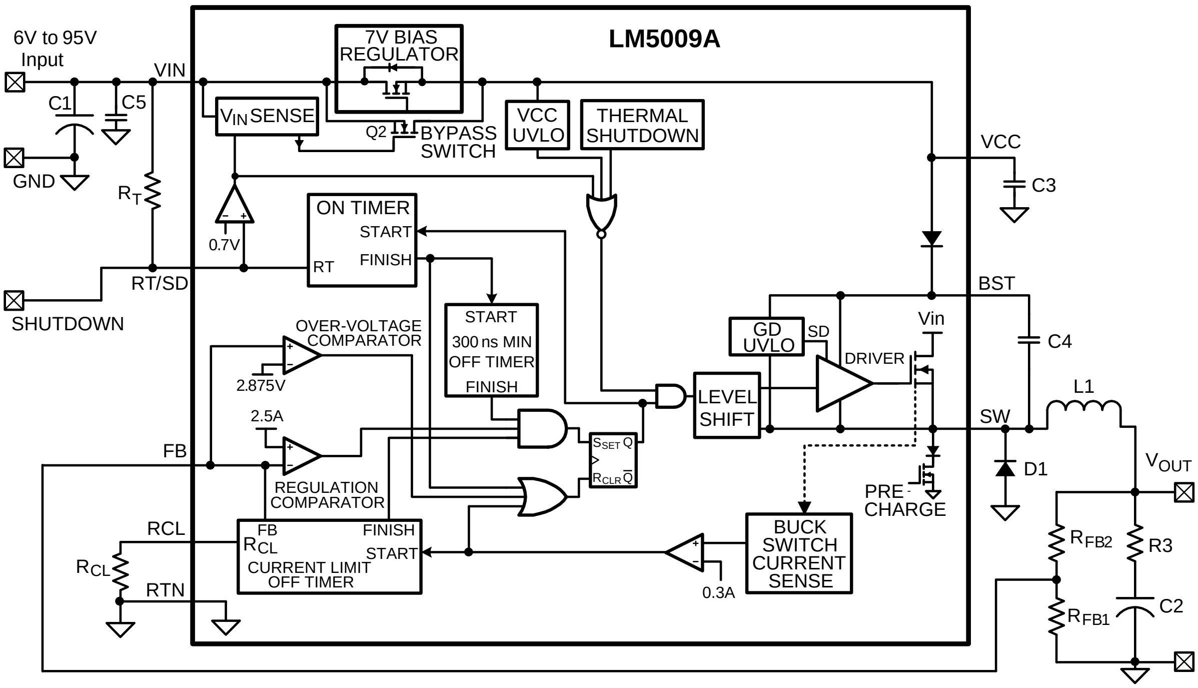


Figure 8.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The LM5009A Step Down Switching Regulator features all the functions needed to implement a low cost, efficient, Buck bias power converter. This high voltage regulator contains a 100 V N-Channel Buck Switch, is easy to implement and is provided in the VSSOP-8 and the thermally enhanced WSON-8 packages. The regulator is based on a control scheme using an on-time inversely proportional to V_{IN}. The control scheme requires no loop compensation. Current limit is implemented with forced off-time, which is inversely proportional to V_{OUT}. This scheme ensures short circuit control while providing minimum foldback.

The LM5009A can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48 Volt Telecom and the new 42V Automotive power bus ranges. Features include: Thermal Shutdown, V_{CC} under-voltage lockout, Gate drive under-voltage lockout, Max Duty Cycle limit timer, intelligent current limit off timer, and a pre-charge switch.

Control Circuit Overview

The LM5009A is a Buck DC-DC regulator that uses a control scheme in which the on-time varies inversely with line voltage (V_{IN}). Control is based on a comparator and the on-time one-shot, with the output voltage feedback (FB) compared to an internal reference (2.5V). If the FB level is below the reference the buck switch is turned on for a fixed time determined by the line voltage and a programming resistor (R_T). Following the ON period the switch will remain off for at least the minimum off-timer period of 300ns. If FB is still below the reference at that time the switch will turn on again for another on-time period. This will continue until regulation is achieved.

The LM5009A operates in discontinuous conduction mode at light load currents, and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the output inductor starts at zero and ramps up to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the internal reference - until then the inductor current remains zero. In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Therefore at light loads the conversion efficiency is maintained, since the switching losses reduce with the reduction in load and frequency. The discontinuous operating frequency can be calculated as follows:

$$F = \frac{V_{OUT}^2 \times L \times 1.04 \times 10^{20}}{R_L \times (R_T)^2} \quad (1)$$

where R_L = the load resistance

In continuous conduction mode, current flows continuously through the inductor and never ramps down to zero. In this mode the operating frequency is greater than the discontinuous mode frequency and remains relatively constant with load and line variations. The approximate continuous mode operating frequency can be calculated as follows:

$$F = \frac{V_{OUT}}{1.385 \times 10^{-10} \times R_T} \tag{2}$$

The output voltage (V_{OUT}) is programmed by two external resistors as shown in the Block Diagram. The regulation point can be calculated as follows:

$$V_{OUT} = 2.5 \times (R_{FB1} + R_{FB2}) / R_{FB1} \tag{3}$$

The LM5009A regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. A minimum of 25mV to 50mV of ripple voltage at the feedback pin (FB) is required for the LM5009A. In cases where the capacitor ESR is too small, additional series resistance may be required (R3 in the Block Diagram).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in Figure 9. However, R3 slightly degrades the load regulation.

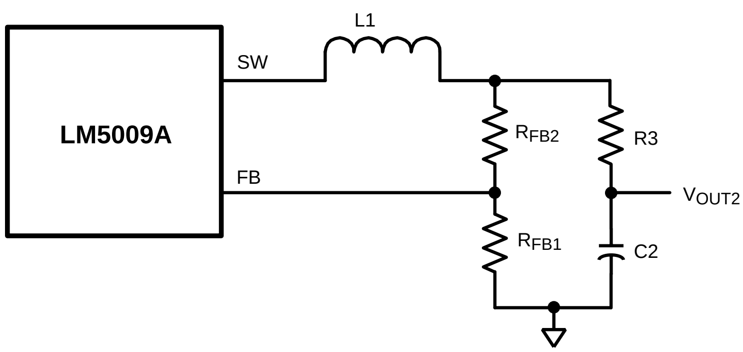


Figure 9. Low Ripple Output Configuration

Start-Up Regulator (V_{CC})

The high voltage bias regulator is integrated within the LM5009A. The input pin (VIN) can be connected directly to line voltages between 6V and 95V, with transient capability to 100V. Referring to the block diagram and the graph of V_{CC} vs V_{IN}, when V_{IN} is between 6V and the bypass threshold (nominally 8.5V), the bypass switch (Q2) is on, and V_{CC} tracks V_{IN} within 100 mV to 150 mV. The bypass switch on-resistance is approximately 100Ω, with inherent current limiting at approximately 100 mA. When V_{IN} is above the bypass threshold Q2 is turned off, and V_{CC} is regulated at 7V. The V_{CC} regulator output current is limited at approximately 9.2 mA. When the LM5009A is shutdown using the RT/SD pin, the V_{CC} bypass switch is shut off regardless of the voltage at V_{IN}.

When VIN exceeds the bypass threshold, the time required for Q2 to shut off is approximately 2 - 3 µs. The capacitor at VCC (C3) must be a minimum of 0.47 µF to prevent the voltage at VCC from rising above its absolute maximum rating in response to a step input applied at V_{IN}. C3 must be located as close as possible to the VCC and RTN pins. In applications with a relatively high input voltage, power dissipation in the bias regulator is a concern. An auxiliary voltage of between 7.5V and 14V can be diode connected to the VCC pin to shut off the V_{CC} regulator, thereby reducing internal power dissipation. The current required into the VCC pin is shown in the graph "I_{CC} Current vs. Applied V_{CC} Voltage". Internally a diode connects VCC to VIN requiring that the auxiliary voltage be less than V_{IN}.

The turn-on sequence is shown in Figure 10. During the initial delay (t1) VCC ramps up at a rate determined by its current limit and C3 while internal circuitry stabilizes. When V_{CC} reaches the upper threshold of its under-voltage lock-out (UVLO, typically 5.3V) the buck switch is enabled. The inductor current increases to the current limit threshold (I_{LIM}) and during t2 V_{OUT} increases as the output capacitor charges up. When V_{OUT} reaches the intended voltage the average inductor current decreases (t3) to the nominal load current (I_O).

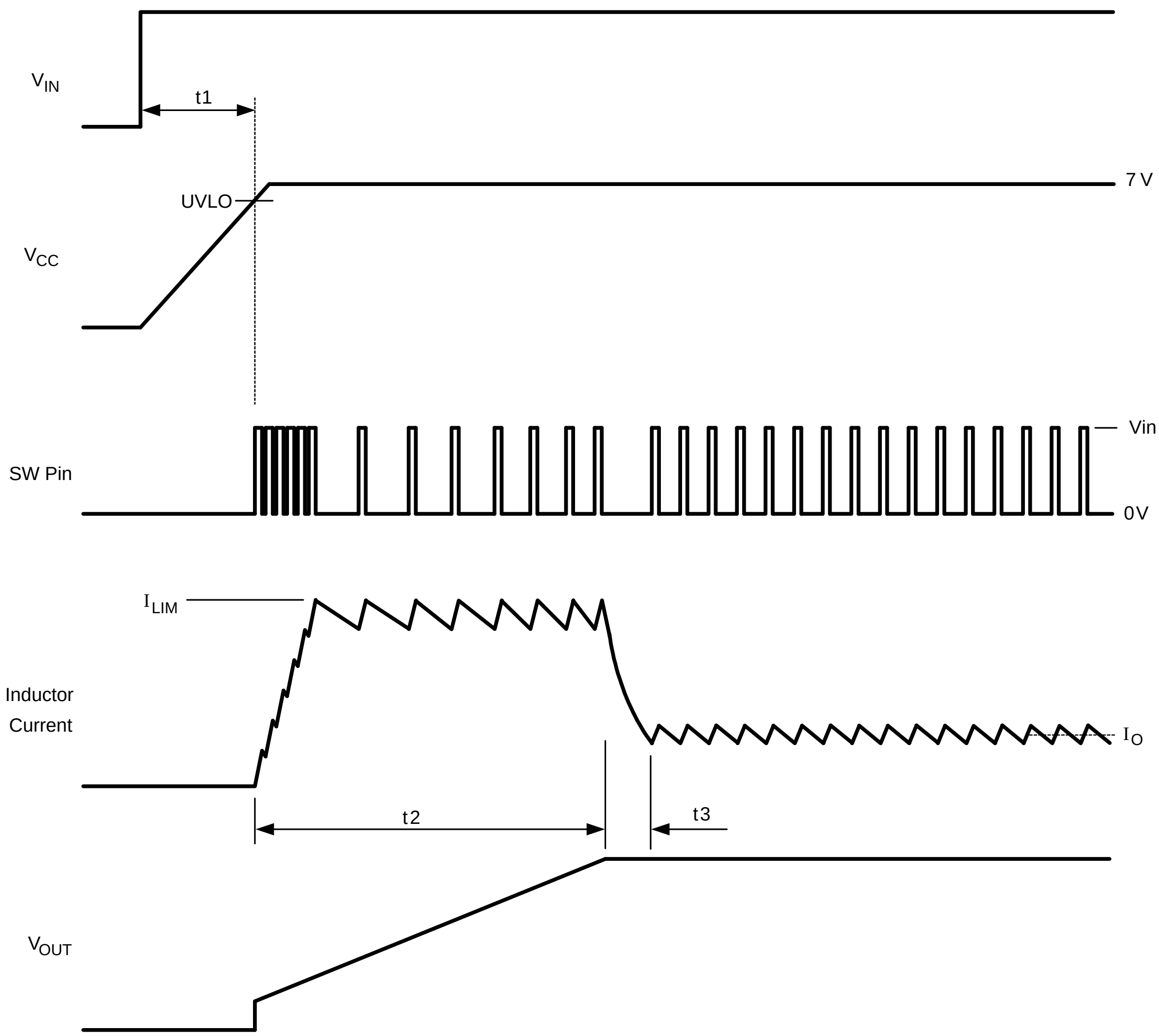


Figure 10. Startup Sequence

Regulation Comparator

The feedback voltage at FB is compared to an internal 2.5V reference. In normal operation (the output voltage is regulated), an on-time period is initiated when the voltage at FB falls below 2.5V. The buck switch will stay on for the on-time, causing the FB voltage to rise above 2.5V. After the on-time period, the buck switch will stay off until the FB voltage again falls below 2.5V. During start-up, the FB voltage will be below 2.5V at the end of each on-time, resulting in the minimum off-time of 300 ns. Bias current at the FB pin is nominally 100 nA.

Over-Voltage Comparator

The feedback voltage at FB is compared to an internal 2.875V reference. If the voltage at FB rises above 2.875V the on-time pulse is immediately terminated. This condition can occur if the input voltage, or the output load, change suddenly. The buck switch will not turn on again until the voltage at FB falls below 2.5V.

On-Time Generator and Shutdown

The on-time for the LM5009A is determined by the R_T resistor, and is inversely proportional to the input voltage (Vin), resulting in a nearly constant frequency as Vin is varied over its range. The on-time equation for the LM5009A is:

$$T_{ON} = 1.385 \times 10^{-10} \times R_T / V_{IN} \quad (4)$$

R_T should be selected for a minimum on-time (at maximum V_{IN}) greater than 400 ns, for proper current limit operation. This requirement limits the maximum frequency for each application, depending on V_{IN} and V_{OUT}.

The LM5009A can be remotely disabled by taking the R_T/SD pin to ground. See Figure 11. The voltage at the R_T/SD pin is between 1.5 and 3.0 volts, depending on Vin and the value of the R_T resistor.

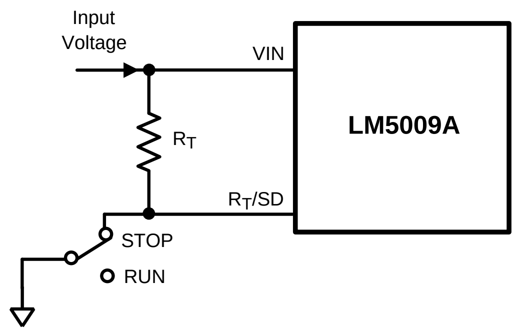


Figure 11. Shutdown Implementation

Current Limit

The LM5009A contains an intelligent current limit OFF timer. If the current in the Buck switch exceeds 0.3A the present cycle is immediately terminated, and a non-resetable OFF timer is initiated. The length of off-time is controlled by an external resistor (R_{CL}) and the FB voltage (see the graph Current Limit Off-Time vs. V_{FB} and R_{CL}). When FB = 0V, a maximum off-time is required, and the time is preset to 35µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation up to the maximum input voltage of 95V. In cases of overload where the FB voltage is above zero volts (not a short circuit) the current limit off-time will be less than 35µs. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and the start-up time. The off-time is calculated from the following equation:

$$T_{OFF} = \frac{10^{-5}}{0.285 + \frac{V_{FB}}{(6.35 \times 10^{-6} \times R_{CL})}} \quad (5)$$

The current limit sensing circuit is blanked for the first 50-70ns of each on-time so it is not falsely tripped by the current surge which occurs at turn-on. The current surge is required by the re-circulating diode (D1) for its turn-off recovery.

N-Channel Buck Switch and Driver

The LM5009A integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01 µF ceramic capacitor (C4) connected between the BST pin and SW pin provides the voltage to the driver during the on-time.

During each off-time, the SW pin is at approximately 0V, and the bootstrap capacitor charges from Vcc through the internal diode. The minimum OFF timer, set to 300ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

The internal pre-charge switch at the SW pin is turned on for ≅150 ns during the minimum off-time period, ensuring sufficient voltage exists across the bootstrap capacitor for the on-time. This feature helps prevent operating problems which can occur during very light load conditions, involving a long off-time, during which the voltage across the bootstrap capacitor could otherwise reduce below the Gate Drive UVLO threshold. The pre-charge switch also helps prevent startup problems which can occur if the output voltage is pre-charged prior to turn-on. After current limit detection, the pre-charge switch is turned on for the entire duration of the forced off-time .

Thermal Protection

The LM5009A should be operated so the junction temperature does not exceed 125°C during normal operation. An internal Thermal Shutdown circuit is provided to shutdown the LM5009A in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state by disabling the buck switch. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 140°C (typical hysteresis = 25°C) normal operation is resumed.

APPLICATIONS INFORMATION

SELECTION OF EXTERNAL COMPONENTS

A guide for determining the component values will be illustrated with a design example. Refer to the Block Diagram. The following steps will configure the LM5009A for:

- Input voltage range (Vin): 12V to 90V
- Output voltage (V_{OUT1}): 10V
- Load current (for continuous conduction mode): 100 mA to 150 mA

R_{FB1}, R_{FB2}: $V_{OUT} = V_{FB} \times (R_{FB1} + R_{FB2}) / R_{FB1}$, and since V_{FB} = 2.5V, the ratio of R_{FB2} to R_{FB1} calculates as 3:1. Standard values of 3.01 kΩ and 1.00 kΩ are chosen. Other values could be used as long as the 3:1 ratio is maintained.

F_s and R_T: The recommended operating frequency range for the LM5009A is 50 kHz to 1.1 MHz. Unless the application requires a specific frequency, the choice of frequency is generally a compromise since it affects the size of L1 and C2, and the switching losses. The maximum allowed frequency, based on a minimum on-time of 400 ns, is calculated from:

$$F_{MAX} = V_{OUT} / (V_{INMAX} \times 400\ ns) \quad (6)$$

For this exercise, Fmax = 277 kHz. From Equation 2, R_T calculates to 260 kΩ. A standard value 309 kΩ resistor will be used to allow for tolerances in Equation 2, resulting in a frequency of 234 kHz.

L1: The main parameter affected by the inductor is the output current ripple amplitude. The choice of inductor value therefore depends on both the minimum and maximum load currents, keeping in mind that the maximum ripple current occurs at maximum Vin.

a) **Minimum load current:** To maintain continuous conduction at minimum Io (100 mA), the ripple amplitude (I_{OR}) must be less than 200 mA peak-to-peak so the lower peak of the waveform does not reach zero. L1 is calculated using the following equation:

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{OR} \times F_s \times V_{IN}} \quad (7)$$

At Vin = 90V, L1(min) calculates to 190 µH. The next larger standard value (220 µH) is chosen and with this value I_{OR} calculates to 173 mA peak-to-peak at Vin = 90V, and 32 mA peak-to-peak at Vin = 12V.

b) **Maximum load current:** At a load current of 150 mA, the peak of the ripple waveform must not reach the minimum value of the LM5009A's current limit threshold (240 mA). Therefore the ripple amplitude must be less than 180 mA peak-to-peak, which is already satisfied in the above calculation. With L1 = 220 µH, at maximum Vin and Io, the peak of the ripple will be 236 mA. While L1 must carry this peak current without saturating or exceeding its temperature rating, it also must be capable of carrying the maximum value of the LM5009A's current limit threshold (360 mA) without saturating, since the current limit is reached during startup.

The DC resistance of the inductor should be as low as possible to minimize its power loss.

C3: The capacitor on the V_{CC} output provides not only noise filtering and stability, but its primary purpose is to prevent false triggering of the V_{CC} UVLO at the buck switch on and off transitions. C3 should be no smaller than 0.47 µF.

C2 and R3: When selecting the output filter capacitor C2, the items to consider are ripple voltage due to its ESR, ripple voltage due to its capacitance, and the nature of the load.

ESR and R3: A low ESR for C2 is generally desirable so as to minimize power losses and heating within the capacitor. However, the regulator requires a minimum amount of ripple voltage at the feedback input for proper loop operation. For the LM5009A the minimum ripple required at pin 5 is 25 mV peak-to-peak, requiring a minimum ripple at V_{OUT} of 100 mV. Since the minimum ripple current (at minimum Vin) is 32 mA peak-to-peak, the minimum ESR required at V_{OUT} is 100 mV/32 mA = 3.12Ω. Since quality capacitors for SMPS applications have an ESR considerably less than this, R3 is inserted as shown in the Block Diagram. R3's value, along with C2's ESR, must result in at least 25 mV peak-to-peak ripple at pin 5. Generally, R3 will be 0.5 to 4.0Ω.

C2: C2 should generally be no smaller than 3.3µF. Typically, its value is 10µF to 20µF, with the optimum value determined by the load. If the load current is fairly constant, a small value suffices for C2. If the load current includes significant transients, a larger value is necessary. For each application, experimentation is needed to determine the optimum values for R3 and C2.

R_{CL}: When current limit is detected, the minimum off-time set by this resistor must be greater than the maximum normal off-time, which occurs at maximum input voltage. Using Equation 4, the minimum on-time is 476 ns, yielding an off-time of 3.8 µs (at 234 kHz). Due to the 25% tolerance on the on-time, the off-time tolerance is also 25%, yielding a maximum off-time of 4.75 µs. Allowing for the response time of the current limit detection circuit (350 ns) increases the maximum off-time to 5.1 µs. This is increased an additional 25% to 6.4 µs to allow for the tolerances of Equation 5. Using Equation 5, R_{CL} calculates to 310 kΩ at V_{FB} = 2.5V. A standard value 316 kΩ resistor will be used.

D1: The important parameters are reverse recovery time and forward voltage. The reverse recovery time determines how long the reverse current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is only this diode's voltage which forces the inductor current to reduce during the forced off-time. For this reason, a higher voltage is better, although that affects efficiency. A good choice is a Schottky power diode, such as the DFLS1100. D1's reverse voltage rating must be at least as great as the maximum Vin, and its current rating be greater than the maximum current limit threshold (360 mA).

C1: This capacitor's purpose is to supply most of the switch current during the on-time, and limit the voltage ripple at Vin, on the assumption that the voltage source feeding Vin has an output impedance greater than zero. At maximum load current, when the buck switch turns on, the current into pin 8 will suddenly increase to the lower peak of the output current waveform, ramp up to the peak value, then drop to zero at turn-off. The average input current during this on-time is the load current (150 mA). For a worst case calculation, C1 must supply this average load current during the maximum on-time. To keep the input voltage ripple to less than 2V (for this exercise), C1 calculates to:

$$C1 = \frac{I \times t_{ON}}{\Delta V} = \frac{0.15\text{A} \times 3.57\ \mu\text{s}}{2.0\text{V}} = 0.268\ \mu\text{F} \tag{8}$$

Quality ceramic capacitors in this value have a low ESR which adds only a few millivolts to the ripple. It is the capacitance which is dominant in this case. To allow for the capacitor's tolerance, temperature effects, and voltage effects, a 1.0 µF, 100V, X7R capacitor will be used.

C4: The recommended value is 0.01µF for C4, as this is appropriate in the majority of applications. A high quality ceramic capacitor, with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turn-on. A low ESR also ensures a quick recharge during each off-time. At minimum Vin, when the on-time is at maximum, it is possible during start-up that C4 will not fully recharge during each 300 ns off-time. The circuit will not be able to complete the start-up, and achieve output regulation. This can occur when the frequency is intended to be low (e.g., R_T = 500K). In this case C4 should be increased so it can maintain sufficient voltage across the buck switch driver during each on-time.

C5: This capacitor helps avoid supply voltage transients and ringing due to long lead inductance at V_{IN}. A low ESR, 0.1µF ceramic chip capacitor is recommended, located close to the LM5009A.

FINAL CIRCUIT

The final circuit is shown in Figure 12. The circuit was tested, and the resulting performance is shown in Figure 13 and Figure 14.

PC BOARD LAYOUT

The LM5009A regulation and over-voltage comparators are very fast, and as such will respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The components at pins 1, 2, 3, 5, and 6 should be as physically close as possible to the IC, thereby minimizing noise pickup in the PC tracks. The current loop formed by D1, L1, and C2 should be as small as possible. The ground connection from D1 to C1 should be as short and direct as possible.

If the internal dissipation of the LM5009A produces excessive junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the WSON-8 package can be soldered to a ground plane on the PC board, and that plane should extend out from beneath the IC to help dissipate the heat. Additionally, the use of wide PC board traces, where possible, can also help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.

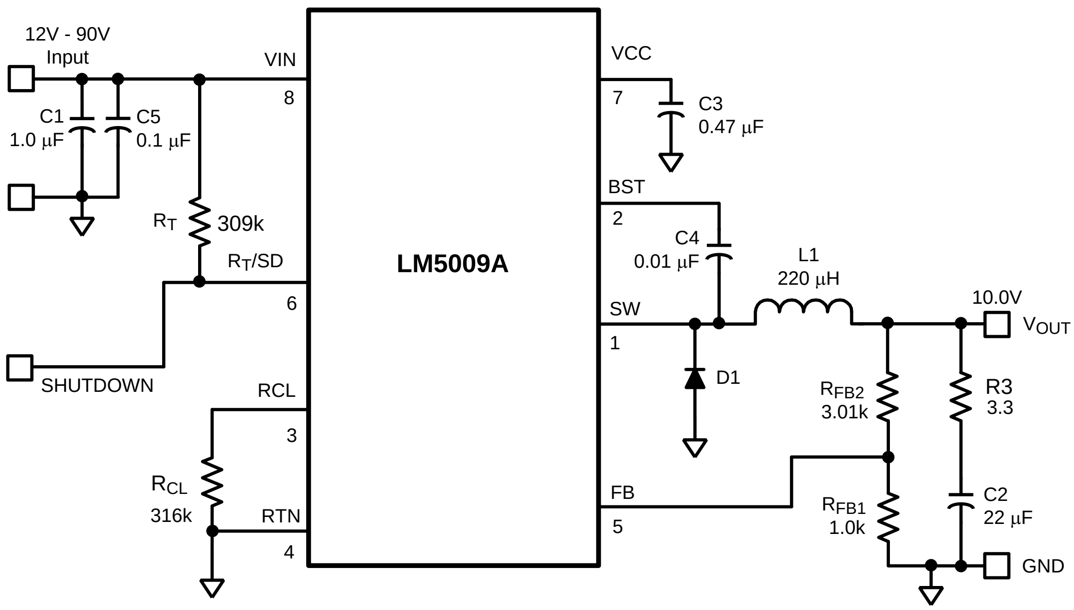


Figure 12. LM5009A Example Circuit

Table 2. Bill of Materials

Item	Description	Part Number	Value
C1	Ceramic Capacitor	TDK C4532X7R2A105M	1 µF, 100V
C2	Ceramic Capacitor	TDK C4532X7R1E226M	22 µF, 25V
C3	Ceramic Capacitor	Kemet C1206C474K5RAC	0.47 µF, 50V
C4	Ceramic Capacitor	Kemet C1206C103K5RAC	0.01 µF, 50V
C5	Ceramic Capacitor	TDK C3216X7R2A104M	0.1 µF, 100V
D1	Schottky Power Diode	Diodes Inc. DFLS1100	100V, 1A
L1	Power Inductor	COILTRONICS DR125-221-R, or	220 µH
		TDK SLF10145T-221MR65	
R_{FB2}	Resistor	Vishay CRCW12063011F	3.01 kΩ
R_{FB1}	Resistor	Vishay CRCW12061001F	1.0 kΩ
R3	Resistor	Vishay CRCW12063R30F	3.3 Ω
R_T	Resistor	Vishay CRCW12063093F	309 kΩ
R_{CL}	Resistor	Vishay CRCW12063163F	316 kΩ
U1	Switching Regulator	Texas Instruments LM5009A	

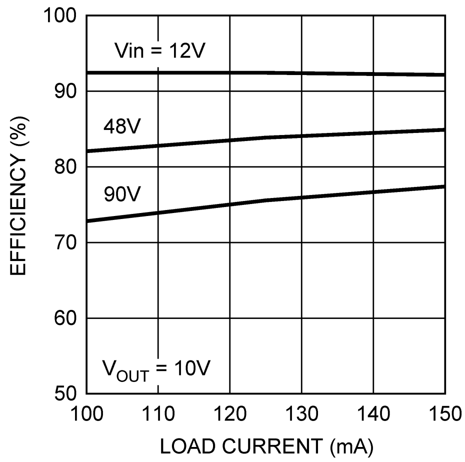


Figure 13. Efficiency vs. Load Current and V_{IN}

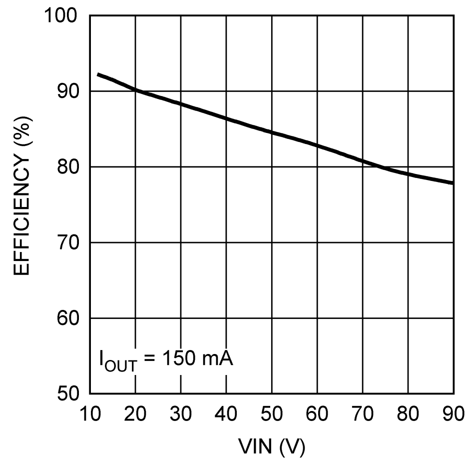


Figure 14. Efficiency vs. V_{IN}

LOW OUTPUT RIPPLE CONFIGURATIONS

For applications where low output ripple is required, the following options can be used to reduce or nearly eliminate the ripple.

a) Reduced ripple configuration: In Figure 15, Cff is added across R_{FB2} to AC-couple the ripple at V_{OUT} directly to the FB pin. This allows the ripple at V_{OUT} to be reduced to a minimum of 25 mVp-p by reducing R3, since the ripple at V_{OUT} is not attenuated by the feedback resistors. The minimum value for Cff is determined from:

$$Cff = \frac{3 \times t_{ON\,(max)}}{(R_{FB1} // R_{FB2})} \quad (9)$$

where $t_{ON(max)}$ is the maximum on-time, which occurs at $V_{IN(min)}$. The next larger standard value capacitor should be used for Cff.

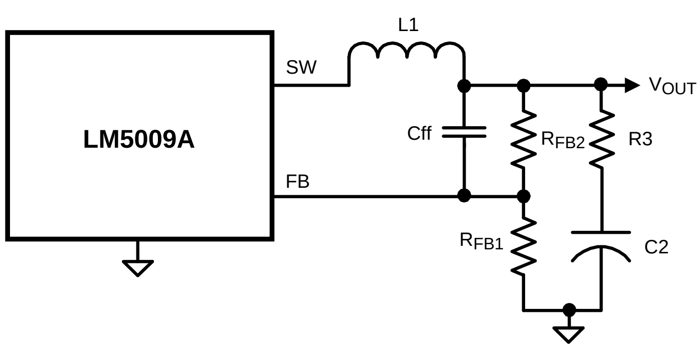


Figure 15. Reduced Ripple Configuration

b) Minimum ripple configuration: If the application requires a lower value of ripple (<10 mVp-p), the circuit of Figure 16 can be used. R3 is removed, and the resulting output ripple voltage is determined by the inductor's ripple current and C2's characteristics. RA and CA are chosen to generate a sawtooth waveform at their junction, and that voltage is AC-coupled to the FB pin via CB. To determine the values for RA, CA and CB, use the following procedure:

Calculate $V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN(min)})))$ (10)

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time (typically 1V). VA is the DC voltage at the RA/CA junction, and is used in Equation 11.

Calculate $RA \times CA = (V_{IN(min)} - V_A) \times t_{ON}/\Delta V$ (11)

where t_{ON} is the maximum on-time (at minimum input voltage), and ΔV is the desired ripple amplitude at the RA/CA junction (typically 40-50 mV). RA and CA are then chosen from standard value components to satisfy the above product. Typically CA is 1000 pF to 5000 pF, and RA is 10 kΩ to 300 kΩ. CB is then chosen large compared to CA, typically 0.1 µF.

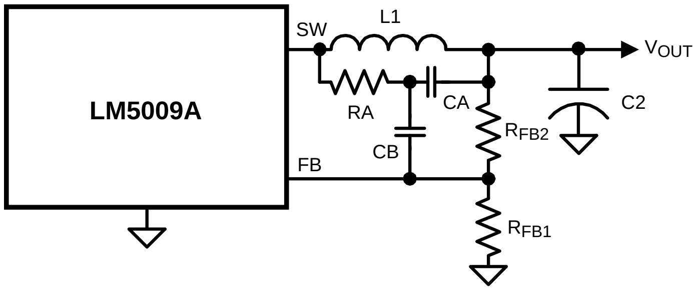


Figure 16. Minimum Output Ripple Using Ripple Injection

c) Alternate minimum ripple configuration: The circuit in Figure 17 is the same as that in the Block Diagram, except the output voltage is taken from the junction of R3 and C2. The ripple at V_{OUT} is determined by the inductor's ripple current and C2's characteristics. However, R3 slightly degrades the load regulation. This circuit may be suitable if the load current is fairly constant.

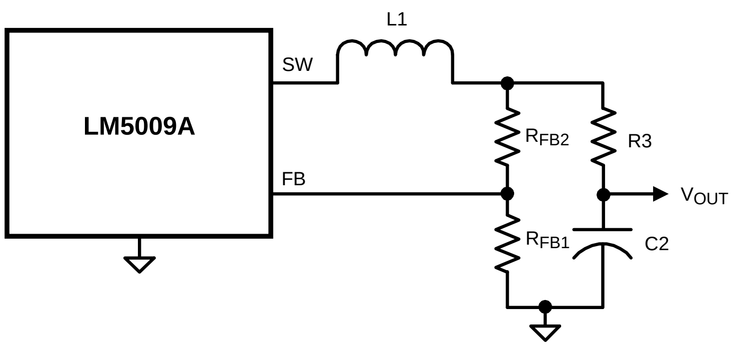


Figure 17. Alternate Minimum Output Ripple

REVISION HISTORY

Changes from Revision F (February 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM5009AMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SLLA	Samples
LM5009AMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SLLA	Samples
LM5009ASD/NOPB	ACTIVE	WSON	NGU	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5009ASD	Samples
LM5009ASDX/NOPB	ACTIVE	WSON	NGU	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	5009ASD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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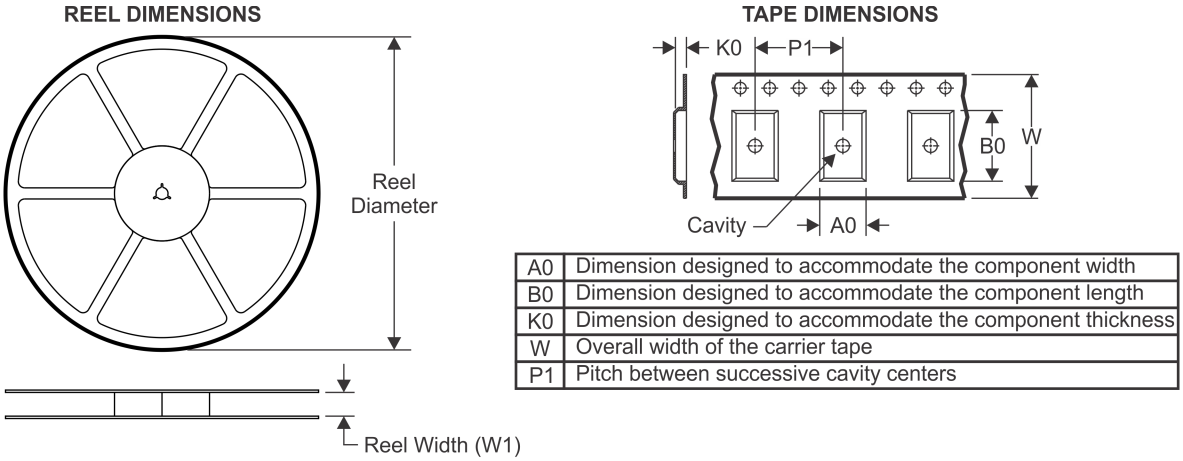
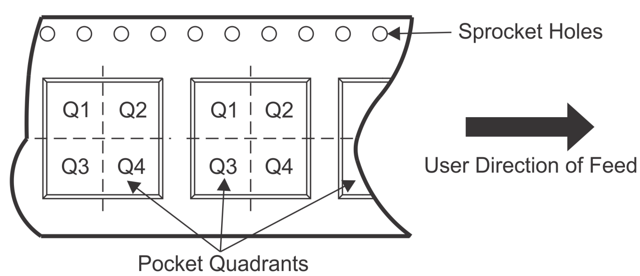


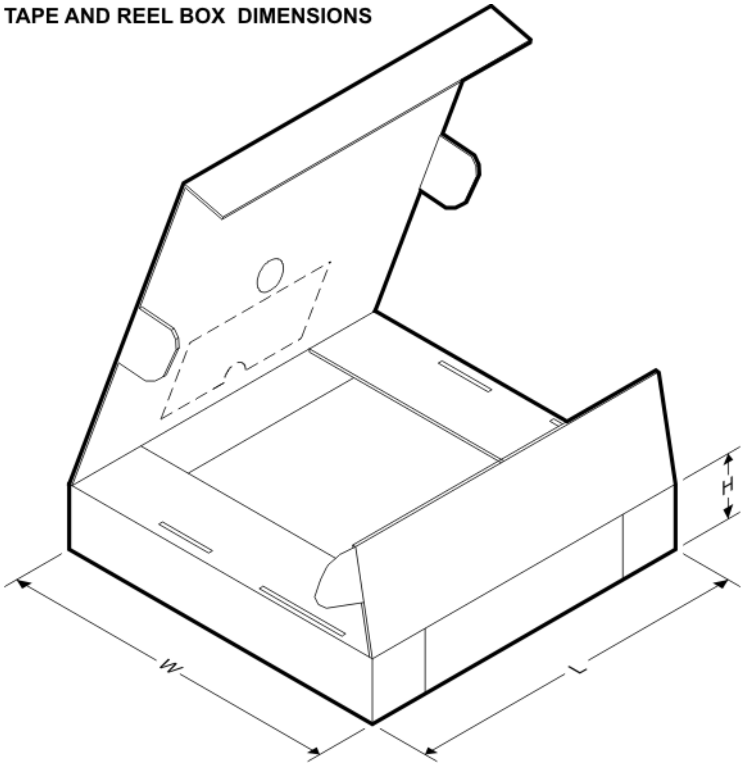
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5009AMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5009AMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5009ASD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5009ASDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

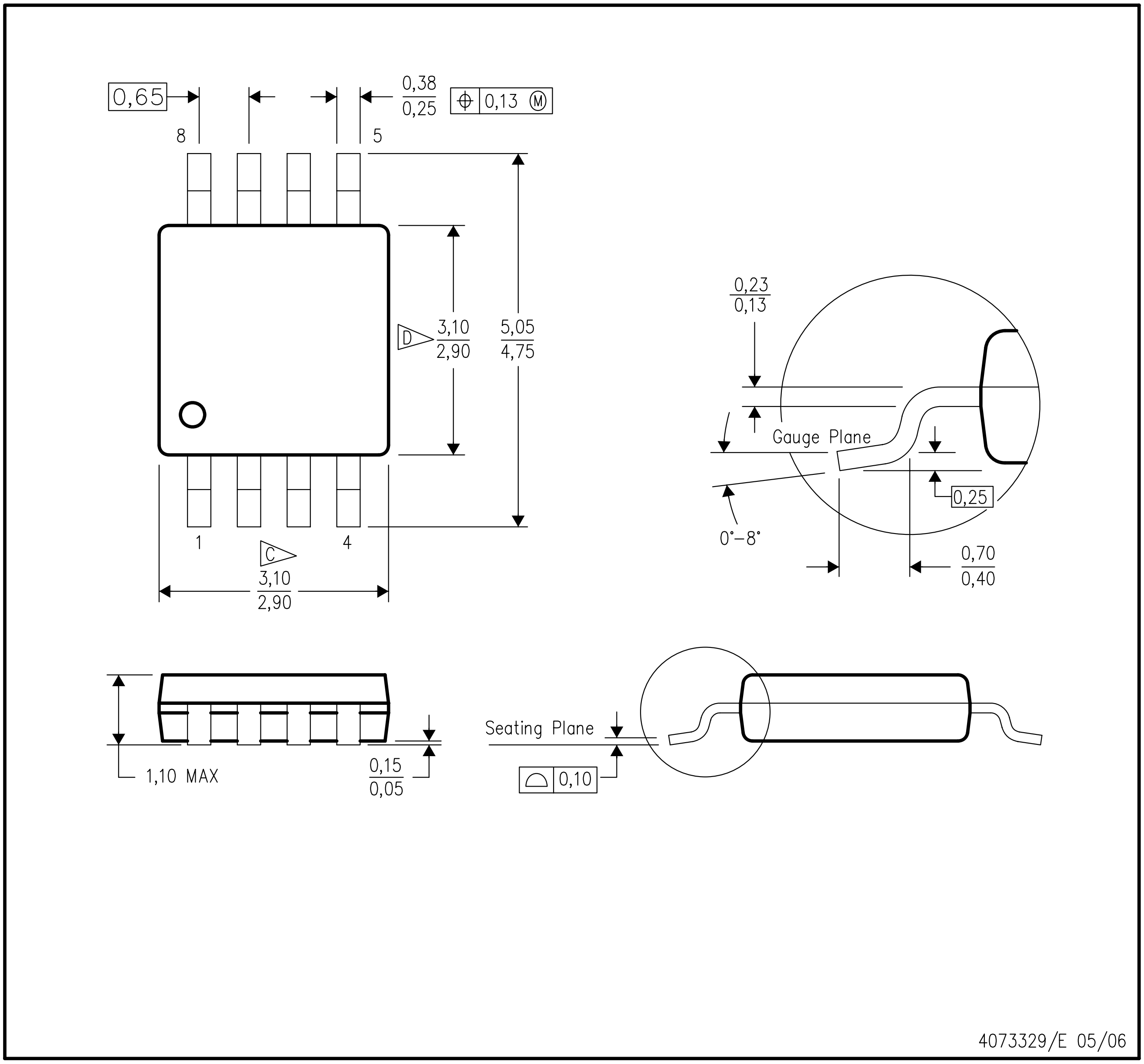
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

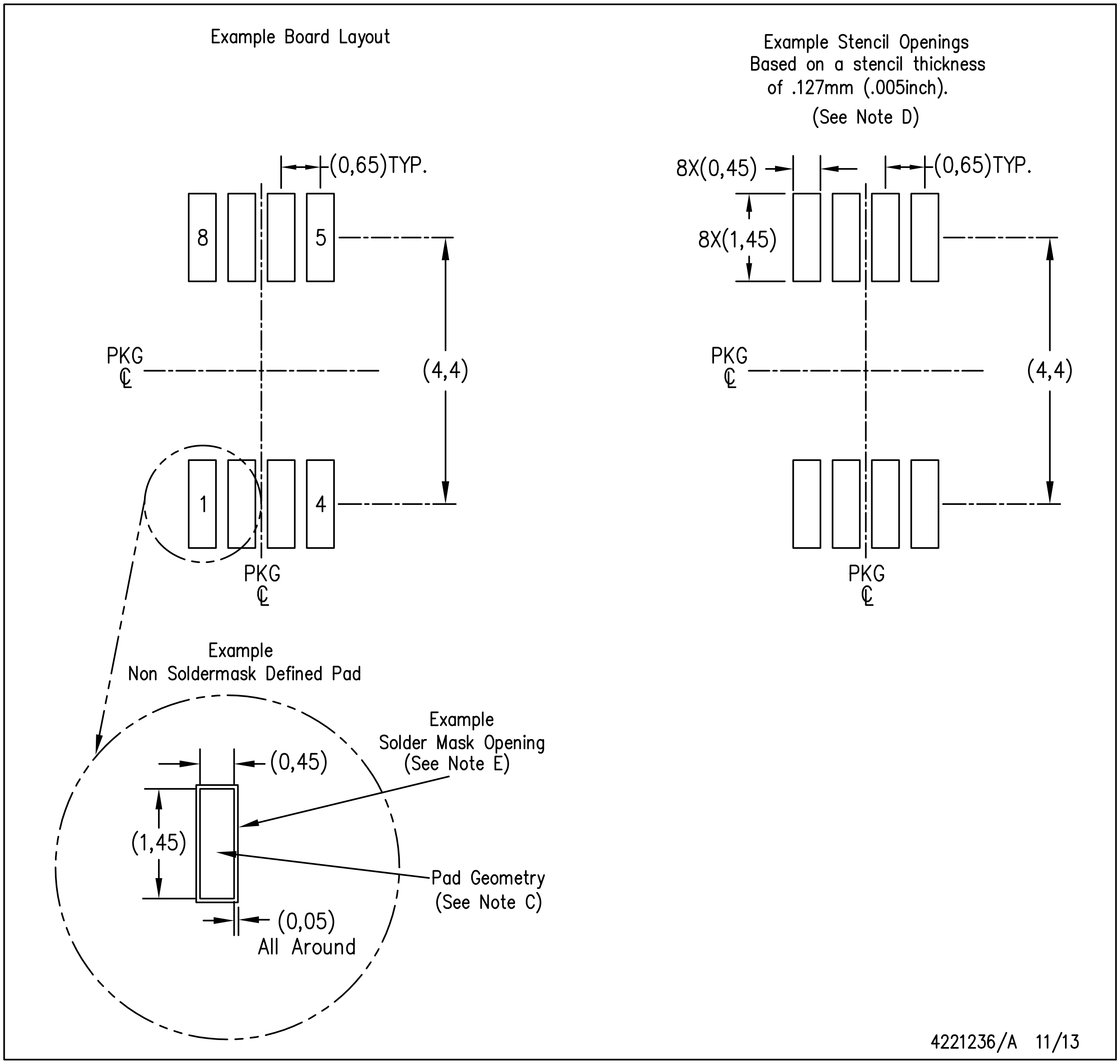
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5009AMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM5009AMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM5009ASD/NOPB	WSON	NGU	8	1000	210.0	185.0	35.0
LM5009ASDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE

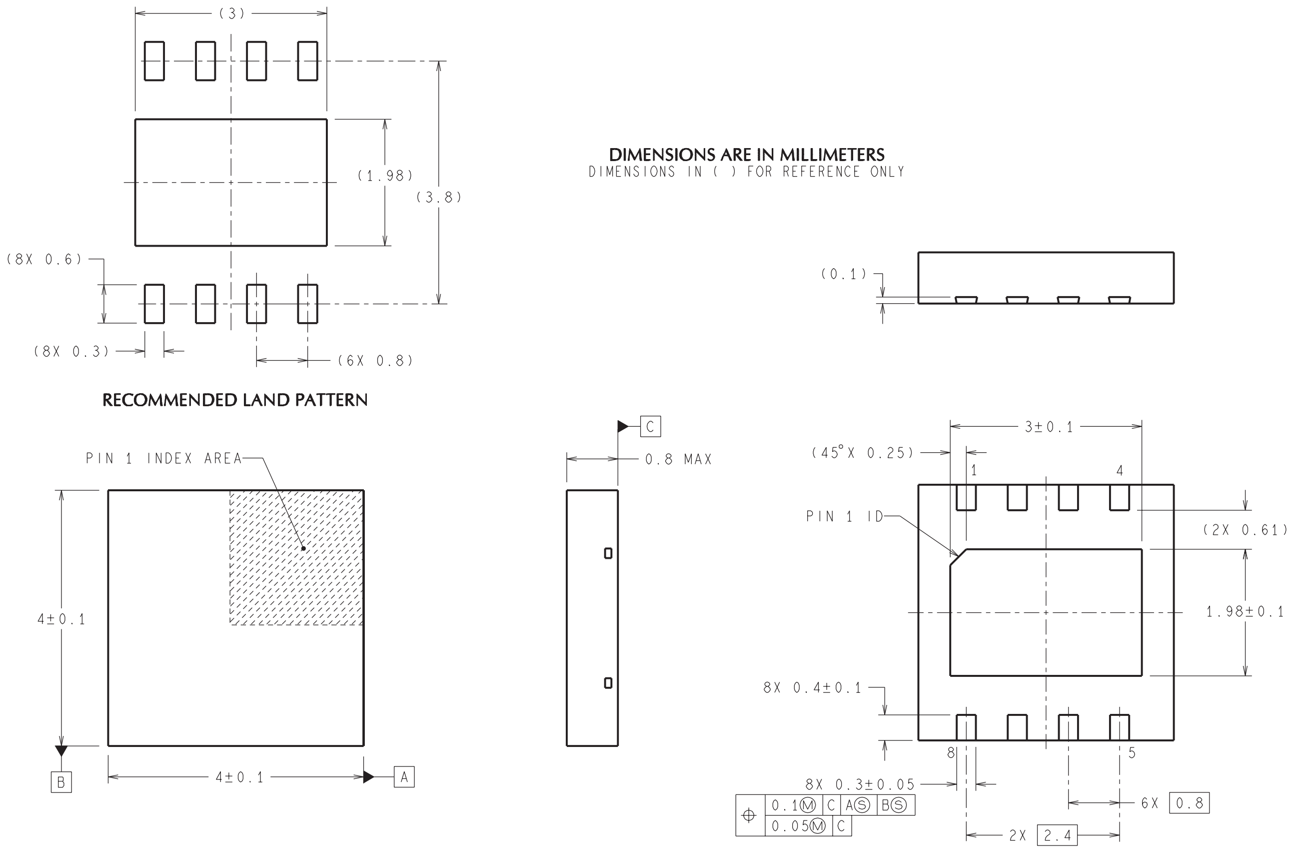


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.


(3)
(1.98)
(3.8)
(8X 0.6)
(8X 0.3)
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RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
PIN 1 INDEX AREA
4±0.1
B
4±0.1
A
C
0.8 MAX
3±0.1
(45° X 0.25)
1
4
PIN 1 ID
(2X 0.61)
1.98±0.1
8X 0.4±0.1
8
5
8X 0.3±0.05
0.1Ⓜ C AⓈ BⓈ
0.05Ⓜ C
6X 0.8
2X 2.4

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