LM34927 Integrated Secondary Side Bias Regulator for Isolated DC-DC Converters

Check for Samples: LM34927

FEATURES

- **Wide 7.5 V to 100 V Input Range**
- **Integrated 100 V, High and Low Side Switches**
- **No Schottky Required**
- **Constant On-Time Control**
- **No Loop Compensation Required**
- **Ultra-Fast Transient Response**
- **Nearly Constant Operating Frequency**
- **Intelligent Peak Current Limit**
- **Adjustable Output Voltage From 1.225 V**
- **Precision 2% Feedback Reference**
- **Frequency Adjustable to 1 MHz**
- **Adjustable Undervoltage Lockout (UVLO)**
- **Remote Shutdown**
- **Thermal Shutdown**
- **Packages:**
  - **WSON-8**
  - **SO PowerPAD-8**

APPLICATIONS

- **Isolated Telecom Bias Supply**
- **Isolated Automotive and Industrial Electronics**

DESCRIPTION

The LM34927 regulator features all of the functions needed to implement a low cost, efficient, isolated bias regulator. This high voltage regulator contains two 100V N-Channel MOSFET switches - a high-side buck switch and a low-side synchronous switch. The Constant-on-time (COT) control scheme employed in the LM34927 requires no loop compensation and provides excellent transient response. The regulator operates with an on-time that is inversely proportional to the input voltage. This feature allows the operating frequency to remain relatively constant. An intelligent peak current limit is implemented with integrated sense circuit. Other features include a programmable input under voltage comparator to inhibit operation during low-voltage conditions. Protection features include thermal shutdown and V_{CC} Undervoltage Lockout (UVLO). The LM34927 is offered in WSON-8 and SO PowerPAD-8 plastic packages.

Typical Application

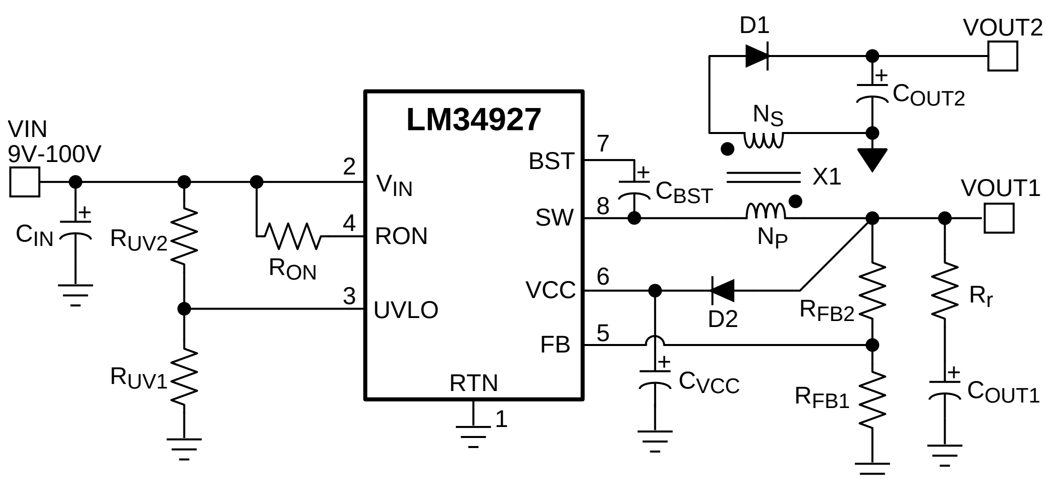


Figure 1. Typical Application Schematic

Connection Diagram

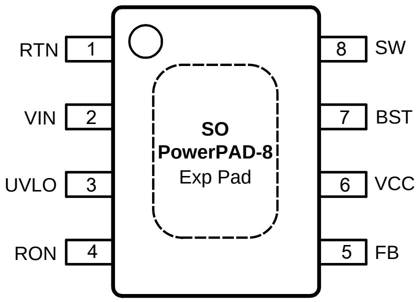


Figure 2. Top View (Connect Exposed Pad to RTN)

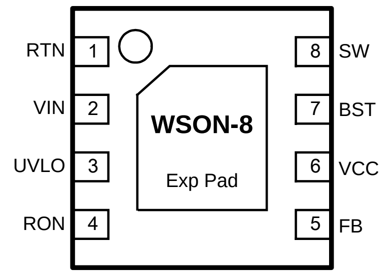


Figure 3. Top View (Connect Exposed Pad to RTN)

Table 1. Pin Descriptions

Pin	Name	Description	Application Information
1	RTN	Ground	Ground connection of the integrated circuit.
2	V_{IN}	Input Voltage	Operating input range is 7.5 V to 100 V.
3	UVLO	Input Pin of Undervoltage Comparator	Resistor divider from V_{IN} to UVLO to GND programs the undervoltage detection threshold. An internal current source is enabled when UVLO is above 1.225V to provide hysteresis. When UVLO pin is pulled below 0.66V externally, the parts goes in shutdown mode.
4	R_{ON}	On-Time Control	A resistor between this pin and V_{IN} sets the switch on-time as a function of V_{IN}. Minimum recommended on-time is 100 ns at max input voltage.
5	FB	Feedback	This pin is connected to the inverting input of the internal regulation comparator. The regulation level is 1.225 V.
6	V_{CC}	Output from the Internal High Voltage Series Pass Regulator. Regulated at 7.6 V.	The internal V_{CC} regulator provides bias supply for the gate drivers and other internal circuitry. A 1.0 μF decoupling capacitor is recommended.
7	BST	Bootstrap Capacitor	An external capacitor is required between the BST and SW pins (0.01 μF ceramic). The BST pin capacitor is charged by the V_{CC} regulator through an internal diode when the SW pin is low.
8	SW	Switching Node	Power switching node. Connect to the output inductor and bootstrap capacitor.
	Exp Pad	Exposed Pad	Exposed pad must be connected to RTN pin. Connect to system ground plane on application board for reduced thermal resistance.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[(1)(2)]

V_{IN}, UVLO to RTN	–0.3 V to 100 V
SW to RTN	–1.5 V to V_{IN} +0.3 V
SW to RTN (100ns transient)	–5 V to VIN +0.3 V
BST to V_{CC}	100 V
BST to SW	13 V
R_{ON} to RTN	–0.3 V to 100 V
V_{CC} to RTN	–0.3 V to 13 V
FB to RTN	–0.3 V to 5 V
ESD Rating, Human Body Model[(3)]	2 kV
Lead Temperature[(4)]	200°C
Storage Temperature Range	–55°C to +150°C
Maximum Junction Temperature	150°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics. The RTN pin is the GND reference electrically connected to the substrate.
(3) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
(4) For detailed information on soldering plastic SO PowerPAD package, refer to the Packaging Data Book. Max solder time not to exceed 4 seconds.

Recommended Operating Ratings[(1)]

V_{IN} Voltage	7.5 V to 100 V
Operating Junction Temperature	−40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics. The RTN pin is the GND reference electrically connected to the substrate.

Thermal Characteristics

		WSON-8	SO PowerPAD-8	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	41.3	41.1	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.2	2.4	°C/W
Ψ_{JB}	Junction-to-board thermal characteristic parameter	19.2	24.4	°C/W
θ_{JB}	Junction-to-board thermal resistance	19.1	30.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34.7	37.3	°C/W
Ψ_{JT}	Junction-to-top thermal characteristic parameter	0.3	6.7	°C/W

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full Operating Junction Temperature range. V_{IN} = 48 V, unless otherwise stated. See [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC} Supply						
V_{CC} Reg	V_{CC} Regulator Output	V_{IN} = 48 V, I_{CC} = 20 mA	**6.25**	7.6	**8.55**	V
	V_{CC} Current Limit	V_{IN} = 48 V[2]	**26**			mA
	V_{CC} UVLO Threshold (V_{CC} increasing)		**4.15**	4.5	**4.9**	V
	V_{CC} UVLO Hysteresis			300		mV
	V_{CC} Drop Out Voltage	V_{IN} = 8 V, I_{CC} = 20 mA		2.3		V
	I_{IN} Operating Current	Non-Switching, FB = 3 V		1.75		mA
	I_{IN} Shutdown Current	UVLO = 0 V		50	**225**	µA
Under-Voltage Sensing Function						
	UV Threshold	UV Rising	**1.19**	1.225	**1.26**	V
	UV Hysteresis Input Current	UV = 2.5 V	**-10**	-20	**-29**	µA
	Remote Shutdown Threshold	Voltage at UVLO Falling	**0.32**	0.66		V
	Remote Shutdown Hysteresis			110		mV
Regulation and Over-Voltage Comparators						
	FB Regulation Level	Internal Reference Trip Point for Switch ON	**1.2**	1.225	**1.25**	V
	FB Overvoltage Threshold	Trip Point for Switch OFF		1.62		V
	FB Bias Current			60		nA
Switch Characteristics						
	Buck Switch $R_{DS(ON)}$	I_{TEST} = 200 mA, BST-SW = 7 V		0.8	**1.8**	Ω
	Synchronous $R_{DS(ON)}$	I_{TEST} = 200 mA		0.45	**1**	Ω
	Gate Drive UVLO	$V_{BST} - V_{SW}$ Rising	**2.4**	3	**3.6**	V
	Gate Drive UVLO Hysteresis			260		mV
Minimum Off-Time						
	Minimum Off-Timer	FB = 0 V		144		ns
On Time Generator						
	T_{ON} Test 1	V_{IN} = 32 V, R_{ON} = 100 k	**270**	350	**460**	ns
	T_{ON} Test 2	V_{IN} = 48 V, R_{ON} = 100 k	**188**	250	**336**	ns
	T_{ON} Test 3	V_{IN} = 75 V, R_{ON} = 250 k	**250**	370	**500**	ns
	T_{ON} Test 4	V_{IN} = 10 V, R_{ON} = 250 k	**1880**	3200	**4425**	ns
Current Limit						
	Current Limit Threshold		**0.7**	1.02	**1.3**	A
	Current Limit Response Time	Time to Switch Off		150		ns
	OFF-Time Generator (Test 1)	FB = 0.1 V, V_{IN} = 48 V		12		µs
	OFF-Time Generator (Test 2)	FB = 1.0 V, V_{IN} = 48 V		2.5		µs
Thermal Shutdown						
Tsd	Thermal Shutdown Temperature			165		°C
	Thermal Shutdown Hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	SO PowerPAD-8		40		°C/W
		WSON-8		40		°C/W

(1) All limits are specified by design. All electrical characteristics having room temperature limits are tested during production at T_A = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) V_{CC} provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Typical Characteristics

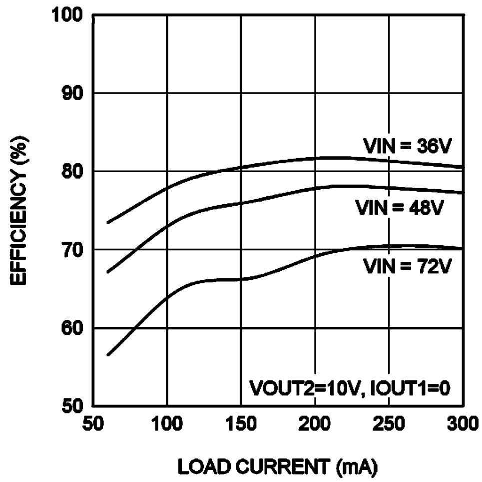


Figure 4. Efficiency at 750 kHz, V_{OUT1} = 10 V

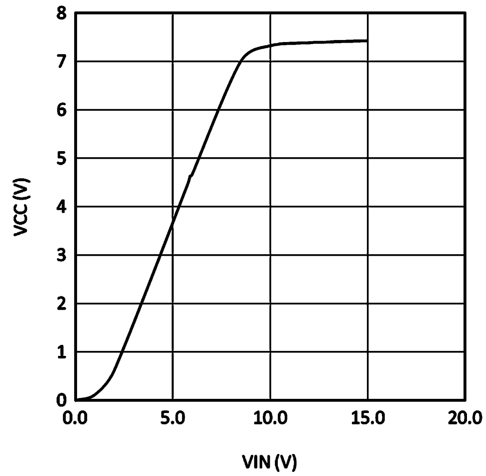


Figure 5. V_{CC} vs V_{IN}

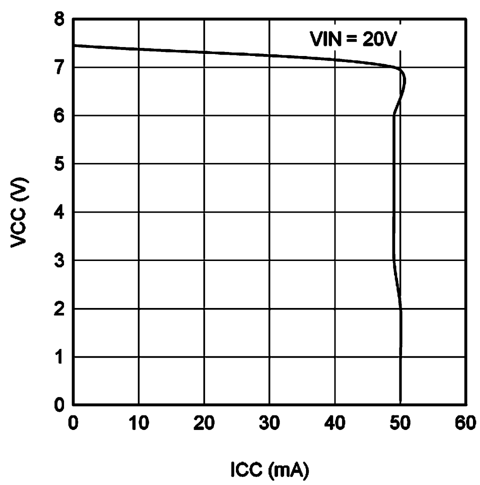


Figure 6. V_{CC} vs I_{CC}

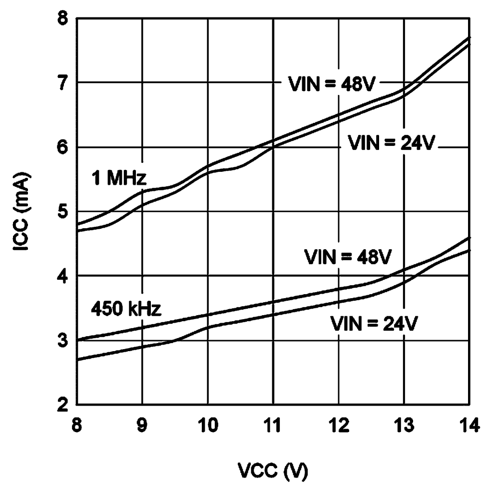


Figure 7. I_{CC} vs External V_{CC}

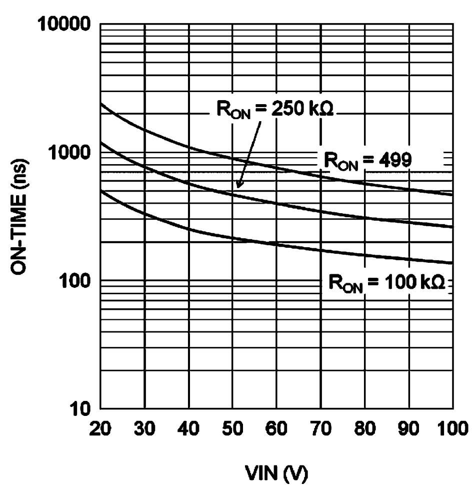


Figure 8. T_{ON} vs V_{IN} and R_{ON}

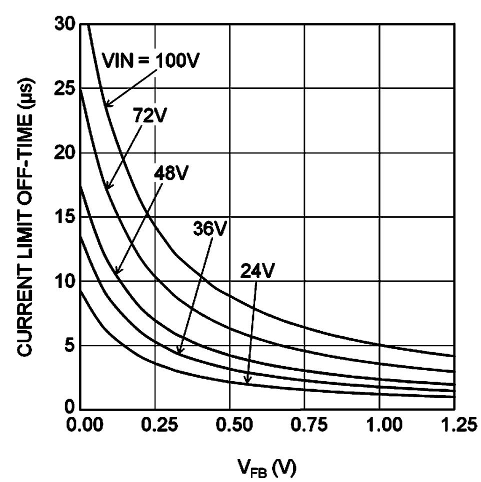


Figure 9. T_{OFF} (I_{LIM}) vs V_{FB} and V_{IN}

Typical Characteristics (continued)

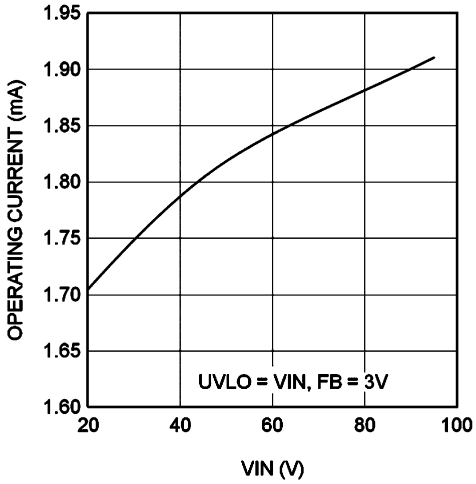


Figure 10. I_{IN} vs V_{IN} (Operating, Non Switching)

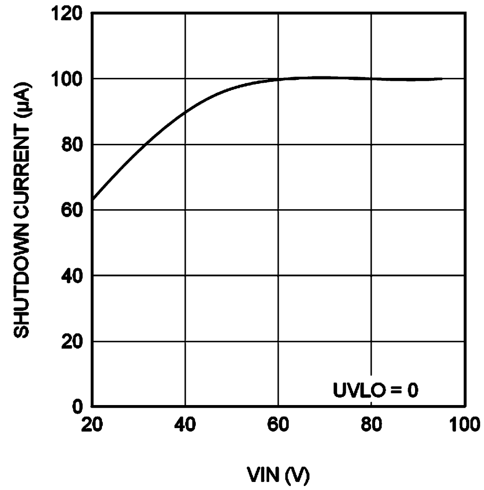


Figure 11. I_{IN} vs V_{IN} (Shutdown)

Functional Block Diagram

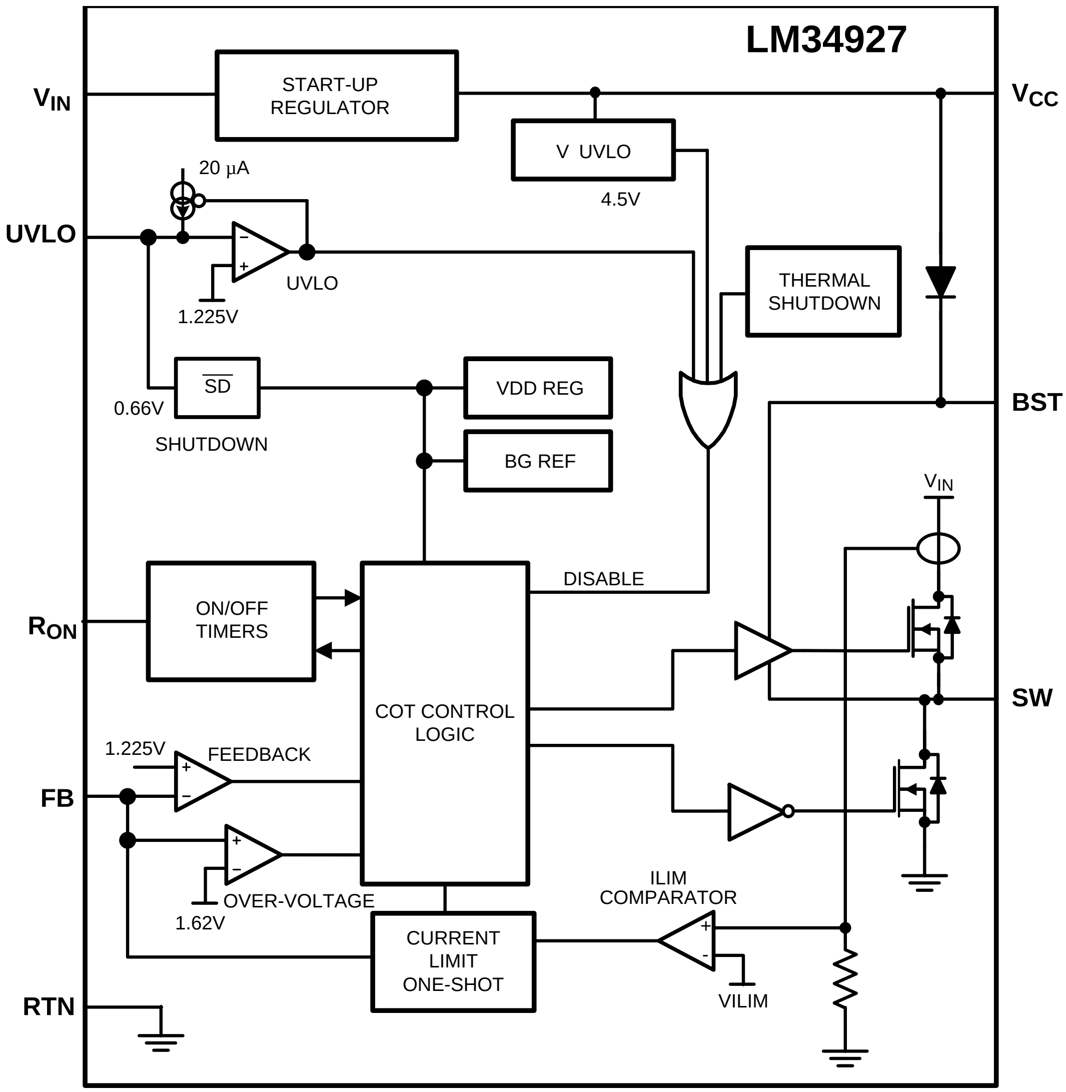


Figure 12. Functional Block Diagram

Functional Description

The LM34927 step-down switching regulator features all the functions needed to implement a low cost, efficient, isolated bias supply. This high voltage regulator contains 100 V, N-channel buck and synchronous switches, is easy to implement, and is provided in thermally enhanced SO PowerPAD-8 and WSON-8 packages. The regulator operation is based on a constant on-time control scheme using an on-time inversely proportional to V_{IN}. This control scheme does not require loop compensation. Current limit is implemented with forced off-time inversely proportional to V_{OUT}. This scheme ensures short circuit protection while providing minimum foldback. The simplified block diagram of the LM34927 is shown in Figure 12.

The LM34927 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48 V telecom and 42 V automotive power bus ranges. Protection features include: thermal shutdown, Undervoltage Lockout, minimum forced off-time, and an intelligent current limit.

Control Overview

The LM34927 regulator employs a control principle based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (1.225 V). If the FB voltage is below the reference the internal buck switch is switched on for the one-shot timer period, which is a function of the input voltage and the programming resistor (RT). Following the on-time the switch remains off until the FB voltage falls below the reference, and the forced minimum off-time has expired. When the FB pin voltage falls below the reference and the off-time one-shot period expires, the buck switch is then turned on for another on-time one-shot period. This will continue until regulation is achieved and the FB voltage is approximately equal to 1.225 V (typ).

In a synchronous buck converter, the low side (sync) FET is 'on' when the high side (buck) FET is 'off'. The inductor current ramps up when the high side switch is 'on' and ramps down when the high side switch is 'off'. There is no diode emulation feature in this IC, and therefore, the inductor current may ramp in the negative direction at light load. This causes the converter to operate in continuous conduction mode (CCM) regardless of the output loading. The operating frequency remains relatively constant with load and line variations. The operating frequency can be calculated as:

$$f\text{sw} = \frac{V_{OUT}}{10^{-10} \times R_{ON}} \tag{1}$$

The output voltage (V_{OUT}) is set by two external resistors (R_{FB1}, R_{FB2}). The regulated output voltage is calculated as:

$$V_{OUT} = 1.225\text{V} \times \frac{R_{FB2} + R_{FB1}}{R_{FB1}} \tag{2}$$

$$\frac{R_{FB2}}{R_{FB1}} = \frac{V_{OUT} - 1.225\text{V}}{1.225\text{V}} \tag{3}$$

This regulator regulates the output voltage based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor (C_{OUT}). A minimum of 25 mV of ripple voltage at the feedback pin (FB) is required for the LM34927. In cases where the capacitor ESR is too small, additional series resistance may be required (R_C in Figure 13).

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor, as shown in Figure 13. However, R_C slightly degrades the load regulation.

V_{CC} Regulator

The LM34927 contains an internal high voltage linear regulator with a nominal output of 7.6 V. The input pin (V_{IN}) can be connected directly to the line voltages up to 100 V. The V_{CC} regulator is internally current limited to 30mA. The regulator sources current into the external capacitor at V_{CC}. This regulator supplies current to internal circuit blocks including the synchronous MOSFET driver and the logic circuits. When the voltage on the V_{CC} pin reaches the Undervoltage Lockout threshold of 4.5 V, the IC is enabled.

The V_{CC} regulator contains an internal diode connection to the BST pin to replenish the charge in the gate drive boot capacitor when SW pin is low.

At high input voltages, the power dissipated in the high voltage regulator is significant and can limit the overall achievable output power. As an example, with the input at 48 V and switching at high frequency, the V_{CC} regulator may supply up to 7 mA of current resulting in 48 V x 7 mA = 336 mW of power dissipation. If the V_{CC} voltage is driven externally by an alternate voltage source, between 8 V and 14 V, the internal regulator is disabled. This reduces the power dissipation in the IC.

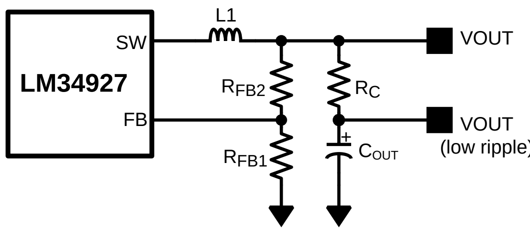


Figure 13. Low Ripple Output Configuration

Regulation Comparator

The feedback voltage at FB is compared to an internal 1.225 V reference. In normal operation, when the output voltage is in regulation, an on-time period is initiated when the voltage at FB falls below 1.225 V. The high side switch will stay on for the on-time, causing the FB voltage to rise above 1.225 V. After the on-time period, the high side switch will stay off until the FB voltage again falls below 1.225 V. During start-up, the FB voltage will be below 1.225 V at the end of each on-time causing the high side switch to turn on immediately after the minimum forced off-time of 144 ns. The high side switch can be turned off before the on-time is over, if peak current in the inductor reaches the current limit threshold.

Overvoltage Comparator

The feedback voltage at FB is compared to an internal 1.62 V reference. If the voltage at FB rises above 1.62 V the on-time pulse is immediately terminated. This condition can occur if the input voltage and/or the output load changes suddenly. The high side switch will not turn on again until the voltage at FB falls below 1.225 V.

On-Time Generator

The on-time for the LM34927 is determined by the R_{ON} resistor, and is inversely proportional to the input voltage (V_{IN}), resulting in a nearly constant frequency as V_{IN} is varied over its range. The on-time equation for the LM34927 is:

$$T_{ON} = \frac{10^{-10} \times R_{ON}}{V_{IN}} \quad (4)$$

See Figure 14. R_{ON} should be selected for a minimum on-time (at maximum V_{IN}) greater than 100 ns, for proper operation. This requirement limits the maximum frequency for each application.

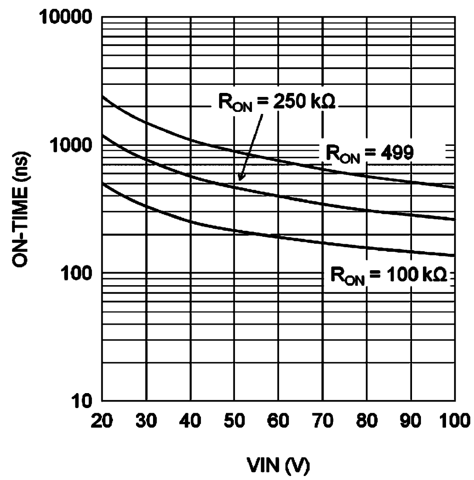


Figure 14. T_{ON} vs V_{IN} and R_{ON}

Current Limit

The LM34927 contains an intelligent current limit off-timer. If the current in the buck switch exceeds 1.02 A the present cycle is immediately terminated, and a non-resetable off-timer is initiated. The length of off-time is controlled by the FB voltage and the input voltage V_{IN}. As an example, when FB = 0 V and V_{IN} = 48 V, a maximum off-time is set to 16 µs. This condition occurs when the output is shorted, and during the initial part of start-up. This amount of time ensures safe short circuit operation even up to the maximum input voltage of 100 V.

In cases of overload where the FB voltage is above zero volts (not a short circuit) the current limit off-time is reduced. Reducing the off-time during less severe overloads reduces the amount of foldback, recovery time, and start-up time. The off-time is calculated from Equation 5:

$$T_{OFF(ILIM)} = \frac{0.07 \times V_{IN}}{V_{FB} + 0.2\,V}\ \mu s \tag{5}$$

The current limit protection feature is peak limited, the maximum average output will be less than the peak.

N-Channel Buck Switch and Driver

The LM34927 integrates an N-Channel Buck switch and associated floating high voltage gate driver. The gate driver circuit works in conjunction with an external bootstrap capacitor and an internal high voltage diode. A 0.01 uF ceramic capacitor connected between the BST pin and SW pin provides the voltage to the driver during the on-time. During each off-time, the SW pin is at approximately 0 V, and the bootstrap capacitor charges from V_{CC} through the internal diode. The minimum off-timer, set to 144 ns, ensures a minimum time each cycle to recharge the bootstrap capacitor.

Synchronous Rectifier

The LM34927 provides an internal synchronous N-Channel MOSFET rectifier. This MOSFET provides a path for the inductor current to flow when the high-side MOSFET is turned off.

The synchronous rectifier has no diode emulation mode, and is designed to keep the regulator in continuous conduction mode even during light loads which would otherwise result in discontinuous operation. This feature specifically allows the user to design a secondary regulator using a transformer winding off the main inductor to generate the alternate regulated output voltage.

Under Voltage Detector

The LM34927 contains a dual level Undervoltage Lockout (UVLO) circuit. When the UVLO pin voltage is below 0.66 V, the controller is in a low current shutdown mode. When the UVLO pin voltage is greater than 0.66 V but less than 1.225 V, the controller is in standby mode. In standby mode the V_{CC} bias regulator is active while the regulator output is disabled. When the V_{CC} pin exceeds the V_{CC} undervoltage thresholds and the UVLO pin voltage is greater than 1.225V, normal operation begins. An external set-point voltage divider from V_{IN} to GND can be used to set the minimum operating voltage of the regulator.

UVLO hysteresis is accomplished with an internal 20 µA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to quickly raise the voltage at the UVLO pin. The hysteresis is equal to the value of this current times the resistance R_{UV2}.

Table 2. Under Voltage Detector

UVLO	V_{CC}	Mode	Description
<0.66 V		Shutdown	V_{CC} regulator disabled. Switcher disabled.
0.66 V-1.225 V		Standby	V_{CC} regulator enabled. Switcher disabled.
>1.225 V	V_{CC} < 4.5 V	Standby	V_{CC} regulator enabled. Switcher disabled.
	V_{CC} > 4.5 V	Operating	V_{CC} enabled. Switcher enabled.

If the UVLO pin is wired directly to the V_{IN} pin, the regulator will begin operation once the V_{CC} undervoltage is satisfied.

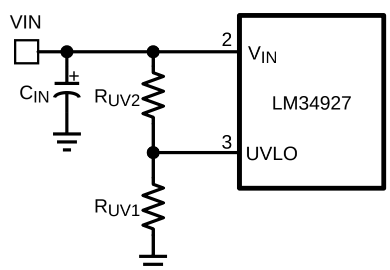


Figure 15. UVLO Resistor Setting

Thermal Protection

The LM34927 should be operated so the junction temperature does not exceed 150°C during normal operation. An internal Thermal Shutdown circuit is provided to protect the LM34927 in the event of a higher than normal junction temperature. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the buck switch and the V_{CC} regulator. This feature prevents catastrophic failures from accidental device overheating. When the junction temperature reduces below 145°C (typical hysteresis = 20°C), the V_{CC} regulator is enabled, and normal operation is resumed.

APPLICATION INFORMATION

Typical Isolated Bias Application Schematic

A typical isolated bias supply application is shown in Figure 16. Inductor (L) in a typical buck circuit is replaced with a coupled inductor (X1). A diode (D1) is used to rectify the voltage on the secondary output. The nominal voltage at the secondary output (V_{OUT2}) is given by:

$$V_{OUT2} = V_{OUT1} \times \frac{N_S}{N_P} - V_F \quad (6)$$

where VF is the forward voltage drop of D1, and NP, NS are the number of turns on the primary and secondary of coupled inductor X1. For output voltage (V_{OUT1}) above the maximum V_{CC} (8.3V), the V_{CC} pin can be diode connected to V_{OUT1} for higher efficiency and low dissipation in the IC.

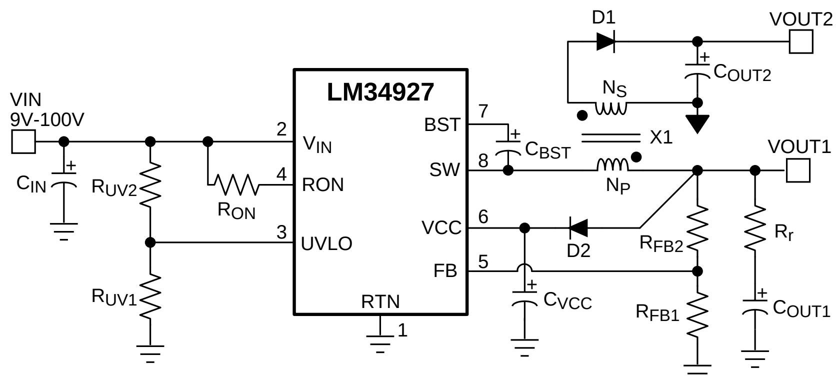


Figure 16. Typical Isolated Application Schematic

3W Isolated Bias Application Schematic

A complete 3 W bias supply for isolated bias supply application is shown in Figure 17.

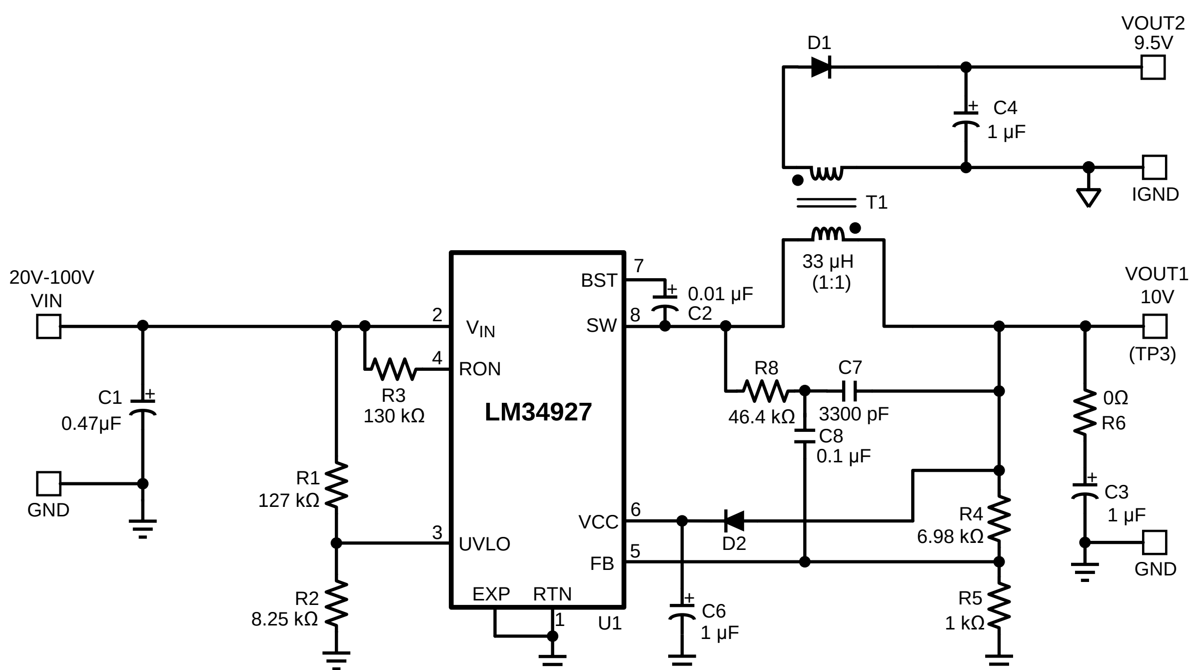


Figure 17. A 3 W Isolated Application Schematic

Lowest Part Count Isolated Application Schematic

A low part count schematic for isolated bias application is shown in Figure 18. The primary should not be loaded in this configuration. If primary loading is required a diode will be required between V_{OUT} primary and V_{CC}.

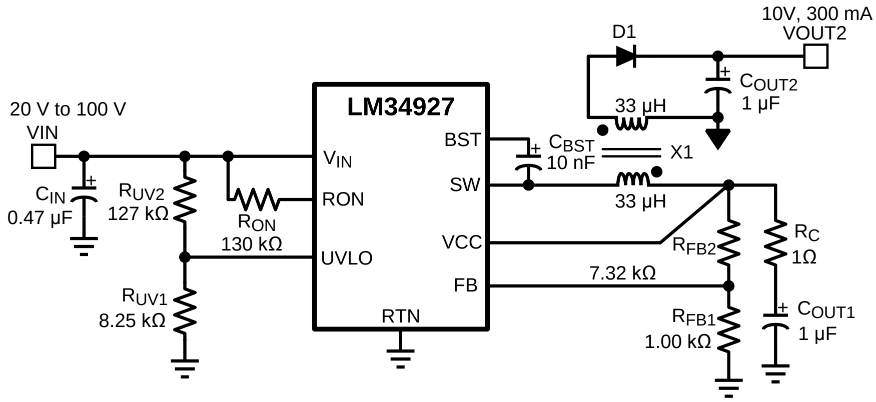


Figure 18. Lowest Part Count Isolated Application Schematic

Ripple Configuration

LM34927 uses Constant-On-Time (COT) control scheme, in which the on-time is terminated by an on-timer, and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore this change in feedback voltage (ΔV_{FB}) during off-time must be large enough to suppress any noise component present at the feedback node.

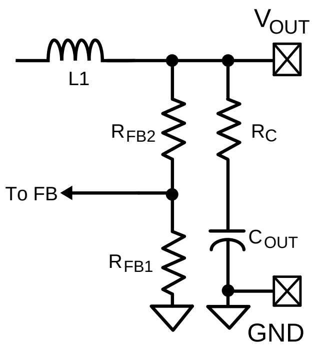
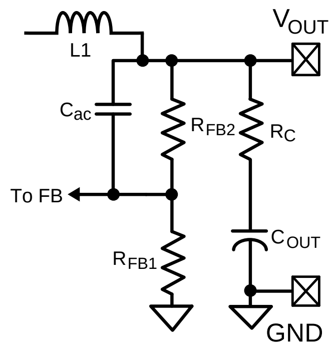
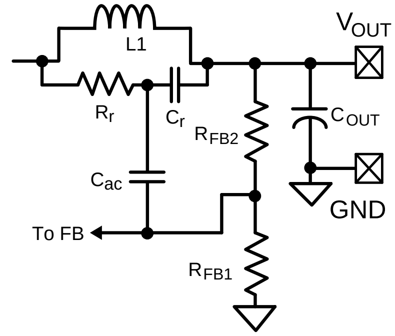
Table 3 shows three different methods for generating appropriate voltage ripple at the feedback node. Type 1 and Type 2 ripple circuits couple the ripple at the output of the converter to the feedback node (FB). The output voltage ripple has two components:

1. Capacitive ripple caused by the inductor current ripple charging/discharging the output capacitor.
2. Resistive ripple caused by the inductor current ripple flowing through the ESR of the output capacitor.

The capacitive ripple is not in phase with the inductor current. As a result of this, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during off-time. The resistive ripple must exceed the capacitive ripple at the output node (V_{OUT}) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

Type 3 ripple method uses R_r and C_r and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is ac coupled using C_{ac} to the feedback node (FB). Since this circuit does not use the output voltage ripple, it is ideally suited for applications where low output voltage ripple is required. See application note AN-1481 for more details for each ripple generation method.

Table 3. Ripple Configuration

Type 1 Lowest Cost Configuration	Type 2 Reduced Ripple Configuration	Type 3 Minimum Ripple Configuration
		
$R_C \geq \frac{25\,mV}{\Delta I_{L(MIN)}} \times \frac{V_{OUT}}{V_{REF}}$ (7)	$C \geq \frac{5}{f_{sw}(R_{FB2}\|\|R_{FB1})}$ $R_C \geq \frac{25\,mV}{\Delta I_{L(MIN)}}$ (8)	$C_r = 3300\,pF$ $C_{ac} = 100\,nF$ $R_rC_r \leq \frac{(V_{IN(MIN)} - V_{OUT}) \times T_{ON}}{25\,mV}$ (9)

Soft Start

A soft-start feature can be implemented to the LM34927 using an external circuit. As shown in Figure 19, the soft-start circuit consists of one capacitor, C_1, two resistors, R_1 and R_2, and a diode, D. During the initial start-up, the VCC voltage is established prior to the V_{OUT} voltage. D is thereby forward biased and the FB voltage is pulled up above the reference voltage (1.225V). The switcher is disabled. With the charging of the capacitor C_1, the voltage at node B gradually decreases. Due to the action of the control circuit, V_{OUT} will gradually rise to maintain the FB voltage at the reference voltage. Once the voltage at node B is lower than the FB voltage, plus the voltage drop of D, the soft-start is finished and D is reverse biased.

During the initial part of the start-up, the FB voltage can be approximated as follows. Please note that the effect of R_1 has been ignored to simplify the calculation:

$$V_{FB} = (VCC - V_D) \times \frac{R_{FB1} \times R_{FB2}}{R_2 \times (R_{FB1} + R_{FB2}) + R_{FB1} \times R_{FB2}} \quad (10)$$

To achieve the desired soft-start, the following design guidance is recommended:

1. R_2 is selected so that V_{FB} is higher than 1.225V for a V_{CC} of 4.5V, but is lower than 5V when V_{CC} is 8.55V. If an external V_{CC} is used, V_{FB} should not exceed 5V at maximum V_{CC}.
2. C_1 is selected to achieve the desired start-up time that can be determined as:

$$t_S = C_1 \times (R_2 + \frac{R_{FB1} \times R_{FB2}}{R_{FB1} + R_{FB2}}) \quad (11)$$

3. R_1 is used to maintain the node B voltage at zero after the soft-start is finished. A value larger than the feedback resistor divider is preferred.

   Based on the schematic shown in Figure 17, selecting C_1 = 1 uF, R_2=1 kΩ, R_1=30 kΩ results in a soft-start time of about 2ms.

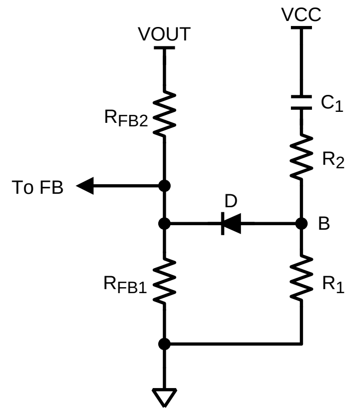


Figure 19. Soft-Start Circuit

Layout Recommendation

A proper layout is essential for optimum performance of the circuit. In particular, the following guidelines should be observed:

1. C_{IN}: The loop consisting of input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore the input capacitor should be placed close to the IC, directly across V_{IN} and RTN pins and the connections to these two pins should be direct to minimize the loop area. In general it is not possible to accommodate all of input capacitance near the IC. A good practice is to use a 0.1µF or 0.47µF capacitor directly across the V_{IN} and RTN pins close to the IC, and the remaining bulk capacitor as close as possible (see Figure 20 Placement of Bypass Capacitors).
2. C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high and low side gate drivers. These two capacitors should also be placed as close to the IC as possible, and the connecting trace lengths and loop area should be minimized (See Figure 20).
3. The Feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of LM34927. Therefore care should be taken while routing the feedback trace so avoid coupling any noise to this pin. In particular, feedback trace should not run close to magnetic components, or parallel to any other switching trace.
4. SW trace: SW node switches rapidly between V_{IN} and GND every cycle and is therefore a possible source of noise. SW node area should be minimized. In particular SW node should not be inadvertently connected to a copper plane or pour.

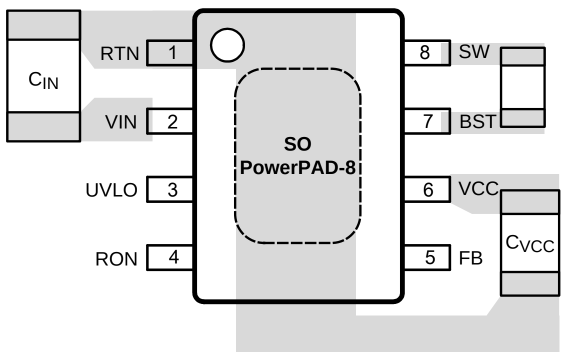


Figure 20. Placement of Bypass Capacitors

Typical Buck Configuration

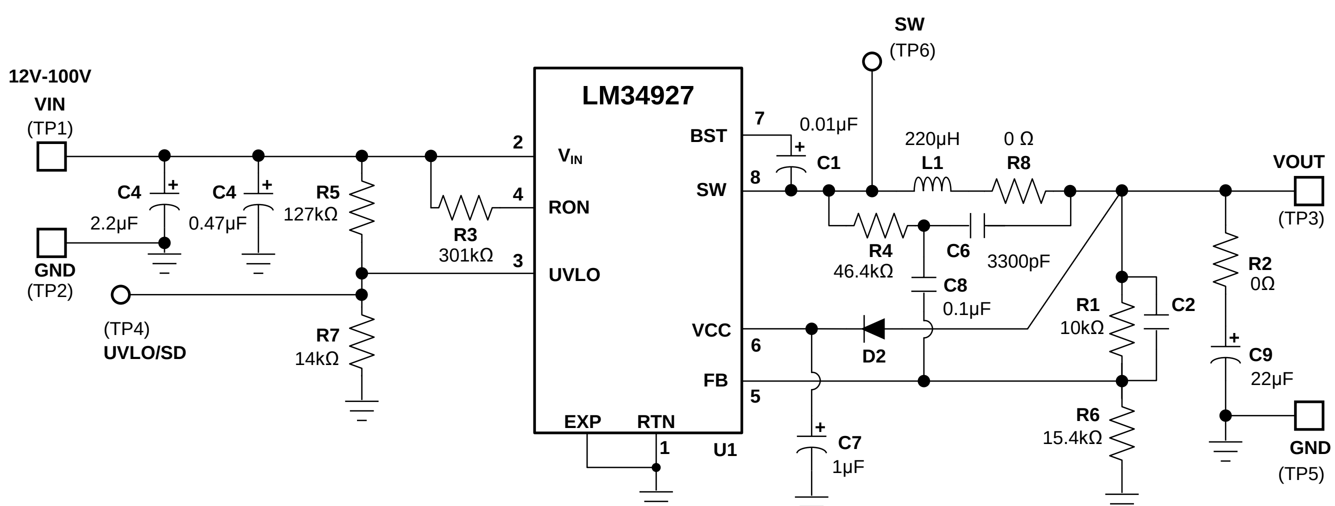


Figure 21. Typical Buck Configuration:
Vin = 9 V to 100 V, Vout = 3.3 V, Iout = 500 mA

Performance Curves

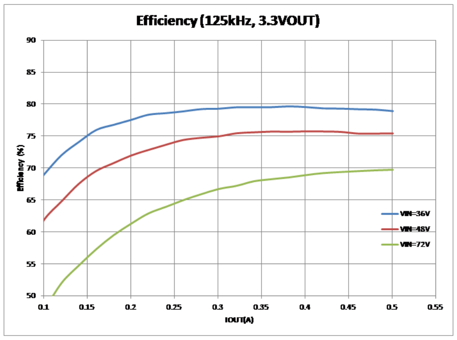


Figure 22. Efficiency

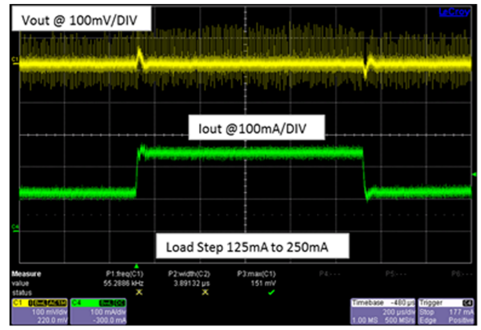


Figure 23. Buck Transient Response 36Vin

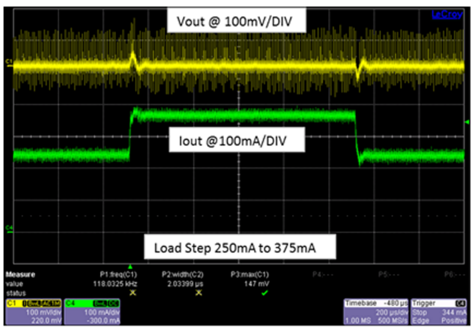


Figure 24. Buck Transient Response 36Vin

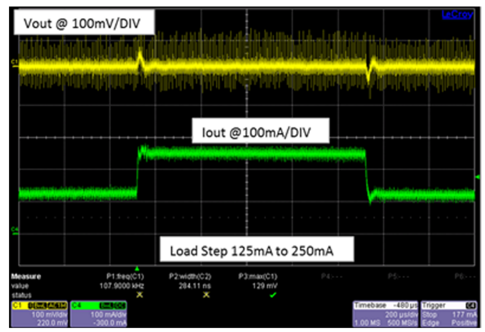


Figure 25. Buck Transient Response 48Vin

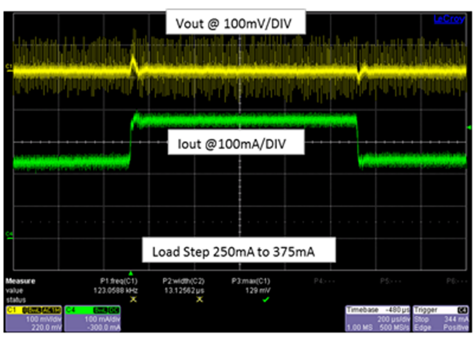


Figure 26. Buck Transient Response 48 Vin

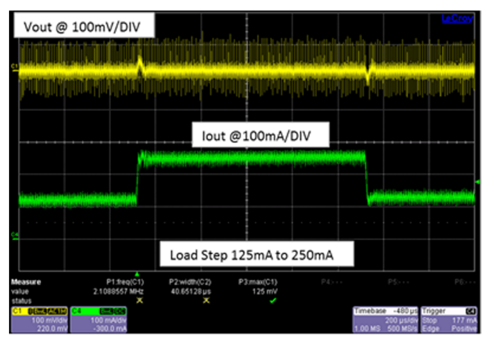


Figure 27. Buck Transient Response 72 Vin

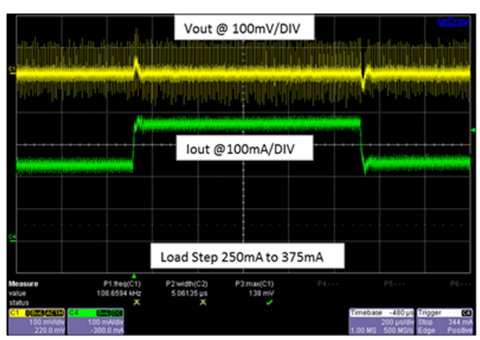


Figure 28. Buck Transient Response 72 Vin

Thermal Curves

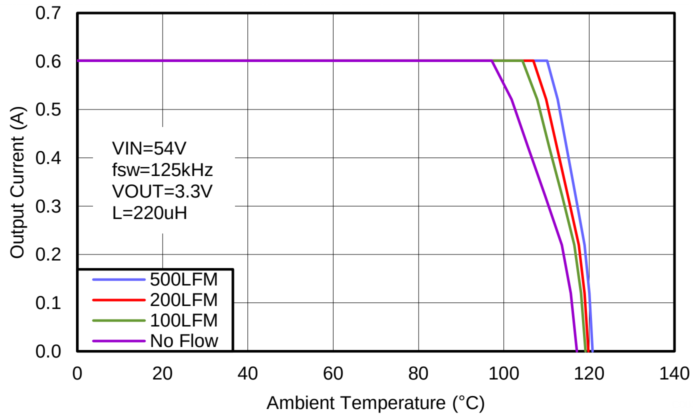


Figure 29. Thermal Derating Curve

REVISION HISTORY

Changes from Revision C (July 2013) to Revision D **Page**

- Added SW to RTN (100 ns transient) 3

Changes from Revision D (September 2013) to Revision E **Page**

- Changed formatting throughout document, to be TI compliant 1
- Changed minimum operating input voltage from 9V to 7.5V in "Features" 1
- Changed minimum operating input voltage from 9V to 7.5V in "Typical Application" 1
- Changed minimum operating input voltage from 9V to 7.5V in "Pin Descriptions" 2
- Added Absolute Maximum Junction Temperature 3
- Changed minimum operating input voltage from 9V to 7.5V in "Recommended Operating Ratings" 3

Changes from Revision E (December 2013) to Revision F **Page**

- Added Thermal Parameters because previous National datasheets did not have, in addition to recurring customer requests. 3
- Added Thermal Derating Curve 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM34927MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L34927	Samples
LM34927MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		L34927	Samples
LM34927SD/NOPB	ACTIVE	WSON	NGU	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L34927	Samples
LM34927SDX/NOPB	ACTIVE	WSON	NGU	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L34927	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

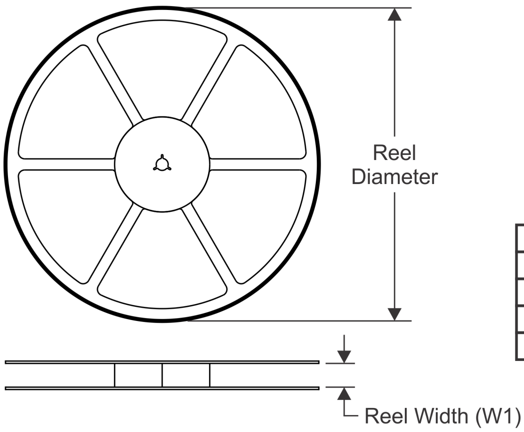
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

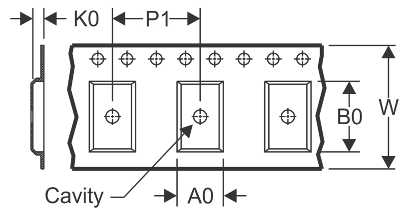
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

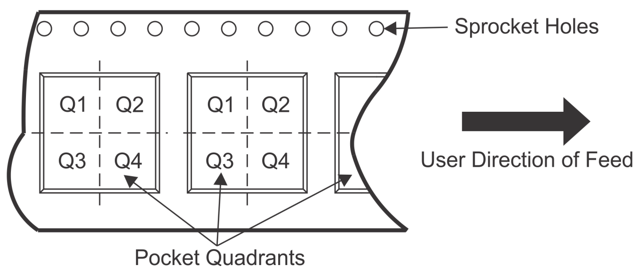


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

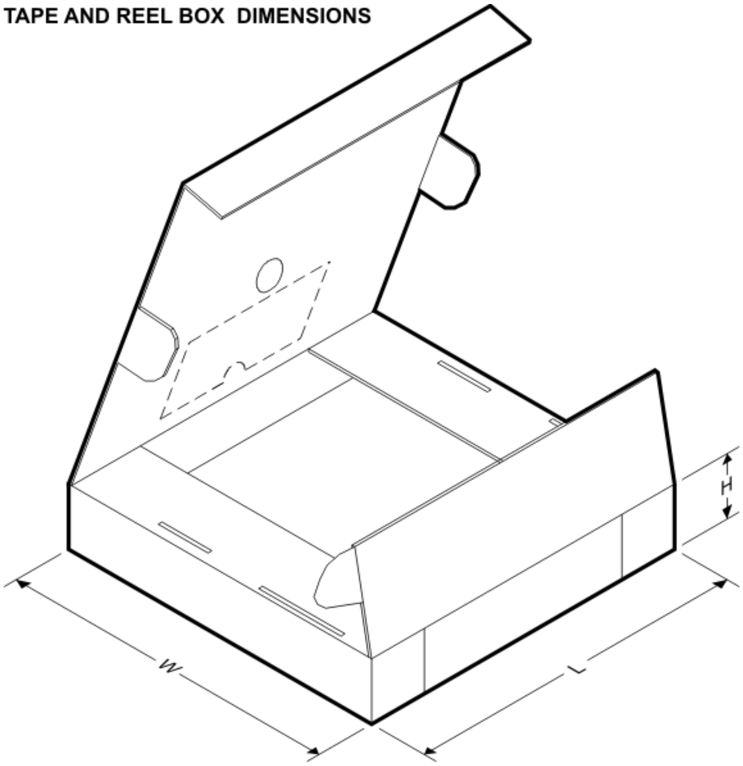
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM34927MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM34927SD/NOPB	WSON	NGU	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM34927SDX/NOPB	WSON	NGU	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

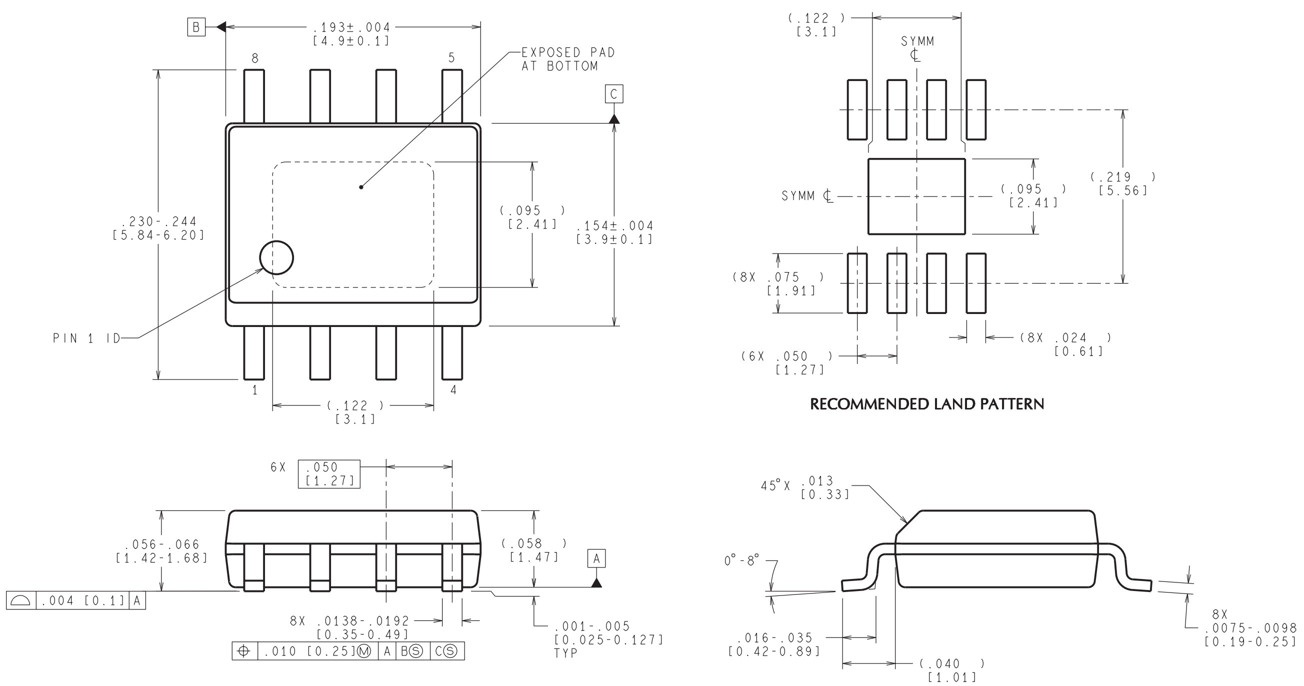
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM34927MRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LM34927SD/NOPB	WSON	NGU	8	1000	210.0	185.0	35.0
LM34927SDX/NOPB	WSON	NGU	8	4500	367.0	367.0	35.0

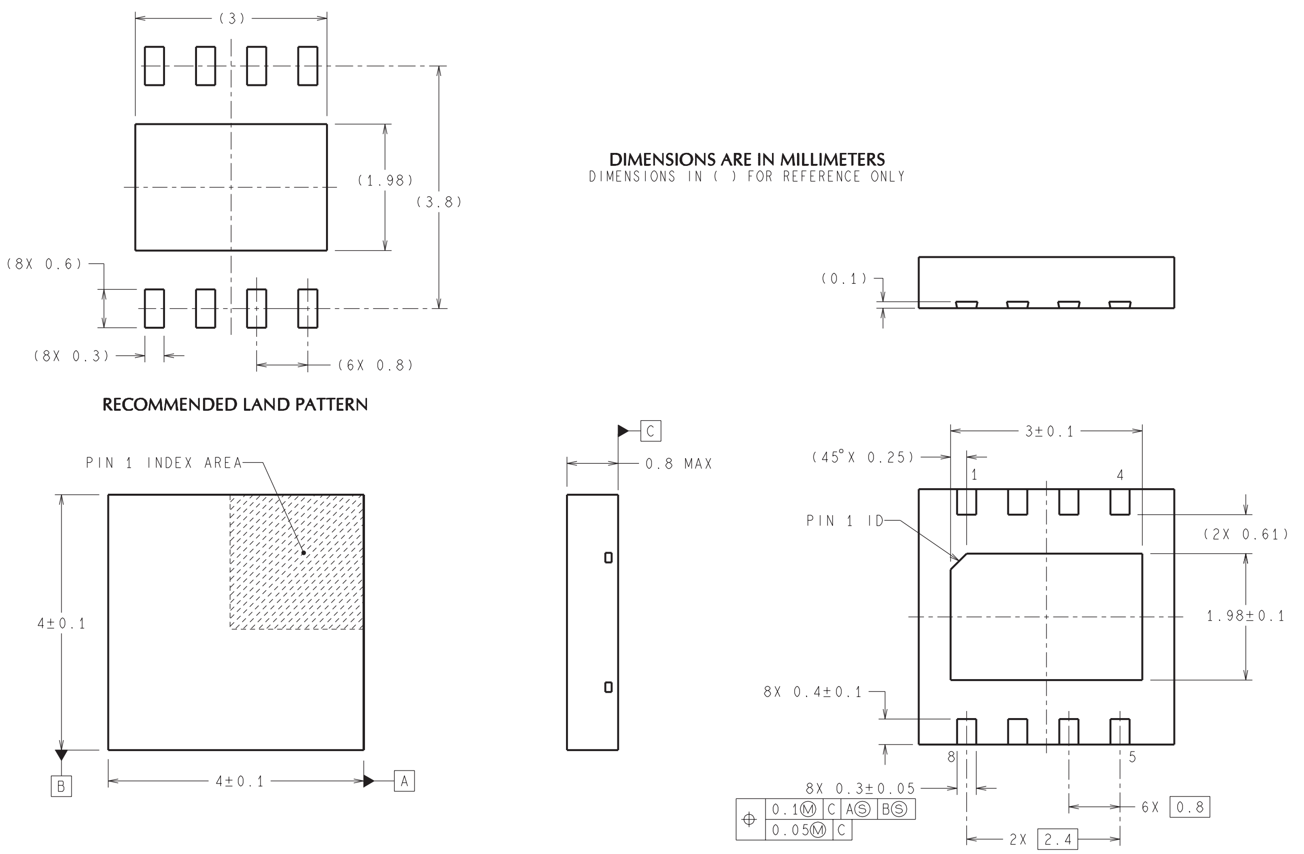
DDA0008B



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MRA08B (Rev B)

NGU0008B



SDC08B (Rev A)

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265