

## Low power dual voltage comparators

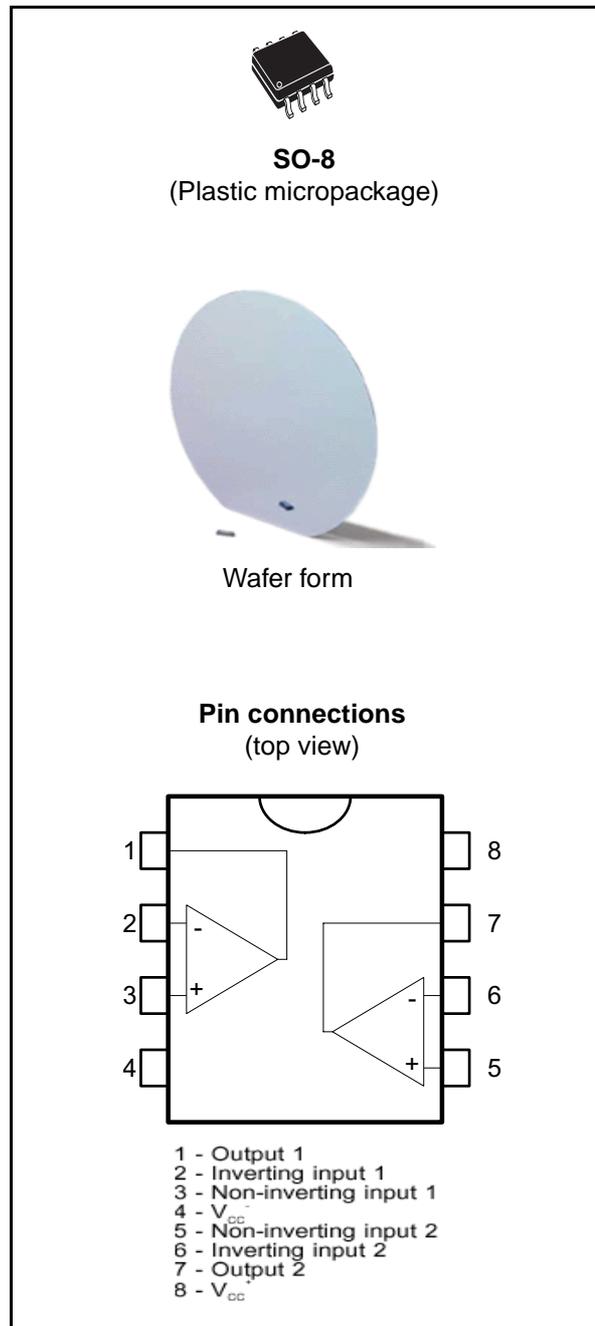
### Features

- Wide single supply voltage range or dual supplies +2 V to +36 V or  $\pm 1$  V to  $\pm 18$  V
- Very low supply current (0.4 mA) independent of supply voltage (1 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current:  $\pm 5$  nA typ.
- Input common-mode voltage range includes ground
- Low output saturation voltage: 250 mV typ. ( $I_O = 4$  mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs

### Description

This device consists of two independent low power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes ground even though operated from a single power supply voltage.



# 1 Absolute maximum ratings and operating conditions

**Table 1. Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	$\pm 18$ or 36	V
$V_{id}$	Differential input voltage	$\pm 36$	V
$V_{in}$	Input voltage	-0.3 to +36	V
	Output short-circuit to ground <sup>(1)</sup>	20	mA
$R_{thja}$	Thermal resistance junction to ambient <sup>(2)</sup> (SO-8)	125	°C/W
$R_{thjc}$	Thermal resistance junction to case <sup>(2)</sup> (SO-8)	40	°C/W
$T_j$	Maximum junction temperature	150	°C
ESD	HBM: human body model <sup>(3)</sup>	800	V
	MM: machine model <sup>(4)</sup>	200	
	CDM: charged device model <sup>(5)</sup>	1500	
$T_{stg}$	Storage temperature range	-65 to +150	°C

- Short-circuit from the output to  $V_{CC}^+$  can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA, independent of the magnitude of  $V_{CC}^+$ .
- Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
- Human body model: A 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- Machine model: A 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
- Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
$V_{CC}^+$	Supply voltage	2 to 36	V
$T_{oper}$	Operating free-air temperature range	-40 to +150	°C
$V_{icm}$	Input common mode voltage range( $V_{CC}=30V$ ) <sup>(1)</sup> $T_{amb} = +25^{\circ}C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 to $V_{CC}^+ - 1.5$ 0 to $V_{CC}^+ - 2$	V

- The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is  $V_{CC}^+ - 1.5$  V, but either or both inputs can go to +30 V without damage.

## 2 Circuit schematics

Figure 1. Schematic diagram (1/2 LM2903)

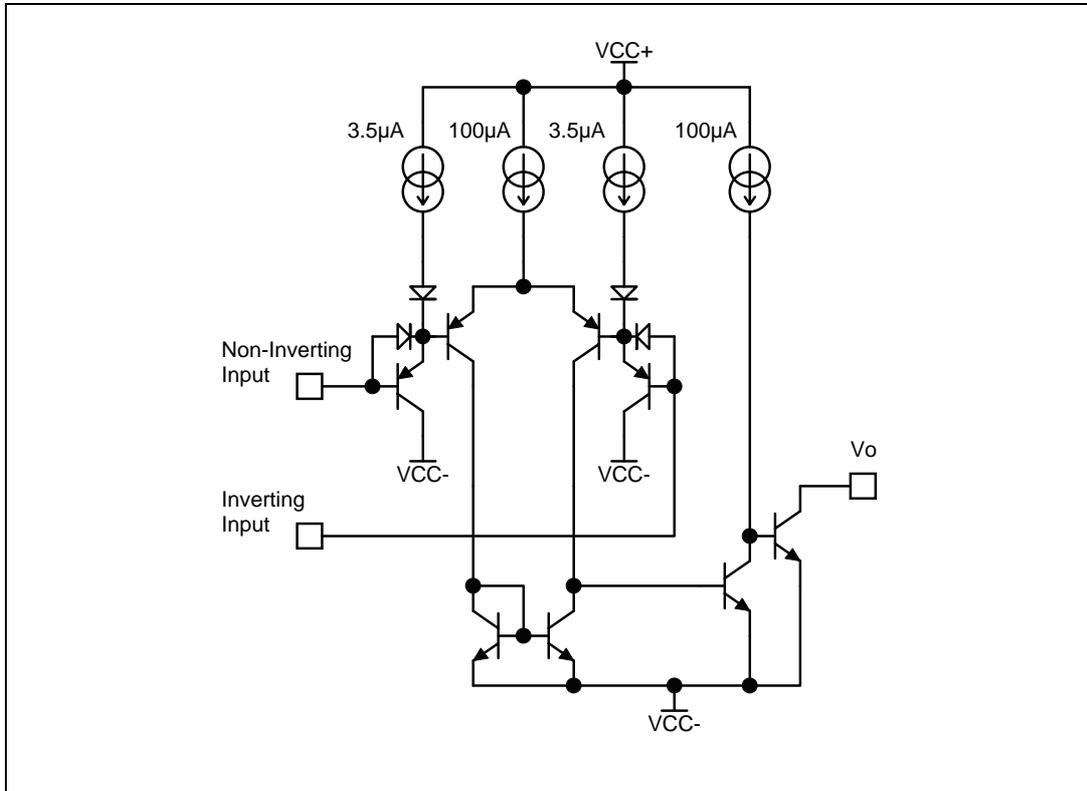
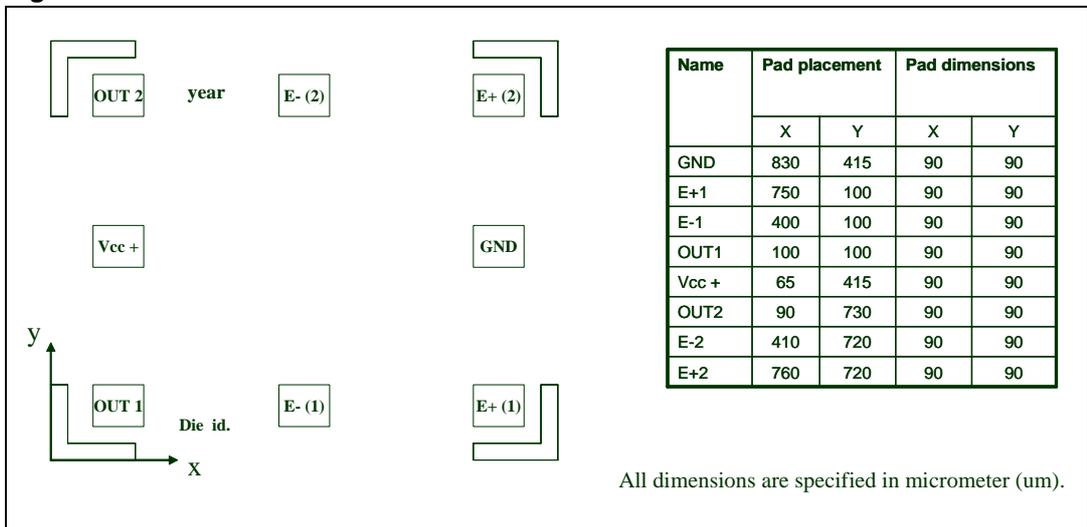


Figure 2. Pad locations



### 3 Electrical characteristics

Table 3.  $V_{CC}^+ = 5V$ ,  $V_{CC}^- = GND$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage <sup>(1)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		1	7 15	mV
$I_{io}$	Input offset current $T_{min} \leq T_{amb} \leq T_{max}$		5	50 150	nA
$I_{ib}$	Input bias current <sup>(2)</sup> $T_{min} \leq T_{amb} \leq T_{max}$		25	250 400	nA
$A_{VD}$	Large signal voltage gain ( $V_{CC}^+ = 15V, R_L = 15k\Omega, V_o = 1$ to $11V$ )	25	200		V/mV
$I_{CC}$	Supply current (all comparators) $V_{CC}^+ = 5V$ , no load $V_{CC}^+ = 30V$ , no load		0.4 1	1 2.5	mA
$V_{id}$	Differential input voltage <sup>(3)</sup>			$V_{CC}^+$	V
$V_{OL}$	Low level output voltage ( $V_{id} = -1V, I_{sink} = 4mA$ ) $T_{min} \leq T_{amb} \leq T_{max}$		250	400 800	mV
$I_{OH}$	High level output current ( $V_{CC}^+ = V_o = 30V, V_{id} = 1V$ ) $T_{min} \leq T_{amb} \leq T_{max}$		0.1	1	nA $\mu A$
$I_{sink}$	Output sink current ( $V_{id} = -1V, V_o = 1.5V$ ) $T_{min} \leq T_{amb} \leq T_{max}$	6 2	16		mA
$t_{re}$	Small signal response time <sup>(4)</sup> ( $R_L = 5.1k\Omega$ to $V_{CC}^+$ )		1.3		$\mu s$
$t_{rel}$	Large signal response time <sup>(5)</sup> TTL input ( $V_{ref} = +1.4V, R_L = 5.1k\Omega$ to $V_{CC}^+$ ) Output signal at 50% of final value Output signal at 95% of final value			500 1	ns $\mu s$

1. At output switch point,  $V_o \approx 1.4V$ ,  $R_S = 0\Omega$  with  $V_{CC}^+$  from 5V to 30V, and over the full input common-mode range (0V to  $V_{CC}^+ - 1.5V$ ).
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so there is no load charge on the reference of input lines.
3. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state.  
The low input voltage state must not be less than  $-0.3V$  (or  $0.3V$  below the negative power supply, if used)
4. The response time specified is for a 100mV input step with 5mV overdrive.
5. Maximum values are guaranteed by design and evaluation.

Figure 3. Supply current vs. supply voltage

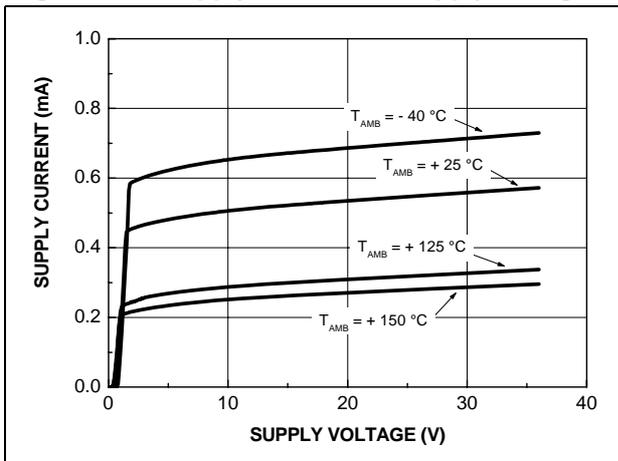


Figure 4. Input current vs. supply voltage

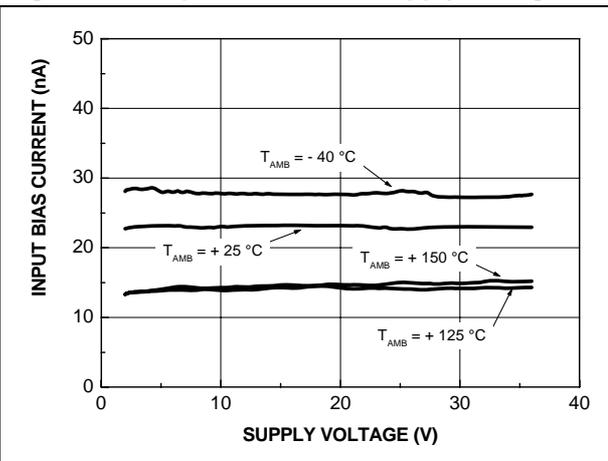


Figure 5. Output saturation voltage vs. output current ( $V_{CC}=5V$ )

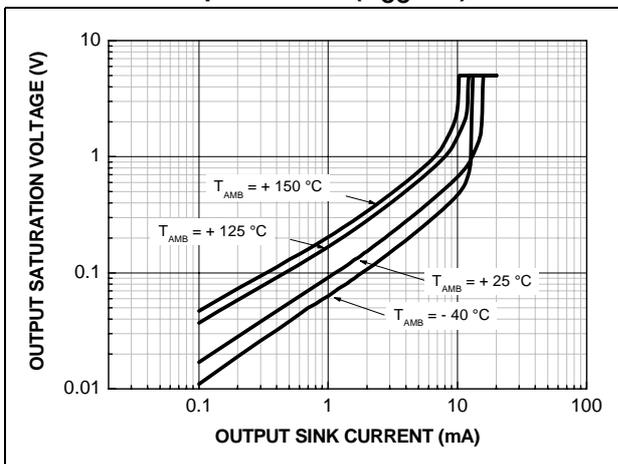


Figure 6. Response time for various input overdrives - negative transition

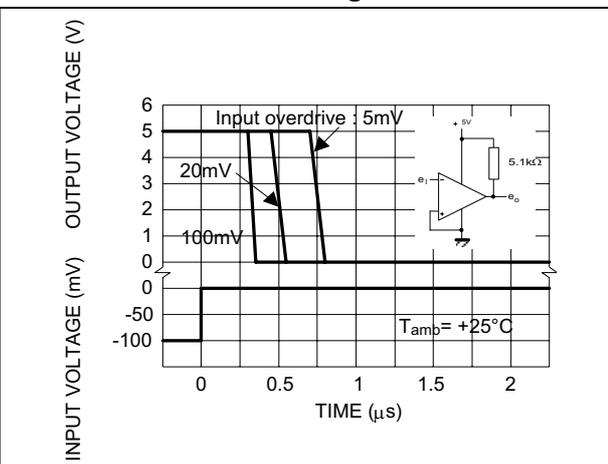
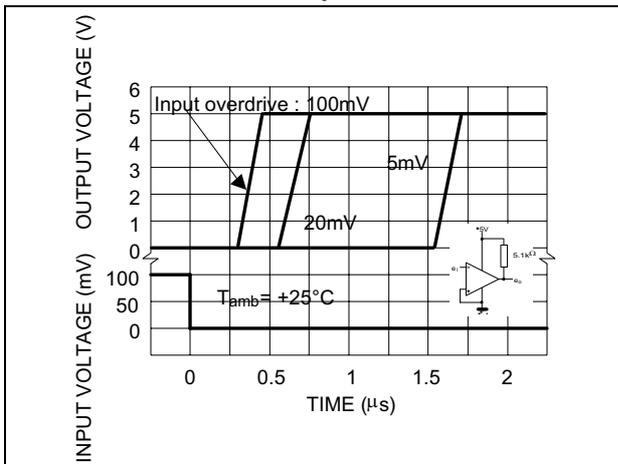


Figure 7. Response time for various input overdrives - positive transition



## 4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Figure 8. SO-8 package mechanical drawing

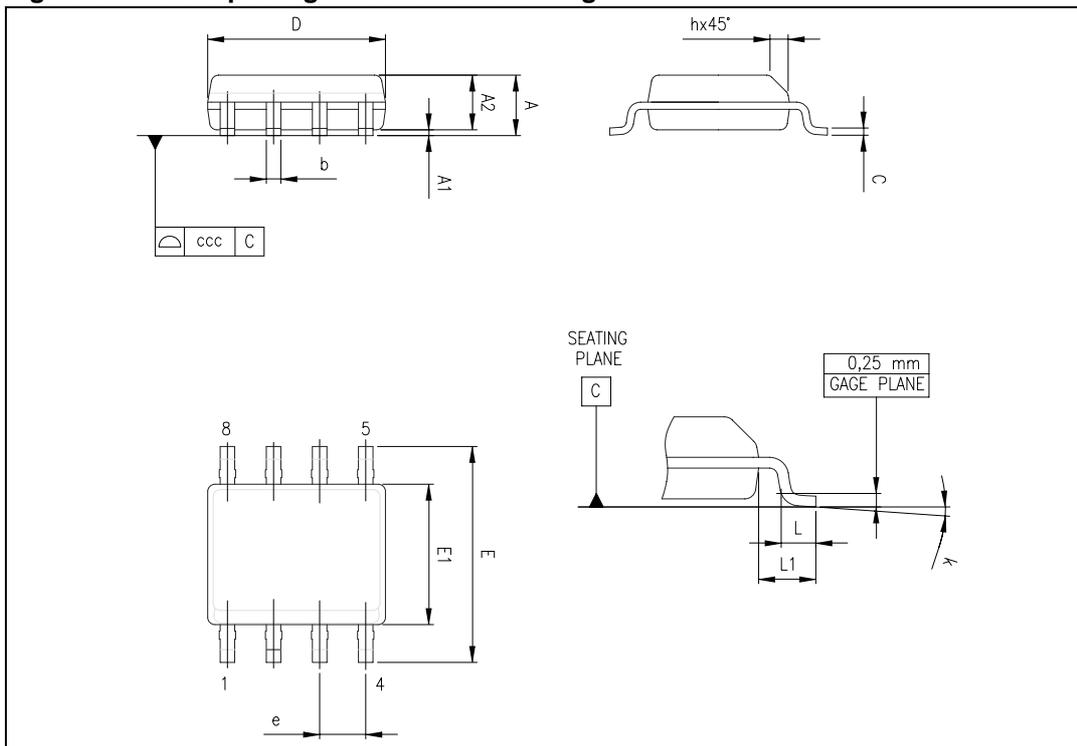


Table 4. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	1°		8°	1°		8°
ccc			0.10			0.004

## 5 Ordering information

**Table 5. Order codes**

Order code	Temperature range	Package	Packing	Marking
JLM2903H- E6D1	-40°C, +150°C	Wafer		
LM2903HD LM2903HDT		SO-8	Tube or Tape & reel	2903H
LM2903HYD <sup>(1)</sup> LM2903HYDT <sup>(1)</sup>		SO-8 (Automotive grade )	Tube or Tape & reel	2903HY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

## 6 Revision history

**Table 6. Document revision history**

Date	Revision	Changes
25-Sep-2003	1	Initial release.
23-Aug-2005	2	PPAP references inserted in the datasheet, see order codes table.
27-Mar-2008	3	Added ESD parameters in AMR table. Updated document format.



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