National Semiconductor

September 2, 2010

LM27402

High Performance Synchronous Buck Controller with DCR Current Sensing

General Description

The LM27402 is a synchronous voltage mode DC/DC buck controller with inductor DCR current sense capability. Sensing the inductor current eliminates the need to add resistive powertrain elements which increases overall efficiency and facilitates accurate continuous current limit sensing. A 0.6V ±1% voltage reference enables high accuracy and low voltage capability at the output. An input operating voltage range of 3V to 20V makes the LM27402 suitable for a large variety of input rails.

The LM27402 voltage mode control loop incorporates input voltage feed-forward to maintain stability throughout the entire input voltage range. The switching frequency is adjustable from 200 kHz to 1.2 MHz. Dual high current integrated N-channel MOSFET drivers support large Q_G, low $R_{DS(ON)}$ MOSFETs. A power good indicator provides power rail sequencing capability and output fault detection. Adjustable external soft-start capability limits inrush current and provides monotonic output control during startup. Other features include external tracking of other power supplies, integrated LDO bias supply, and synchronization capability. The LM27402 is offered in a 16 pin eTSSOP package and a 4 mm x 4 mm 16 pin exposed LLP.

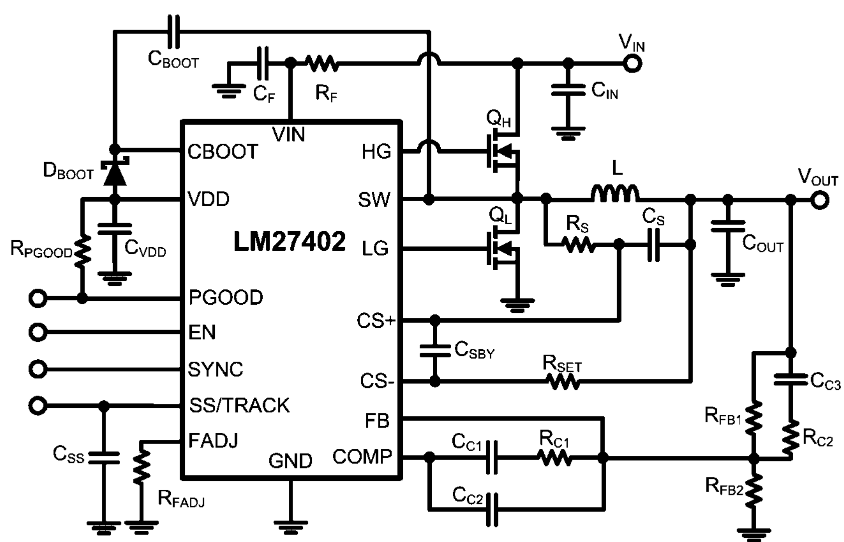
Features

- Input operating voltage range of 3V to 20V
- Continuous inductor DCR or shunt resistor current sensing
- 0.6V ±1% reference (-40°C to 125°C junction temperature)
- Output voltage as high as 95% of input voltage
- Integrated MOSFET drivers
- Internal LDO bias supply
- External clock synchronization
- Adjustable soft-start with external capacitor
- Pre-biased startup capability
- Power supply tracking
- Input voltage feed-forward
- Power good indicator
- Precision enable with hysteresis

Applications

- High current, low voltage FPGA/ASIC DC/DC converters
- General purpose high current buck converters
- Telecom, datacom, networking, distributed power architectures

Typical Application Circuit



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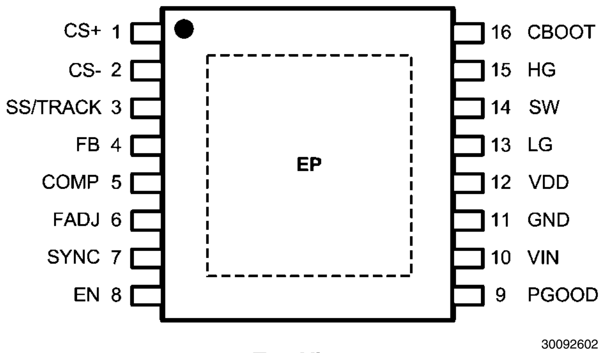
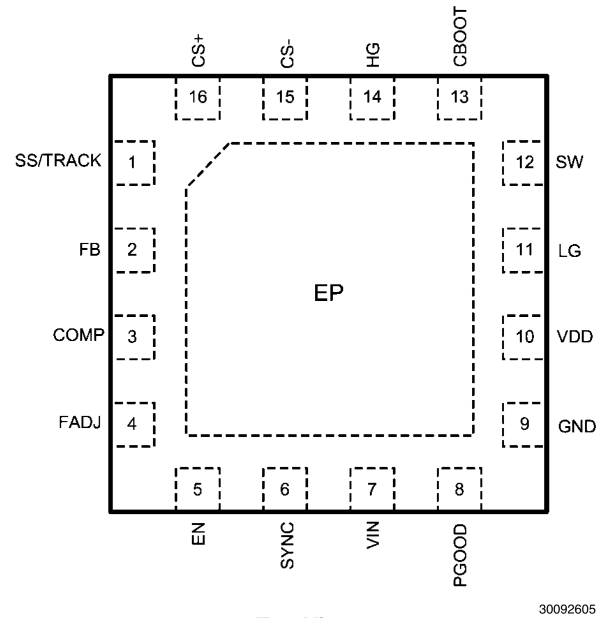
Connection Diagrams



Top View
eTSSOP-16 Package
4.4 mm x 5 mm x 0.9 mm
0.65 mm PITCH



Top View
LLP-16 Package
4 mm x 4 mm x 0.8 mm
0.65 mm PITCH

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM27402MH	eTSSOP-16	MXA16A	Coming Soon
LM27402MHX			Coming Soon

Order Number	Package Type	NSC Package Drawing	Supplied As
LM27402SQ	LLP-16	SQB16A	1000 Units per Tape and Reel
LM27402SQX			4500 Units per Tape and Reel

Pin Descriptions

eTSSOP Pin #	LLP Pin #	Name	Description
1	16	CS+	Non-inverting input to the current sense comparator.
2	15	CS-	Inverting input to the current sense comparator with +10 µA offset current for adjustable current limit setpoint.
3	1	SS/TRACK	Soft-start or tracking input. A startup rate can be defined with the use of an external soft-start capacitor from SS/TRACK to GND. A +3 µA current source charges the soft-start capacitor to set the output voltage rise time during startup. SS/TRACK can also be controlled with an external voltage source for tracking. SS/TRACK should not exceed the voltage on VDD.
4	2	FB	Inverting input to the error amplifier to set the output voltage and compensate the voltage mode control loop.
5	3	COMP	Output of the internal error amplifier. The COMP voltage is compared to an internally generated ramp of the PWM comparator to establish the duty cycle command.
6	4	FADJ	Frequency adjust pin. The switching frequency can be set to a predetermined rate by connecting a resistor between FADJ and GND.
7	6	SYNC	Frequency synchronization pin. An external clock signal can be applied to SYNC to set the switching frequency. The SYNC frequency must be greater than the frequency set by the FADJ pin. If the signal is not present, the switching frequency will decrease to the frequency set by the FADJ resistor. SYNC should not exceed the voltage on VDD and should be grounded if not used.
8	5	EN	LM27402 enable pin. Apply a voltage typically higher than 1.17V to EN and the LM27402 will begin to switch if VIN and VDD have exceeded the UVLO voltage. A hysteresis of 100 mV on EN provides noise immunity. EN is internally tied to VDD through a 2 µA pullup current source. EN should not exceed the voltage on VDD.
9	8	PGOOD	Power good output flag. PGOOD is connected to the drain of a pulldown FET. The PGOOD pin is typically connected to VDD through a pull-up resistor.
10	7	VIN	Input supply rail. The VIN operating range is 3V to 20V and is connected to the input rail through an RC filter.
11	9	GND	Common ground.
12	10	VDD	Internal sub-regulated 4.5V bias supply. VDD is used to supply the voltage on CBOOT to facilitate high-side FET switching. Connect a 1 µF ceramic capacitor from VDD to GND as close as possible to the LM27402. VDD cannot be connected to a separate voltage rail. However, VDD can be connected to VIN to provide increased gate drive only if $V_{IN} \leq 5.5V$. A 1Ω, 1 µF input filter can be used for increased noise rejection.
13	11	LG	Low-side N-FET gate drive.
14	12	SW	Switch-node connection and return path for the high-side gate driver.
15	14	HG	High-side N-FET gate drive.
16	13	CBOOT	High-side gate driver supply rail. Connect a ceramic capacitor from CBOOT to SW and a Schottky diode from VDD to CBOOT.
EP	EP	EP	Exposed Pad. The EP must be connected to GND but cannot be used as the primary ground connection. Use multiple vias under this pad for optimal thermal performance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Unless otherwise specified, voltages are from the indicated pins to GND.

VIN, CS+, CS-, SW	-0.3V to +22V
VDD, PGOOD	-0.3V to +6V
EN, SYNC, SS/TRACK, FADJ, COMP, FB, LG	-0.3V to VDD
CBOOT	-0.3V to +24V
CBOOT to SW	+6V
CS+ to CS-	-2V to +2V
Storage Temperature	-65°C to 150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
Minimum ESD Rating (Note 2)	±2kV

Operating Ratings (Note 1)

Input Voltage Range (Note 3)

VIN	+3.0V to +20V
VIN (VDD = VIN)	+3.0V to +5.5V
VDD to GND	+2.2V to +5.5V
SS/TRACK, SYNC, EN	0V to V_{VDD}
PGOOD	0V to +5.5V
Junction Temperature	-40°C to + 125°C
θ_{JA} (LLP-16) (Note 4)	40°C/W
θ_{JA} (eTSSOP-16) (Note 4)	40°C/W

Electrical Characteristics

Unless otherwise stated, the following conditions apply: V_{IN} = 12V. Limits in standard type are for T_J = 25°C only, limits in **bold face type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

System Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OPERATIONAL SPECIFICATIONS						
I_Q	Quiescent Current	V_{FB} = 0.6V (not switching)		4.5	**6.0**	mA
I_{QSD}	Quiescent Current In Shutdown	V_{EN} = 0V		25	**45**	µA
UVLO						
UVLO	Input Under Voltage Lockout	V_{VIN} Rising, V_{VDD} Rising	**2.7**	2.9	**2.99**	V
$UVLO_{HYS}$	UVLO Hysteresis	V_{VIN} Falling, V_{VDD} Falling		300		mV
REFERENCE						
V_{FB}	Feedback Voltage		**0.594**	0.600	**0.606**	V
I_{FB}	Feedback Pin Bias Current	V_{FB} = 0.65V	-50	0	50	nA
SWITCHING						
F_{SW}	Switching Frequency	R_{FADJ} = 4.12 kΩ	**950**	1150	**1350**	kHz
F_{SW}	Switching Frequency	R_{FADJ} = 20 kΩ	**400**	500	**600**	kHz
F_{SW}	Switching Frequency	R_{FADJ} = 95.3 kΩ	**175**	214	**265**	kHz
D_{MAX}	Maximum Duty Cycle	F_{SW} = 300 kHz	**93**	95		%
T_{OFF_MIN}	Minimum Off Time	V_{FB} = 0.5V	**125**	165	**205**	ns
VDD SUB-REGULATOR						
V_{DD}	Sub-Regulator Output Voltage	I_{DD} = 25 mA	**4.0**	4.5	**5.0**	V
ERROR AMPLIFIER						
B_{W-3db}	Open Loop Bandwidth			2		MHz
A_{VOL}	Error Amp DC Gain			50		dB
V_{SLEW_RISE}	Error Amplifier Rising Slew Rate	V_{FB} = 0.5V		5		V/µs
V_{SLEW_FALL}	Error Amplifier Falling Slew Rate	V_{FB} = 0.7V		3		V/µs
I_{SOURCE}	COMP Source Current	V_{FB} = 0.5V	8	12		mA
I_{SINK}	COMP Sink Current	V_{FB} = 0.7V	4	12		mA
V_{COMP_MAX}	Max COMP Voltage	V_{FB} = 0.5V		3.1		V
V_{COMP_MIN}	Min COMP Voltage	V_{FB} = 0.7V		0.5		V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OVER CURRENT						
V_{OFFSET}	Comparator Voltage Offset		**-5**	0	**5**	mV
I_{CS-}	Current Limit Offset Current	$V_{CS-} = 5V$	**9.5**	10.0	**10.5**	μA
GATE DRIVE						
R_{DSON1}	High-Side FET Driver Pull-Up On Resistance	$V_{CBOOT} - V_{SW} = 4.7V$, $I_{HG} = +100$ mA		1.7		Ω
R_{DSON2}	High-Side FET Driver Pull-Down On Resistance	$V_{CBOOT} - V_{SW} = 4.7V$, $I_{HG} = -100$ mA		1.2		Ω
R_{DSON3}	Low-Side FET Driver Pull-Up On Resistance	$V_{VDD} = 4.7V$, $I_{LG} = +100$ mA		1.7		Ω
R_{DSON4}	Low-Side FET Driver Pull-Down On Resistance	$V_{VDD} = 4.7V$, $I_{LG} = -100$ mA		1.0		Ω
T_{DT}	Deadtime Timeout	$F_{SW} = 500$ kHz		40		ns
SOFT-START						
I_{SS}	Soft-Start Source Current	$V_{SS/TRACK} = 0V$	**2**	3	**4**	μA
R_{SS_PD}	Soft-Start Pull-Down Resistance	$V_{SS/TRACK} = 0.6V$		288		Ω
T_{SS_INT}	Internal Soft-Start Time			1.28		ms
POWERGOOD						
I_{PGS}	PGOOD Low Sink Current	$V_{PGOOD} = 0.2V$, $V_{FB} = 0.75V$	**60**	100		μA
I_{PGL}	PGOOD Leakage Current	$V_{PGOOD} = 5V$		1	10	μA
O_{VT}	Over-Voltage Threshold	V_{FB} Rising	**114**	117	**120**	%
O_{VT_HYS}	O_{VT} Hysteresis	V_{FB} Falling		2		%
U_{VT}	Under-Voltage Threshold	V_{FB} Rising	**91**	94	**97**	%
U_{VT_HYS}	U_{VT} Hysteresis	V_{FB} Falling		3		%
$T_{DEGLITCH}$	Deglitch Time	V_{PGOOD} Rising and Falling		20		μs
ENABLE						
V_{EN}	Enable Logic High Threshold	V_{EN} Rising	**1.10**	1.17	**1.24**	V
V_{EN_HYS}	Enable Hysteresis	V_{EN} Falling		100		mV
I_{EN}	Enable Pin Pull-Up Current	$V_{EN} = 0V$		2		μA
FREQUENCY SYNCHRONIZATION						
V_{LH_SYNC}	SYNC Pin Logic High	$V_{VDD} = 4.7V$	**2.0**			V
V_{LL_SYNC}	SYNC Pin Logic Low	$V_{VDD} = 4.7V$			**0.8**	V
$SYNC_{FSW\_L}$	Minimum Clock Sync Frequency		**200**			kHz
$SYNC_{FSW\_H}$	Maximum Clock Sync Frequency				**1200**	kHz
THERMAL SHUTDOWN						
T_{SHD}	Thermal Shutdown	Temperature Rising		165		°C
T_{SHD_HYS}	Thermal Shutdown Hysteresis	Temperature Falling		15		°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor to each pin.

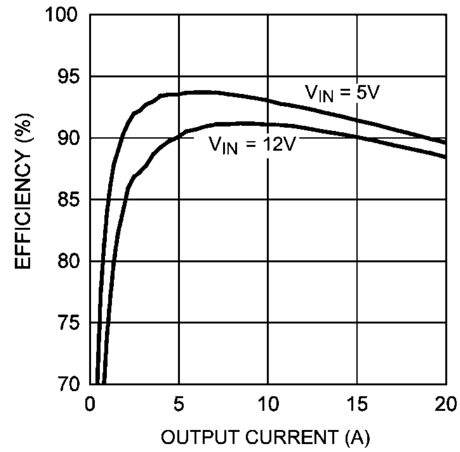
Note 3: VDD is the output of an internal linear regulator. Under normal operating conditions where VIN is greater than 5.5V, VDD must not be connected to any external voltage source. In an application where VIN is between 3.0V and 5.5V, it is recommended to connect VDD to VIN. In order to have better noise rejection under these conditions, a 1Ω and 1μF RC input filter may be used.

Note 4: Tested on a four layer JEDEC board. Four vias are provided under the LLP exposed pad and nine vias are provided under the eTSSOP exposed pad.

Typical Performance Characteristics

Unless otherwise stated, all data sheet curves were recorded using example circuit 1 at the end of this datasheet. V_{IN} = 12V.

Efficiency (Vout = 1.5V)



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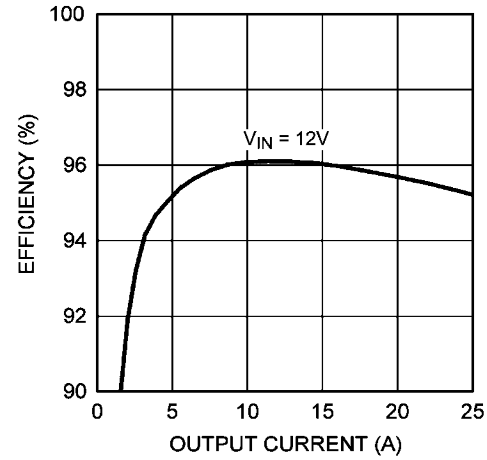
Efficiency (Vout = 5V, Example Circuit 2)



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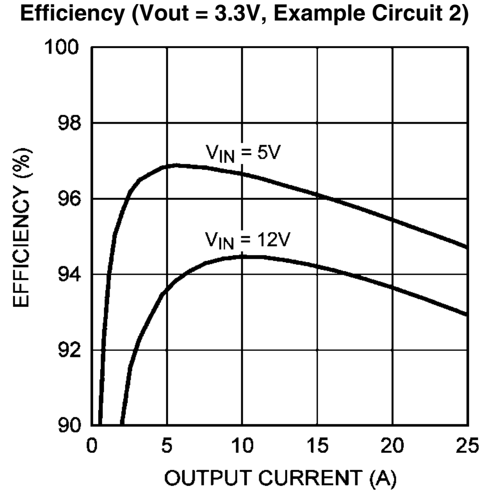
Efficiency (Vout = 3.3V, Example Circuit 2)



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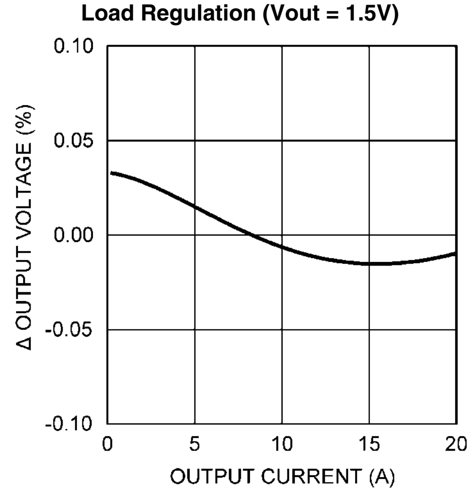
Load Regulation (Vout = 1.5V)



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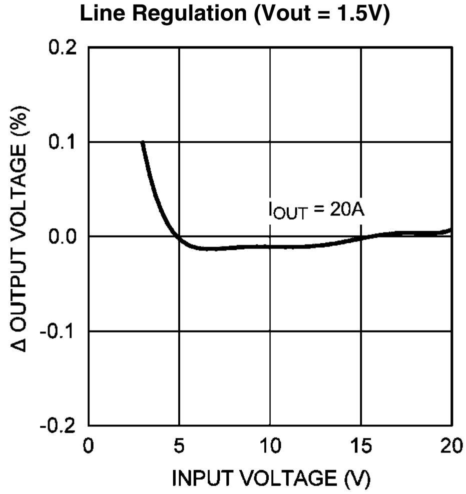
Line Regulation (Vout = 1.5V)



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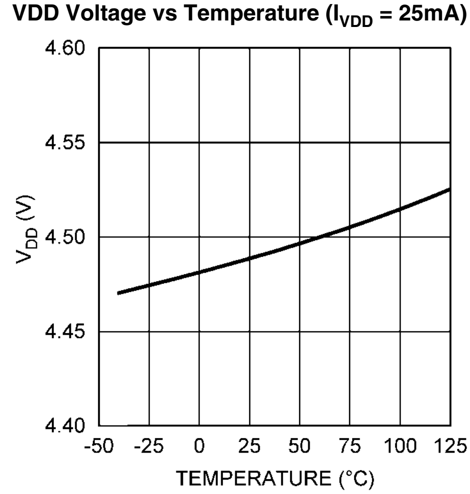
VDD Voltage vs Temperature (I_{VDD} = 25mA)



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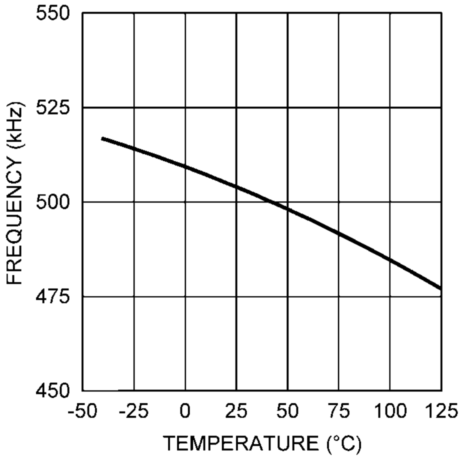
Frequency vs Temperature (R_{FADJ} = 20kΩ)



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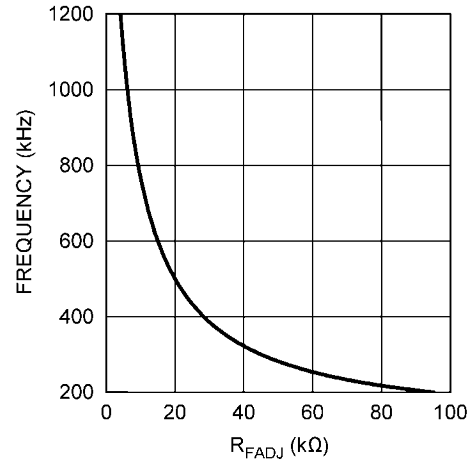
Frequency vs R_{FADJ}



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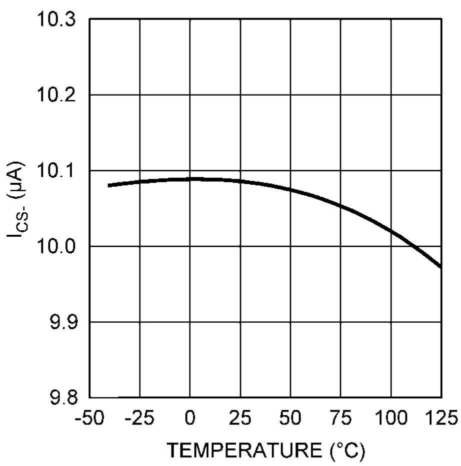
CS- Current Source vs Temperature



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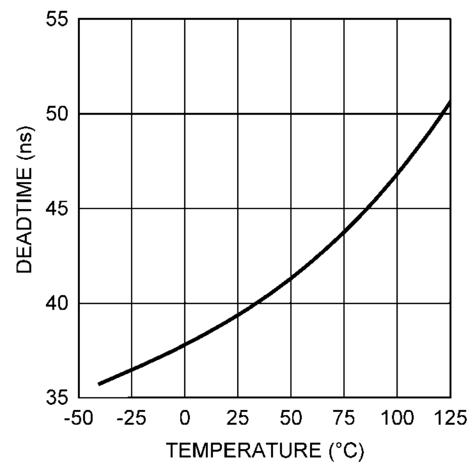
Deadtime vs Temperature



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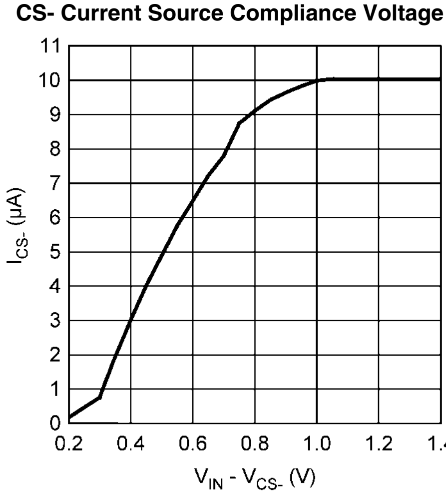
CS- Current Source Compliance Voltage



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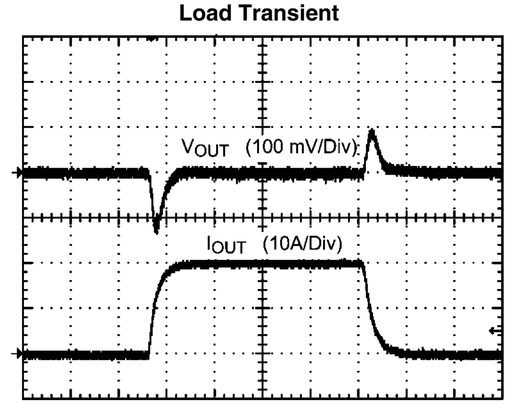
Load Transient



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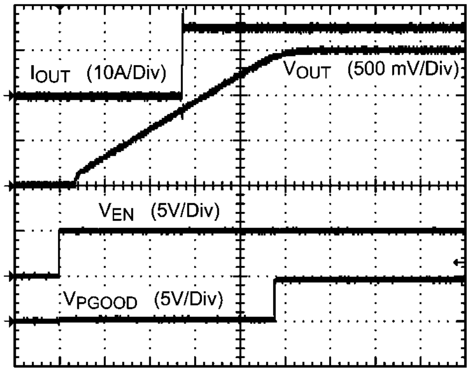
100 µs/DIV

Startup Waveforms



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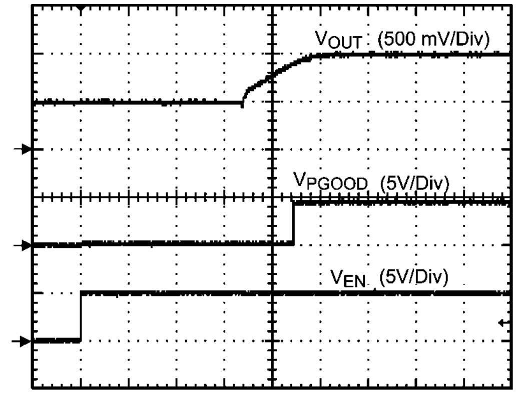
2 ms/DIV

Pre-Bias Startup Waveforms



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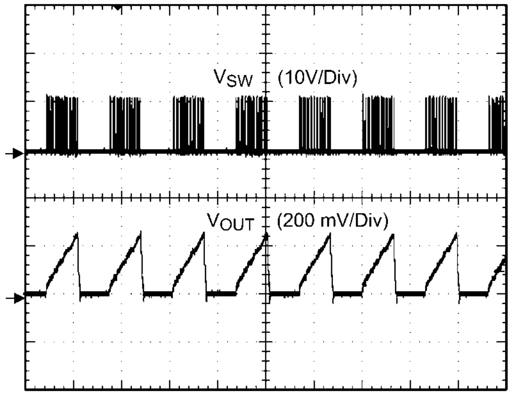
2 ms/DIV

OCP Hiccup



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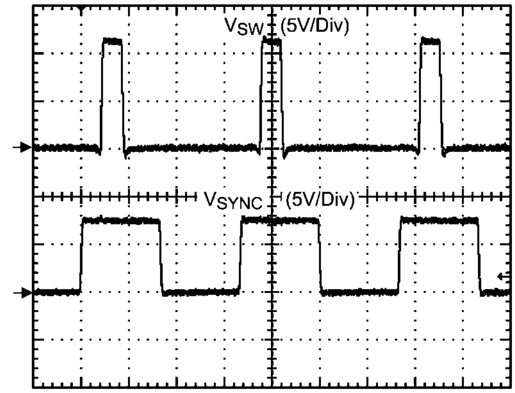
2 ms/DIV

Sync



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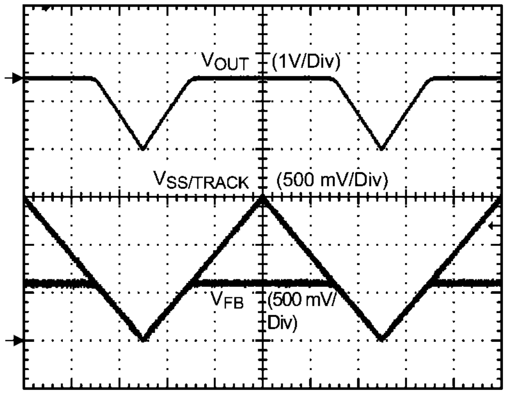
400 ns/DIV

Tracking



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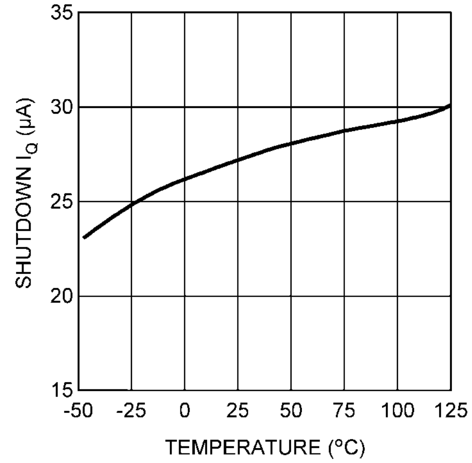
2 ms/DIV

Shutdown Quiescent Current vs Temperature



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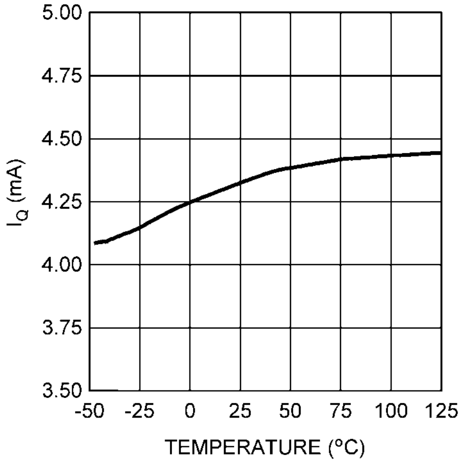
Quiescent Current vs Temperature



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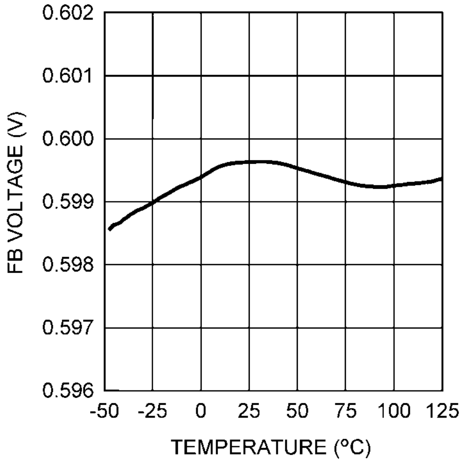
Feedback Voltage vs Temperature



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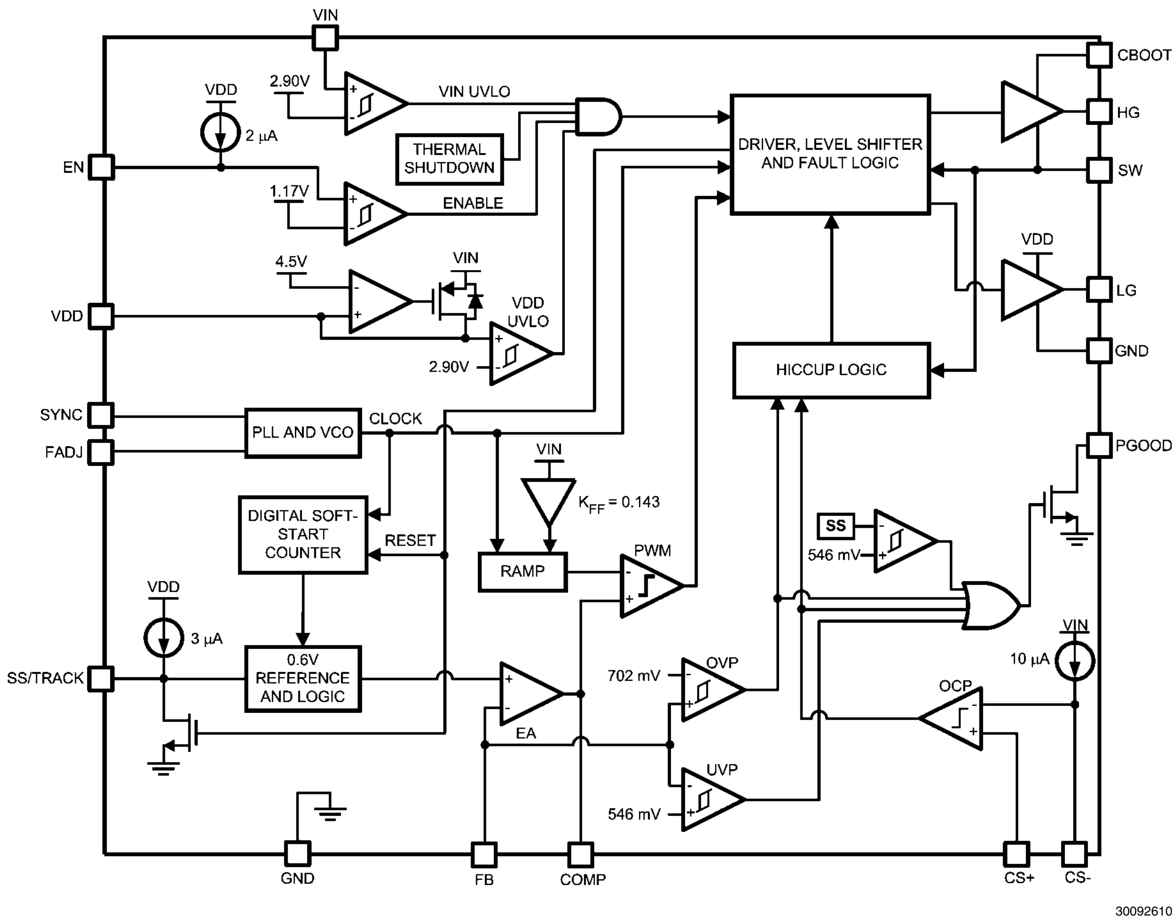
Block Diagram



Theory of Operation

GENERAL INFORMATION

The LM27402 is a single-phase synchronous voltage mode DC/DC buck controller. The inductor DCR sense capability and integrated low impedance gate drivers allow the LM27402 to be used in high current, high power density applications. Multiple fault conditions are supported including over-voltage, under-voltage, over-temperature, and over-current. The switching frequency can be adjusted over a wide range either by connecting a clock signal to SYNC pin or a resistor from FADJ to GND. The LM27402 supports pre-biased outputs while maintaining synchronous mode operation. Input voltage feed-forward is incorporated into the control loop to mitigate the effects of input voltage variation.

UVLO

An under-voltage lockout is built into the LM27402 which allows the device to only switch if the input voltage (VIN) and the internal sub-regulated voltage (VDD) both exceed 2.9V. A 300mV UVLO hysteresis exists on both VDD and VIN to prevent power on and off anomalies related to input voltage deviations.

PRECISION ENABLE (EN)

The enable pin of the LM27402 allows the output to be toggled on and off and is a precision analog input. When the EN voltage exceeds 1.17V, the controller will initiate the soft-start sequence as long as the input voltage and sub-regulated voltage have exceeded their UVLO thresholds of 2.9V. The EN pin has an absolute maximum voltage rating of 6.0V and should not exceed the voltage on VDD. There is an internal 2 µA pull-up current source connected to the EN pin. If EN is open, the LM27402 will turn on automatically if VIN and VDD exceed 2.9V. If the EN voltage is held below 0.8V, the LM27402 enters a deep shutdown state where the internal bias circuitry is off. The quiescent current is approximately 35 µA in deep shutdown. The EN pin has 100mV of hysteresis to reject noise and allow the pin to be resistively coupled to the input voltage or sequenced with other rails.

SOFT-START AND VOLTAGE TRACKING (SS/TRACK)

When the enable pin has exceeded 1.17V and both VIN and VDD have exceeded their UVLO thresholds, the LM27402 will begin charging the output linearly to the voltage level dictated by the feedback resistor network. The soft-start time is set by connecting a capacitor from SS/TRACK to GND. After EN exceeds 1.17V, an internal 3 µA current source begins to linearly charge the soft-start capacitor. Soft-start allows the user to limit inrush currents related to high output capacitance and output slew rate. If a soft-start capacitor is not used, the LM27402 defaults to a 1.28 ms digitally controlled startup time. The SS/TRACK pin can also be used to ratiometrically or coincidentally track an external voltage source. See the SETTING THE SOFT-START TIME and TRACKING sections of the design guide for more information.

PRE-BIAS STARTUP

In certain applications, the output may acquire a pre-bias voltage before the LM27402 is powered on or enabled. Pre-biased conditions are managed by preventing switching until the soft-start (SS/TRACK) voltage exceeds the feedback (FB) voltage. Once $V_{SS/TRACK}$ has exceeded V_{FB}, the LM27402 will begin to switch synchronously and regulate the output voltage.

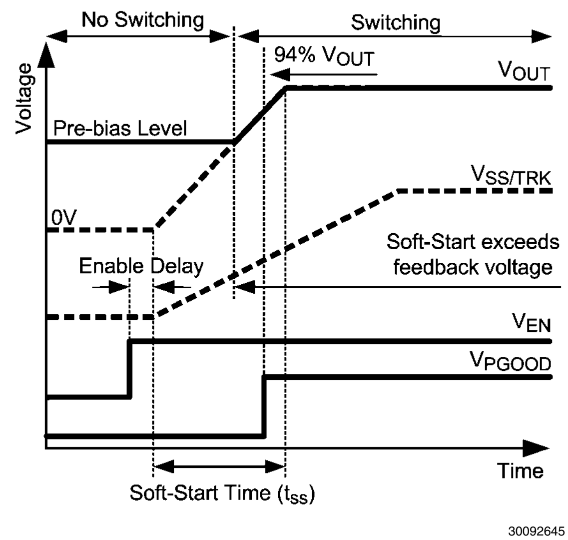


FIGURE 1. Pre-Bias Startup

Prohibiting switching during a pre-biased startup condition prevents the output from forcing parasitic paths to conduct excessive current. The LM27402 will not switch if the output is pre-biased to a voltage higher than the nominally set output voltage.

CURRENT LIMIT

The LM27402 may enter two states when a current limit event is detected. If a current limit condition has occurred, the high-side FET is immediately turned off until the next switching cycle. This is considered the first current limit state and provides an immediate response to any current limit event. During the first state, an internal counter will begin to record the number of over-current events. The counter is reset if 32 consecutive switching cycles occur with no current limit events detected. If five over-current events are detected within 32 switching cycles, the LM27402 then enters into a hiccup mode state. During hiccup mode, the LM27402 will shutdown for 1.28 ms and then attempt to restart again. When transitioning into hiccup mode, the high-side FET is turned off and the low-side FET is turned on. As the inductor current reaches zero subsequent to the over-current event, the low-side FET is turned off and the switch-node becomes high impedance to prepare for the next startup sequence. The soft-start capacitor is discharged through an internal pull-down FET to reinitialize the startup sequence. To illustrate how the LM27402 behaves during current limit faults, an over-current scenario is illustrated in *Figure 2*.

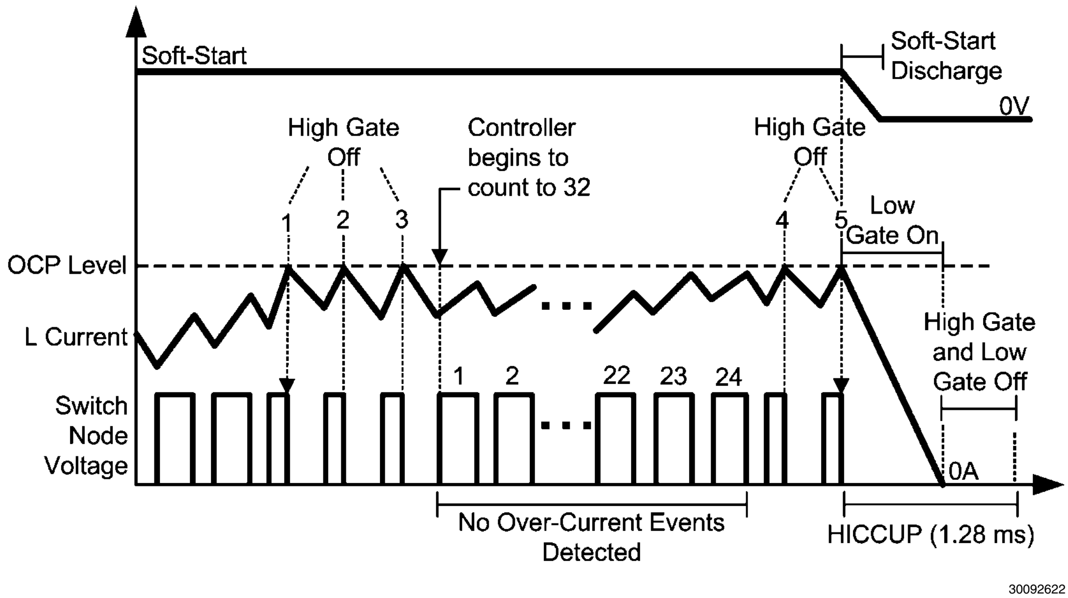


FIGURE 2. Current Limit Timing Diagram

In the example shown in *Figure 2*, the LM27402 immediately turns off the high-side FET when an over-current pulse is detected. After the third over-current event is detected, 24 switching cycles occur before the fourth over-current pulse is detected. Since the current limit logic does not count 32 switching cycles between two over-current events, the internal current limit counter is not reset and continues counting until the LM27402 enters hiccup mode. The soft-start capacitor is then discharged to initialize startup and a wait period of 1.28 ms occurs.

NEGATIVE CURRENT LIMIT

To prevent excess negative current, the LM27402 implements a negative current limit through the low-side FET. Negative current limit is only enabled when an over-voltage event is detected. Should an over-voltage fault occur, the low-side FET will turn off if the SW pin voltage exceeds a positive 100mV during the low-side on time, thereby protecting the powertrain from excessive negative current.

POWER GOOD

The PGOOD pin of the LM27402 is used to signal when the output is out of regulation or during non-regulated pre-biased conditions. This means that current limit, UVLO, over-voltage threshold, under-voltage threshold, or a non regulated output will cause the PGOOD pin to pull low. To prevent glitches to PGOOD, a 20 μs de-glitch filter is built into the LM27402. *Figure 3* illustrates when the PGOOD flag is asserted low.

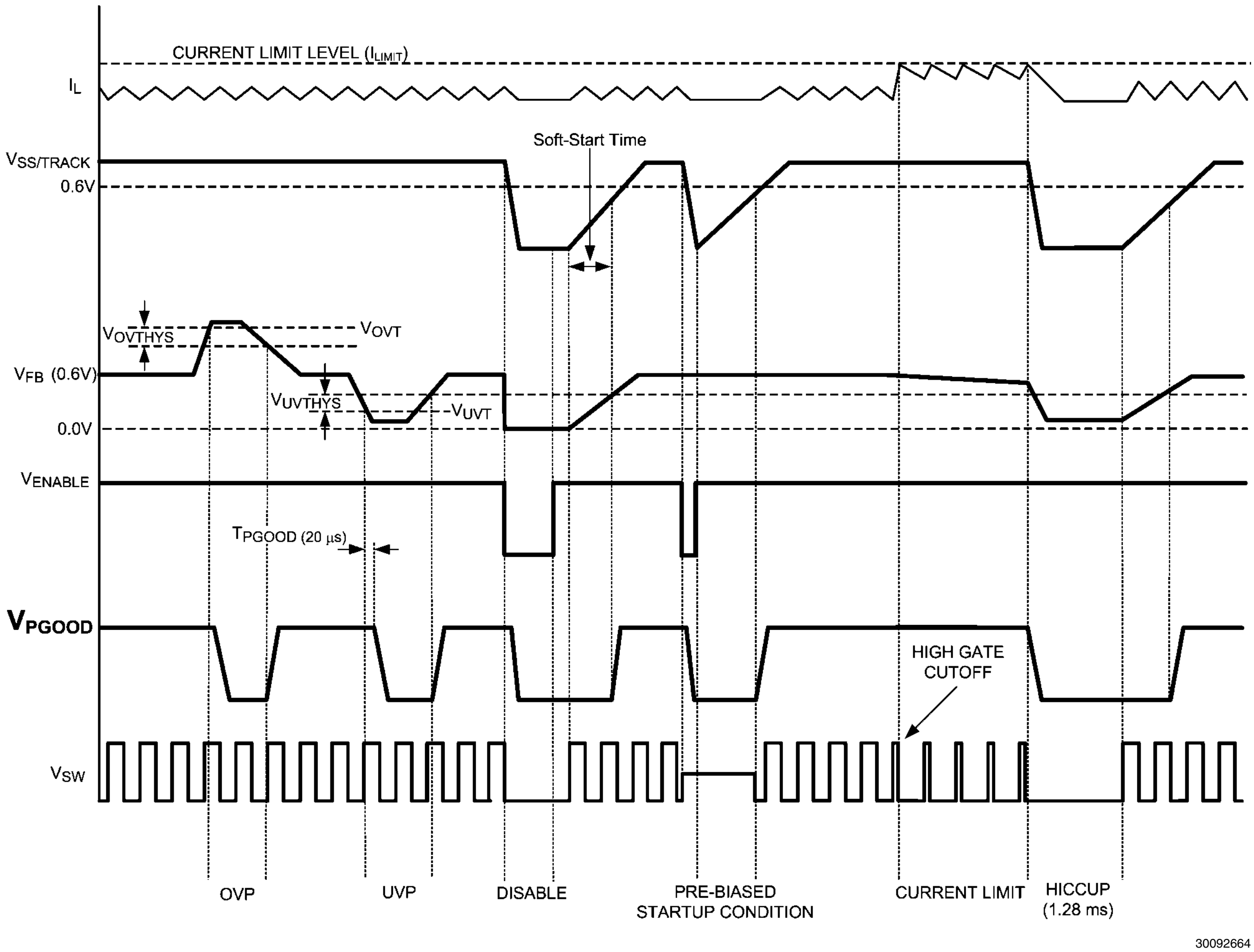


FIGURE 3. Power Good Behavior

THERMAL PROTECTION

Internal thermal shutdown is provided to protect the controller in the event that the maximum junction temperature of approximately 165°C has been exceeded. Both the high-side and low-side FETs are turned off during this condition. During a thermal fault condition, PGOOD is held at logic zero.

Design Guide

The Design Guide assists the designer with the steps necessary to select the external components to build a fully functional power supply. As with any DC-DC converter numerous tradeoffs are possible to optimize the design for efficiency, size, or performance. These tradeoffs will be taken into account and highlighted throughout the discussion. To facilitate component selection, the circuit shown in *Figure 4* below may be used as a reference. Unless otherwise indicated, all formulae assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance and Volts (V) for voltage.

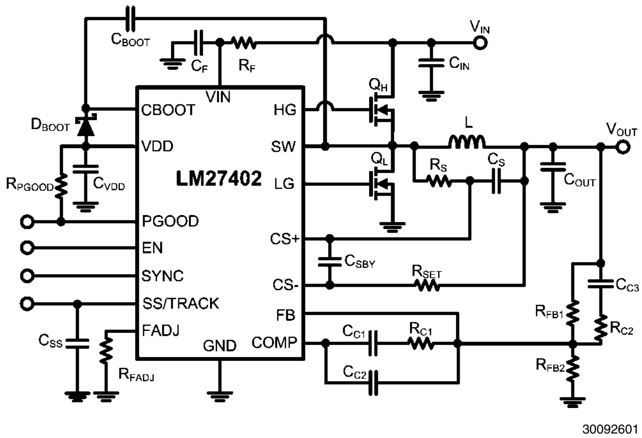


FIGURE 4. Typical Application Circuit

The above schematic shows R_F and C_F acting as an RC filter to the input of the LM27402. The filter is used to attenuate voltage ripple that may exist on the input rail particularly during high output currents. The recommended values of R_F and C_F are 2.2Ω and 1 µF, respectively. There is a practical limit to the size of R_F as it can cause a large voltage drop if large operating bias currents are present. The VIN pin of the LM27402 should not exceed 150 mV difference from the input voltage rail (V_{IN}).

The first equation to calculate for any buck converter is duty ratio:

$$D = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta}$$

Due to the resistive powertrain losses, the duty ratio will increase based on the overall efficiency, η. Calculation of η can be found in the POWER/EFFICIENCY CALCULATIONS section of this datasheet.

INDUCTOR SELECTION (L)

The inductor value is determined based on the operating frequency, load current, ripple current, and duty ratio. The selected inductor should have a saturation current rating greater than the peak current limit of the LM27402. To optimize the performance, the inductance is typically selected such that the ripple current, ΔI_L, is between 20% and 40% of the rated output current. *Figure 5* illustrates the switch voltage and inductor ripple current waveforms. Once the nominal input voltage, output voltage, operating frequency, and desired ripple current are known, the minimum inductance value can be calculated by:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

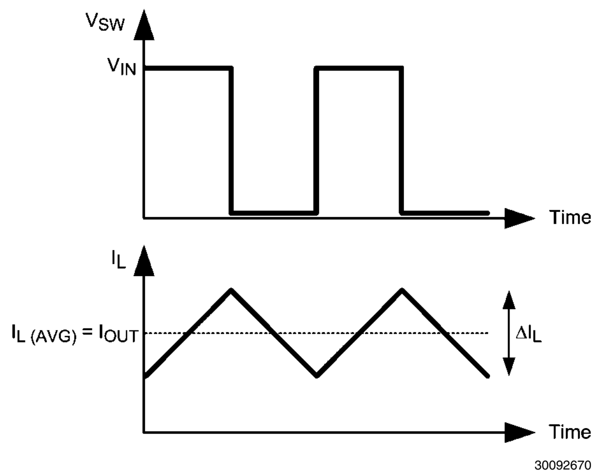


FIGURE 5. Switch Voltage and Inductor Current Waveforms

The peak inductor current at maximum load, $I_{OUT} + \Delta I_L/2$, should be kept adequately below the peak current limit setpoint of the device.

OUTPUT CAPACITOR SELECTION (C_{OUT})

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load events. A wide range of output capacitors may be used with the LM27402 that provide excellent performance. The best performance is typically obtained using ceramic, tantalum, or electrolytic type chemistries. Typically, ceramic capacitors provide extremely low ESR to reduce the output ripple voltage and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a small size for transient loading events. When selecting the output capacitance value, the two performance characteristics to consider are the output voltage ripple and transient response. The output voltage ripple can be approximated by:

$$\Delta V_{OUT} = \Delta I_L \times \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2}$$

where ΔV_{OUT} (V) is the amount of peak to peak voltage ripple at the power supply output, R_{ESR} (Ω) is the series resistance of the output capacitor, f_{SW} (Hz) is the switching frequency, and C_{OUT} (F) is the output capacitance used in the design. The amount of output ripple that can be tolerated is application specific; however a general recommendation is to keep the output ripple less than 1% of the rated output voltage. Note that ceramic capacitors are sometimes preferred because they have very low ESR; however, depending on package and voltage rating of the capacitor, the value of capacitance can drop significantly with applied voltage and operating temperature.

The output capacitor will affect the output voltage droop during a load transient. The peak output voltage deviation is dependent on many factors such as output capacitance, output capacitor ESR, inductor size, control loop bandwidth, powertrain parasitics, etc. Given sufficient control loop bandwidth, a good approximation of the output voltage deviation is:

$$\Delta V_{TR} = \frac{L \times \Delta I_O^2}{2 \times C_{OUT} \times V_L} + \frac{R_{ESR}^2 \times C_{OUT} \times V_L}{2 \times L}$$

ΔV_{TR} (V) is the transient output voltage deviation, ΔI_{OUT} (A) is the load current step change and L (H) is the filter inductance. V_L is the minimum inductor voltage which is duty ratio dependent.

$V_L = V_{OUT}$, if D ≤ 0.5,

$V_L = V_{IN} - V_{OUT}$, if D > 0.5

For a desired ΔV_{TR} (V), a minimum output capacitance can be found by:

$$C_{OUT} \geq \frac{L \times \Delta I_{OUT}^2}{\Delta V_{TR} \times V_L} \times \frac{1}{1 + \sqrt{1 - \left(\frac{R_{ESR} \times \Delta I_{OUT}}{\Delta V_{TR}}\right)^2}}$$

INPUT CAPACITOR SELECTION (C_{IN})

Input capacitors are necessary to limit the input ripple voltage while supplying much of the switch current during the high-side FET on-time. It is generally recommended to use ceramic capacitors at the input as they provide both a low impedance and a high RMS current rating. It is important to choose a stable dielectric for the ceramic capacitor such as X5R or X7R. A quality dielectric provides better temperature performance and also avoids the DC voltage derating inherent with Y5V capacitors. The input capacitor should be placed as close as possible to the drain of the high-side FET and the source of the low-side FET. Non-ceramic input capacitors should be selected for RMS current rating, minimum ripple voltage, and to provide damping. A good approximation for the required ripple current rating is given by the relationship:

$$I_{CIN\_RMS} \approx I_{OUT} \times \sqrt{D \times (1 - D)}$$

The highest requirement for RMS current rating occurs for D = 0.5. When D = 0.5, the RMS ripple current rating of the input capacitor should be greater than half the output current. Low ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitors to provide optimized input filtering for the regulator.

The input voltage ripple can be calculated using:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{C_{IN} \times f_{SW}} + \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \times R_{ESR\_CIN}$$

The minimum amount of input capacitance as a function of desired input voltage ripple can be calculated using:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{\left(\Delta V_{IN} - \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \times R_{ESR\_CIN}\right) \times f_{SW}}$$

USING PRECISION ENABLE

If enable (EN) is not controlled directly, the LM27402 can be pre-programmed to turn on at an input voltage higher than the UVLO voltage. This can be done with an external resistor divider from VIN to EN and EN to GND as shown in *Figure 6*.

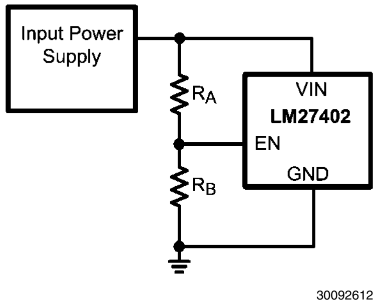


FIGURE 6. Enable Sequencing

The resistor values of R_A and R_B can be relatively sized to allow the EN pin to reach the enable threshold voltage (1.17V) at the appropriate input supply voltage. With the enable current source considered, the equation to solve for R_A is:

$$R_A = \frac{R_B(V_{IN} - 1.17V)}{1.17V - I_{EN} \times R_B}$$

where R_A is the resistor from VIN to EN, R_B is the resistor from EN to GND, I_{EN} is the internal enable pull-up current (2µA) and 1.17V is the fixed precision enable threshold voltage. Typical values for R_B range from 10kΩ to 100kΩ.

SETTING THE SOFT-START TIME

Adding a soft-start capacitor can reduce inrush currents and provide a monotonic startup. The size of the soft-start capacitor can be calculated by:

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{0.6V}$$

The size of the C_{SS} capacitor is influenced by the desired soft-start time t_{ss} (s) , the soft-start current I_{ss} (A) (3 µA) and the nominal feedback (FB) voltage level of 0.6V. If V_{VIN} and V_{VDD} are above the UVLO voltage level (2.90V) and EN is above the enable threshold (1.17V), the soft-start sequence will begin. The LM27402 defaults to a minimum startup time of 1.28 ms when no soft-start capacitor is connected. In other words, the LM27402 will not startup faster than 1.28 ms. The soft-start capacitor is discharged when enable is cycled, during UVLO, OTP, or when the LM27402 enters hiccup mode from an over-current event.

There is a delay between EN transitioning above 1.17V and the beginning of the soft-start sequence. The delay allows the LM27402 to initialize its internal circuitry. Once the output has charged to 94% of the nominal output voltage and SS/TRACK has exceeded 564 mV, the PGOOD indicator will transition high as illustrated in *Figure 7*.

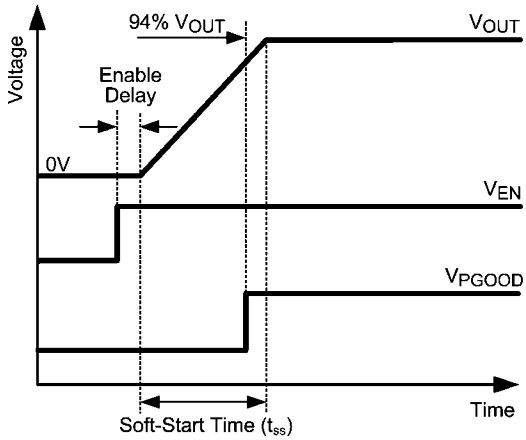


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FIGURE 7. Soft-Start Timing

TRACKING

The SS/TRACK pin also functions as a tracking pin when external power supply tracking is needed. Tracking is achieved by simply dividing down the external supply voltage with a simple resistor network shown in *Figure 8*. With the correct resistor divider configuration, the LM27402 can track an external voltage source to obtain a coincident or ratiometric startup behavior.

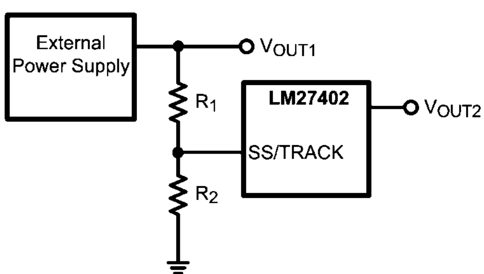

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FIGURE 8. Tracking an External Power Supply

Since the soft-start charging current I_{SS} is sourced from the SS/TRACK pin, the size of R_2 should be less than 10 kΩ to minimize errors in the tracking output. Once a value for R_2 is selected, the value for R_1 can be calculated using the appropriate equation in *Figure 9* to give the desired startup sequence. *Figure 9* shows two common startup sequences; the top waveform shows a coincidental startup while the bottom waveform illustrates a ratiometric startup. A coincidental configuration provides a robust startup sequence for certain applications since it avoids turning on any parasitic conduction paths that may exist between loads. A ratiometric configuration is preferred in applications where both supplies need to be at the final value at the same time.

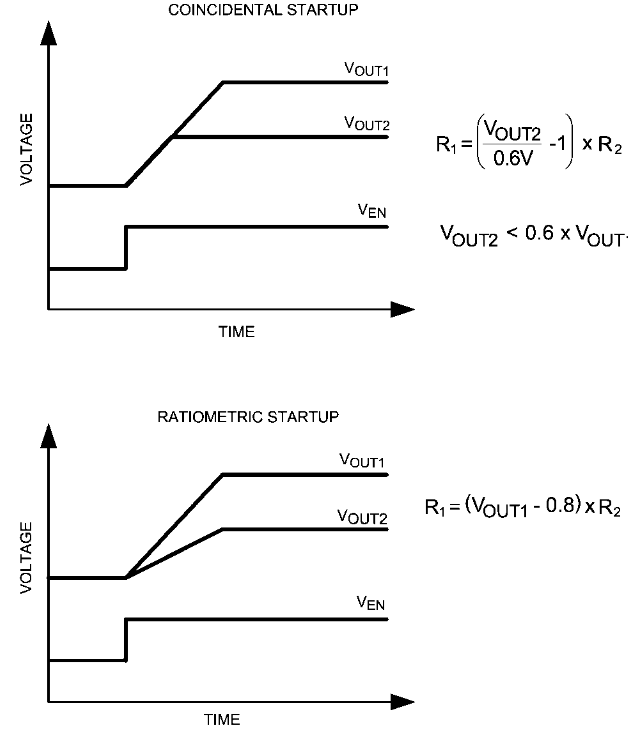

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FIGURE 9. Tracking Startup Sequences

Similar to the soft-start function, the fastest possible startup time is 1.28 ms regardless of the rise time of the tracking voltage. When using the track feature, the final voltage seen by the SS/TRACK pin should exceed 0.8V to provide sufficient overdrive and transient immunity.

SETTING THE SWITCHING FREQUENCY

There are two options for setting the switching frequency of the LM27402. The frequency can be adjusted by an external resistor from FADJ to GND, or the user can synchronize the LM27402 to an external clock signal through SYNC. The LM27402 will only synchronize to frequencies above the frequency set by the R_{FADJ} resistor. The clock signal must range from less than 0.8V to greater than 2.0V to ensure proper operation. If the clock signal ceases, the switching frequency will reduce to the frequency set by the FADJ resistor. The frequency range is 200 kHz to 1.2 MHz. The sync-in clock can synchronize a maximum of 400 kHz above the frequency set by the resistor. To find the value of resistance needed for a given frequency use the following equation: (f_{SW} (kHz), R_{FADJ} (kΩ))

$$R_{FADJ} = \frac{100}{\frac{f_{SW}}{100} - 1} - 5$$

SETTING THE CURRENT LIMIT THRESHOLD

The LM27402 exploits the filter inductor DCR (DC resistance) to detect over current events. If desired, the user can employ inductors with low tolerance DCR to increase the accuracy of the current limit threshold. The most common topology for sensing the DCR is shown in *Figure 10*.

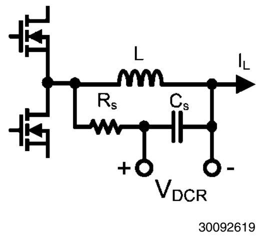


FIGURE 10. DCR Sensing Circuit

The most accurate sensing of voltage across the DCR is achieved by matching the time constant of the R_SC_S filter with the inductor L/R_{DCR} time constant. If the time constants are matched, the voltage across the capacitor follows the voltage across the DCR. A typical range of capacitance used in the R_SC_S network is 100 nF to 1µF. The equation matching the time constants is:

$$R_SC_S = \frac{L}{R_{DCR}}$$

The current limit threshold can be adjusted to any level with a single resistor from the current limit comparator to the output voltage pin. Use the circuit in *Figure 11* to set the current limit.

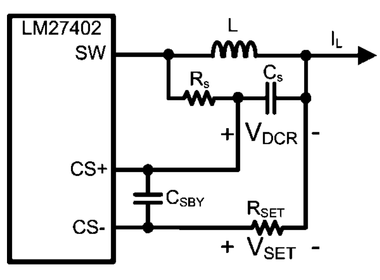


FIGURE 11. Setting the Current Limit Level

Since the voltage across the inductor DCR follows the current through the inductor, the device will trip at the peak of the inductor current. Capacitor C_{SBY} shown in *Figure 11* filters the input to the current sense comparator. A working range for this capacitance is 47 pF to 100 pF. The equation to set the resistor value of R_{SET} is:

$$R_{SET} = \frac{I_{LIMIT}\, R_{DCR}}{I_{CS-}}$$

I_{LIMIT} (A) is the desired current limit level, R_{DCR} (Ω) is the rated DC resistance of the inductor and I_{cs-} (A) is the 10 µA current source flowing out of the CS- pin.

The internal current source I_{CS-} is powered from the input voltage rail (VIN). The minimum voltage required to power the current source is 1V from VIN to V_{OUT}. If a condition occurs where VIN - V_{OUT} < 1V, the LM27402 may prematurely initiate hiccup mode. There are multiple options to avoid this situation. The first option is to enable the LM27402 after the input voltage has risen 1V above the nominal output voltage as seen in *Figure 6*. The second option is to lower the comparator common mode voltage shown in *Figure 12* such that the I_{CS-} current source has enough headroom voltage.

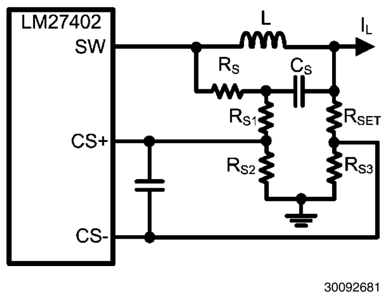


FIGURE 12. Common Mode Voltage Resistor Divider Network

Please refer to Application Note AN-2060 for design guidelines to adjust the common mode voltage of the current sense comparator.

CONTROL LOOP COMPENSATION

The LM27402 voltage mode control system incorporates input voltage feed-forward to eliminate the input voltage dependence of the PWM gain. Input voltage feed-forward allows the LM27402 to be stable throughout the entire input voltage range and makes it easier for the designer to select the compensation and power components. The following text will describe how to set the output voltage and obtain the open loop transfer function.

During steady state operation, the DC output voltage is set by a feedback resistor network between V_{OUT}, FB and GND. The FB voltage is nominally 0.6V ±1%. The equation describing the output voltage is:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}}\, 0.6V$$

A good starting value for R_{FB1} is 20 kΩ. If an output voltage of 0.6V is required, R_{FB2} should not be used.

There are three main blocks of a voltage mode buck switcher that the power supply designer must consider when designing the control system: the powertrain, PWM modulator, and the compensator. A diagram representing the control loop is shown in *Figure 13*.

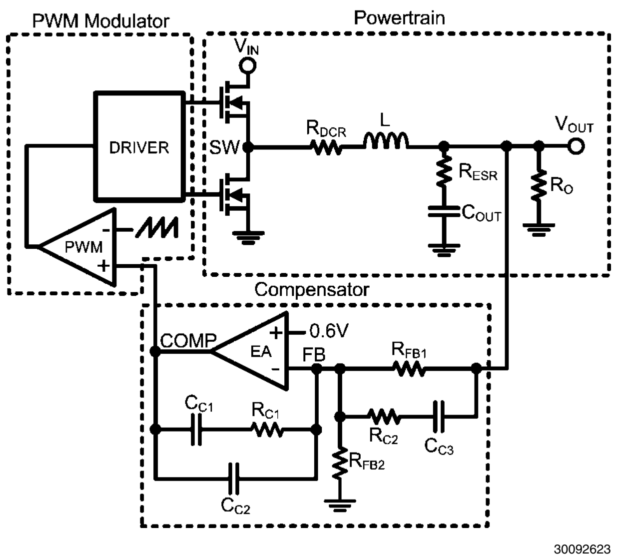


FIGURE 13. Control Loop Schematic Diagram

The powertrain consists of the filter inductor (L) with DCR (R_{DCR}), output capacitor (C_{OUT}) with ESR (effective series resistance R_{ESR}), and effective load resistance (R_O). The error amplifier (EA) regulates the feedback pin (FB) to 0.6V. The passive compensation components around the error amplifier help maintain system stability. Type III compensation is shown in *Figure 13*. The PWM modulator establishes the duty cycle command by comparing the error amplifier output (COMP) with an internally generated ramp set at the switching frequency.

The modulator gain, powertrain and compensator transfer functions must be taken into consideration when obtaining the total open loop transfer function. The PWM modulator adds a DC gain to the open loop transfer function. In a basic voltage mode system, the PWM gain will vary with input voltage. However the LM27402 internal voltage feed-forward circuitry maintains a constant PWM gain of 7:

$$G_{PWM} = \frac{1}{k_{FF}} = 7$$

The powertrain transfer function includes the output inductor with DCR, output capacitor with ESR, and load resistance. The inductor and capacitor create two complex poles at a frequency described by:

$$f_{LC} = \frac{1}{2\pi}\sqrt{\frac{R_O + R_{DCR}}{LC_{OUT}(R_O + R_{ESR})}}$$

A left half plane zero is created by the output capacitor ESR located at a frequency described by:

$$f_{ESR} = \frac{1}{2\pi C_{OUT} R_{ESR}}$$

The complete powertrain transfer function is:

$$G_P(s) = \frac{1 + \frac{s}{2\pi f_{ESR}}}{1 + \frac{s}{Q_O 2\pi f_{LC}} + \left(\frac{s}{2\pi f_{LC}}\right)^2}$$

The bode plot of the above transfer function can be seen in *Figure 14*.

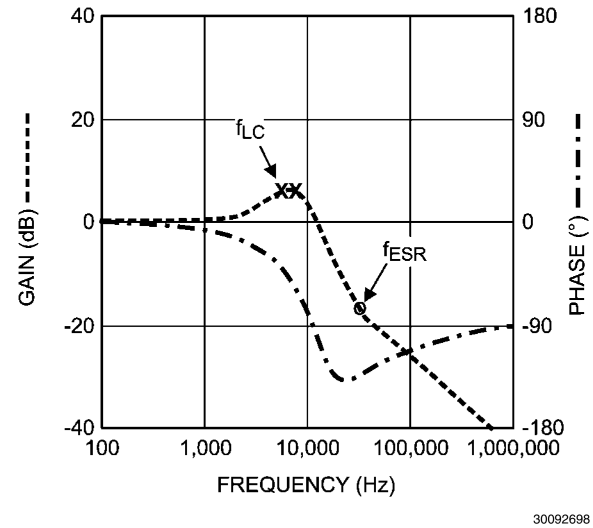


FIGURE 14. Powertrain Bode Plot

The complex poles (f_{LC}) created by the filter inductor and output capacitor cause a 180° phase shift as seen in *Figure 14*. The phase is boosted back up to -90° by virtue of the output capacitor ESR zero. The phase shift caused by the complex poles must be compensated to stabilize the loop response. The compensation network shown around the error amplifier in *Figure 13* creates two poles, two zeros and a pole at the origin. Placing these poles and zeros at the correct frequencies will optimize the loop response. The compensator transfer function is:

$$G_{EA}(s) = K_m \frac{\left(\frac{2\pi f_{Z1}}{s} + 1\right)\left(\frac{s}{2\pi f_{Z2}} + 1\right)}{\left(\frac{s}{2\pi f_{P1}} + 1\right)\left(\frac{s}{2\pi f_{P2}} + 1\right)}$$

The pole located at the origin provides high DC gain to optimize DC load regulation performance. The other two poles and two zeros can be located accordingly to stabilize the voltage mode loop depending on the power stage complex poles and damping characteristic Q. *Figure 15* is an illustration of what the error amplifier compensation transfer function will look like.

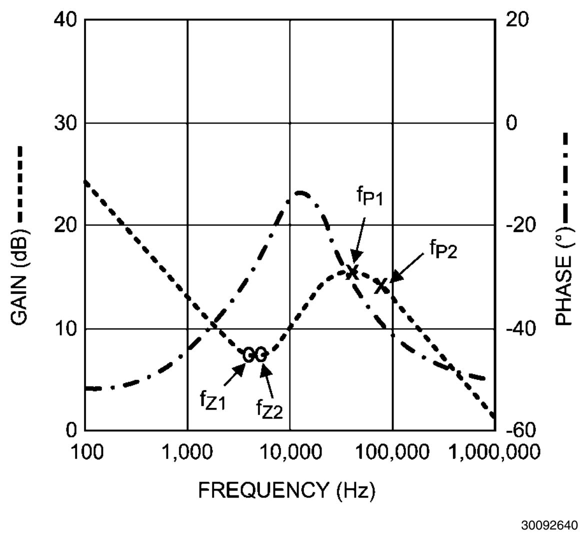


FIGURE 15. Type III Compensation Network Bode Plot

K_m is the mid-band gain of the compensator and can be estimated by:

$$K_m = \frac{f_C\, k_{FF}}{f_{LC}}$$

f_C (Hz) is the desired crossover frequency and is usually selected between one tenth and one fifth of the switching frequency (f_{SW}). The next set of equations show pole and zero locations expressed in terms of the components in the compensator feedback loop.

$$f_{Z1} = \frac{1}{2\pi R_{C1} C_{C1}} \qquad f_{Z2} = \frac{1}{2\pi (R_{C2} + R_{FB1}) C_{C3}}$$

$$f_{P1} = \frac{1}{2\pi R_{C2} C_{C3}} \qquad f_{P2} = \frac{C_{C1} + C_{C2}}{2\pi R_{C1} C_{C1} C_{C2}} \qquad K_m = \frac{R_{C1}}{R_{FB1}}$$

Depending on Q, the complex double pole can cause an increase in gain at the LC resonant frequency and a precipitous drop in phase. To compensate for the phase drop, it is common practice to place both compensator zeros created by the type III compensation network at or slightly below the LC double pole frequency. The other two poles should be located beyond this point. One pole is located at the zero caused by the output capacitor ESR and the other pole is placed at half the switching frequency to roll off the higher frequency response.

$$f_{Z1} = f_{Z2} = f_{LC}$$

$$f_{P1} = f_{ESR}$$

$$f_{P2} = \frac{f_{SW}}{2}$$

Conservative values for the compensation components can be found by using the following equations.

$$R_{C1} = R_{FB1} K_m$$

$$C_{C1} = \frac{1}{2\pi f_{LC} R_{C1}}$$

$$R_{C2} = \frac{R_{FB1}\, f_{LC}}{f_{ESR} - f_{LC}}$$

$$C_{C3} = \frac{1}{2\pi f_{ESR} R_{C2}}$$

$$C_{C2} = \frac{C_{C1}}{\pi f_{SW} R_{C1}\, C_{C1} - 1}$$

After finding the compensation components it is wise to create a bode plot of the loop response using all three transfer functions. An illustration of the loop response is provided in *Figure 16* .

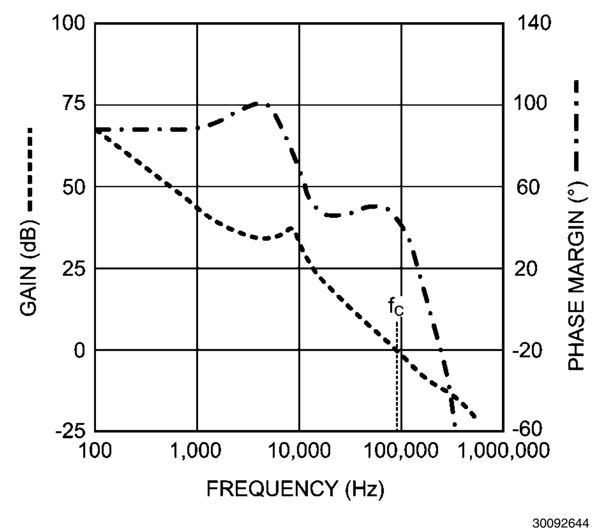


FIGURE 16. Loop Response

It is important to always verify the stability by either observing the load transient response or by using a network analyzer. A phase margin between 45° and 70° is usually desired for voltage mode controlled systems. Excessive phase margin can cause slow system response to load transients and low phase margin may cause an oscillatory load transient response. If the load transient response peak deviation is larger than desired, increasing f_C and recalculating the compensation components may help but usually at the expense of phase margin.

MOSFET GATE DRIVE

To drive large MOSFETs with high gate charge, the LM27402 includes low impedance high-side and low-side gate drivers. Low impedance gate drivers allow high current designs by enabling fast transition times and increased efficiency. The high-side gate drive is powered from a charge pump common to the switch-node and the low-side gate is powered by the VDD rail shown in *Figure 17*.

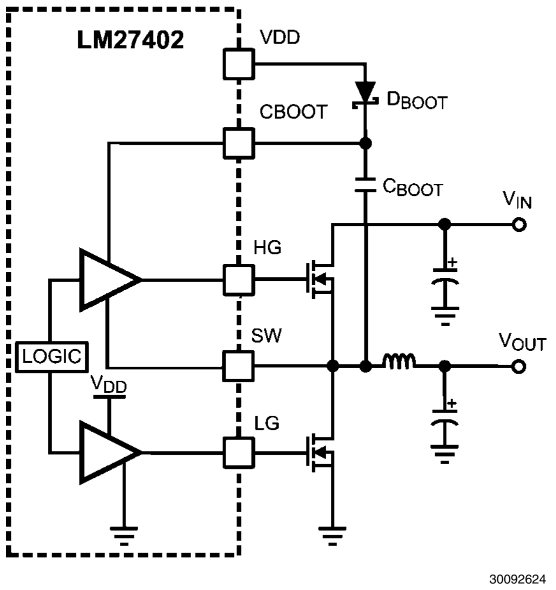


FIGURE 17. VDD Charge Pump Circuit

The circuit in *Figure 17* will effectively supply close to the VDD voltage (4.5V) between the gate and the source of the high-side MOSFET during the on time. It is recommended to use a Schottky diode for D_{BOOT} with sufficient reverse standoff voltage and continuous current rating. The average current through this diode is dependent on the gate charge of the high-side FET and the frequency. It can be calculated using the following equation

$$I_{DBOOT} = f_{SW} Q_{GHS}$$

I_{DBOOT} is the average current through the D_{BOOT} diode, f_{SW} (Hz) is the switching frequency and Q_{GHS} (C) is the gate charge of the high-side MOSFET. If the input voltage is below 5.5V, it is recommended to connect VDD to the input supply of the LM27402 through a 1Ω resistor shown in *Figure 18*. This will increase the gate voltage of both the low-side and high-side FETs.

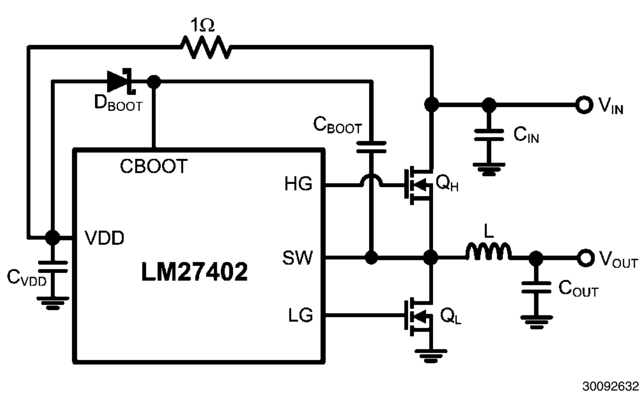


FIGURE 18. Tie V_{DD} to V_{IN} when VIN ≤ 5.5V

POWER / EFFICIENCY CALCULATIONS

The overall efficiency of a buck regulator is simply the ratio of output power to input power. Accurately predicting the overall efficiency can be tedious and depends on many variables. Although power losses can be found in almost every component of a buck regulator, the following sections present equations detailing components with the highest relative power loss.

MOSFETS

Selecting the correct MOSFET for a design is important to the overall operation of the circuit. If inappropriate FETs are selected for the application, it can result in poor efficiency, high temperature issues, shoot-through and other impairments. It is important to calculate the power dissipation for each MOSFET at the maximum output current and make sure the maximum allowable power dissipation is not exceeded. MOSFET datasheets should also specify a junction-to-ambient thermal resistance (θ_{JA}) so the temperature rise can be estimated from this specification .

Both high-side and low-side FETs contribute significant loss to the system relative to the other components. The high-side FET contributes transition switching losses, conduction losses and gate charge losses. The low-side FET also contributes conduction and gate charge losses, but the FET body diode voltage drop during deadtime and reverse recovery loss must also be considered. The transition losses for the low-side FET are small and usually ignored.

High-Side MOSFET

The next set of equations can be used to calculate the losses associated with the high-side FET.

$$P_{CND\_HS} \approx I_{OUT}^2 \times R_{DS(ON)\_HS} \times D \times 1.3$$

$$P_{SW\_HS} = \frac{V_{IN} \times I_{OUT} \times f_{SW} \times (tr+tf)}{2}$$

$$P_{TOT\_HS} = P_{CND\_HS} + P_{SW\_HS}$$

P_{CND_HS} is the conduction loss of the high-side FET during the D cycle when current is flowing through the FET on-resistance. A self heating coefficient of 1.3 is included in this equation to approximate the effects of the $R_{DS(ON)}$ temperature coefficient. $R_{DS(ON)\_HS}$ (Ω) is the drain to source resistance, I_{OUT} (A) is the output current and D is the duty ratio. P_{SW_HS} is the switching power loss during the high-side FET transition time. V_{IN} (V) is the input voltage, f_{SW} (Hz) is the switching frequency, and t_r and t_f (s) are the rise and fall times of the switch-node voltage respectively. P_{TOT_HS} is the total power dissipation of the high-side FET.

The gate charge of the high-side MOSFET can greatly affect the turn-on transition time and therefore efficiency. Furthermore, it is wise to consider the ratio of switching loss to conduction loss associated with the high-side FET. If the duty ratio is small and the input voltage is high, it may be beneficial to tradeoff Q_G for higher $R_{DS(ON)}$ to avoid high switching losses relative to conduction losses. If the duty ratio is large and the input voltage is low, then a lower $R_{DS(ON)}$ FET in tandem with a higher Q_G may result in less power dissipation.

Low-Side MOSFET

The next set of equations can be used to calculate the losses due to the low-side FET.

$$P_{CND\_LS} \approx I_{OUT}^2 \times R_{DS(ON)\_LS} \times (1-D) \times 1.3$$

$$P_D = T_{deadtime} \times f_{SW} \times I_{OUT} \times V_{FD}$$

$$P_{RR} = Q_{RR} \times f_{SW} \times V_{IN}$$

$$P_{TOT\_LS} = P_{CND\_LS} + P_D + P_{RR}$$

P_{CND_LS} is the conduction loss of the low-side FET during the 1-D cycle when current is flowing through the on-resistance of the FET. $R_{DS(ON)\_LS}$ (Ω) is the drain to source resistance.

P_D is the deadtime power loss due to the body diode drop of the low-side FET. $T_{deadtime}$ (s) is the total deadtime.

P_{RR} is the reverse recovery charge power loss. Q_{RR} (C) is the total reverse recovery charge usually specified in the FET datasheet. P_{TOT_LS} is the total power dissipation of the low-side FET.

Gate Charge Loss

A finite amount of gate charge is required in order to switch the high-side and low-side FETs. This gate charge is continuously charging the FETs during every switching cycle and appears as a constant current flowing into the controller from the input supply. The next equation describes the power loss due to the gate charge.

$$P_{QG} = V_{IN} \times (Q_{GHS} + Q_{GLS}) \times f_{SW}$$

P_{QG} is the total gate charge power loss, Q_{GHS} (C) and Q_{GLS} (C) are the high-side and low-side FET gate charges respectively, and can be found in the FET datasheets, V_{IN} (V) is the input voltage, and f_{SW} (Hz) is the switching frequency.

Input and Output Capacitor ESR Losses

Both the input and output capacitors are subject to steady state AC current and must be taken into consideration when calculating power losses. The next equation shown is the input capacitor ESR power loss.

$$P_{IN\_CAP} = I_{CIN\_RMS}^2 \times R_{ESR\_CIN}$$

The input capacitor power loss equation includes the effective series resistance or R_{ESR_IN} (Ω) of the input capacitor. The power loss due to the ESR of the output capacitor is:

$$P_{OUT\_CAP} = \frac{\Delta I_L^2}{12} \times R_{ESR}$$

The output capacitor power loss equation includes the peak to peak inductor current, ΔI_L(A), and the effective series resistance or R_{ESR} (Ω) of the output capacitor.

Inductor Losses

The losses due to the inductor are caused primarily by the DCR. The next equation calculates the inductor DCR power loss.

$$P_{DCR} = I_{RMS}^2 \times R_{DCR} \times 1.2$$

P_{DCR} is the total power loss of the Inductor. A self heating coefficient of 1.2 is included in this equation to approximate the effects of the copper temperature coefficient approximately equal to 3900ppm/°C. R_{DCR} (Ω) is the inductor DC resistance.

Controller Losses

The controller loss remains constant and contributes to a very small loss of power. The quiescent current is the main factor in terms of power loss attributed to the controller and it remains constant at 4 mA. The quiescent current power loss equation is:

$$P_{IQ} = V_{IN} \times I_Q$$

The controller I_Q power loss equation includes the I_Q current (4 mA) and input voltage V_{IN} (V).

It is also important to calculate the power dissipated in the controller itself due to the gate charge current flowing from VIN to the output of the LDO (VDD). The gate charge current essentially passes through a resistance dropping the input voltage VIN to the LDO voltage (4.5V). This can cause the controller to operate at an elevated temperature since it must dissipate the power of the LDO pass device. The next equation calculates the power dissipated by the internal LDO of the controller.

$$P_{LDO} = (V_{VIN} - 4.5) \times (Q_{GLS} + Q_{GHS}) \times f_{SW}$$

P_{LDO} is the power dissipated in the LDO, Q_{GHS} (C) and Q_{GLS} are the high-side and low-side FET gate charges, respectively, and can be found in the FET datasheets.

Overall Efficiency

After calculating the losses, the efficiency can then be calculated using:

$$\eta\ (\%) = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \times 100$$

$$P_{LOSS} = P_{TOT\_HS} + P_{TOT\_LS} + P_{QG} + P_{DCR} + P_{IN\_CAP} + P_{OUT\_CAP} + P_{IQ}$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

PCB LAYOUT CONSIDERATIONS

After selecting the correct components, PCB layout is another crucial step in optimizing a buck regulator. The layout must be able to handle large DC and AC currents, minimize switch-node noise, and spread heat. The following layout guidelines and tips will help increase the chances of a successful design and should be taken seriously during the layout process.

Input and Output Capacitor Layout

A buck regulator is a switching converter with switched currents and voltages. The high di/dt and dv/dt nature of buck switching calls for careful layout of decoupling capacitors. The next figures shows the switching currents for the D and 1-D intervals of a buck regulator.

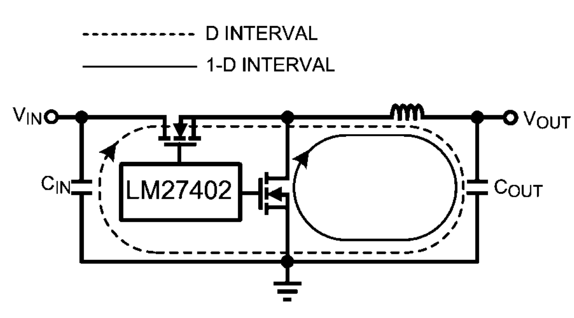


FIGURE 19. Power Flow

During the high-side FET on time, the AC component of the input current is supplied by the input capacitor. Due to the high di/dt nature of this current, it is essential that the input capacitor is closely coupled to the drain of the high-side FET to minimize any parasitic inductance. The output capacitor return and input capacitor return should also be closely coupled to minimize parasitic ground inductance. During the low-side FET on time, current flows from ground through the low-side FET and to the output capacitor through the inductor. It is essential the input capacitor is also closely coupled with the low-side FET source.

MOSFET Layout

With FETs acting as switches in a switching regulator, good layout is essential. Current is constantly transitioning from the high-side FET to the low-side FET so it is essential to place the source of the high-side FET next to the drain of the low-side FET and the switch-node side of the inductor. This will minimize any parasitic inductance between the switch-node and the FETs which can cause switch-node ringing. The FETs can become very hot due to internal power dissipation. Using vias to connect the drain of the FETs to other layers may help spread the heat. The switch-node copper area should not be so small that the low-side FET will not be able to spread its heat.

As seen in the POWER / EFFICIENCY CALCULATIONS section, the rise times of the FETs can significantly affect the efficiency. Therefore, it is good layout practice to maintain the shortest path from the LG/HG gate pins to the pins of the low-side/high-side FETs to minimize the parasitic inductance. The high-side gate trace should be coupled with the switch-node trace since the internal high-side gate drive is connect between CBOOT and SW. The low-side FET gate trace should be coupled with ground return since the internal low-side gate driver is powered between VDD and ground. A good trace width is around 0.015 inches to support the high transient currents. During switching transition, it is common to see peak transient currents of 1 - 2A flowing through gate traces so minimizing the parasitic inductance is crucial to fast and efficient switching.

Noise

Because of the high energy switching characteristic of the switching regulator, it is good practice to separate noise generating circuitry from noise sensitive circuitry. For a buck regulator, this means separating the switch-node from the feedback circuitry. This can be achieved by distance or can be shielded on the back side of the board through an internal copper ground plane.

Reducing the noise in the DCR sense circuitry is imperative to realize accurate effective over-current response. Separation of this circuitry from the switch-node and gate drivers will reduce the amount of switching noise pickup at the input of the current limit comparator. Running the DCR sense traces in parallel as a differential pair can significantly reduce the effect of any system noise (including switch-node pickup) at the input of the current limit comparator.

The SW pin of the LM27402 receives signals directly from the switch-node of the regulator to collect switching information. This is an unimpeded noise path that may cause erratic switching behavior if excessive noise is injected from the switch-node. If needed, a snubber can be used to limit the dv/dt of the signal effectively reducing the noise into the switch-node sense pin.

Controller Layout

Proper layout practices of the controller can help guarantee proper operation.Locating the input decoupling capacitor (C_F), as close as possible to the VDD capacitor (C_{VDD}) with the LM27402 GND will help increase noise immunity.

EXAMPLE CIRCUIT 1

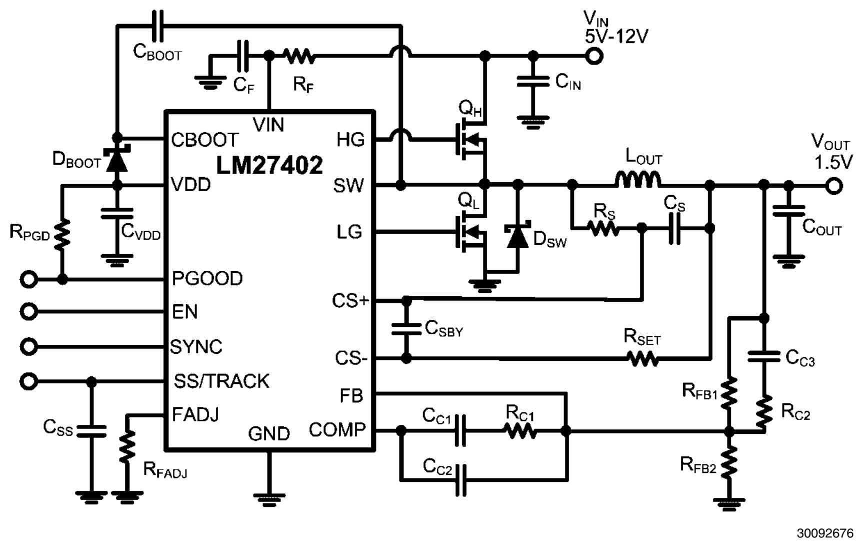


FIGURE 20. 5V - 12V V_{IN} to 1.5V V_{OUT}, 20A I_{OUT}, fsw = 300 kHz

Bill of Materials

Designator	Type	Parameters	Part Number	Qty	Manufacturer
U1	Synchronous Buck Controller		LM27402	1	National Semiconductor
C_{BOOT}	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{C1}	Capacitor	3900 pF, Ceramic, X7R, 50V, 10%	GRM188R71H392KA01D	1	Murata
C_{C2}	Capacitor	150 pF, Ceramic, C0G, 50V, 5%	GRM1885C1H151JA01D	1	Murata
C_{C3}	Capacitor	820 pF, Ceramic, C0G, 50V, 5%	GRM1885C1H821JA01D	1	Murata
C_{VDD}	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_F	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_{IN}	Capacitor	22 µF, Ceramic, X5R, 25V, 10%	GRM32ER61E226KE15L	5	Murata
C_{OUT}	Capacitor	100 µF, Ceramic, X5R, 6.3V, 20%	C1210C107M9PACTU	4	Kemet
C_S	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{SS}	Capacitor	47000 pF, Ceramic, X7R, 16V, 10%	GRM188R71C473KA01D	1	Murata
C_{SBY}	Capacitor	100 pF, Ceramic, C0G, 50V, 5%	GRM1885C1H101JA01D	1	Murata
D_{BOOT}	Diode	Schottky Diode, Average I = 100 mA, Max Surge I = 750 mA	CMOSH-3	1	Central Semi
D_{SW}	Diode	Schottky Diode, Average I = 3A, Max Surge I = 80A	CMSH3-40M	1	Central Semi
L_{OUT}	Inductor	.68 µH, 2.34 mΩ	IHLP5050CEERR68M06	1	Vishay

Designator	Type	Parameters	Part Number	Qty	Manufacturer
Q_L	N-CH MOSFET	30V, 60A, 43.5 nC, $R_{DS(ON)}$ @ 4.5V = 1.85 mΩ	Si7192DP	1	Vishay
Q_H	N-CH MOSFET	25V, 40A, 13 nC, $R_{DS(ON)}$ @ 4.5V = 6.2 mΩ	SiR436DP	1	Vishay
R_{C1}	Resistor	8.06 kΩ, 1%, 0.1W	CRCW06038k06FKEA	1	Vishay
R_{C2}	Resistor	261Ω, 1%, 0.1W	CRCW0603261RFKEA	1	Vishay
R_{FADJ}	Resistor	45.3 kΩ, 1%, 0.1W	CRCW060345K3FKEA	1	Vishay
R_{FB1}	Resistor	20.0 kΩ, 1%, 0.1W	CRCW060320K0FKEA	1	Vishay
R_{FB2}	Resistor	20.0 kΩ, 1%, 0.1W	CRCW060320K0FKEA	1	Vishay
R_F	Resistor	2.2Ω, 5%, 0.1W	CRCW06032R20JNEA	1	Vishay
R_{PGD}	Resistor	51.1 kΩ, 5%, 0.1W	CRCW060351K1JNEA	1	Vishay
R_S	Resistor	1.3 kΩ, 1%, 0.1W	CRCW06031K30FKEA	1	Vishay
R_{SET}	Resistor	6.34 kΩ, 1%, 0.1W	CRCW06036K34FKEA	1	Vishay

EXAMPLE CIRCUIT 2

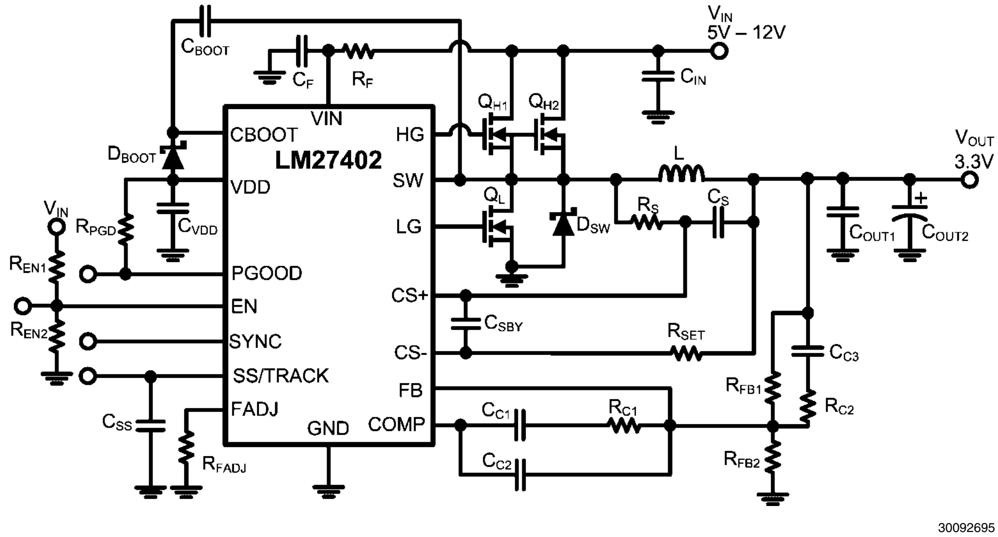


FIGURE 21. 5V - 12V V_{IN} to 3.3V V_{OUT}, 25A I_{OUT} , fsw = 300 kHz

Bill Of Materials

Designator	Type	Parameters	Part Number	Qty	Manufacturer
U1	Synchronous Buck Controller		LM27402	1	National Semiconductor
C_{BOOT}	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{C1}	Capacitor	1200 pF, Ceramic, COG, 50V, 5%	GRM1885C1H122JA01D	1	Murata
C_{C2}	Capacitor	56 pF, Ceramic, COG, 50V, 5%	GRM1885C1H560JA01D	1	Murata
C_{C3}	Capacitor	820 pF, Ceramic, COG, 50V, 5%	GRM1885C1H821JA01D	1	Murata
C_{VDD}	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_F	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_{IN}	Capacitor	22 µF, Ceramic, X5R, 25V, 10%	GRM32ER61E226KE15L	5	Murata
$C_{OUT\ 1}$	Capacitor	100 µF, Ceramic, X5R, 6.3V, 20%	C1210C107M9PACTU	1	Kemet
C_{OUT2}	Capacitor	330 µF, POSCAP, 6.3V, 20%	6TPE1330MIL	1	Sanyo
C_S	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{SS}	Capacitor	47000 pF, Ceramic, X7R, 16V, 10%	GRM188R71E473KA01D	1	Murata
C_{SBY}	Capacitor	100 pF, Ceramic, C0G, 50V, 5%	GRM1885C1H101JA01D	1	Murata
D_{BOOT}	Diode	Schottky Diode, Average I = 100 mA, Max Surge I = 750 mA	CMOSH-3	1	Central Semi

Designator	Type	Parameters	Part Number	Qty	Manufacturer
D_{SW}	Diode	Schottky Diode, Average I = 3A, Max Surge I = 80A	CMSH3-40M	1	Central Semi
L_{OUT}	Inductor	1 µH, 0.9 mΩ	SER2010-102ML	1	Coilcraft
Q_L	N-CH MOSFET	30V, 60A, 43.5 nC, $R_{DS(ON)}$ @ 4.5V = 1.85 mΩ	Si7192DP	1	Vishay
$Q_{H(1,2)}$	N-CH MOSFET	25V, 50A, 20 nC, $R_{DS(ON)}$ @ 4.5V = 3.4 mΩ	SiR892DP	1	Vishay
R_{C1}	Resistor	18.7 kΩ, 1%, 0.1W	CRCW060318K7FKEA	1	Vishay
R_{C2}	Resistor	4.75 kΩ, 1%, 0.1W	CRCW06034K75FKEA	1	Vishay
R_{FADJ}	Resistor	45.3 kΩ, 1%, 0.1W	CRCW060345K3FKEA	1	Vishay
R_{FB1}	Resistor	20.0 kΩ, 1%, 0.1W	CRCW060320K0FKEA	1	Vishay
R_{FB2}	Resistor	4.42 kΩ, 1%, 0.1W	CRCW06034K42FKEA	1	Vishay
R_F	Resistor	2.2Ω, 5%, 0.1W	CRCW06032R20JNEA	1	Vishay
R_{PGD}	Resistor	51.1 kΩ, 5%, 0.1W	CRCW060351K1JNEA	1	Vishay
R_S	Resistor	4.12 kΩ, 1%, 0.1W	CRCW06034K12FKEA	1	Vishay
R_{SET}	Resistor	4.53 kΩ, 1%, 0.1W	CRCW06034K53FKEA	1	Vishay

EXAMPLE CIRCUIT 3

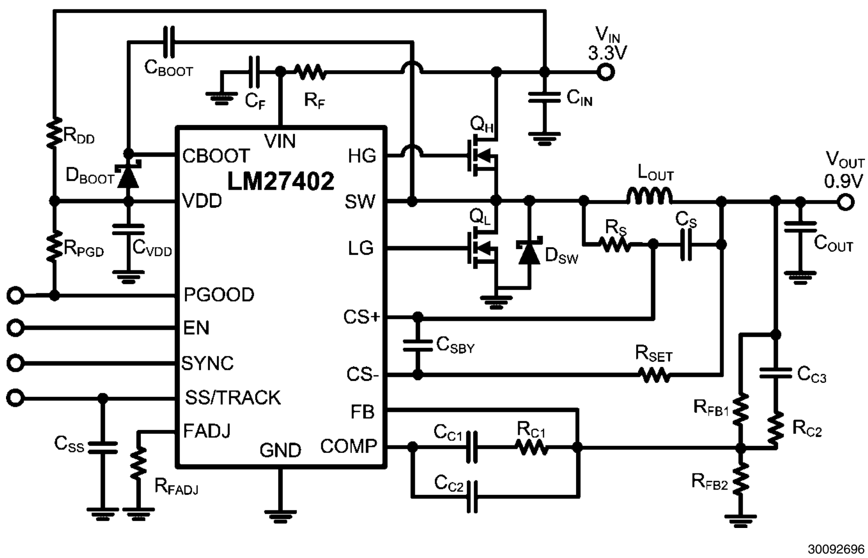


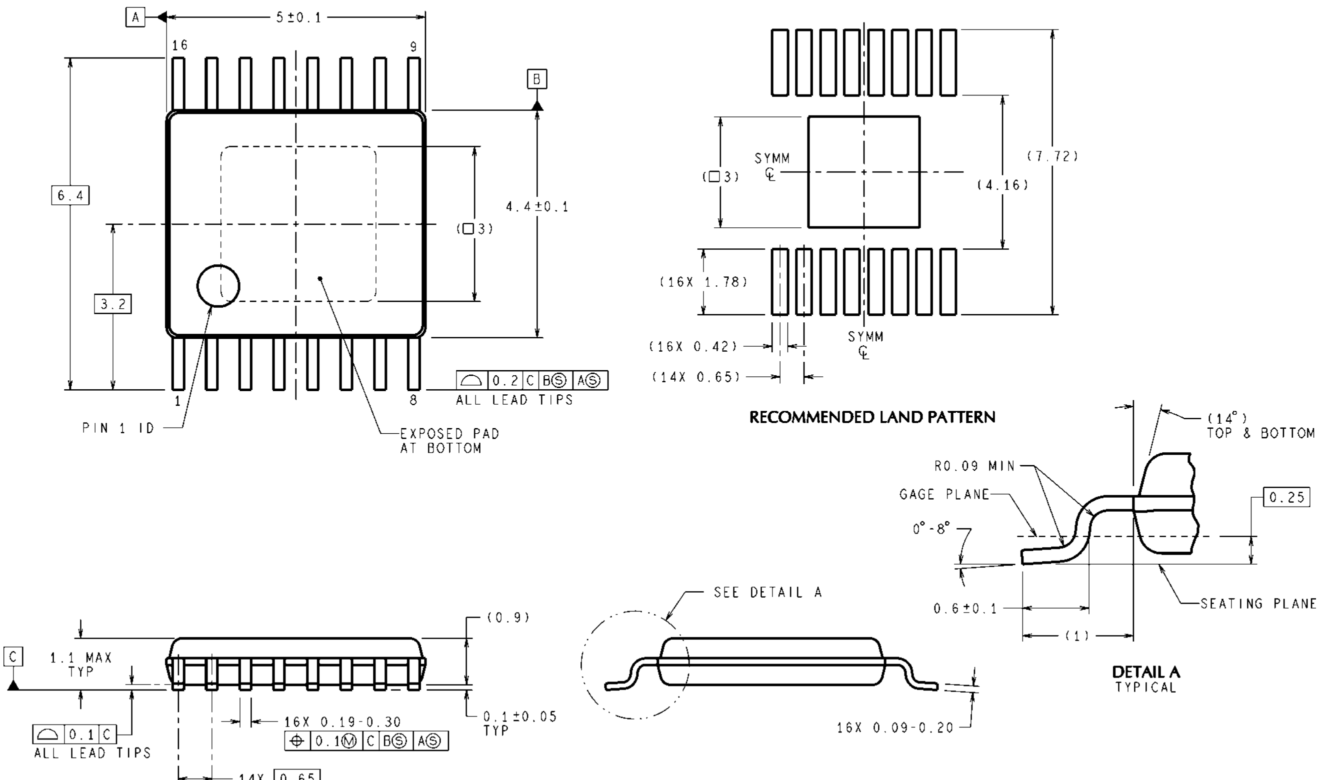
FIGURE 22. 3.3V V_{IN} to 0.9V V_{OUT}, 20A I_{OUT} , fsw = 500 kHz

Bill Of Materials

Designator	Type	Parameters	Part Number	Qty	Manufacturer
U1	Synchronous Buck Controller		LM27402	1	National Semiconductor
C_{BOOT}	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{C1}	Capacitor	820 pF, Ceramic, COG, 50V, 5%	GRM1885C1H821JA01D	1	Murata
C_{C2}	Capacitor	68 pF, Ceramic, COG, 50V, 5%	GRM1885C1H680JA01D	1	Murata
C_{C3}	Capacitor	390 pF, Ceramic, COG, 50V, 5%	GRM1885C1H391JA01D	1	Murata
C_{VDD}	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_F	Capacitor	1 µF, Ceramic, X5R, 25V, 10%	GRM188R61E105KA12D	1	Murata
C_{IN}	Capacitor	22 µF, Ceramic, X5R, 25V, 10%	C2012X5R0J226M	5	TDK
C_{OUT}	Capacitor	100 µF, Ceramic, X5R, 6.3V, 20%	JMK316BJ107ML	3	Taiyo Yuden
C_S	Capacitor	0.22 µF, Ceramic, X7R, 25V, 10%	GRM188R71E224KA88D	1	Murata
C_{SS}	Capacitor	22000 pF, Ceramic, X7R, 16V, 10%	GRM188R71E223KA01D	1	Murata
C_{SBY}	Capacitor	68 pF, Ceramic, C0G, 50V, 5%	GRM1885C1H680JA01D	1	Murata
D_{BOOT}	Diode	Schottky Diode, Average I = 100 mA, Max Surge I = 750 mA	CMOSH-3	1	Central Semi
D_{SW}	Diode	Schottky Diode, Average I = 3A, Max Surge I = 80A	CMSH3-40M	1	Central Semi
L_{OUT}	Inductor	0.33 µH, 1.4 mΩ	RL-8250-1.4-R33M	1	Renco

Designator	Type	Parameters	Part Number	Qty	Manufacturer
Q_L	N-CH MOSFET	20V, 100A, 64 nC, $R_{DS(ON)}$ @ 4.5V = 1.6 mΩ	BSC019N02KS	1	Infineon
Q_H	N-CH MOSFET	20V, 100A, 40 nC, $R_{DS(ON)}$ @ 4.5V = 2.1 mΩ	BSC026N02KS	1	Infineon
R_{C1}	Resistor	10.0 kΩ, 1%, 0.1W	CRCW060310K0FKEA	1	Vishay
R_{C2}	Resistor	150Ω, 1%, 0.1W	CRCW0603150RFKEA	1	Vishay
R_{DD}	Resistor	1Ω, 5%, 0.1W	CRCW06031R00JNEA	1	Vishay
R_{FADJ}	Resistor	20.0 kΩ, 1%, 0.1W	CRCW060320K0FKEA	1	Vishay
R_{FB1}	Resistor	20.0 kΩ, 1%, 0.1W	CRCW060320K0FKEA	1	Vishay
R_{FB2}	Resistor	40.2 kΩ, 1%, 0.1W	CRCW060340K2FKEA	1	Vishay
R_F	Resistor	2.2Ω, 5%, 0.1W	CRCW06032R20JNEA	1	Vishay
R_{PGD}	Resistor	51.1 kΩ, 5%, 0.1W	CRCW060351K1JNEA	1	Vishay
R_S	Resistor	1.07 kΩ, 1%, 0.1W	CRCW06031K07FKEA	1	Vishay
R_{SET}	Resistor	5.11 kΩ, 1%, 0.1W	CRCW06035K11FKEA	1	Vishay

Physical Dimensions inches (millimeters) unless otherwise noted



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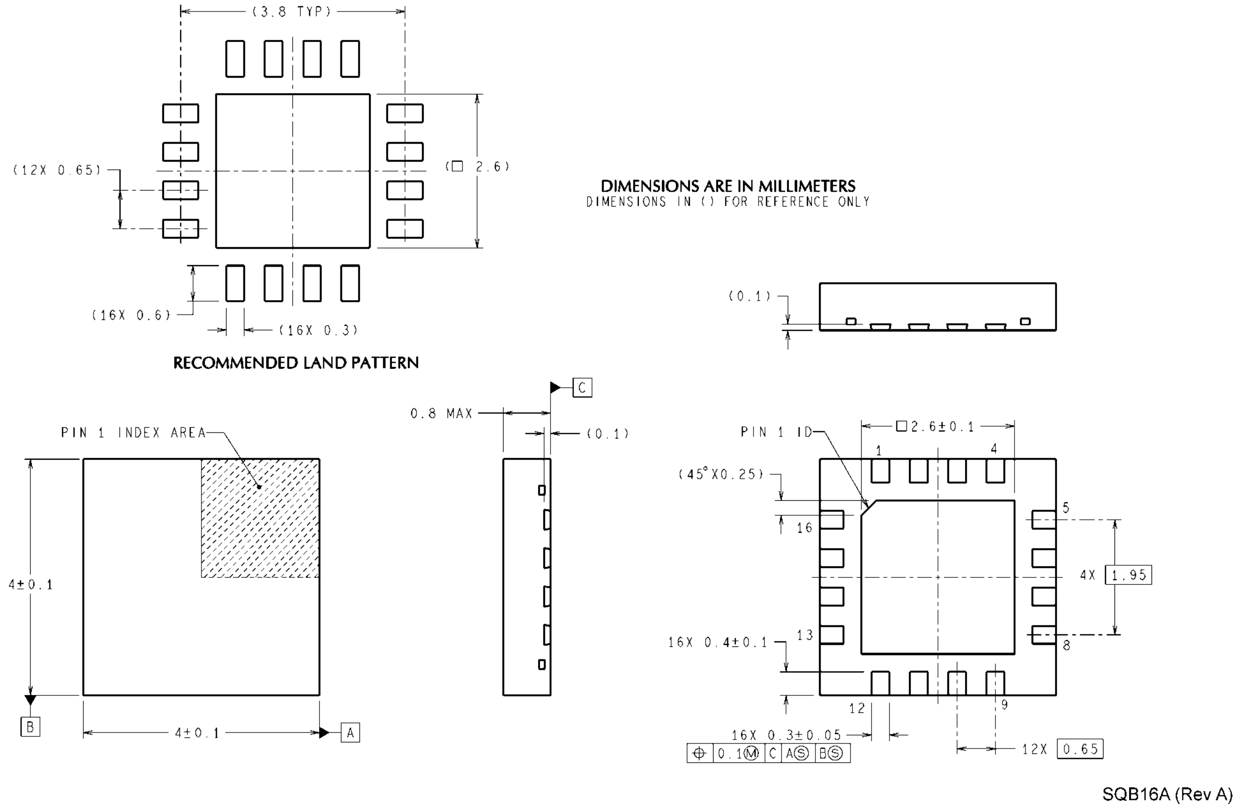

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Notes

Notes

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